NOVOSENSE

NSI1300-Q1
High Reliability Reinforced Isolated Amplifier

Datasheet (EN) 1.2

Product Overview

NSI1300-Q1 is a high-performance isolated amplifier with output separated from input based on the NOVOSENSE capacitive isolation technology. The device has a linear differential input signal range of ±50mV (±64mV full-scale) or ±250mV (±320mV full-scale). The differential input is ideally suited to shunt resistor-based current sensing in high voltage applications where isolation is required.

The device has a fixed gain (8.2 or 41) and provides a differential analog output.

The low offset and gain drift ensure the accuracy over the entire temperature range. High common-mode transient immunity ensures that the device is able to provide accurate and reliable measurements even in the presence of high-power switching such as in motor control applications.

The fail-safe functions including input common-mode overvoltage detection and missing VDD1 detection simplify system-level design and diagnostics.

Key Features

- Up to 5700V_{rms} Insulation voltage
- ±50mV or ±250mV linear Input Voltage Range
- Fixed Gain: 8.2 or 41
- Low Offset Error and Drift:
  NSI1300D25: ±0.2mV (Max), -2~4μV/℃ (Max)
  NSI1300D05: ±0.1mV (Max), -0.8~1μV/℃ (Max)
- Low Gain Error and Drift:
  ±0.3% (Max), ±50ppm/℃ (Max)
- Low Nonlinearity and Drift:
  ±0.03% (Max), ±1ppm/℃ (Typ)
- SNR: 86dB (Typ, BW=10kHz), 72dB (Typ, BW=100kHz)
- Wide bandwidth: 310kHz (Typ)
- High CMTI: 150kV/μs (Typ)
- System-Level Diagnostic Features:
  - VDD1 monitoring
  - Input common-mode overvoltage detection
- Operation Temperature: -40℃ ~125℃
- AEC-Q100 qualified for automotive applications
- RoHS-Compliant Packages:
  SOP8(300mil)

Safety Regulatory Approvals

- UL recognition per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Shunt Current Monitoring
- AC Motor Controls
- Uninterruptible Power Suppliers
- Automotive Onboard Chargers

Device Information

Part Number	*Package*	*Body Size*
NSI1300D25-Q1SWVR	SOP8(300mil)	5.85mm × 7.50mm
NSI1300D05-Q1SWVR	SOP8(300mil)	5.85mm × 7.50mm

Functional Block Diagrams

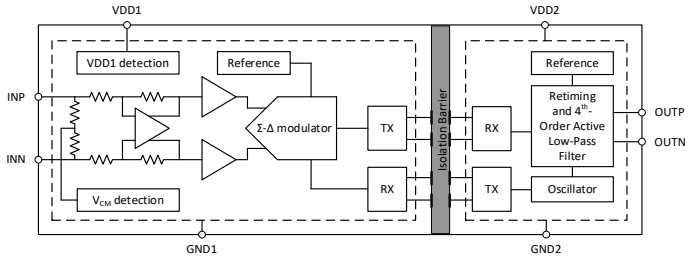

Figure 1. NSI1300-Q1 Block Diagram

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1. Pin Configuration and Functions

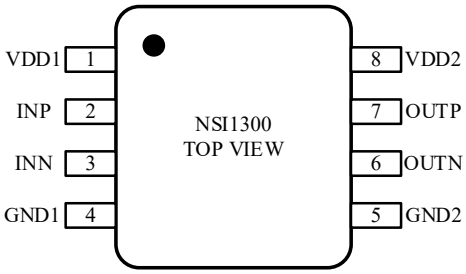


Figure 1.1 Package

Table 1.1 Pin Configuration and Description

NSI1300 PIN NO.	*SYMBOL*	*FUNCTION*
1	VDD1	Power supply for isolator side 1(3.0V to 5.5V)
2	INP	Positive analog input (±250mV recommended for NSI1300D25 and ±50mV recommended for NSI1300D05)
3	INN	Negative analog input
4	GND1	Ground 1, the ground reference for Isolator Side 1
5	GND2	Ground 2, the ground reference for Isolator Side 2
6	OUTN	Negative output
7	OUTP	Positive output
8	VDD2	Power supply for isolator side 2 (3.0V to 5.5V)

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	VDD1, VDD2	-0.3		6.5	V
Input Voltage	INP, INN	GND1-6		VDD1+0.5	V
Output Voltage	OUTP, OUTN	GND2-0.5		VDD2+0.5	V
Output current per Output Pin	Io	-10		10	mA
Operating Temperature	T_{OPR}	-40		125	℃
Junction Temperature	T_J	-40		150	℃
Storage Temperature	T_{STG}	-55		150	℃
Electrostatic discharge	HBM (1)	±2000			V
	CDM (2)	±1000			V

(1) Human body model (HBM), per AEC-Q100-002-RevD

(2) Charged device model (CDM), per AEC-Q100-011-RevB

3. Recommended Operating Conditions

Parameters		Symbol	Min	Typ	Max	Unit
Side1 Power Supply		VDD1	3.0	5.0	5.5	V
Side2 Power Supply		VDD2	3.0	3.3	5.5	V
NSI1300D05	Differential input voltage before clipping output	$V_{Clipping}$		±64		mV
	Linear differential input full scale voltage	V_{FSR}	-50		50	mV
	Operating common-mode input voltage	V_{CM}	-0.032		0.8	V
NSI1300D25	Differential input voltage before clipping output	$V_{Clipping}$		±320		mV
	Linear differential input full scale voltage	V_{FSR}	-250		250	mV
	Operating common-mode input voltage	V_{CM}	-0.16		0.8	V
Operating Ambient Temperature		T_A	-40		125	℃

4. Thermal Information

Parameters	Symbol	SOP8(300mil)	Unit
Junction–to-ambient thermal resistance	$R_{\theta JA}$	86	℃/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	28	℃/W
Junction-to-board thermal resistance	$R_{\theta JB}$	42	℃/W
Junction–to-top characterization parameter	Ψ_{JT}	4	℃/W
Junction-to-board characterization parameter	Ψ_{JB}	42	℃/W

5. Specifications

5.1. Electrical Characteristics: NSI1300D05

(VDD1 = 3.0V ~ 5.5V, VDD2 = 3.0V ~ 5.5V, INP = -50mV to +50mV, and INN = GND1 = 0V, T_A = -40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 3.3V, T_A = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Side1 Supply Voltage	VDD1	3.0	5.0	5.5	V	
Side2 Supply Voltage	VDD2	3.0	3.3	5.5	V	
Side1 Supply Current	IDD1		11.4	15.1	mA	
Side2 Supply Current	IDD2		6.3	8.4	mA	
VDD1 undervoltage detection threshold voltage	$VDD1_{UV}$	1.8	2.3	2.7	V	VDD1 falling
Analog Input						
Common-mode overvoltage detection level	V_{CMov}	0.9			V	Detection level has a typical hysteresis of 96 mV
Input offset voltage	V_{OS}	-0.1	±0.01	0.1	mV	T_A = 25℃,INP = INN = GND1
Input offset drift	TCV_{OS}	-0.8	±0.15	1	μV/℃	
Common-mode rejection ratio	$CMRR_{dc}$		-120		dB	INP = INN, f_{IN} = 0 Hz, $V_{CM\ min} \le VIN \le V_{CM\ max}$
	$CMRR_{ac}$		-112		dB	INP = INN, f_{IN} = 10 kHz, $V_{CM\ min} \le VIN \le V_{CM\ max}$
Single-ended input resistance	R_{IN}		4.75		kΩ	INN = GND1

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Differential input resistance	R_{IND}		4.9		kΩ	
Input capacitance	C_I		2		pF	
Input bias current	I_{IB}	-29	-22	-14	μA	T_A = 25℃,INP = INN = GND1, $I_{IB} = (I_{IBP} + I_{IBN}) / 2$
Input bias current drift	TCI_{IB}		±1.5		nA/℃	
Analog Output						
Nominal Gain			41		V/V	
Gain error	E_G	-0.3%	±0.05%	0.3%		T_A = 25℃
Gain error thermal drift	TCE_G	-50	±15	50	ppm/℃	
Nonlinearity		-0.04%	±0.01%	0.04%		T_A = 25℃
Nonlinearity drift			±1		ppm/℃	
Total harmonic distortion	THD		-85		dB	V_{IN} =100mVpp, f_{IN} = 10kHz, BW = 100kHz
Output noise			260		μV_{RMS}	INP = INN = GND1, BW = 100kHz
Signal to noise ratio	SNR	80	84		dB	V_{IN} = 100mVpp, f_{IN} = 1kHz, BW = 10kHz
			72		dB	V_{IN} = 100mVpp, f_{IN} = 10kHz, BW = 100kHz
Common-mode output voltage	V_{CMout}	1.39	1.44	1.49	V	
Failsafe differential output voltage	$V_{FAILSAFE}$		-2.6	-2.5	V	V_{CM}>V_{CMov}, or VDD1 missing
Output bandwidth	BW	250	310		kHz	
Power supply rejection ratio (1)	$PSRR_{dc}$		-118		dB	PSRR vs VDD1, at DC
	$PSRR_{ac}$		-116		dB	PSRR vs VDD1, 100mV and 10kHz ripple
	$PSRR_{dc}$		-108		dB	PSRR vs VDD2, at DC
	$PSRR_{ac}$		-97		dB	PSRR vs VDD2, 100mV and 10kHz ripple
Output resistance	R_{OUT}		< 0.2		Ω	
Output short-circuit current	$I_{OUT.OC}$		±13		mA	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Common-mode transient immunity	CMTI	100	150		kV/μs	Common-mode transient immunity
Timing						
Rising time of OUTP, OUTN	t_r		1.3		μs	
Falling time of OUTP, OUTN	t_f		1.3		μs	
INP, INN to OUTP, OUTN signal delay (50% - 50%)	t_{PD}		1.6	2.1	μs	
Analog setting time	t_{AS}		0.5		ms	VDD1 step to 3.0 V with VDD2 ≥ 3.0 V, to OUTP, OUTN valid, 0.1% settling

(1) Input referred.

5.2. Electrical Characteristics: NSI1300D25

(VDD1 = 3.0V ~ 5.5V, VDD2 = 3.0V ~ 5.5V, INP = -250mV to +250mV, and INN = GND1 = 0V, T_A = -40℃ to 125℃.

Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 3.3V, T_A = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Side1 Supply Voltage	VDD1	3.0	5.0	5.5	V	
Side2 Supply Voltage	VDD2	3.0	3.3	5.5	V	
Side1 Supply Current	IDD1		11.4	15.1	mA	
Side2 Supply Current	IDD2		6.3	8.4	mA	
VDD1 undervoltage detection threshold voltage	$VDD1_{UV}$	1.8	2.3	2.7	V	VDD1 falling
Analog Input						
Common-mode overvoltage detection level	V_{CMov}	0.9			V	Detection level has a typical hysteresis of 96 mV
Input offset voltage	V_{OS}	-0.2	±0.01	0.2	mV	T_A = 25℃,INP = INN = GND1
Input offset drift	TCV_{OS}	-2	1	4	μV/℃	
Common-mode rejection ratio	$CMRR_{dc}$		-106		dB	INP = INN, f_{IN} = 0 Hz, $V_{CM\ min}$ ≤ VIN ≤ $V_{CM\ max}$
	$CMRR_{ac}$		-106		dB	INP = INN, f_{IN} = 10 kHz, $V_{CM\ min}$ ≤ VIN ≤ $V_{CM\ max}$

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Single-ended input resistance	R_{IN}		19		kΩ	INN = GND1
Differential input resistance	R_{IND}		22		kΩ	
Input capacitance	C_I		2		pF	
Input bias current	I_{IB}	-24	-18	-12	μA	T_A = 25℃,INP = INN = GND1, $I_{IB} = (I_{IBP} + I_{IBN}) / 2$
Input bias current drift	TCI_{IB}		±1		nA/℃	
Analog Output						
Nominal Gain			8.2		V/V	
Gain error	E_G	-0.3%	±0.05%	0.3%		T_A = 25℃
Gain error thermal drift	TCE_G	-50	±15	50	ppm/℃	
Nonlinearity		-0.04%	±0.01%	0.04%		T_A = 25℃
Nonlinearity drift			±1		ppm/℃	
Total harmonic distortion	THD		-85		dB	V_{IN} =500mVpp, f_{IN} = 10kHz, BW = 100kHz
Output noise			195		$μV_{RMS}$	INP = INN = GND1, BW = 100kHz
Signal to noise ratio	SNR	80	86		dB	V_{IN} = 500mVpp, f_{IN} = 1kHz, BW = 10kHz
			72		dB	V_{IN} = 500mVpp, f_{IN} = 10kHz, BW = 100kHz
Common-mode output voltage	V_{CMout}	1.39	1.44	1.49	V	
Failsafe differential output voltage	$V_{FAILSAFE}$		-2.6	-2.5	V	V_{CM}>V_{CMov}, or VDD1 missing
Output bandwidth	BW	250	310		kHz	
Power supply rejection ratio (1)	$PSRR_{dc}$		-104		dB	PSRR vs VDD1, at DC
	$PSRR_{ac}$		-102		dB	PSRR vs VDD1, 100mV and 10kHz ripple
	$PSRR_{dc}$		-90		dB	PSRR vs VDD2, at DC
	$PSRR_{ac}$		-85		dB	PSRR vs VDD2, 100mV and 10kHz ripple

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Output resistance	R_{OUT}		< 0.2		Ω	
Common-mode transient immunity	CMTI	100	150		kV/μs	Common-mode transient immunity
Timing						
Rising time of OUTP, OUTN	t_r		1.3		μs	
Falling time of OUTP, OUTN	t_f		1.3		μs	
INP, INN to OUTP, OUTN signal delay (50% - 50%)	t_{PD}		1.6	2.1	μs	
Analog setting time	t_{AS}		0.5		ms	VDD1 step to 3.0 V with VDD2 ≥ 3.0 V, to OUTP, OUTN valid, 0.1% settling

(1) Input referred.

5.3. Typical Performance Characteristics

Unless otherwise noted, test at VDD1 = 5V, VDD2 = 3.3V, Vin = -250mV to 250mV (NSI1300D25) or -50mV to 50mV (NSI1300D05).

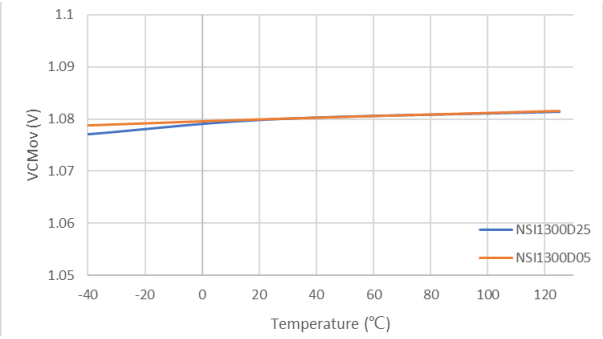


Figure 5.1 Common-Mode Overvoltage Detection Level vs Temperature

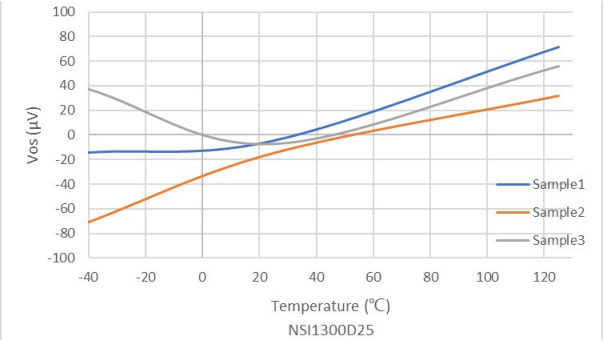


Figure 5.2 Input Offset Voltage vs Temperature (NSI1300D25)

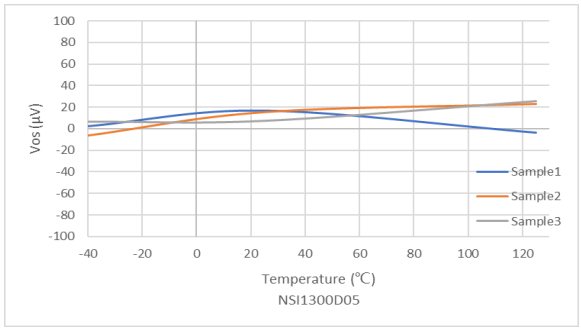


Figure 5.3 Input Offset Voltage vs Temperature (NSI1300D05)

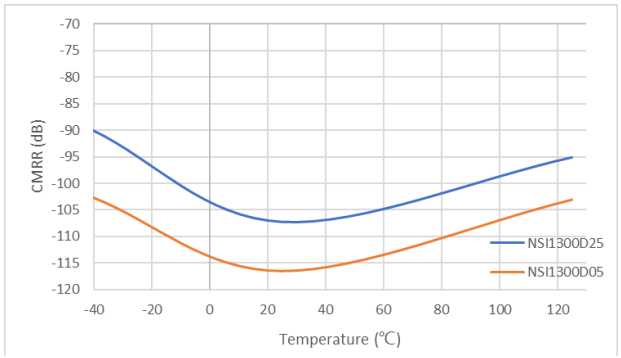


Figure 5.4 Common-Mode Rejection Ratio vs Temperature

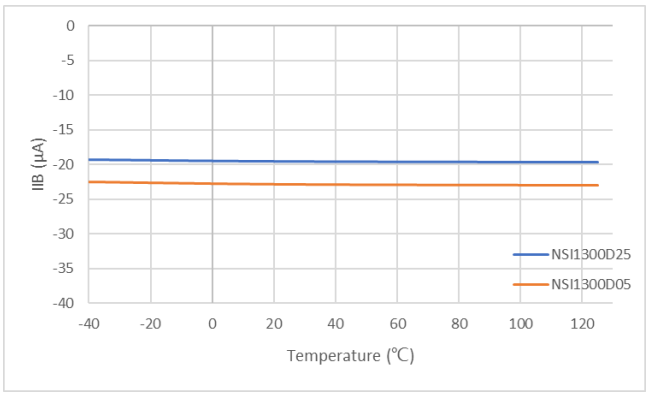


Figure 5.5 Input Bias Current vs Temperature

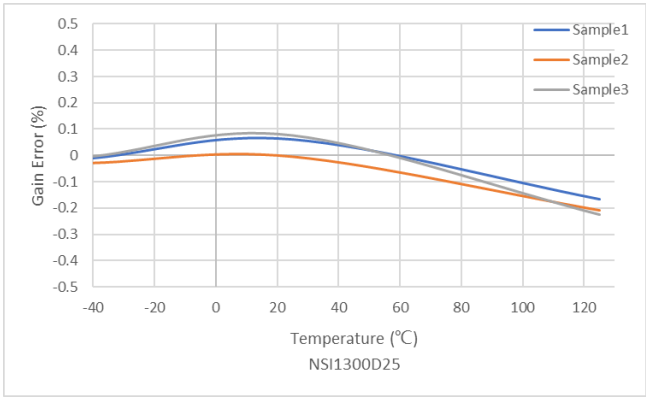


Figure 5.6 Gain Error vs Temperature (NSI1300D25)

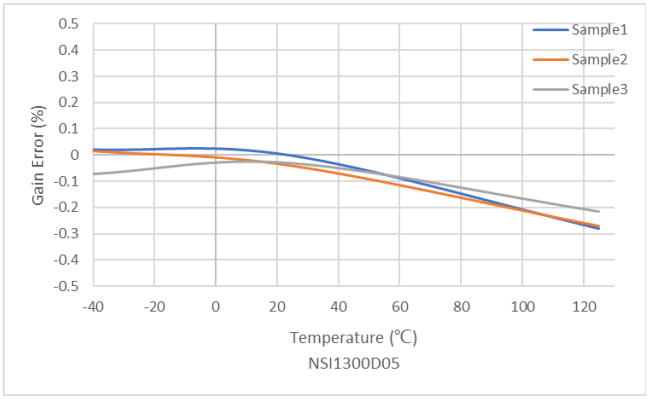


Figure 5.7 Gain Error vs Temperature (NSI1300D05)

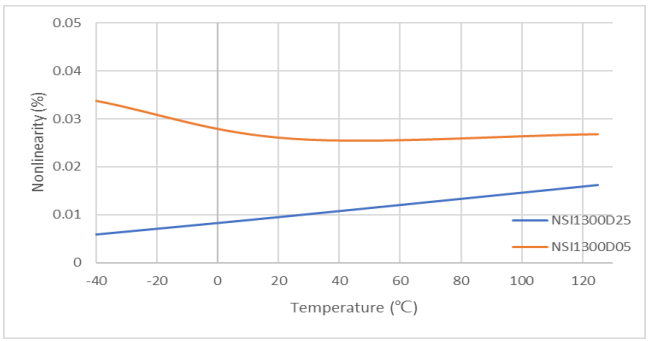


Figure 5.8 Nonlinearity vs Temperature

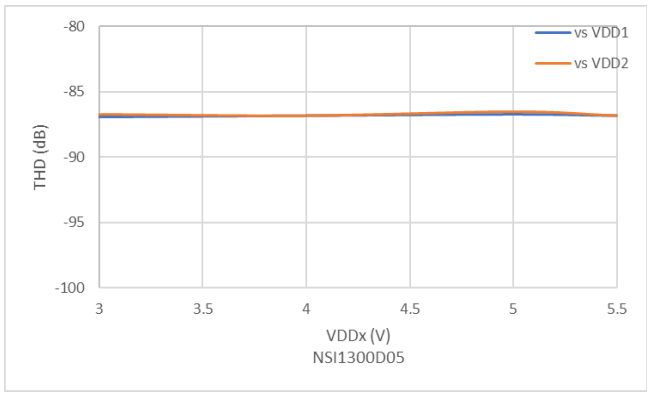


Figure 5.9 THD vs Supply Voltage (NSI1300D05)

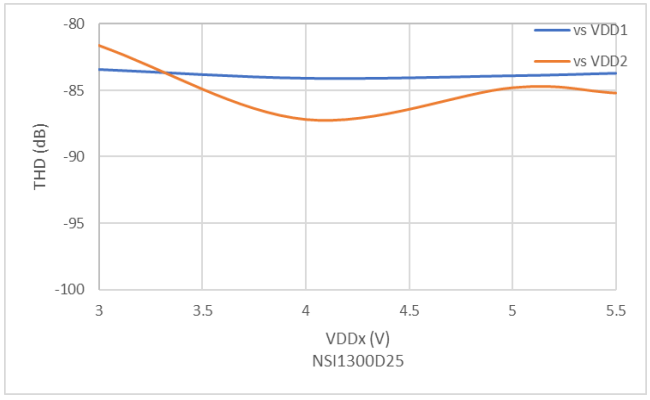


Figure 5.10 THD vs Supply Voltage (NSI1300D25)

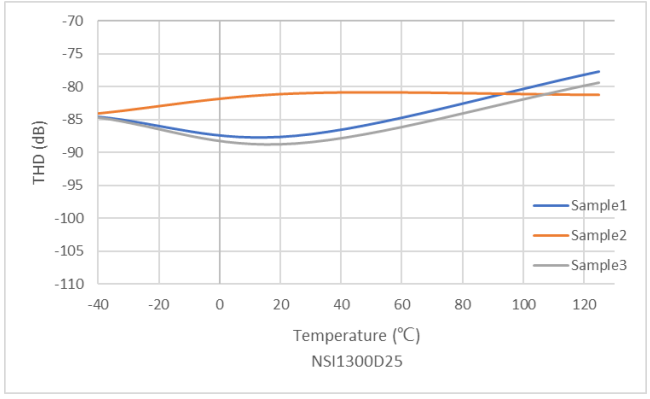


Figure 5.11 THD vs Temperature (NSI1300D25)

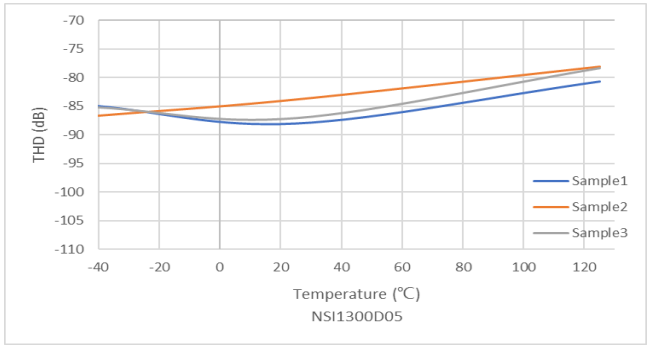


Figure 5.12 THD vs Temperature (NSI1300D05)

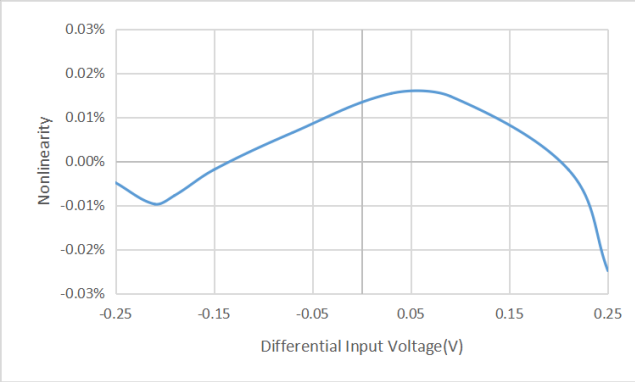


Figure 5.13 Nonlinearity vs Input Voltage (NSI1300D25)

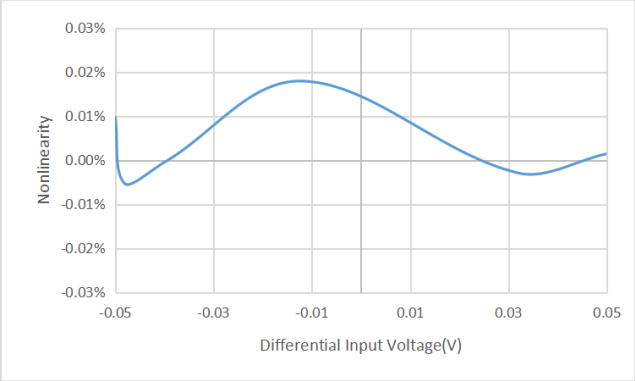


Figure 5.14 Nonlinearity vs Input Voltage (NSI1300D05)

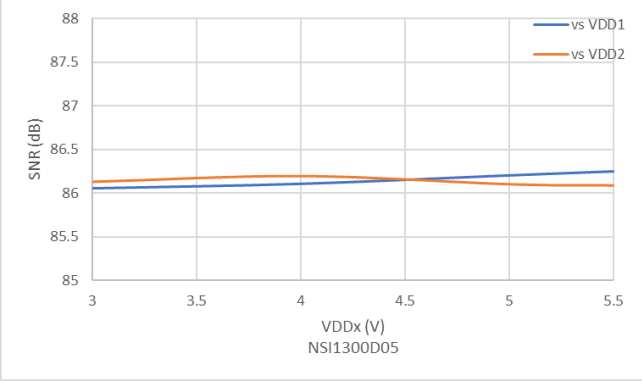


Figure 5.14 SNR vs Supply Voltage (NSI1300D05)

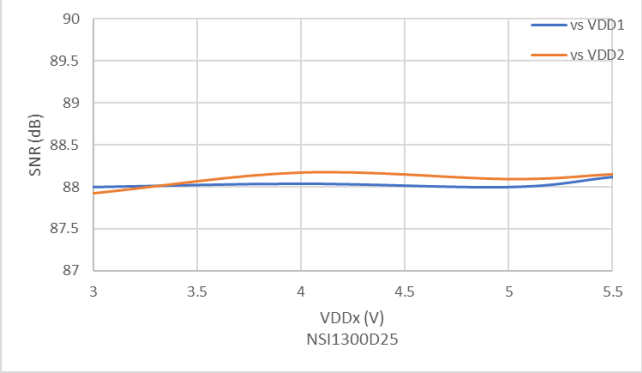


Figure 5.156 SNR vs Supply Voltage (NSI1300D25)

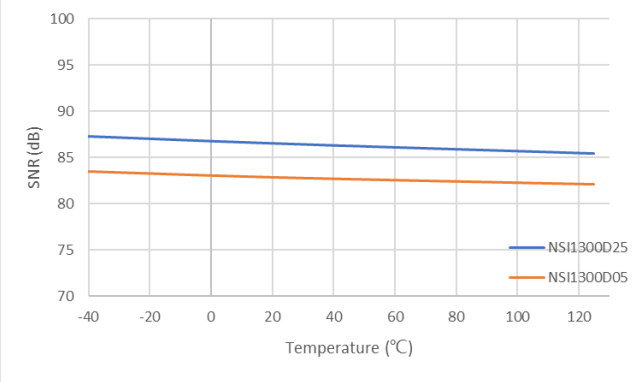


Figure 5.167 SNR vs Temperature

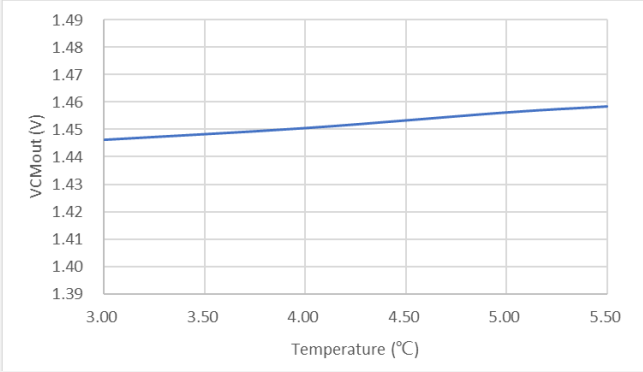


Figure 5.178 Output Common-Mode Voltage vs Side2 Supply Voltage

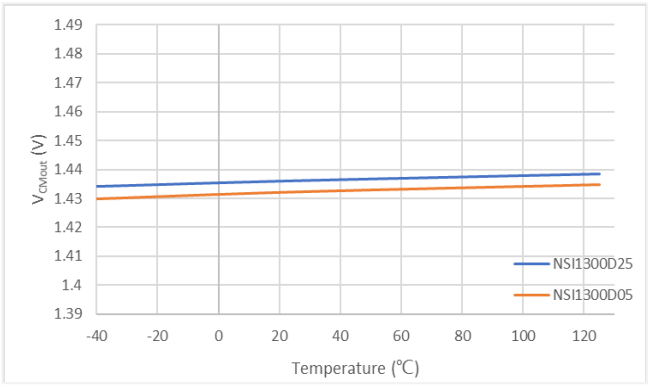


Figure 5.189 Output Common-Mode Voltage vs Temperature

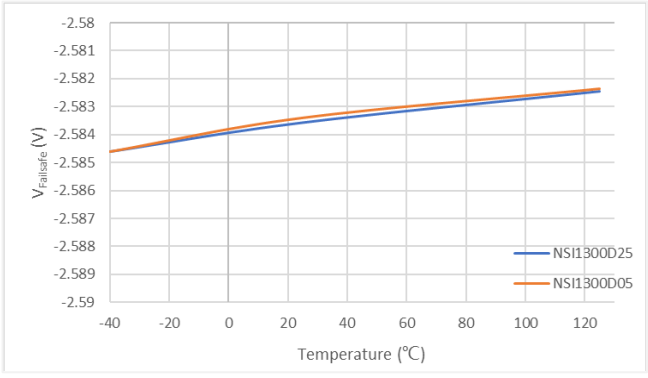


Figure 5.1920 Fail-Safe Output Voltage vs Temperature

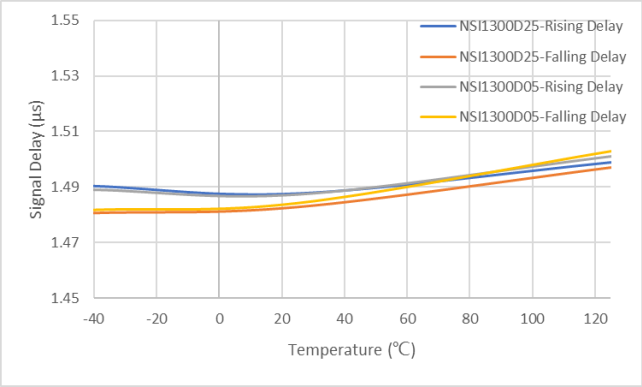


Figure 5.2021 Vin to Vout Delay vs Temperature

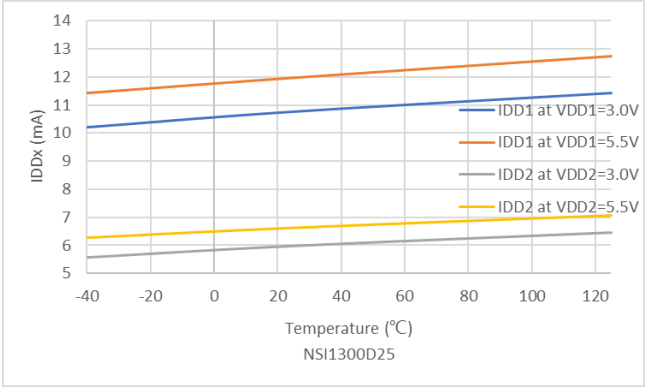


Figure 5.24 Supply Current vs Temperature (NSI1300D25)

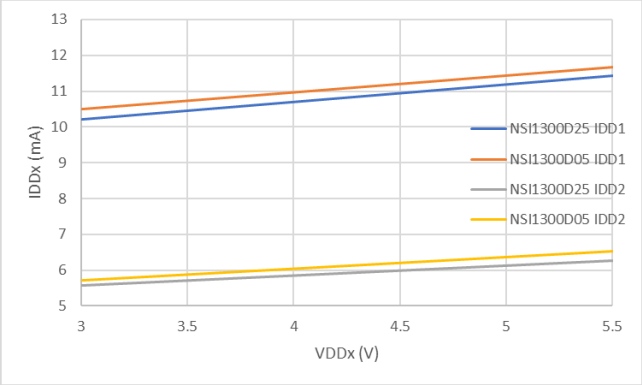


Figure 5.22 Supply Current vs Supply Voltage

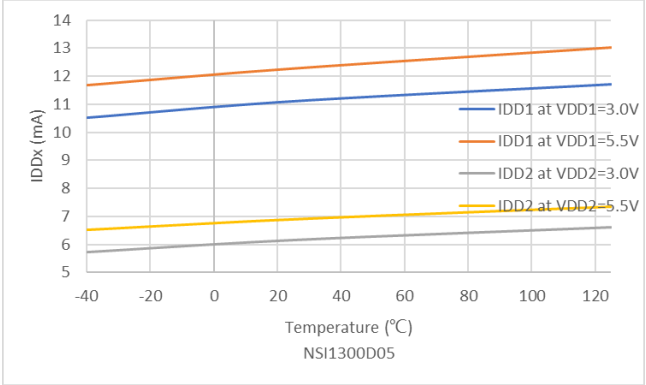


Figure 5.25 Supply Current vs Temperature (NSI1300D05)

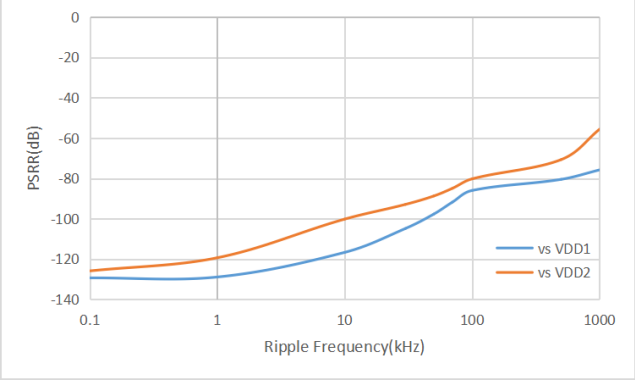


Figure 5.23 Power-Supply Rejection Ratio vs Ripple Frequency

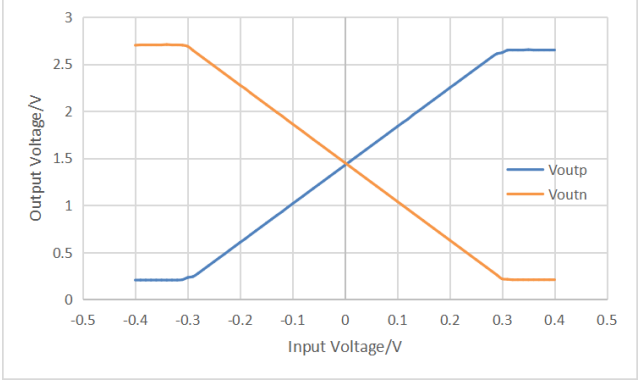


Figure 5.26 Output Voltage vs Input Voltage (NSi1300D25)

5.4. Parameter Measurement Information

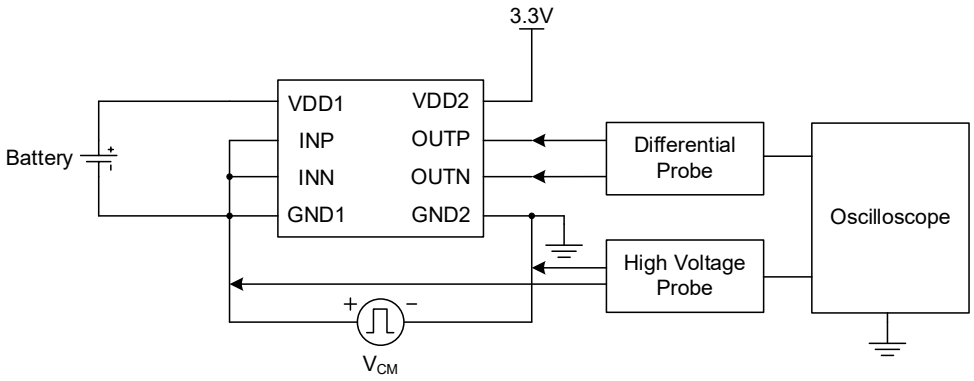


Figure 5.27 Common-Mode Transient Immunity Test Circuit

6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

Parameters	*Symbol*	*Value*	*Unit*	*Comments*
Minimum External Clearance	CLR	8	mm	IEC 60664-1:2007
Minimum External Creepage	CPG	8	mm	IEC 60664-1:2007
Distance Through Insulation	DTI	28	μm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

Description	*Test Condition*	*Value*
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	I to IV
	For Rated Mains Voltage ≤ 300Vrms	I to IV
	For Rated Mains Voltage ≤ 600Vrms	I to IV
Climatic Classification		40/125/21
Pollution Degree per DIN VDE 0110, Table 1		2

6.2. Insulation Characteristics

Description	*Test Condition*	*Symbol*	*Value*	*Unit*
Maximum repetitive isolation voltage		V_{IORM}	2121	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	1500	V_{RMS}

Description	Test Condition	Symbol	Value	Unit
	DC Voltage		2121	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, Vini=V_{IOTM}, t_{ini} = 60 s , $V_{pd(m)}$=1.2*V_{IORM}, t_m=10s.	q_{pd}	<5	pC
	Method a, after environmental tests subgroup 1, Vini=V_{IOTM}, t_{ini}=60s ,$V_{pd(m)}$=1.6*V_{IORM}, t_m=10s			
	Method b, routine test (100% production) and preconditioning (type test);V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd\ (m)}$=1.875*V_{IORM}, t_m=1s（method b1）or $V_{pd(m)}$=Vini, t_m=t_{ini}(method b2)			
Maximum impulse voltage	Tested in air, 1.2/50-us waveform per IEC62368-1	V_{IMP}	6250	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$	V_{IOSM}	10000	V_{PEAK}
Isolation resistance	V_{IO} =500V, T_{amb}=25℃	R_{IO}	$>10^{12}$	Ω
	V_{IO} =500V, 100℃ ≤ T_{amb} ≤ 125℃	R_{IO}	$>10^{11}$	Ω
	V_{IO} =500V, T_{amb}=T_s	R_{IO}	$>10^{9}$	Ω
Isolation capacitance	f = 1MHz	C_{IO}	0.8	pF
Safety total power dissipation	V_I = 5.5V, T_J = 150 ℃, T_A = 25 ℃	Ps	1430	mW
Safety input, output, or supply current	V_I = 5.5V, T_J = 150 ℃, T_A = 25 ℃	Is	260	mA
Maximum safety temperature		Ts	150	℃
UL1577				
Insulation voltage per UL	V_{TEST} = V_{ISO}, t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO}, t = 1 s (100% production test)	V_{ISO}	5700	V_{RMS}

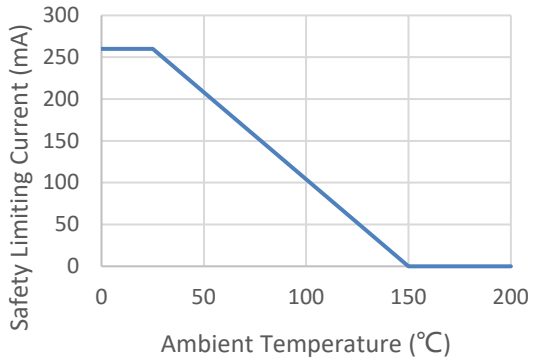


Figure 6.1 NSI1300 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per VDE0884-17

6.3. Regulatory Information

The NSI1300 are approved or pending approval by the organizations listed in table.

UL		VDE	CQC	TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1
Single Protection, 5700V_{rms} Isolation voltage	Single Protection, 5700V_{rms} Isolation voltage	Reinforce Insulation V_{IORM}=2121Vpeak VIOTM=8000Vpeak VIOSM=10000Vpeak	Reinforced insulation	5000Vrms for 1min
E500602	E500602	40052820	CQC20001264938	R50574061

7. Function Description

7.1. Overview

The NSI1300 is a high performance isolated amplifier that accept fully-differential input. The fully-differential input is ideally suited to shunt current monitoring in high voltage applications where isolation is required. The analog input is continuously sampled by a second-order Σ-Δ modulator in the device, which is driven by a pre-stage fully-differential amplifier in the device. With the internal voltage reference and clock generator, the modulator convert the analog input signal to a digital bitstream. The output of the modulator is transferred by the drivers (called TX in the Functional Block Diagram) across the isolation barrier that separates the isolated side1 and side2 voltage. The received bitstream and clock are synchronized and processed, as shown in the Functional Block Diagram, by a fourth-order analog filter on the side2 and has a differential output.

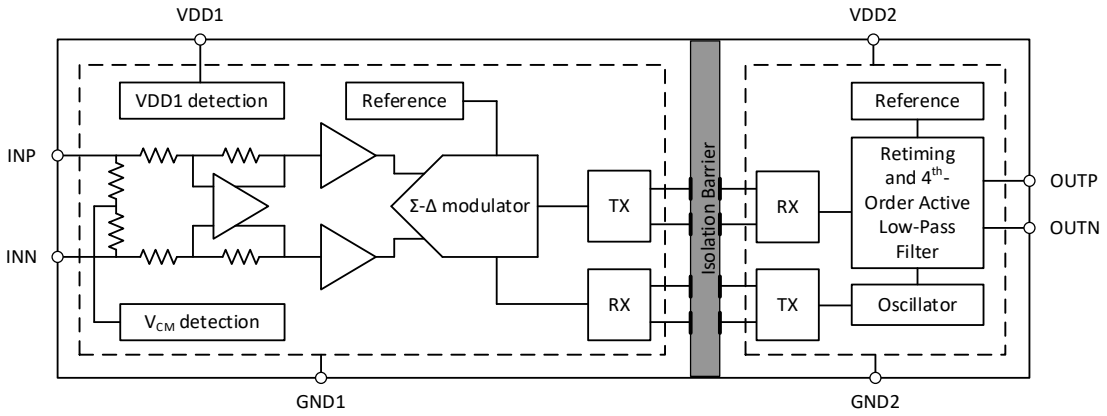


Figure 7.1 Function Block Diagram

7.2. Analog Input

There are two restrictions on the analog input signals (VINP and VINN).

- If the input voltage exceeds the range GND1 – 6 V to VDD1 + 0.5 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on.
- The linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

7.3. Analog Output

For linear input range, the analog output of NSI1300 has a fixed gain (8.2 for NSI1300D25 and 41 for NSI1300D05). If a full-scale input signal is applied to the NSI1300 ($V_{IN} \geq V_{Clipping}$), the analog output will be clipped (typically, 2.45V for positive clipping and -2.45V for negative clipping).

In addition, NSI1300 integrates some diagnostic measures and offers a fail-safe output to simplify system-level design. The fail-safe output is a negative differential output voltage that does not occur under normal device operation, and it will only be activated in following conditions:

- When the undervoltage of VDD1 is detected (VDD1< $VDD1_{UV}$).
- When the overvoltage of common-mode input voltage is detected (V_{CM}>V_{CMov}).

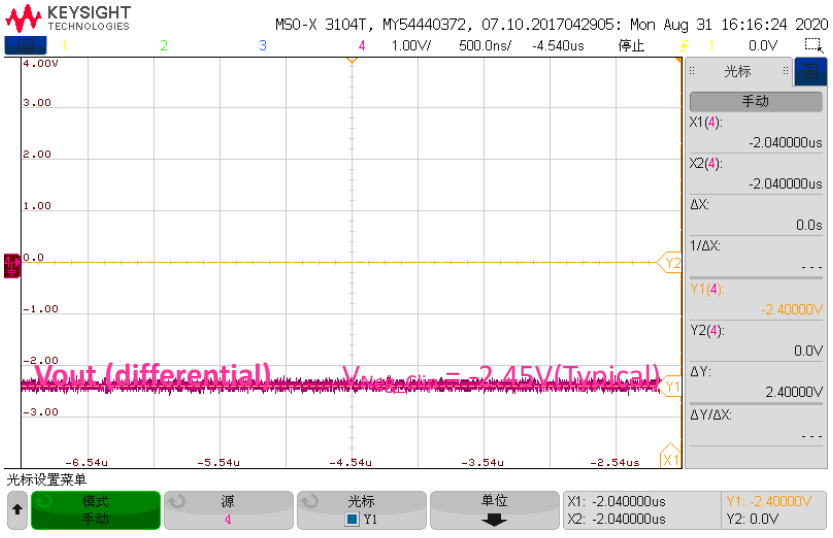


Figure 7.2 Typical negative clipping output

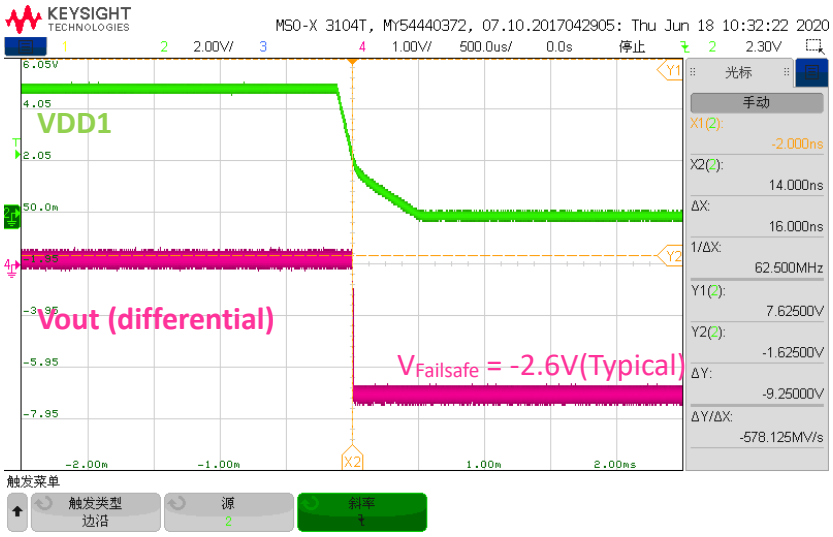


Figure 7.3 Typical Failsafe output when VDD1 undervoltage

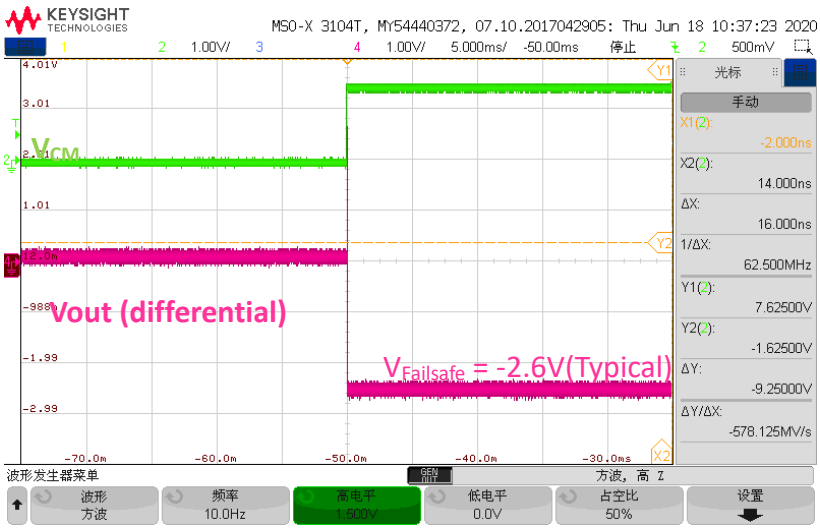


Figure 7.4 Typical Failsafe output when input common mode signal overvoltage

8. Application Note

8.1. Typical Application Circuit

NSI1300 is ideally suited to shunt resistor-based current sensing in high voltage applications such as frequency inverters. The typical application circuit is shown in Figure 8.1.

The voltage across the shunt resistor R_{sense} is applied to the differential input of NSI1300 through a RC filter. The differential output of the isolated amplifier is converted to a single-ended analog output with an operational-amplifier-based circuit. Suggest to add >1kΩ resistor on the OUTP and OUTN pin to prevent output over-current. An analog-to-digital converter usually receives the analog output and converts to digital signal for controller processing.

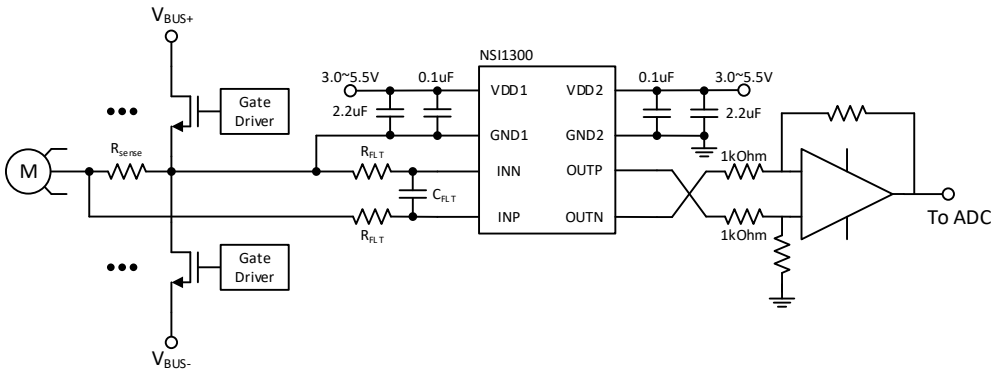


Figure 8.1 Typical application circuit in phase current sensing

8.2. Shunt Resistor Selection

Choosing a particular shunt resistor is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller sense resistor decreases power dissipation, while larger sense resistor can improve measure accuracy by utilizing the full input range of isolated amplifier.

There are two other factors should be considered when selecting the shunt resistor:

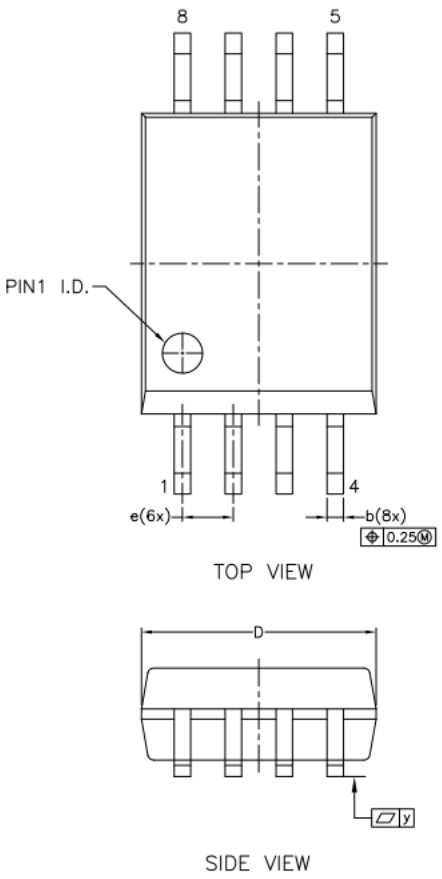
- The voltage-drop caused by the rated current range must not exceed the recommended linear input voltage range: $V_{SHUNT} \leq FSR$.
- The voltage-drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $V_{SHUNT} \leq V_{Clipping}$.

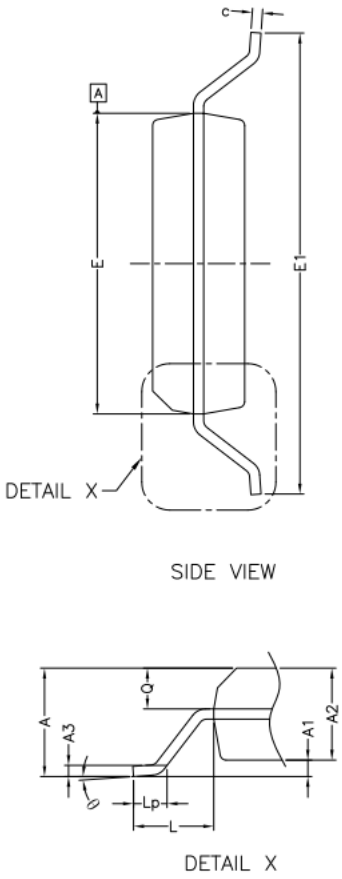
8.3. PCB Layout

There are some key guidelines or considerations for optimizing performance in PCB layout:

- NSI1300 requires a 0.1μF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the VDD pin. If better filtering is required, an additional 1~10μF capacitor may be used.
- Kelvin rules is recommended for the connection between shunt resistor to NSI1300. Because of the Kelvin connection, any voltage drops across the trace and leads should have no impact on the measured voltage.
- Place the shunt resistor close to the INP and INN inputs and keep the layout of both connections symmetrical and run very close to each other to the input of the NSI1300. This minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal.

9. Package Information

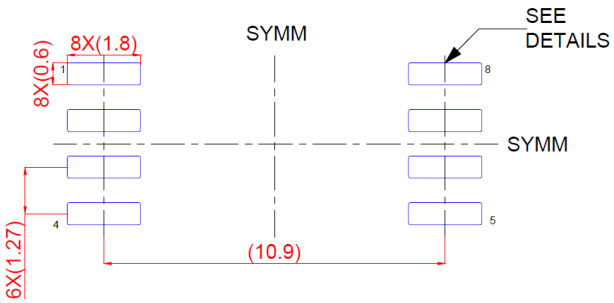




* CONTROLLING DIMENSION : MM

SYMBOL	MM		
	MIN.	NOM.	MAX.
A	--	--	2.80
A1	0.36	--	0.46
A2	2.20	2.30	2.40
A3	--	0.25	--
Q	0.97	1.02	1.07
b	0.31	0.41	0.51
c	0.13	--	0.33
D	5.75	5.85	5.95
E	7.40	7.50	7.60
E1	11.25	11.50	11.75
e	1.27 bsc		
L	2.00 bsc		
Lp	0.50	--	1.00
y	--	0.10	--
θ	0°	--	8°

Figure 9.1 SOW8 Package Shape and Dimension in millimeters



LAND PATTERN EXAMPLE(mm)
9.1 mm NOMINAL
CLEARANCE/CREEPAGE

Figure 9.2 SOW8 Package Board Layout Example

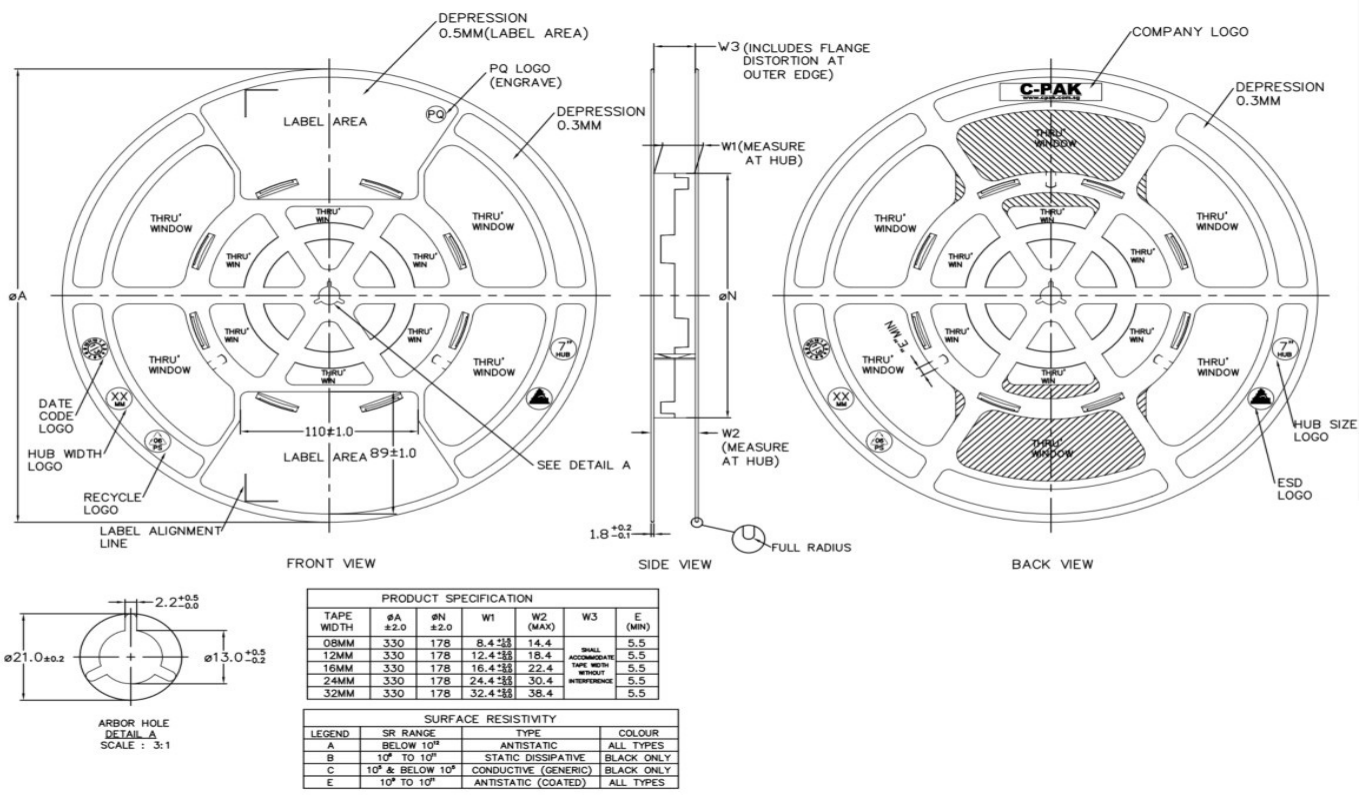
10. Ordering Information

Part No.	Isolation Rating(kV)	Linear Input Range(mV)	Moisture Sensitivity Level	Temperature	Automotive	Package Type	Package Drawing	SPQ
NSI1300D05 -Q1SWVR	5	-50 ~ 50	Level-3	-40 to 125℃	YES	SOP8 (300mil)	SOW8	1000
NSI1300D25 -Q1SWVR	5	-250 ~ 250	Level-3	-40 to 125℃	YES	SOP8 (300mil)	SOW8	1000

11. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NSI1300	Click here	Click here	Click here	Click here

12. Tape and Reel Information

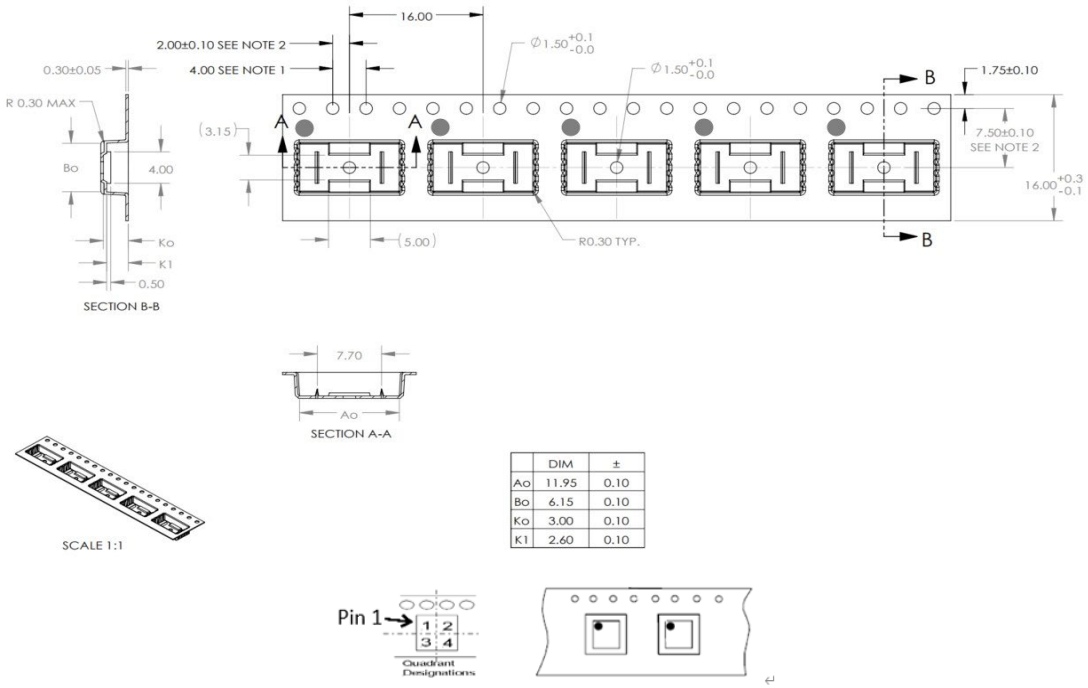


PRODUCT SPECIFICATION

TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +1.5 -0.0	18.4		5.5
16MM	330	178	16.4 +1.5 -0.0	22.4		5.5
24MM	330	178	24.4 +1.5 -0.0	30.4		5.5
32MM	330	178	32.4 +1.5 -0.0	38.4		5.5

SURFACE RESISTIVITY

LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{9} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{9}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{6} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES



	DIM	±
Ao	11.95	0.10
Bo	6.15	0.10
Ko	3.00	0.10
K1	2.60	0.10

Figure 12.1 Tape and Reel Information of SOP8(300mil)

13. Revision History

Revision	Description	Date
1.0	Initial Release	2021/6/23
1.1	Update insulation characteristics and add board layout example	2021/7/17
1.2	Update all NSi to NSI. Update test temperature condition of Vos, I_{IB}, E_G and Nonlinearity Update safety regulatory info	2024/11/27

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