

Product Overview

NCA8244L is an octal buffer/driver used for improving driver ability of bus-oriented receivers and transmitters, clock drivers etc. and ensuring the accuracy of signal timing. It provides four channels in each direction with separate output-enable(/OE) input that low active. When /OE is active, NCA8244L transmits data from A to Y. When /OE is high, the outputs are in the high-impedance state. During power up and power down, /OE should be tied to VCC through a pull-up resistor to ensure the high impedance state.

NCA8244L can tolerate up to 5.5V input voltage and each channel supports maximum 24 mA current drive. All unused inputs must be held at V_{CC} or GND to prevent excess supply current.

Key Features

- Qualified for Automotive applications:
NCA8244L-Q1TSTR
- Inputs are TTL compatible
- Power supply voltage:
1.65V to 3.6V
- 5.5 V Tolerant Inputs
- ESD Protection Exceeds JESD 22
 - 4000V Human-Body Model (A114-A)
 - 2000V Charged-Device Model (C101)
- Operation temperature: -40°C~125°C
- RoHS-compliant packages: TSSOP20

Applications

- Motor driver
- Traction inverter
- I/O modules
- LED displays

Device Information

Part Number	Package	Body Size
NCA8244L-DTSTR	TSSOP20	6.50mm × 4.50mm
NCA8244L-Q1TSTR	TSSOP20	6.50mm × 4.50mm

Functional Block Diagrams

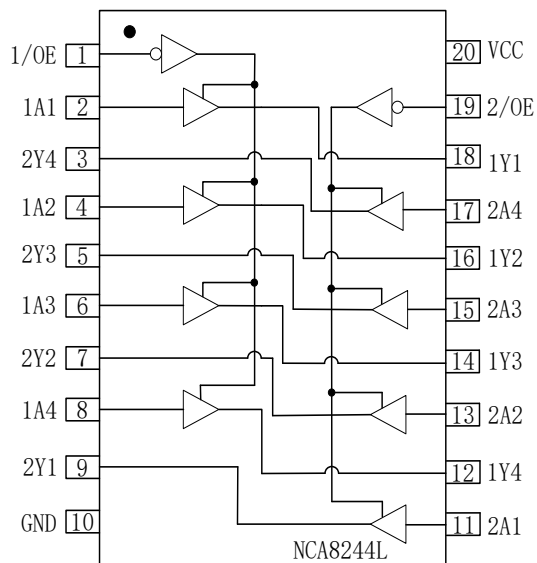


Figure 1. NCA8244L Block Diagram

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1. Pin Configuration and Functions

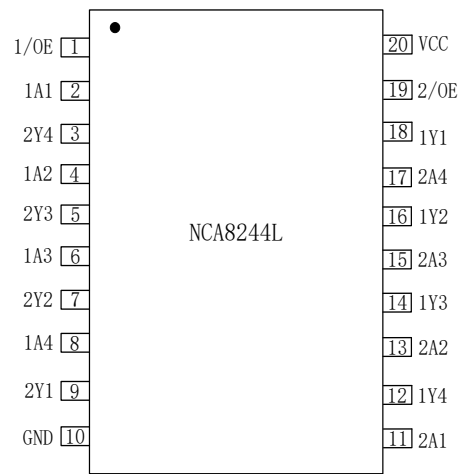


Figure 1.1 NCA8244L Package

Table 1.1 NCA8244L Pin Configuration and Description

NCA8244L PIN NO.	SYMBOL	FUNCTION
1	1/OE	1 Active low Output enable
2	1A1	Input of 1Y1
3	2Y4	Output of 2A4
4	1A2	Input of 1Y2
5	2Y3	Output of 2Y3
6	1A3	Input of 1Y3
7	2Y2	Output of 2A2
8	1A4	Input of 1Y4
9	2Y1	Output of 2A1
10	GND	Ground
11	2A1	Input of 2Y1
12	1Y4	Output of 1A4
13	2A2	Input of 2Y2
14	1Y3	Output of 1A3
15	2A3	Input of 2Y3
16	1Y2	Output of 1A2
17	2A4	Input of 2Y4
18	1Y1	Output of 1A1

19	2/OE	2 Active low Output enable
20	V _{CC}	Power

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	V _{CC}	-0.5		5.5	V	
Maximum Input Voltage	V _I	-0.5		V _{CC} +0.5	V	The maximum voltage must not exceed 5.5V
Maximum Output Voltage	V _O	-0.5		V _{CC} +0.5	V	The maximum voltage must not exceed 5.5V
Input clamp current	I _{IK}	-20		20	mA	V _I < 0 or V _I > V _{CC}
Output clamp current	I _{OK}	-20		20	mA	V _I < 0 or V _I > V _{CC}
Continuous output current	I _O	-50		50	mA	V _O =0 to V _{CC}
Ambient Temperature	T _a	-40		125	°C	
Junction Temperature	T _J			150	°C	
Storage Temperature	T _{stg}	-65		150	°C	
Electrostatic discharge	HBM	-4000		4000	V	Per ANSI/ESDA/JEDEC JS-001
	CDM	-2000		2000	V	Per JEDEC specification JESD22- C101

3. Recommended Operating Conditions

Over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	V _{CC}	1.65		3.6	V	
High-level output current	I _{OH}	-4			mA	V _{CC} =1.65V
		-8				V _{CC} =2.3V
		-12				V _{CC} =2.7V
		-24				V _{CC} =3V
Low-level output current	I _{OL}			4	mA	V _{CC} =1.65V
				8		V _{CC} =2.3V
				12		V _{CC} =2.7V
				24		V _{CC} =3V

Input transition rise or fall rate	$\Delta t/\Delta v$			8	ns/V	
Operating free-air temperature	T_a	-40		125	°C	

(1) All unused inputs of the device must be held at VCC or GND to ensure proper device operation.

4. Thermal Information

Parameters	Symbol	TSSOP20	Unit
Junction-to-ambient thermal resistance	$R_{\theta JA}$	103	°C/W
Junction-to-case(top) thermal resistance	$R_{\theta JC(top)}$	37.7	°C/W
Junction-to-board thermal resistance	$R_{\theta JB}$	54	°C/W
Junction-to- top characterization parameter	Ψ_{JT}	6.8	°C/W
Junction-to- board characterization parameter	Ψ_{JB}	65.1	°C/W

5. Specifications

5.1. Electrical Characteristics

($V_{CC}=1.65V\sim 3.6V$, $T_a=-40^{\circ}C$ to $125^{\circ}C$. Unless otherwise noted, Typical values are at $T_a = 25^{\circ}C$)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	I_{CC}			40	uA	$V_{CC}=3.6V$, $V_I = V_{CC}$ or GND, $I_O = 0$
				40		$V_{CC}=3.6V$, $3.6V \leq V_I \leq 5.5V^{(1)}$, $I_O = 0$
Increasing supply current ⁽²⁾	ΔI_{CC}			5	mA	One input at $V_{CC}-0.6V$, Other inputs at GND or V_{CC} , $2.7V \leq V_{CC} \leq 3.6V$
High-level input voltage	V_{IH}	0.65*VCC			V	$V_{CC}=1.65V$ to $1.95V$
		1.7				$V_{CC}=2.3V$ to $2.7V$
		2				$V_{CC}=2.7V$ to $3.6V$
Low-level input voltage	V_{IL}			0.35*VCC	V	$V_{CC}=1.65V$ to $1.95V$
				0.7		$V_{CC}=2.3V$ to $2.7V$
				0.8		$V_{CC}=2.7V$ to $3.6V$
High-level output voltage	V_{OH}	$V_{CC}-0.3$			V	$1.65V \leq V_{CC} \leq 3.6V$, $I_{OH}=-100uA$
		1.05			V	$V_{CC}=1.65V$, $I_{OH}=-4mA$
		1.55			V	$V_{CC}=2.3V$, $I_{OH}=-8mA$

		2.05			V	$V_{CC}=2.7V, I_{OH}=-12mA$
		2.25			V	$V_{CC}=3V, I_{OH}=-12mA$
		2			V	$V_{CC}=3V, I_{OH}=-24mA$
Low-level output voltage	V_{OL}			0.3	V	$1.65V \leq V_{CC} \leq 3.6V, I_{OL}=100\mu A$
				0.6	V	$V_{CC}=1.65V, I_{OL}=4mA$
				0.75	V	$V_{CC}=2.3V, I_{OL}=8mA$
				0.6	V	$V_{CC}=2.7V, I_{OL}=12mA$
				0.8	V	$V_{CC}=3V, I_{OL}=24mA$
Three-state output current	I_{OZ}	-2.5		2.5	μA	$V_{CC}=3.6V, V_O=0 \text{ to } 5.5V$
Off-state leakage output current	I_{off}	-20		20	μA	$V_{CC}=0V, V_I/V_O=5.5V$
Input current	I_I	-1		1	μA	$V_{CC}=3.6V, V_I=V_{CC} \text{ or } GND$
Input capacitance	C_i		4.5		pF	
Output capacitance	C_o		8		pF	

(1) This applies in the disabled state only.

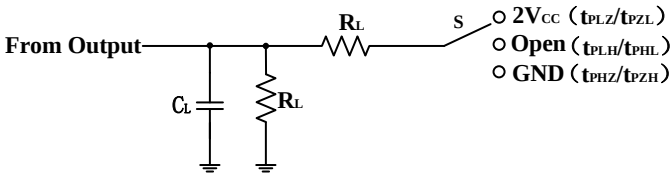
(2) The increasing of supply current for each input that is at one of the specified TTL voltage levels, rather than 0V or V_{CC} .

5.2. Dynamic Characteristics

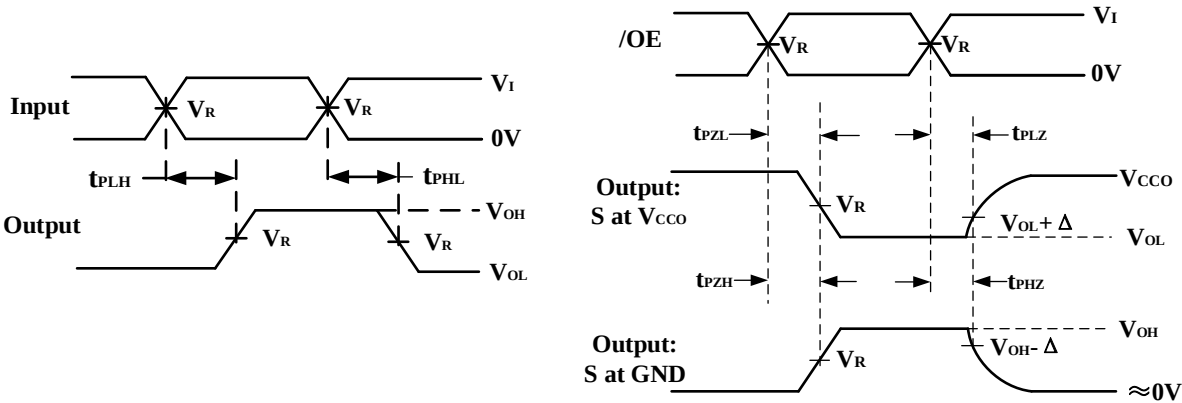
($T_a=-40^\circ C$ to $125^\circ C$. Unless otherwise noted, Typical values are at $T_a=25^\circ C$, See [figure 1](#))

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Propagation Delay	t_{pd}		6.8	15	ns	$V_{CC}=1.65V$
			7.2	15		$V_{CC}=2.5V$
			7.4	15		$V_{CC}=3.3V$
Enable to Data Valid	t_{EN}			25	ns	$V_{CC}=1.65V$
				18		$V_{CC}=2.5V$
				18		$V_{CC}=3.3V$
Disable to tri-state	t_{DIS}			25	ns	$V_{CC}=1.65V$
				18		$V_{CC}=2.5V$
				18		$V_{CC}=3.3V$

5.3. Parameter measurement information



VCC	Input		VR	VCCO	CL	RL	Δ
	VI	ti/tr					
1.65V	VCC	≤2ns	VCC/2	2*VCC	15pF	2kΩ	0.1V
2.5V	VCC	≤2ns	VCC/2	2*VCC	15pF	2kΩ	0.15V
3.3V	2.7V	≤2.5ns	1.5V	6V	15pF	2kΩ	0.3V



Note:

- 1) All input pulses with the following characteristics: PRR ≤1MHz, ZO = 50 Ω, tr ≤ 2.5ns, tf ≤ 2.5ns;
- 2) CL includes probe and test-fixture capacitance.

Figure 5.1 Load Circuit and Voltage Waveforms for NCA8244L

6. Function Description

6.1. Overview

NCA8244L is an octal buffer used for improving driver ability of 3-state memory address, clock drivers, and bus-oriented receivers and transmitters and ensuring the accuracy of signal timing. It provides four channels in each direction with separate output-enable(/OE) inputs low active. When /OE is active, NCA8244L transmits data from A to Y. When /OE is high, the outputs are in the high-impedance state. During power up and power down, /OE should be tied to VCC through a pull-up resistor to ensure the high impedance state. All unused inputs of NCA8244L must be held at VCC or GND to prevent excess ICC.

Table 6.1 Function Table

A_IN ⁽¹⁾	/OE status	VCC status	Y_OUT	Comment
L	L	Ready	L	Normal operation.
H	L	Ready	H	
X	H	Ready	Z	Output Disabled, the output is high impedance.
X	X	Unready	Z	The output follows the same status with the input after VCC is powered on and output is enabled.

(1) L=Logic low; H=Logic high; X=Logic low or logic high.

7. Application Note

7.1. Application Information

The NCA8244L can be used in Motor driver、Traction inverter、IO modules and LED displays. The maximum output current can be up to 24 mA.

7.2. Typical Application Circuit

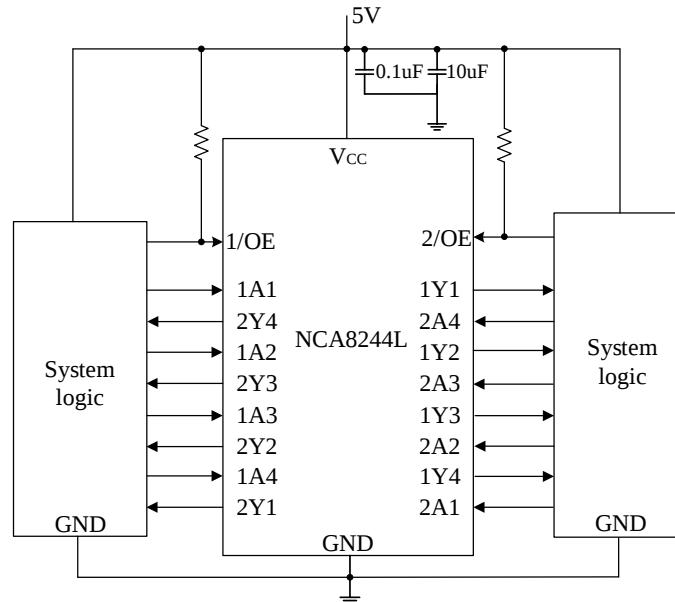
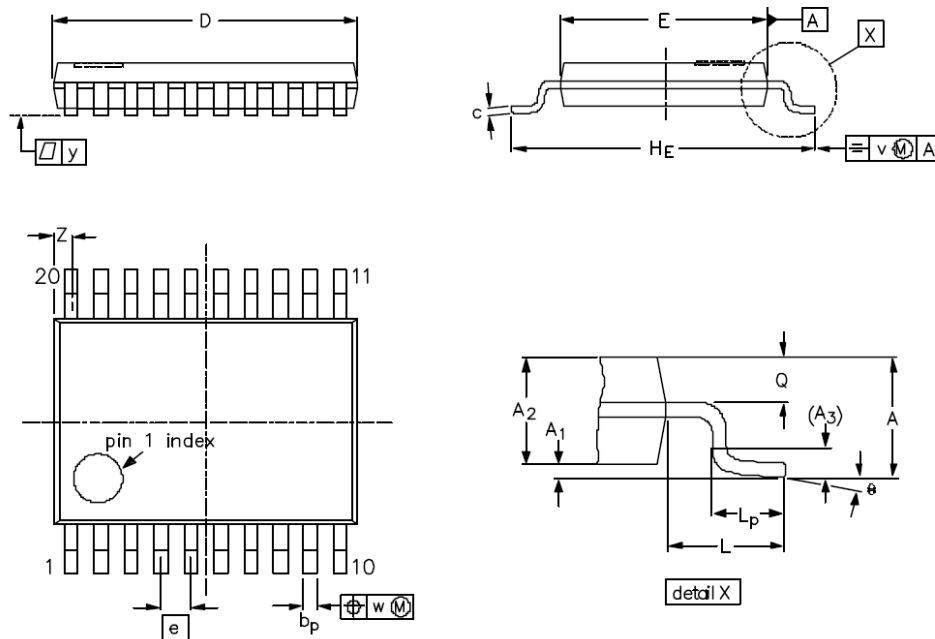


Figure 7.1 Typical application circuit for NCA8244L

8. Package Information



DIMENSIONS (mm are the original dimensions)

UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

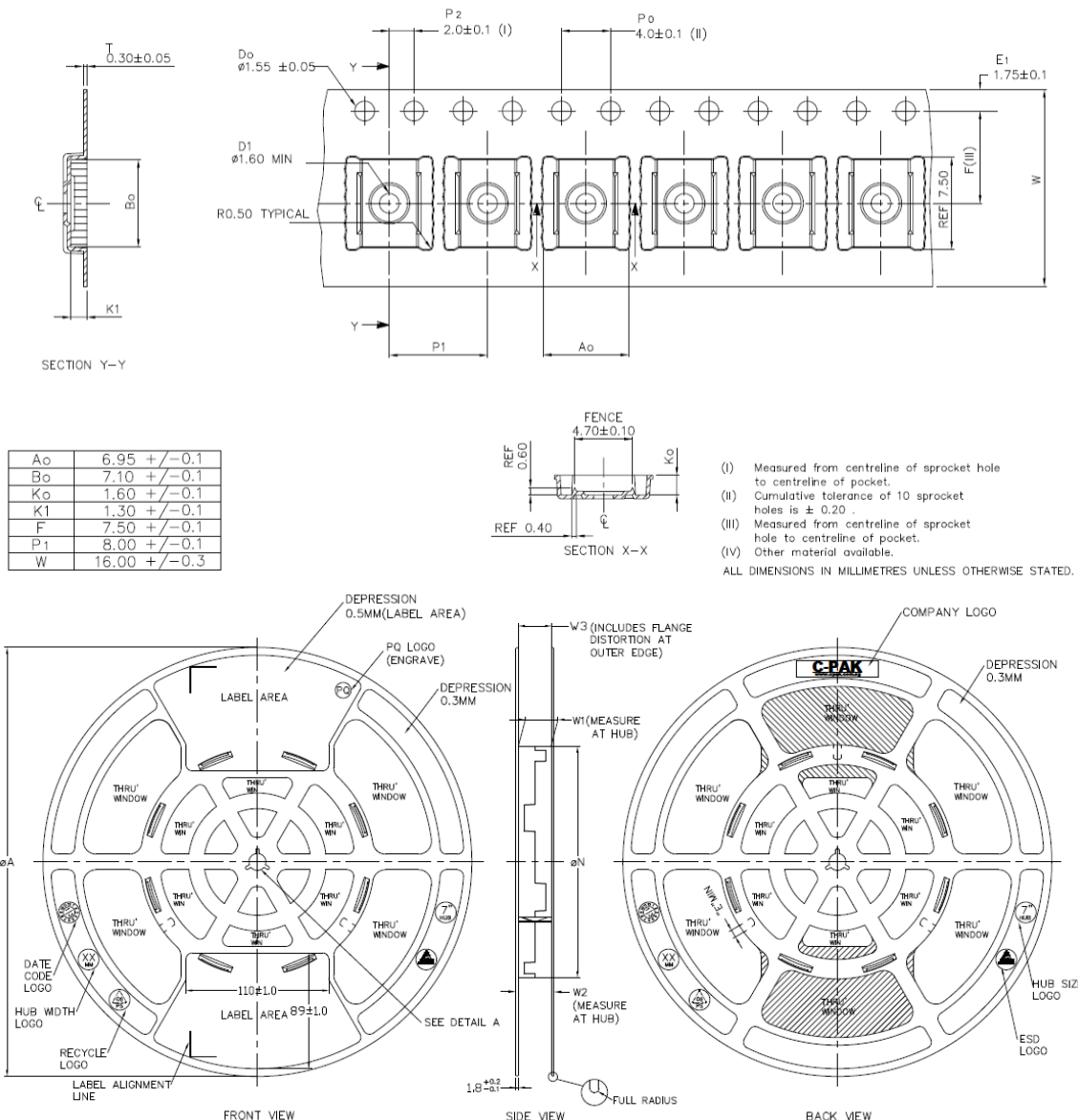
Figure 8.1 TSSOP20 Package Shape and Dimension in millimeters

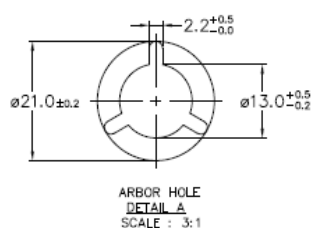
9. Ordering Information

Part Number	PINS	Temperature	MSL	Package Type	Package Drawing	SPQ
NCA8244L-DTSTR	20	-40 to 125 °C	1	TSSOP20	TSSOP20	2500
NCA8244L-Q1TSTR	20	-40 to 125 °C	1	TSSOP20	TSSOP20	2500

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.

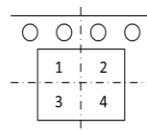
10. Tape and Reel Information





PRODUCT SPECIFICATION					
TAPE WIDTH	ØA ±2.0	ØN ±2.0	W1	W2 (MAX)	W3 (MIN)
08MM	330	178	8.4 ± 0.3	14.4	5.5
12MM	330	178	12.4 ± 0.3	18.4	5.5
16MM	330	178	16.4 ± 0.3	22.4	5.5
24MM	330	178	24.4 ± 0.3	30.4	5.5
32MM	330	178	32.4 ± 0.3	38.4	5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10 ⁹	ANTISTATIC	ALL TYPES
B	10 ⁹ TO 10 ¹¹	STATIC DISSIPATIVE	BLACK ONLY
C	10 ⁹ & BELOW 10 ⁸	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10 ⁸ TO 10 ¹⁰	ANTISTATIC (COATED)	ALL TYPES



Quadrant Designations

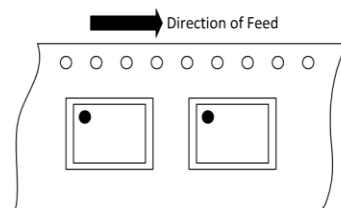


Figure 10.1 Tape and Reel Information of TSSOP

11. Revision History

Revision	Description	Date
1.0	Initial Version.	2023/4/23

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