NOVOSENSE

# NSI6602Vx-DLAMR

# Functional Isolated Dual-Channel Gate Driver

Datasheet (EN) 1.0

## Product Overview

NSI6602Vx-DLAMR is a family of high reliability isolated dual-channel gate driver ICs which can be designed to drive power transistor up to 2MHz switching frequency. Each output could source 6A and sink 8A peak current with fast 33ns propagation delay and 6ns maximum delay matching.

The NSI6602Vx-DLAMR provides 1600Vrms isolation per UL1577 in 4-mm x 4-mm LGA13 package. System robustness is supported by 150kV/us typical common-mode transient immunity (CMTI).

The driver operates with a maximum supply voltage of 25V, while the input-side accepts from 3V to 18V supply voltage. Under voltage lock-out (UVLO) protection is supported by all the power supply voltage pins.

## Key Features

- Isolated dual channel driver
- Input side supply voltage: 3V to 18V
- Driver side supply voltage: up to 25V with UVLO
- 6A peak source and 8A peak sink output
- High CMTI: ±150kV/us typical
- 33ns typical propagation delay
- 6ns maximum delay matching
- 9ns maximum pulse width distortion
- Programmable deadtime
- Accepts minimum input pulse width 20ns
- Operation temperature: -40℃~125℃
- RoHS & REACH Compliant

## Applications

- Isolated DC-DC and AC-to-DC power supplies in server, telecom, and industry
- DC-to-AC solar inverters
- Motor drives and EV charging
- UPS and battery chargers

## Functional Block Diagram

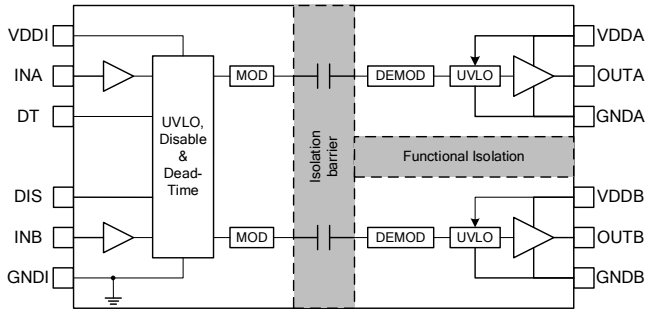



Figure 0.1 NSI6602Vx-DLAMR Block Diagram

# INDEX

# 1. Pin Configuration and Functions

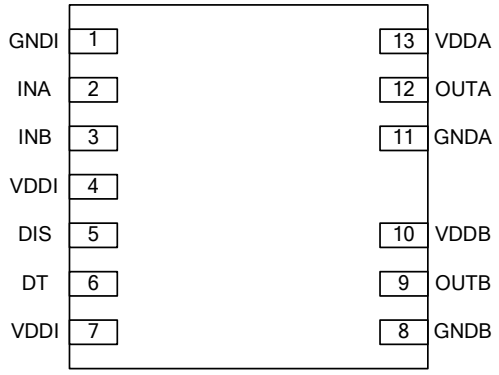



Figure 1.1 NSI6602Vx-DLAMR Package

Table 1.1 NSI6602Vx-DLAMR Pin Configuration and Description

| PIN NO. | SYMBOL | FUNCTION |
|---|---|---|
| 1 | GNDI | Input-side ground reference. |
| 2 | INA | TTL compatible input signal for channel A with internal pull down to GNDI. It is recommended to connect this pin to GNDI if not used. |
| 3 | INB | TTL compatible input signal for channel B with internal pull down to GNDI. It is recommended to connect this pin to GNDI if not used. |
| 4, 7 | VDDI | Input-side supply voltage. It is recommended to place a bypass capacitor from this pin to GNDI as close as possible. |
| 5 | DIS | Disables the isolator inputs and driver outputs if asserted high, enables if asserted low or left open. It is recommended to connect this pin to GNDI if not used. |
| 6 | DT | Programmable deadtime control.<br>• DT pin short to VCCI disables dead time interlock function to allow the outputs overlapping.<br>• DT pin open or floating enables interlock function, deadtime will be typically 8ns.<br>• Place a 1kΩ to 200kΩ resistor ($R_{DT}$) between DT and GNDI to adjust deadtime following: $t_{DT}$ (ns) = 10 x $R_{DT}$ (kΩ).<br>Connecting with a low ESR 2.2nF capacitor to GNDI is recommended to limit the noise interference. |
| 8 | GNDB | Ground for output channel B |
| 9 | OUTB | Output gate driver for channel B |
| 10 | VDDB | Supply voltage for channel B |
| 11 | GNDA | Ground for output channel A |
| 12 | OUTA | Output gate driver for channel A |

| | | |
|---|---|---|
| 13 | VDDA | Supply voltage for channel A |

## 2. Absolute Maximum Ratings

| *Parameters* | *Symbol* | *Min* | *Max* | *Unit* |
|---|---|---|---|---|
| Input Side Supply Voltage | VDDI to GNDI | -0.3 | 24 | V |
| Output Side Supply Voltage | VDDA to GNDA, VDDB to GNDB | -0.3 | 30 | V |
| Input Signal Voltage | INA, INB, DIS, DT to GNDI | -0.3 | $V_{VDDI}$+0.3 | V |
| | INA, INB, DIS, DT to GNDI, Transient for 50ns | -5 | $V_{VDDI}$+0.3 | V |
| Output Signal Voltage | OUTA to GNDA, OUTB to GNDB | -0.3 | $V_{VDDA}$+0.3<br>$V_{VDDB}$+0.3 | V |
| | OUTA to GNDA, OUTB to GNDB, Transient for 200ns | -2 | $V_{VDDA}$+0.3<br>$V_{VDDB}$+0.3 | V |
| Input to Output Isolation Voltage | - | | 1600 | V |
| Junction Temperature | $T_J$ | -40 | 150 | °C |
| Storage Temperature | $T_{stg}$ | -65 | 150 | °C |

## 3. ESD RATINGS

| | *Ratings* | *Value* | *Unit* |
|---|---|---|---|
| Electrostatic discharge | Human body model (HBM), per AEC-Q100-002-RevD<br>● All pins | ±3.0 | kV |
| | Charged device model (CDM), per AEC-Q100-011-RevB<br>● All pins | ±1500 | V |

## 4. Recommended Operating Conditions

| *Parameters* | *Symbol* | *Min* | *Max* | *Unit* |
|---|---|---|---|---|
| Input Side Supply Voltage | VDDI to GNDI | 3 | 18 | V |
| Driver Side Supply Voltage | VDDA to GNDA, VDDB to GNDB | $V_{VDDA\_ON}$, $V_{VDDB\_ON}$ | 25 | V |
| Input Signal Voltage | INA, INB, DIS, DT | 0 | $V_{VDDI}$ | V |
| Ambient Temperature | $T_a$ | -40 | 125 | °C |

# 5. Thermal Information

| *Parameters* | *Symbol* | *LGA13* | *Unit* |
|---|---|---|---|
| Junction-to-ambient thermal resistance[1)] | $R_{JA}$ | 150 | °C/W |
| Junction-to-case(top) thermal resistance[2)] | $R_{JC(top)}$ | 62.3 | °C/W |
| Junction-to-top characterization parameter[3)] | $\Psi_{JT}$ | 10.8 | °C/W |
| Junction-to-board characterization parameter[3)] | $\Psi_{JB}$ | 95.7 | °C/W |

1) Standard JESD51-3 Low Effective Thermal Conductivity Test Board (2s2p) in an environment described in JESD51-2a.

2) Standard JESD51-3 Low Effective Thermal Conductivity Test Board (2s2p) by transient dual interface test method described in JESD51-14.

3) Obtained by Simulating in an environment described in JESD51-2a.

# 6. Specifications

## 6.1. Electrical Characteristics

VDDI=3.3V or 5V, VDDA=VDDB=15V, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at Ta=25℃.

| *Parameter* | *Symbol* | *Min* | *Typ* | *Max* | *Unit* | *Comments* |
|---|---|---|---|---|---|---|
| Input Side Supply | | | | | | |
| VDDI Quiescent Current | $I_{VDDIQ}$ | | 1.0 | 2 | mA | INA=0, INB=0 |
| VDDI Operating Current | $I_{VDDI}$ | | 2 | 3 | mA | Input frequency 500kHz |
| VDDI UVLO Rising Threshold | $V_{VDDI\_ON}$ | 2.5 | 2.7 | 2.9 | V | |
| VDDI UVLO Falling Threshold | $V_{VDDI\_OFF}$ | 2.3 | 2.5 | 2.7 | V | |
| VDDI UVLO Hysteresis | $V_{VDDI\_HYS}$ | | 0.2 | | V | |
| Output Side Supply | | | | | | |
| VDDA/B Quiescent Current, per Channel | $I_{VDDAQ}$, $I_{VDDBQ}$ | | 1 | 2 | mA | INA=0, INB=0 |
| VDDA/B Operation Current, per Channel | $I_{VDDA}$, $I_{VDDB}$ | | 3 | 4.5 | mA | 100pF, 500kHz, VDDx=15V |
| VDDA/B UVLO Rising Threshold | $V_{VDDA\_ON}$, $V_{VDDB\_ON}$ | 5.7 | 6.15 | 6.5 | V | NSI6602VA-DLAMR (6V) |
| VDDA/B UVLO Falling Threshold | $V_{VDDA\_OFF}$, $V_{VDDB\_OFF}$ | 5.4 | 5.85 | 6.2 | V | |
| VDDA/B UVLO Hysteresis | $V_{VDDA\_HYS}$, $V_{VDDB\_HYS}$ | | 0.3 | | V | |
| VDDA/B UVLO Rising Threshold | $V_{VDDA\_ON}$, $V_{VDDB\_ON}$ | 8.1 | 8.5 | 8.9 | V | NSI6602VB-DLAMR (8V) |
| VDDA/B UVLO Falling Threshold | $V_{VDDA\_OFF}$, $V_{VDDB\_OFF}$ | 7.6 | 8.0 | 8.4 | V | |
| VDDA/B UVLO Hysteresis | $V_{VDDA\_HYS}$, $V_{VDDB\_HYS}$ | | 0.5 | | V | |
| VDDA/B UVLO Rising Threshold | $V_{VDDA\_ON}$, $V_{VDDB\_ON}$ | 12.7 | 13.2 | 13.7 | V | NSI6602VC-DLAMR (12V) |
| VDDA/B UVLO Falling Threshold | $V_{VDDA\_OFF}$, $V_{VDDB\_OFF}$ | 11.7 | 12.2 | 12.7 | V | |
| VDDA/B UVLO Hysteresis | $V_{VDDA\_HYS}$, $V_{VDDB\_HYS}$ | | 1 | | V | |
| VDDA/B UVLO Rising Threshold | $V_{VDDA\_ON}$, $V_{VDDB\_ON}$ | 3.9 | 4.2 | 4.4 | V | NSI6602VD-DLAMR (4V) |
| VDDA/B UVLO Falling Threshold | $V_{VDDA\_OFF}$, $V_{VDDB\_OFF}$ | 3.5 | 3.8 | 4.1 | V | |
| VDDA/B UVLO Hysteresis | $V_{VDDA\_HYS}$, $V_{VDDB\_HYS}$ | | 0.4 | | V | |
| Input Side Characteristic | | | | | | |
| Input Pin Pull Down Resistance, INA, INB | $R_{INA\_PD}$, $R_{INB\_PD}$ | 80 | 100 | 125 | kΩ | |
| Input Pin Pull Down Resistance, DIS (EN) | $R_{DIS\_PD}$ | 80 | 100 | 125 | kΩ | |
| Logic High Input Threshold | $V_{INA\_H}$, $V_{INB\_H}$, $V_{DIS\_H}$ | 1.5 | 1.8 | 2 | V | |
| Logic Low Input Threshold | $V_{INA\_L}$, $V_{INB\_L}$, $V_{DIS\_L}$ | 0.8 | 1.1 | 1.4 | V | |
| Input Hysteresis | $V_{INA\_HYS}$, $V_{INB\_HYS}$, $V_{DIS\_HYS}$ | | 0.7 | | V | |

| Parameter | Symbol | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| Output Side Characteristic | | | | | | |
| Logic High Output Voltage | $V_{VDDA}$-$V_{OUTA\_H}$, $V_{VDDB}$-$V_{OUTB\_H}$ | | 0.1 | | V | $I_{out}$ = 100mA |
| Logic Low Output Voltage | $V_{OUTA\_L}$, $V_{OUTB\_L}$ | | 35 | | mV | $I_{out}$ = -100mA |
| Output Source Resistance | $R_{OUTA\_H}$, $R_{OUTB\_H}$ | | 1 | | Ω | $I_{out}$ = 100mA |
| Output Sink Resistance | $R_{OUTA\_L}$, $R_{OUTB\_L}$ | | 0.35 | | Ω | $I_{out}$ = -100mA |
| Peak Output Source Current | $I_{OUTA+}$, $I_{OUTB+}$ | | 6 | | A | |
| Peak Output Sink Current | $I_{OUTA-}$, $I_{OUTB-}$ | | 8 | | A | |

## 6.2. Switching Characteristics

VDDI=3.3V or 5V, VDDA=VDDB=15V, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at Ta=25℃.

| Parameter | Symbol | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| Minimum Pulse Width | $t_{PWmin}$ | | 15 | 25 | ns | |
| Propagation Delay | $t_{PDHL}$, $t_{PDLH}$ | | 33 | 45 | ns | |
| Pulse Width Distortion $\lvert t_{PDLH}-t_{PDHL}\rvert$ | $t_{PWD}$ | | | 9 | ns | |
| Channel to Channel Delay Matching | $t_{DMLH}$, $t_{DMHL}$ | | | 6 | ns | |
| Programmed Deadtime | $t_{DT}$ | 160 | 200 | 240 | ns | $t_{DT}$(ns)=10*R(kΩ); Test for R = 20kΩ |
| Output Rise Time (10% to 90%) | $t_R$ | | 15 | | ns | CL=1.8nF，VDDx=15V |
| Output Fall Time (90% to 10%) | $t_F$ | | 15 | | ns | CL=1.8nF，VDDx=15V |
| Shutdown Time from Disable True | $t_{DIS}$ | | 50 | 80 | ns | |
| Recovery Time from Disable False | $t_{EN}$ | | 50 | 80 | ns | |
| VDDI Power-up Time Delay<br>(Time from VDDI = $V_{VDDI\_ON}$ to OUTA/B = INA/B) | $t_{start\_VDDI}$ | | 12 | 25 | μs | INA or INB tied to VDDI |
| VDDA/B Power-up Time Delay<br>(Time from VDDA/B = $V_{VDD\_ON}$ to OUTA/B = INA/B) | $t_{start\_VDDA}$, $t_{start\_VDDB}$ | | 18 | 26 | μs | INA or INB tied to VDDI<br>$C_{OUTA/B}$=1.8nF |
| Common Mode Transient Immunity | CMTI | 100 | 150 | | kV/ μs | verified by design |

## 6.3. Typical Performance Characteristics

VDDI=3.3V or 5V, VDDA=VDDB=15V, TA = 25°C. Output has no load unless otherwise noted.

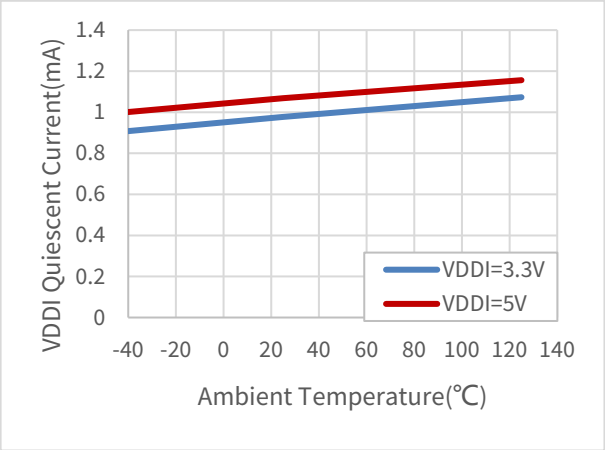



Figure 6.1 VDDI Quiescent Current vs Temperature

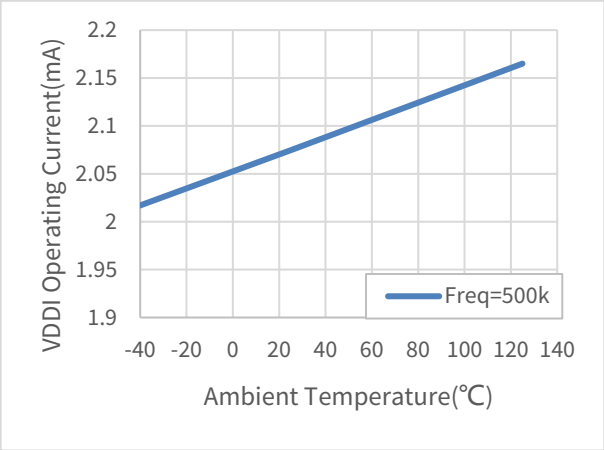



Figure 6.2 VDDI Operating Current vs Temperature

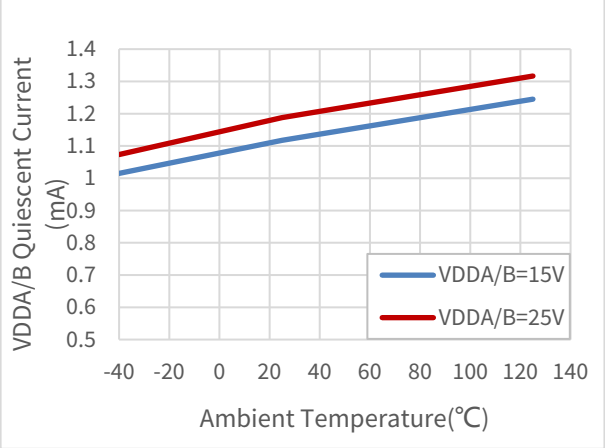



Figure 6.3 VDDA/B Quiescent Current vs Temperature

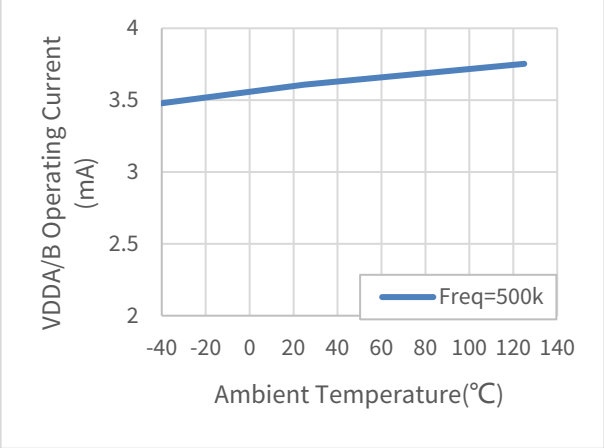



Figure 6.4 VDDA/B Operating Current vs Temperature

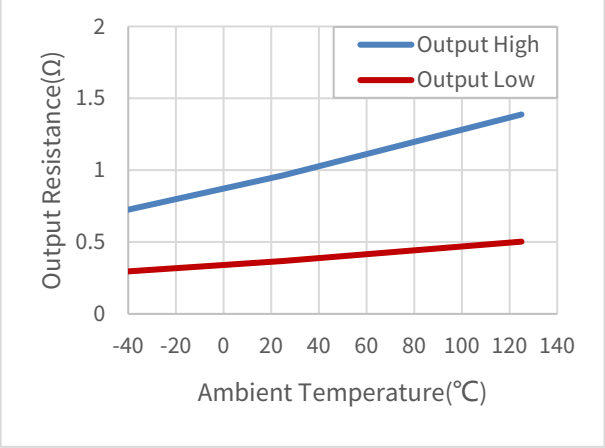



Figure 6.5 Output Resistance vs Temperature

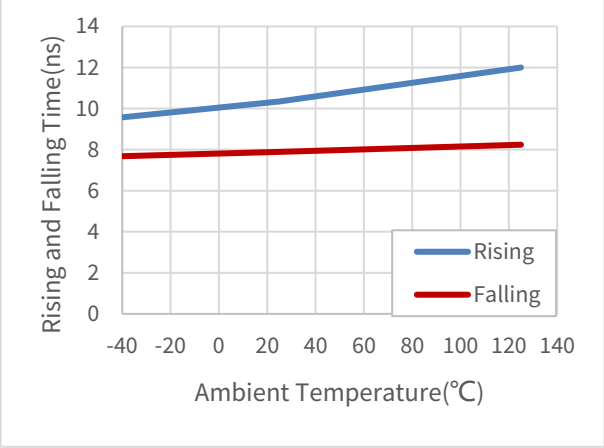



Figure 6.6 Typical Rise Time & Fall Time vs Temperature

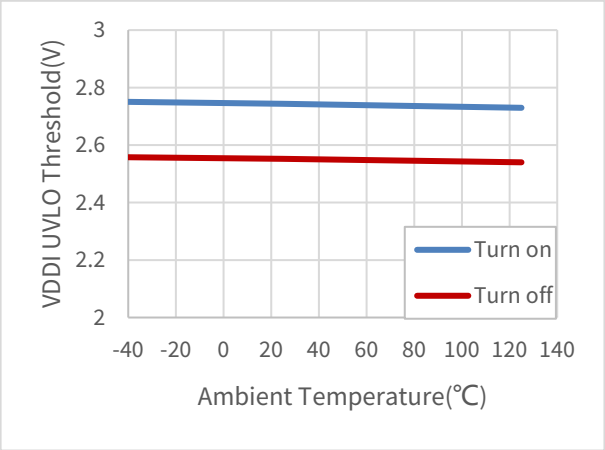



Figure 6.7 VDDI UVLO Threshold vs Temperature

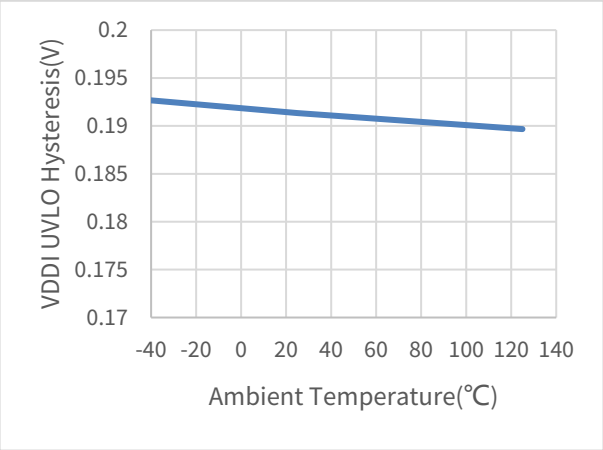



Figure 6.8 VDDI UVLO Hysteresis vs Temperature

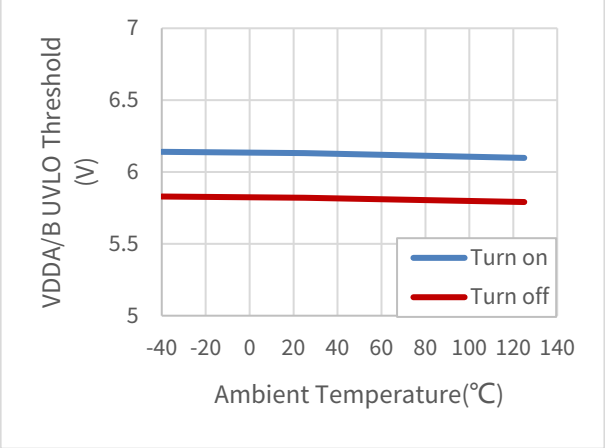



Figure 6.9 6V VDDA/B UVLO Threshold vs Temperature

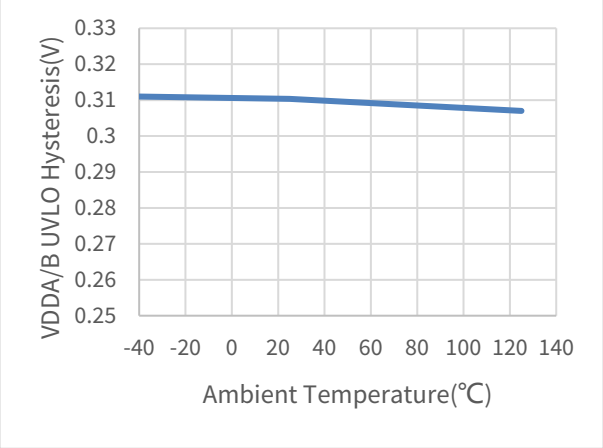



Figure 6.10 6V VDDA/B UVLO Hysteresis vs Temperature

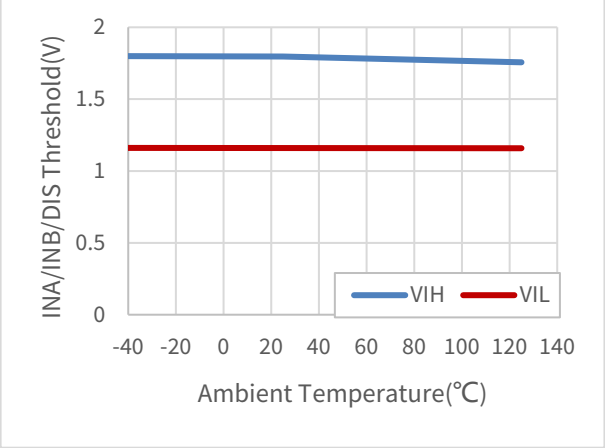



Figure 6.11 INA/INB/DIS Threshold vs Temperature

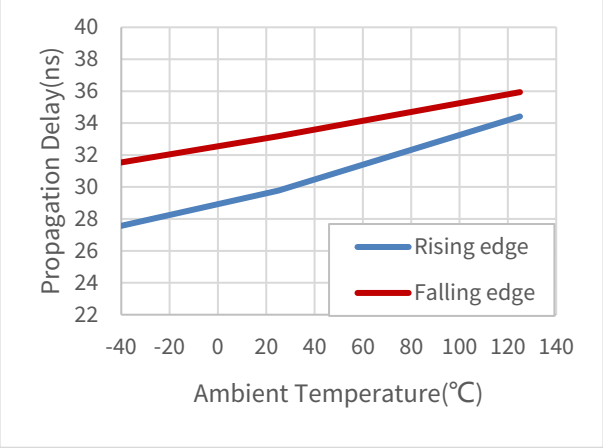



Figure 6.12 Propagation Delay vs Temperature

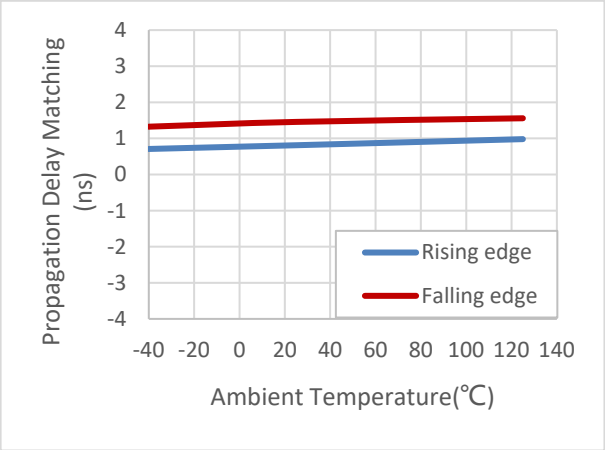



Figure 6.13 Propagation Delay Matching vs Temperature

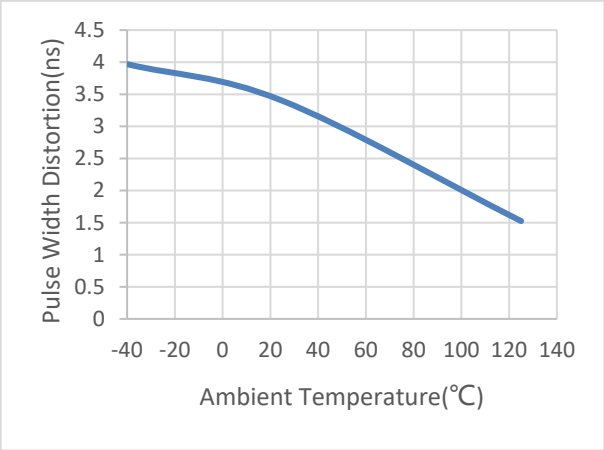



Figure 6.14 Pulse Width Distortion vs Temperature

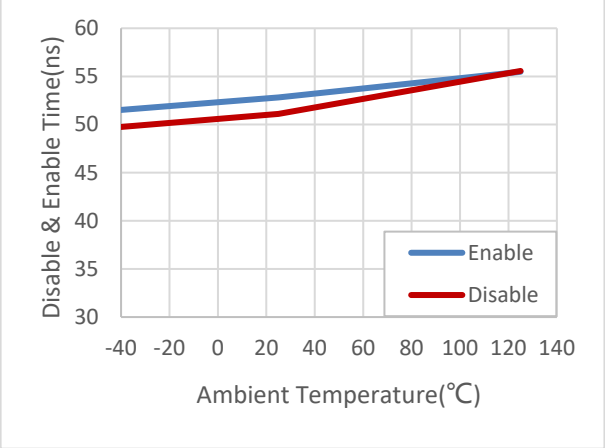



Figure 6.15 Disable & Enable Time vs Temperature

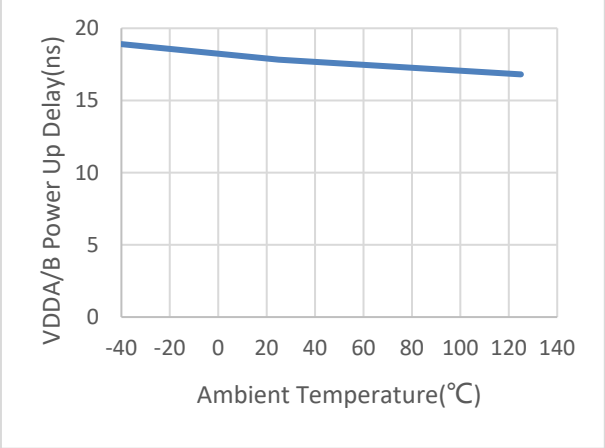



Figure 6.16 VDDA/B power up delay vs Temperature

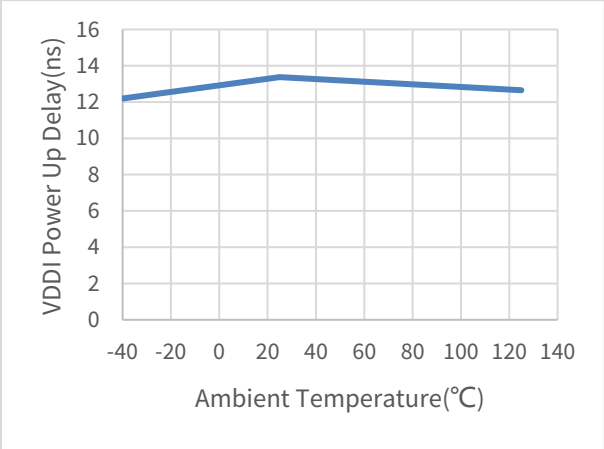



Figure 6.17 VDDI power up delay vs Temperature

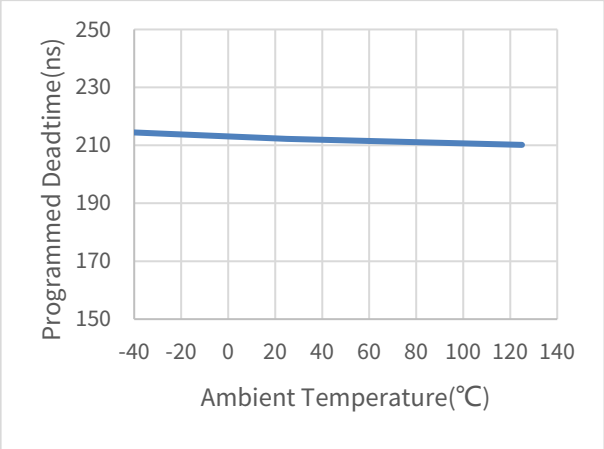



Figure 6.18 Deadtime (RDT=20kΩ) vs Temperature

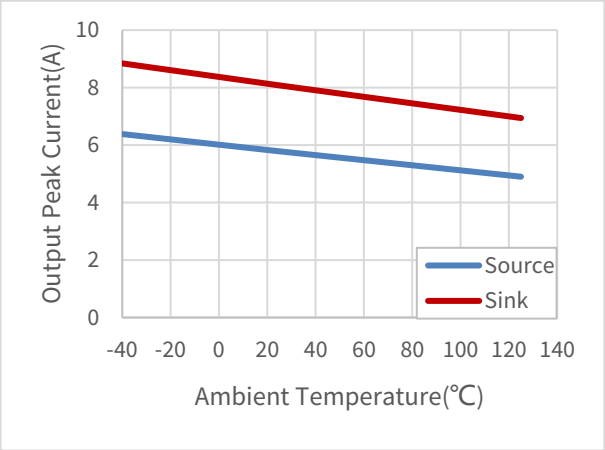



Figure 6.19 Peak current vs Temperature

## 6.4. Parameter Measurement Information

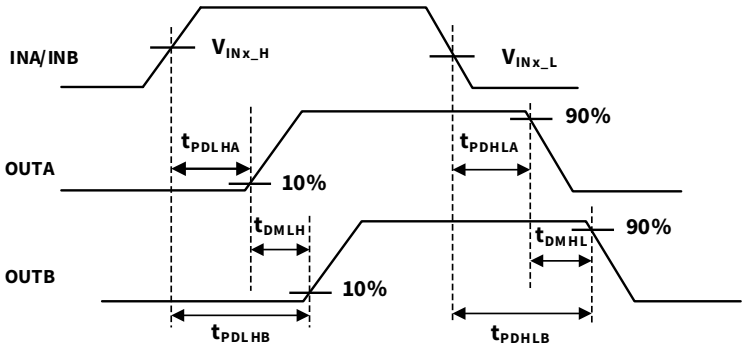



Figure 6.20 Propagation Delay and Channel to Channel Delay Match Time, connect DT to VDDI

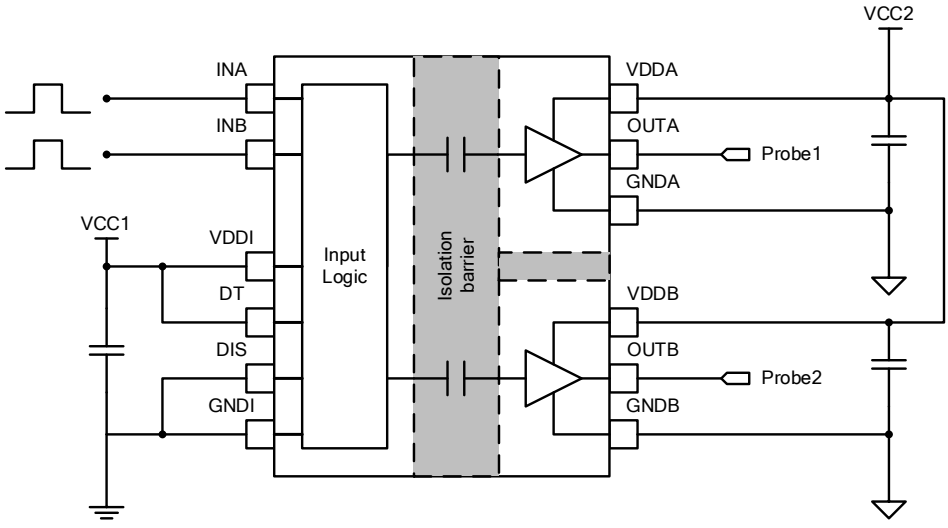



Figure 6.21 Channel to Channel Delay Match Test Circuit

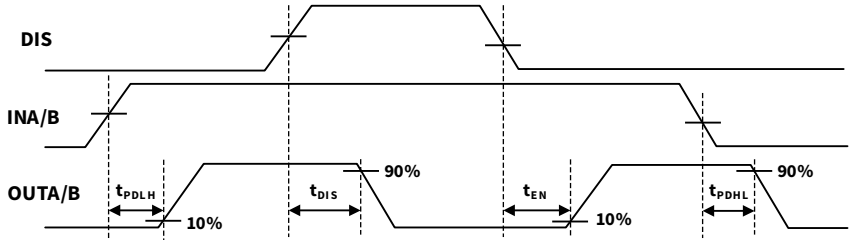



Figure 6.22 Disable Time and Enable Time

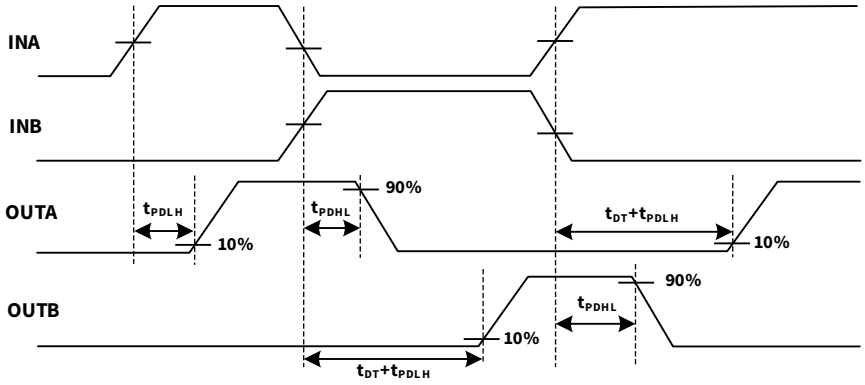



Figure 6.23 Deadtime, Determined by RDT

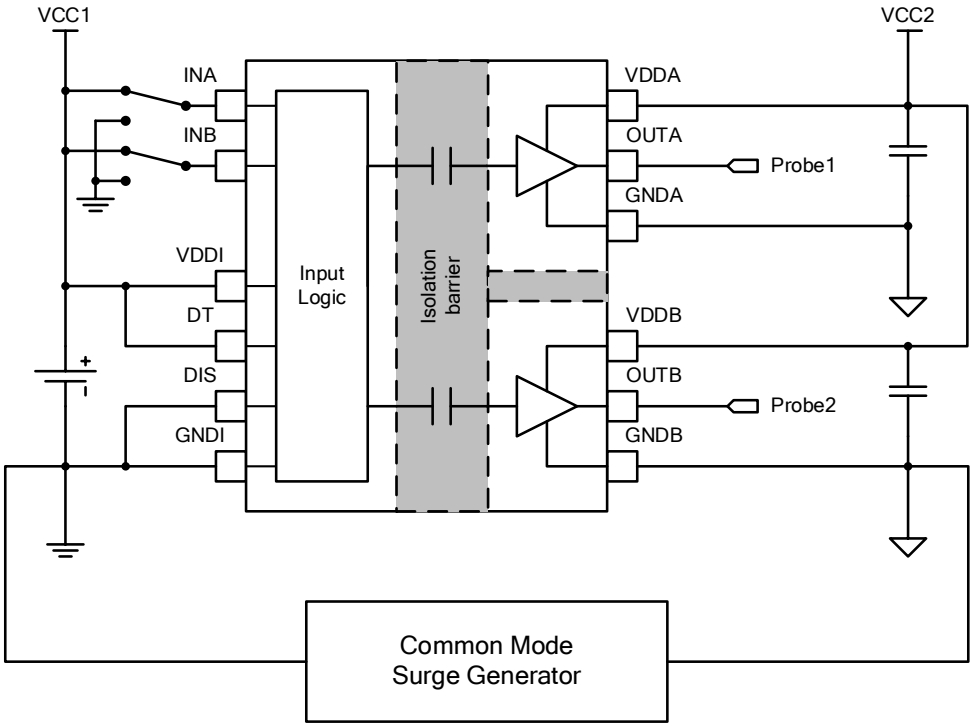



Figure 6.24 Common-Mode Transient Immunity Test Circuit

# 7. High Voltage Feature Description

## 7.1. Insulation Characteristics

| Description | Test Condition | Symbol | Value | Unit |
|---|---|---|---|---|
| Min. External Air Gap (Clearance) | | CLR | 3.0 | mm |
| Min. External Tracking (Creepage) | | CPG | 3.0 | mm |
| Distance through the Insulation | | DTI | 28 | um |
| Comparative Tracking Index | DIN EN 60112 (VDE 0303-11) | CTI | >600 | V |
| Material Group | IEC 60664-1 | | I | |
| Isolation Resistance | VIO = 500 V, Tamb = $T_S$ | $R_{IO}$ | $>10^9$ | Ω |
| Isolation Capacitance | f = 1MHz | $C_{IO}$ | 1.2 | pF |

## 7.2. Safety-Limiting Values

Basic isolation safety-limiting values as outlined in VDE-0884-11 of NSI6602Vx-DLAMRx

| Description | Test Condition | Side | Value | Unit |
|---|---|---|---|---|
| Safety Supply Power | $R_{\theta JA}$ = 150 °C/W[1)], $T_J$ = 150 °C, $T_A$ = 25 °C | Input | 90 | mW |
| | | Driver A, Driver B | 355 | mW |
| | | Total | 800 | mW |
| Safety Supply Current | $R_{\theta JA}$ = 150 °C/ W[1)], VDDA/B = 12V, $T_J$ = 150 °C, $T_A$ = 25 °C | Driver A, Driver B | 29.6 | mA |
| | $R_{\theta JA}$ =150 °C/ W[1)], VDDA/B = 25V, $T_J$ = 150 °C, $T_A$ = 25 °C | Driver A, Driver B | 14.2 | mA |
| Safety Temperature[2)] | | | 150 | °C |

1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of LGA13 4mm x 4mm package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (2s2p) according to JESD51-3.

2) The maximum safety temperature has the same value as the maximum junction temperature ($T_J$) specified for the device.

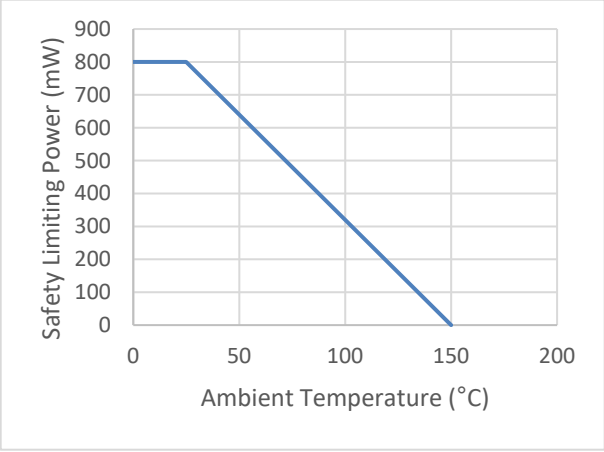



Figure 7.1 NSI6602Vx-DLAMRx Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature.

# 8. Function Description

## 8.1. Overview

NSI6602Vx-DLAMR is a high reliability dual channel isolated gate driver which could be designed in variety switching power and motor drive topologies. NSI6602Vx-DLAMR has some useful protections, such as under voltage lock out (UVLO) for both input and output supply, a disable pin, deadtime control, default low output as input is floating. The functional circuit block diagram is shown as below:

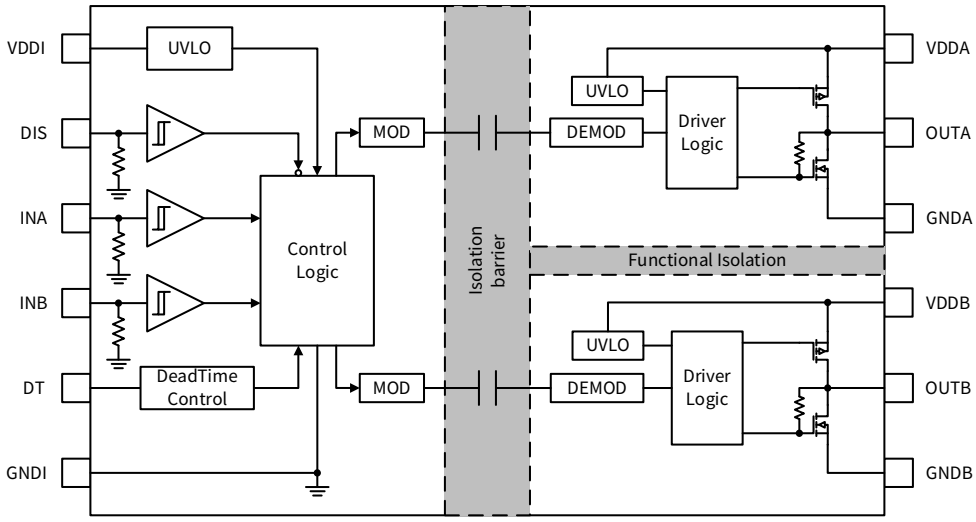



Figure 8.1 Functional Block Diagram

## 8.2. Undervoltage Lockout (UVLO)

The NSI6602Vx-DLAMR has an internal under voltage lock out (UVLO) protection on both input and output supply circuit blocks. The driver output is held low by an active clamp circuit when the supply voltage of VDDI or VDDA/VDDB is lower than $V_{VDD\_ON}$ at power-up status or lower than $V_{VDD\_OFF}$ after power-up, regardless of the status of the input pins.

The VDDI and VDDA/B ULVO protections have hysteresis ($V_{VDD\_HYS}$) to prevent chatter noise from VDD supply and allow small drops in supply power which are usually happened in startup.

## 8.3. Input and Output Logic Table

When the device is power up, setting the DIS pin high can shut down both outputs simultaneously. Left open or grounding the DIS pin can allow the device operating normally.

Table 8.1 Output status vs Input and Power status

| VDDI status | VDDA/B status | DIS | IN | | OUT | | NOTE[1] |
|---|---|---|---|---|---|---|---|
| | | | A | B | A | B | |
| PU | PU | L or O | L | H | L | H | If Deadtime function is used, output transits to high after the deadtime expires. |
| PU | PU | L or O | H | L | H | L | |
| PU | PU | L or O | H | H | H | H | DT pin is pulled to VDDI. |
| PU | PU | L or O | H | H | L | L | DT is left open or programmed with $R_{DT}$. |
| PU | PU | L or O | L | L | L | L | |
| PU | PU | L or O | O | O | L | L | |
| PU | PU | H | X | X | L | L | |
| PU | PD | X | X | X | L | L | |
| PD | PU | X | X | X | L | L | |

1) PD= Power Down; PU= Power Up; H= Logic High; L= Logic Low; O= Left Open; X= Irrelevant.

## 8.4. Programmable Deadtime (DT pin)

### 8.4.1. Pulling the DT Pin to VDDI

This allows outputs match inputs completely and no deadtime is asserted.

### 8.4.2. DT Pin Left Open or Connected to a Programming Resistor between DT and GNDI Pins

If the DT pin is left open, the deadtime duration ($t_{DT}$) is set to <35ns. $t_{DT}$ can be programmed by placing a resistor, $R_{DT}$, between the DT pin and GNDI. The appropriate $R_{DT}$ value can be determined from Equation 1, where $R_{DT}$ is in kΩ and $t_{DT}$ in ns:

$$t_{DT} \approx 10 \times R_{DT} \quad (1)$$

The recommended value of $R_{DT}$ is between from 1kΩ to 200kΩ. The steady state voltage at DT pin is about 0.8V and the DT pin current will be less than 10uA when $R_{DT}$ =100kΩ. It is also recommended to parallel a ceramic capacitor, for example 2.2nF, with $R_{DT}$ to achieve better noise immunity.

The programmed deadtime is activated by the input signal's falling edge to prevent shoot-through when the device is designed in an application of high side and low side driver. The details of input and output logic with deadtime are shown as Figure 8.2:

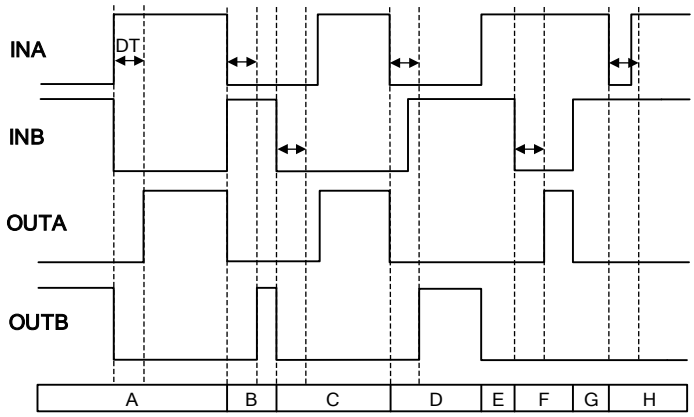



Figure 8.2 Input and Output Logic with the Programmed Deadtime

| *Condition* | *Result* |
|---|---|
| A: INA goes high, and INB goes low. | OUTB goes low immediately, then OUTA goes high after the programmed deadtime which is assigned at INB goes low. |
| B: INA goes low, and INB goes high. | OUTA goes low immediately, then OUTB goes high after the programmed deadtime which is assigned at INA goes low. |
| C: INB goes low, then INA goes high after deadtime. | OUTB goes low immediately, then OUTA goes high immediately when INA goes high. |
| D: INA goes low, then INB goes high before deadtime. | OUTA goes low immediately, then OUTB goes high after deadtime |
| E: INA goes high, INB is still high. | OUTB goes low immediately and OUTA keeps low. |
| F: INA is still high, INB goes low. | OUTA goes high after deadtime while INB is low and OUTB keeps low. |
| G: INA is still high, INB goes high after deadtime | OUTA goes low immediately and OUTB keeps low. |
| H: INA goes low then goes high before deadtime while INB is still high. | OUTA keeps low and OUTB keeps low because deadtime control. |

## 8.5. ESD Protection

Figure 8.3 shows the multiple diodes involved in the ESD protection part of NSI6602Vx-DLAMR.

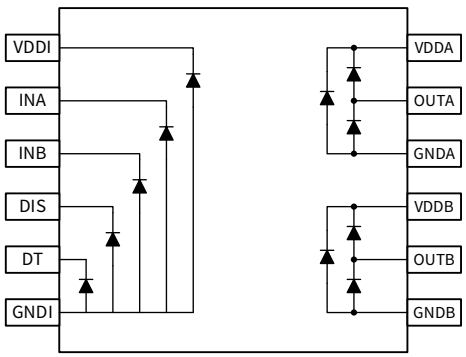


Figure 8.3 ESD Structure

# 9. Application Note

## 9.1. Typical Application Circuit

The circuit shows a typical half-bridge configuration by using the driver NSI6602Vx-DLAMR which could be used in several popular power converter topologies such as half-bridge/ full bridge / LLC isolated topologies, buck-boost topologies and 3-phase motor drive applications.

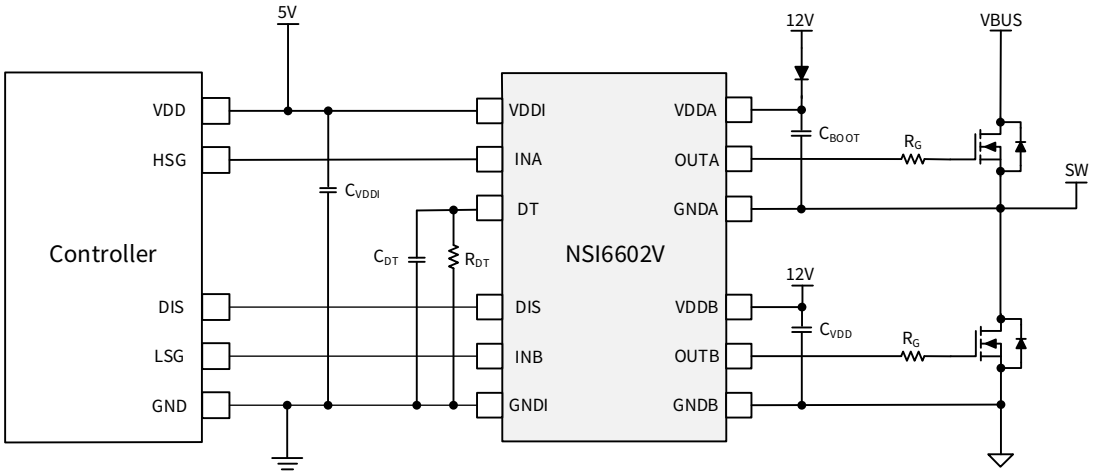


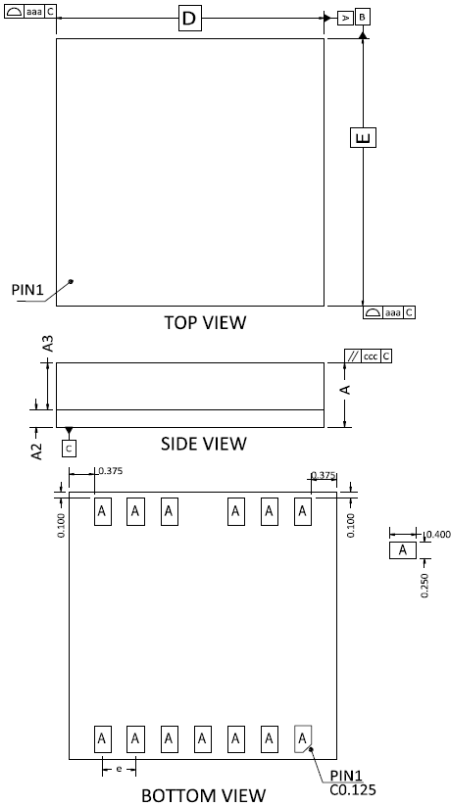

Figure 9.1 Typical Half-Bridge Application Schematic

## 9.2. PCB Layout

PCB layout is important to get optimal performance. Some key guidelines are given as below:

- Low-ESR and low-ESL bypass capacitors should be placed close to the device between pin VDDI to GNDI and pin VDDA/B to GNDA/B.
- There is high frequency switching current that charges and discharges the gate of external power transistor, leading to EMI and ring issues. The parasitic inductance of this loop should be minimized, by decreasing loop area and placing NSI6602Vx-DLAMR close to power transistor.
- Large amount of copper should be placed at VDDA/B pin and GNDA/B pin for thermal dissipation.
- To ensure isolation performance between primary and secondary side, the space under the device should keep free from any plane, trace, pad or via.

# 10. Package information




| MILLIMETER | | | |
|---|---|---|---|
| SYMBOL | MIN | NOR | MAX |
| A | 0.77 | 0.85 | 0.93 |
| A2 | 0.22 | 0.25 | 0.28 |
| A3 | 0.55 | 0.60 | 0.65 |
| D | 3.90 | 4.00 | 4.10 |
| E | 3.90 | 4.00 | 4.10 |
| e | 0.50 BSC | | |
| aaa | 0.10 | | |
| ccc | 0.05 | | |

Figure 10.1 Package Shape and Dimension

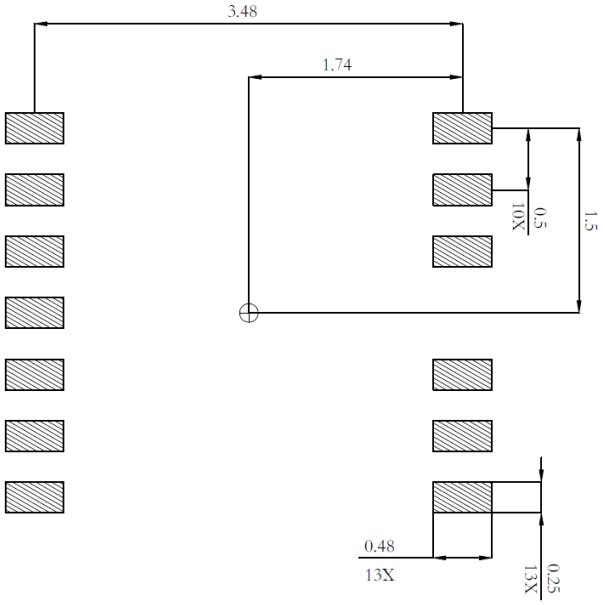



Figure 10.2 Package Board Layout Example(mm)

# 11. Ordering Information

| *Part No.* | *Driver-side UVLO TYP.* | *Temperature* | *Body Size (mm)* | *MSL* | *SPQ* |
|---|---|---|---|---|---|
| NSI6602VA-DLAMR | 6V | -40 to 125℃ | 4x4x0.85 | 3 | 2500 |
| NSI6602VB-DLAMR | 8V | -40 to 125℃ | 4x4x0.85 | 3 | 2500 |
| NSI6602VC-DLAMR | 13V | -40 to 125℃ | 4x4x0.85 | 3 | 2500 |
| NSI6602VD-DLAMR | 4V | -40 to 125℃ | 4x4x0.85 | 3 | 2500 |

# 12. Tape and Reel Information

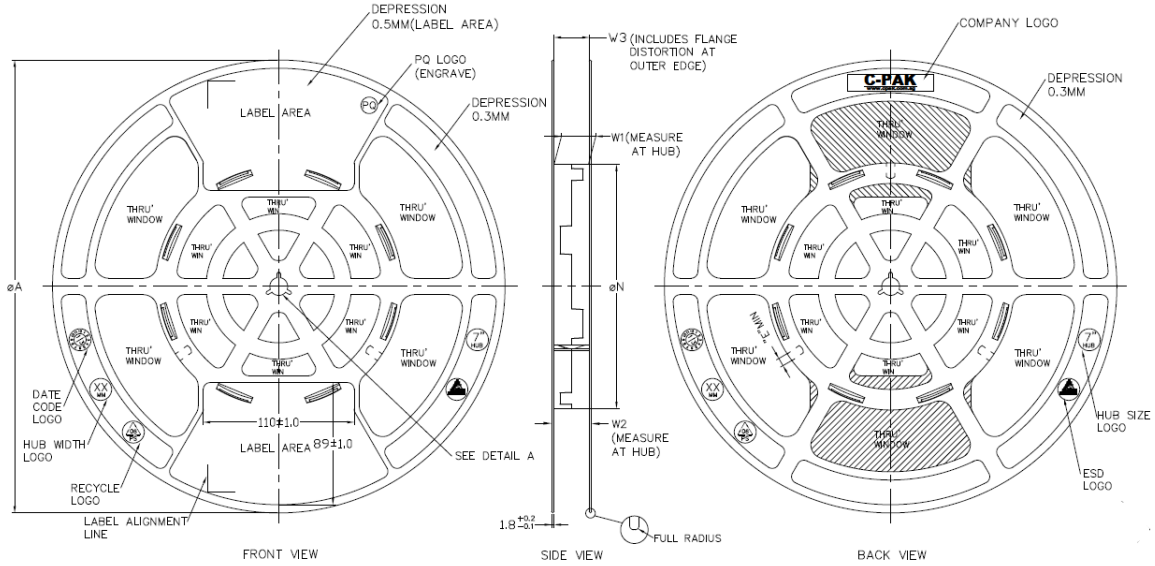



Figure 12.1 Tape Information

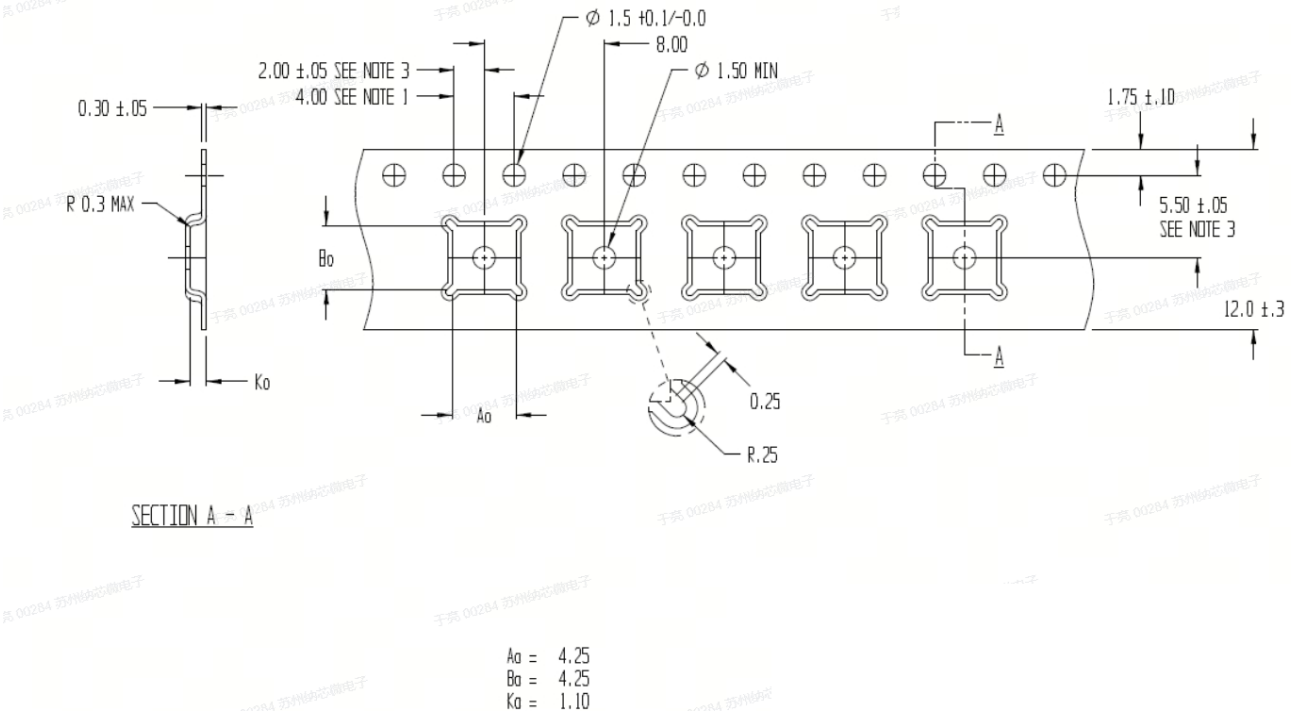



Figure 12.2 Reel Information

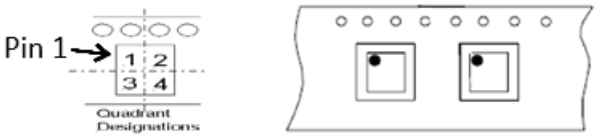



Figure 12.3 Quadrant Designation for Pin1 Orientation in Tape

# 13. Revision History

| Revision | Description | Date |
|---|---|---|
| 1.0 | Initial version | 2025/1/10 |

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