NOVOSENSE

NSI1200C
High Reliability Reinforced Isolated Amplifier
Datasheet (EN) 1.1

Product Overview

NSI1200C is a high-performance isolated amplifier with output separated from input based on the NOVOSENSE capacitive isolation technology. The device has a linear differential input signal range of ±250mV (±320mV full-scale). The differential input is ideally suited to shunt resistor-based current sensing in high voltage applications where isolation is required.

The device has a fixed gain of 8.0 and provides a differential analog output.

The low offset and gain drift ensure the accuracy over the entire temperature range. High common-mode transient immunity ensures that the device is able to provide accurate and reliable measurements even in the presence of high-power switching such as in motor control applications.

The fail-safe functions including input common-mode overvoltage detection and missing VDD1 detection simplify system-level design and diagnostics.

Key Features

- Up to 5000V_{rms} Insulation voltage
- ±250mV linear Input Voltage Range
- Fixed Gain: 8.0
- Low Offset Error and Drift:
  ±0.5mV (Max), ±5μV/°C (Max)
- Low Gain Error and Drift:
  ±0.3% (Max), ±30ppm/°C (Max)
- Low Nonlinearity and Drift:
  ±0.05% (Max), ±1ppm/°C (Typ)
- SNR: 72dB (Typ, BW=100kHz)
- Wide bandwidth: 220kHz (Typ)
- High CMTI: 125kV/μs (Typ)
- System-Level Diagnostic Features:
  - VDD1 monitoring
  - Input common-mode overvoltage detection
- Operation Temperature: -40°C ~125°C
- RoHS-Compliant Packages:
  SOP8(300mil), DUB8, SOP8(150mil)

Safety Regulatory Approvals

- UL recognition:
  - SOW8, DUB8: 5000V_{rms} for 1 minute per UL1577
  - SOP8: 3000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Shunt current monitoring
- Motor Drives
- Uninterruptible Power Suppliers
- Solar Inverters

Device Information

Part Number	Package	Body Size
NSI1200C-DSWVR	SOP8(300mil)	5.85mm × 7.50mm
NSI1200C-DDBR	DUB8	9.32mm × 6.40mm
NSI1200C-DSPR	SOP8(150mil)	4.90mm × 3.90mm

Functional Block Diagrams

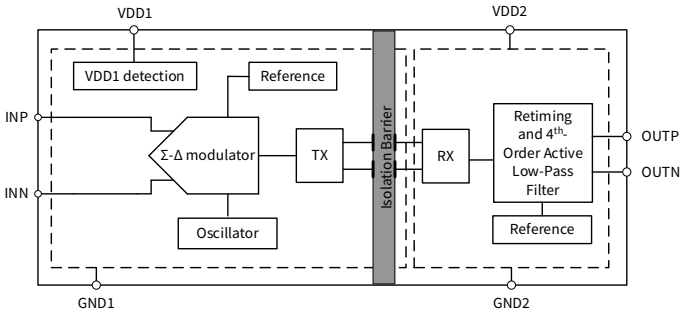

Figure 1. NSI1200C Block Diagram

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INDEX

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1. Pin Configuration and Functions

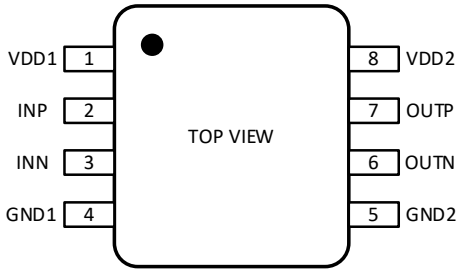

Figure 1.1 NSI1200C Package

Table 1.1 NSI1200C Pin Configuration and Description

NSI1200C PIN NO.	*SYMBOL*	*FUNCTION*
1	VDD1	Power supply for input side (3.0V to 5.5V)
2	INP	Positive analog input (±250mV recommended for NSI1200C)
3	INN	Negative analog input
4	GND1	Ground 1, the ground reference for input side
5	GND2	Ground 2, the ground reference for output side
6	OUTN	Negative output
7	OUTP	Positive output
8	VDD2	Power supply for output side (3.0V to 5.5V)

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2. Absolute Maximum Ratings(1)

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage(2)	VDD1, VDD2	-0.3		6.5	V
Input Voltage	INP, INN	GND1-6		VDD1+0.5	V
Output Voltage	OUTP, OUTN	GND2-0.5		VDD2+0.5	V
Input current per IO Pin	I_{in}	-10		10	mA
Junction Temperature	T_J	-40		150	°C
Storage Temperature	T_{STG}	-55		150	°C

(1) The device cannot operate beyond the listed Absolute Maximum Ratings to prevent permanent device damage. The device is not fully functional if operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings. Long-time stress of the absolute maximum conditions may affect the device lifetime.

(2) VDD1 to GND1, VDD2 to GND2

3. ESD Ratings(1)

Parameters	Test condition	Value	Unit
Electrostatic discharge (ESD)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±4000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(3)	±1000	V

(1) Though this device features proprietary protection circuitry, proper ESD precautions should be considered to avoid performance degradation of damage due to high energy ESD event. Charged devices and circuit boards may discharge without detection.

(2) Safe manufacturing requires 500-V HBM and standard ESD precautions, per JEDEC document JEP155.

(3) Safe manufacturing requires 250-V CDM and standard ESD precautions, per JEDEC document JEP157.

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Side1 Power Supply	VDD1	3.0	5.0	5.5	V
Side2 Power Supply	VDD2	3.0	3.3	5.5	V
Differential input voltage before clipping output	$V_{Clipping}$		±320		mV
Linear differential input full scale voltage	V_{FSR}	-250		250	mV
Operating common-mode input voltage	V_{CM}	-0.16		2.6	V
Operating Ambient Temperature	T_A	-40		125	°C

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5. Thermal Information

Parameters	Symbol	SOP8(150mil)	DUB8	SOP8(300mil)	Unit
Junction–to-ambient thermal resistance	$R_{\theta JA}$	137.7	76	86	°C/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	54.9	58	28	°C/W
Junction-to-board thermal resistance	$R_{\theta JB}$	71.7	40	42	°C/W
Junction–to-top characterization parameter	Ψ_{JT}	12	27	4	°C/W
Junction-to-board characterization parameter	Ψ_{JB}	46	38	42	°C/W

6. Specifications

6.1. Electrical Characteristics

(VDD1 = 3.0V ~ 5.5V, VDD2 = 3.0V ~ 5.5V, INP = -250mV to +250mV, and INN = GND1 = 0V, T_A = -40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 3.3V, T_A = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Side1 Supply Voltage	VDD1	3.0	5.0	5.5	V	
Side2 Supply Voltage	VDD2	3.0	3.3	5.5	V	
Side1 Supply Current	IDD1	4.0	5.8	7.2	mA	
Side2 Supply Current	IDD2	4.0	5.1	6.3	mA	
VDD1 undervoltage detection threshold voltage	$VDD1_{UV}$	1.8	2.3	2.7	V	VDD1 falling
Analog Input						
Common-mode overvoltage detection level	V_{CMov}		2.8		V	Detection level has a typical hysteresis of 96 mV
Input offset voltage(1)	V_{OS}	-0.5	±0.1	0.5	mV	INP = INN = GND1, at T_A =25°C
Input offset drift (2)	TCV_{OS}	-5	±1.5	5	μV/°C	
Common-mode rejection ratio	$CMRR_{dc}$		-98		dB	INP = INN, f_{IN} = 0 Hz, $V_{CM\ min} \le VIN \le V_{CM\ max}$
	$CMRR_{ac}$		-95		dB	INP = INN, f_{IN} = 10 kHz, $V_{CM\ min} \le VIN \le V_{CM\ max}$
Single-ended input resistance	R_{IN}		29		kΩ	INN = GND1
Differential input resistance	R_{IND}		29.5		kΩ	
Input capacitance	C_I		12		pF	
Input bias current	I_{IB}		-0.1		μA	INP = INN = GND1, $I_{IB} = (I_{IBP} + I_{IBN}) / 2$, at T_A =25°C
Input bias current drift (2)	TCI_{IB}		±1		nA/°C	

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Parameters	Symbol	Min	Typ	Max	Unit	Comments
Analog Output						
Nominal Gain			8.0		V/V	
Gain error (1)	E_G	-0.3%	±0.05%	0.3%		at T_A =25°C
Gain error thermal drift (1) (2)	TCE_G	-30	±5	30	ppm/°C	
Nonlinearity (1) (3)		-0.05%	±0.01%	0.05%		at T_A =25°C
Nonlinearity drift (1) (2)			±1		ppm/°C	
Total harmonic distortion (4)	THD		-90	-70	dB	V_{IN} =500mVpp, f_{IN} = 1kHz, BW = 10kHz
			-75		dB	V_{IN} =500mVpp, f_{IN} = 10kHz, BW = 100kHz
Output noise			360		μV_{RMS}	INP = INN = GND1, BW = 100kHz
Signal to noise ratio	SNR		85		dB	V_{IN} = 500mVpp, f_{IN} = 1kHz, BW = 10kHz
			72		dB	V_{IN} = 500mVpp, f_{IN} = 10kHz, BW = 100kHz
Common-mode output voltage	V_{CMout}	1.38	1.45	1.49	V	
Failsafe differential output voltage	$V_{FAILSAFE}$		-2.6	-2.5	V	V_{CM}>V_{CMov}, or VDD1 missing
Output bandwidth	BW	175	220		kHz	
Power supply rejection ratio (5)	$PSRR_{dc}$		-110		dB	PSRR vs VDD1, at DC
	$PSRR_{ac}$		-100		dB	PSRR vs VDD1, 100mV and 10kHz ripple
	$PSRR_{dc}$		-110		dB	PSRR vs VDD2, at DC
	$PSRR_{ac}$		-90		dB	PSRR vs VDD2, 100mV and 10kHz ripple
Output resistance	R_{OUT}		< 0.2		Ω	
Output current limit	I_{OUT}		±13		mA	
Common-mode transient immunity	CMTI	100	125		kV/μs	Common-mode transient immunity
Timing						
Rising time of OUTP, OUTN	t_r		1.7		μs	
Falling time of OUTP, OUTN	t_f		1.7		μs	
INP, INN to OUTP, OUTN signal delay (50% - 50%)	t_{PD}		1.6	2.0	μs	C_{LOAD}=15pF
Analog setting time	t_{AS}		0.5		ms	VDD1 step to 3.0 V with VDD2 ≥ 3.0 V, to OUTP, OUTN valid, 0.1% settling

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(1) The typical value includes one standard deviation (sigma) range under typical operating conditions.

(2) The temperature drift is calculated with the whole temperature range (-40°C to 125°C).

(3) Nonlinearity is defined as half of the peak-peak value of the deviation between the measuring point and the fitting curve divided by the full-scale range of the output voltage.

(4) THD is defined as the ratio of the sum of the rms value of first nine higher harmonics to the amplitude of the fundamental.

(5) Input referred.

6.2. Typical Performance Characteristics

Unless otherwise noted, test at VDD1 = 5V, VDD2 = 3.3V, INN=GND1=0V, INP = -250mV to 250mV, f_{IN} = 1kHz, BW = 10kHz.

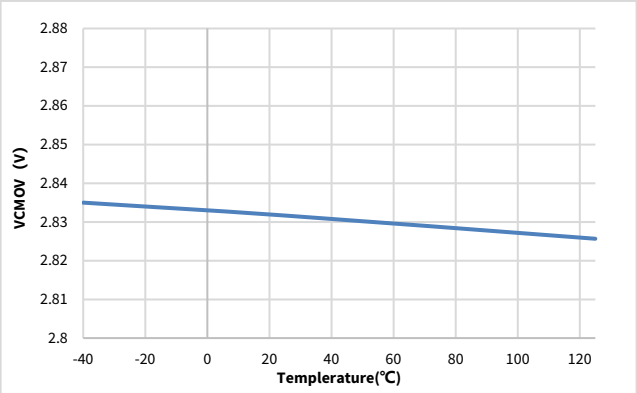

Figure 6.1 Common-Mode Overvoltage Detection Level vs Temperature

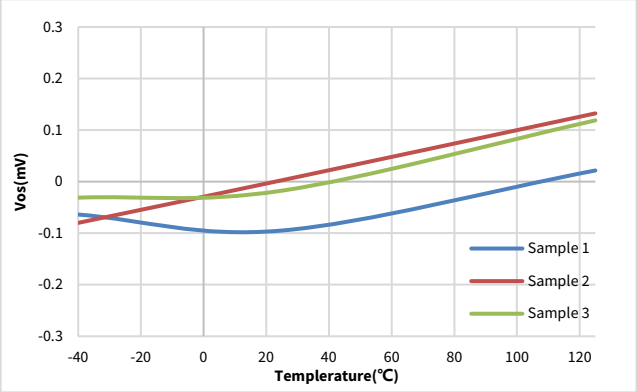

Figure 6.2 Input Offset Voltage vs Temperature

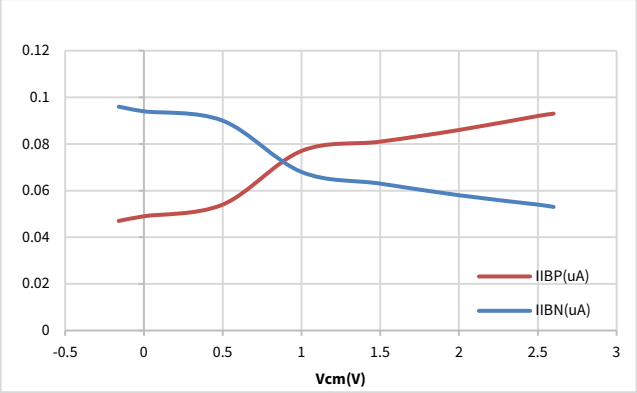

Figure 6.3 Input Bias Current vs Common-Mode Voltage

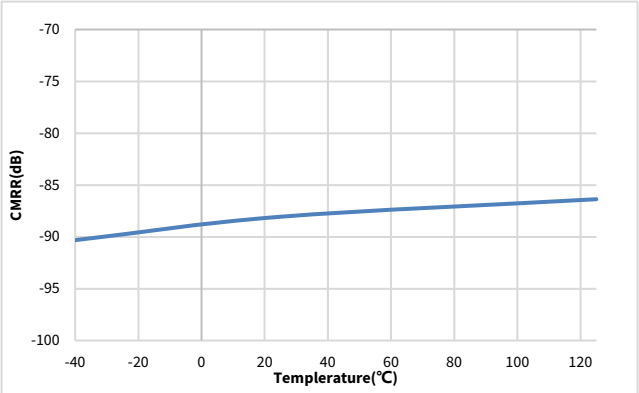

Figure 6.4 Common-Mode Rejection Ratio vs Temperature

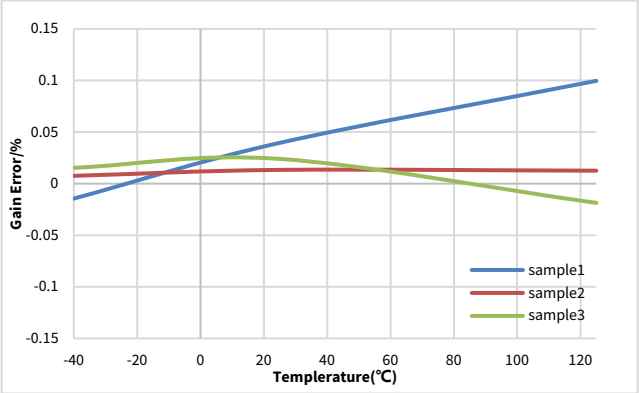

Figure 6.5 Gain Error vs Temperature

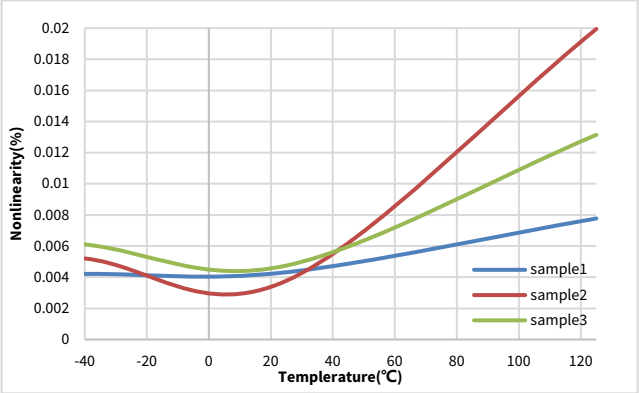

Figure 6.6 Nonlinearity vs Temperature

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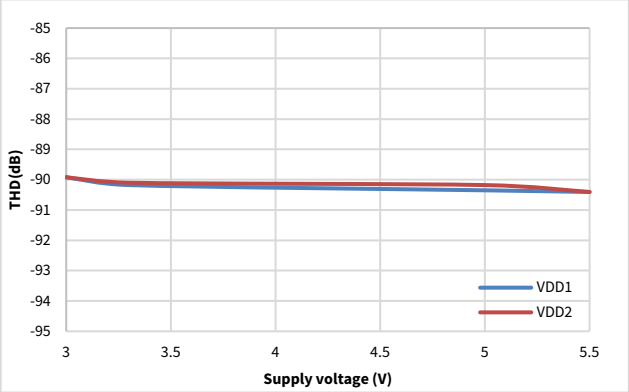

Figure 6.7 THD vs Supply Voltage

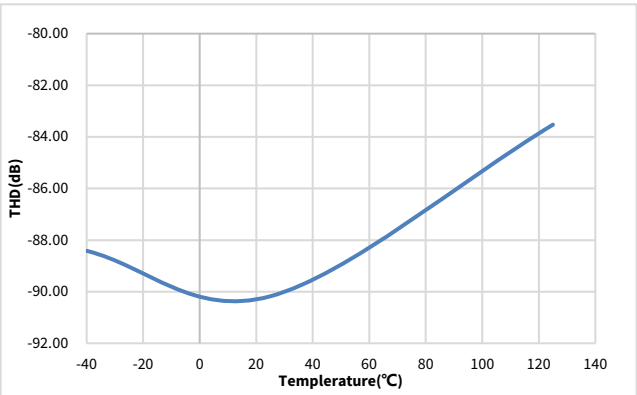

Figure 6.8 THD vs Temperature

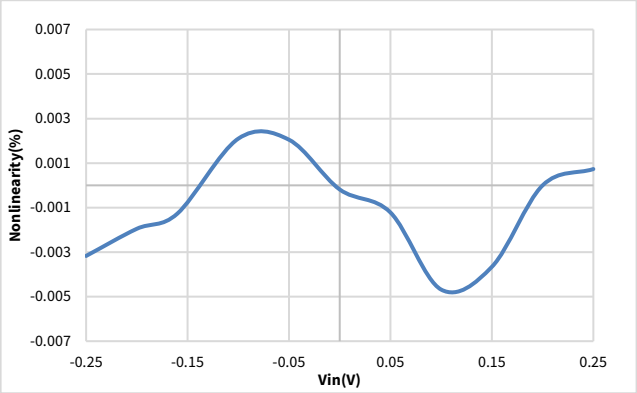

Figure 6.9 Nonlinearity vs Input Voltage

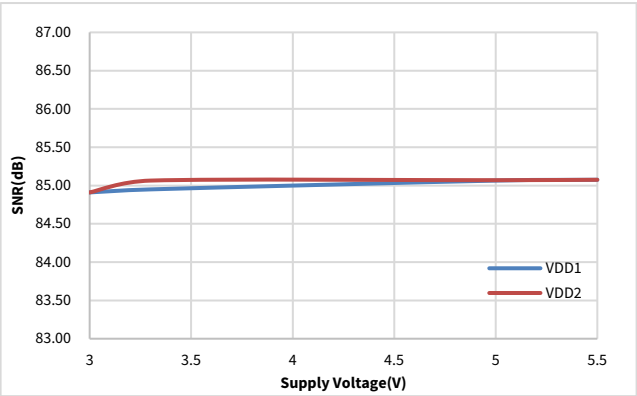

Figure 6.10 SNR vs Supply Voltage

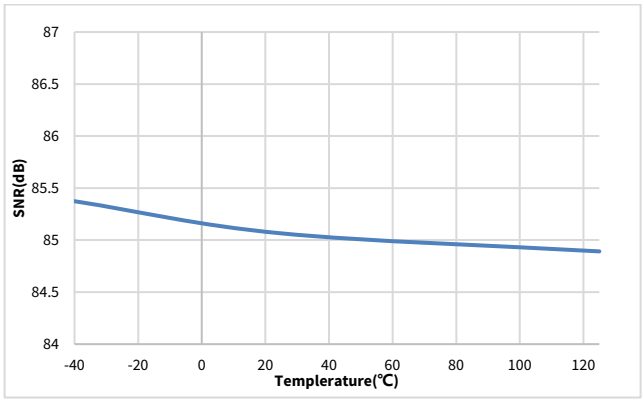

Figure 6.11 SNR vs Temperature

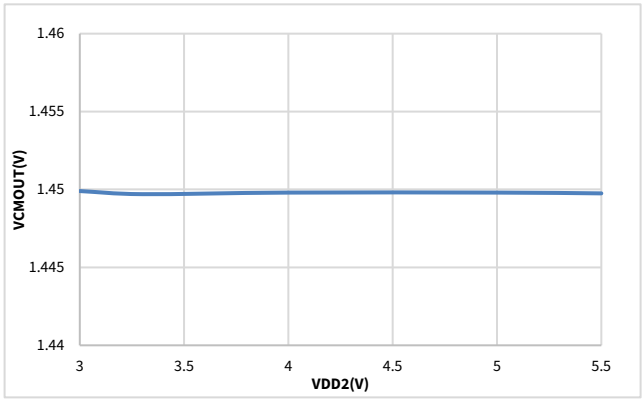

Figure 6.12 Output Common-Mode Voltage vs Side2 Supply Voltage

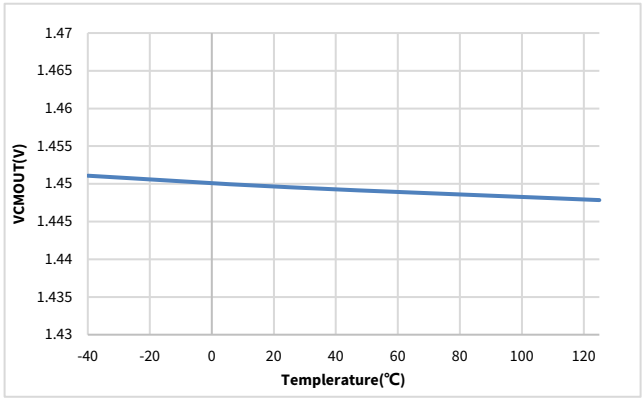

Figure 6.13 Output Common-Mode Voltage vs Temperature

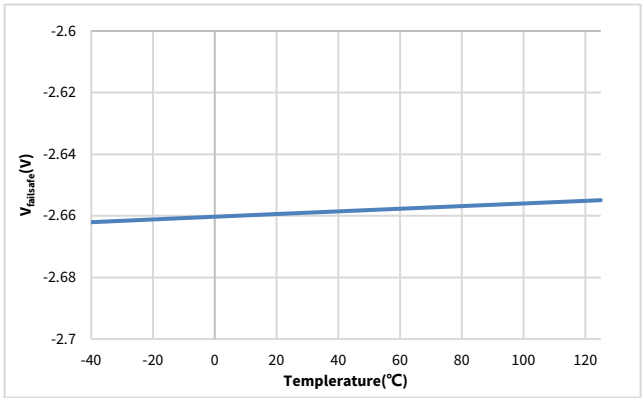

Figure 6.14 Fail-Safe Output Voltage vs Temperature

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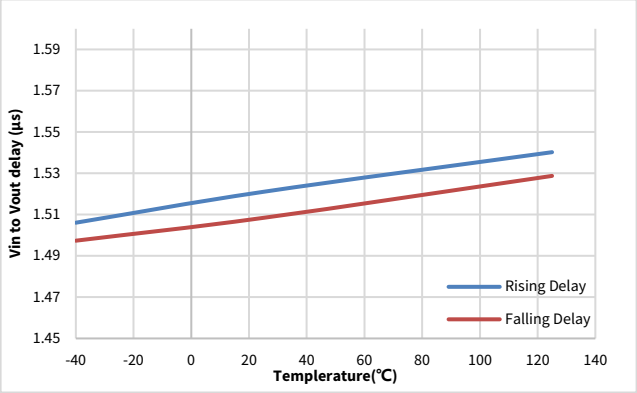

Figure 6.15 Vin to Vout Delay vs Temperature

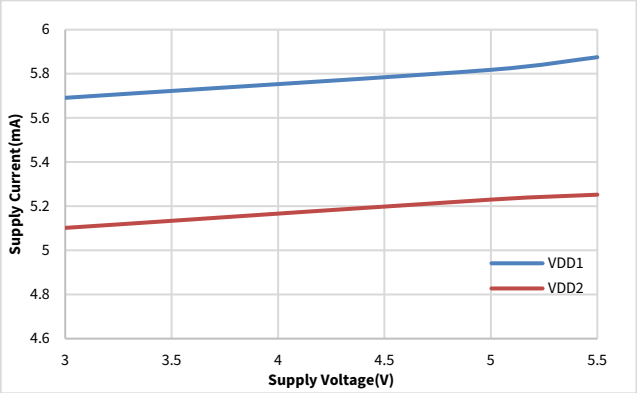

Figure 6.16 Supply Current vs Supply Voltage

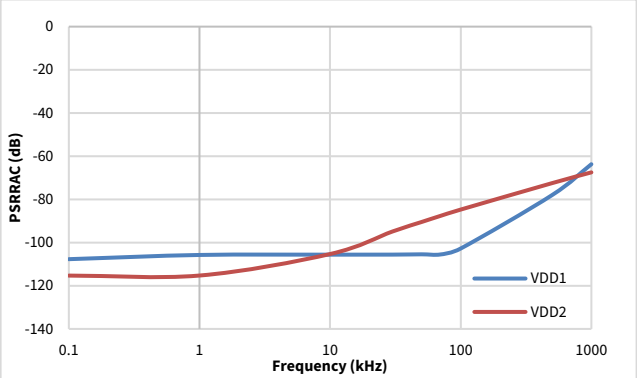

Figure 6.17 Power-Supply Rejection Ratio vs Ripple Frequency

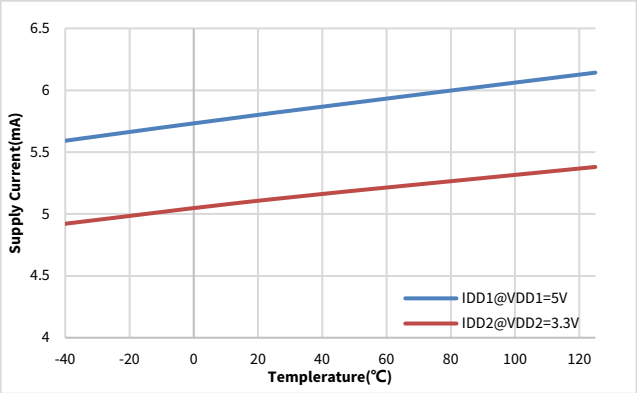

Figure 6.18 Supply Current vs Temperature

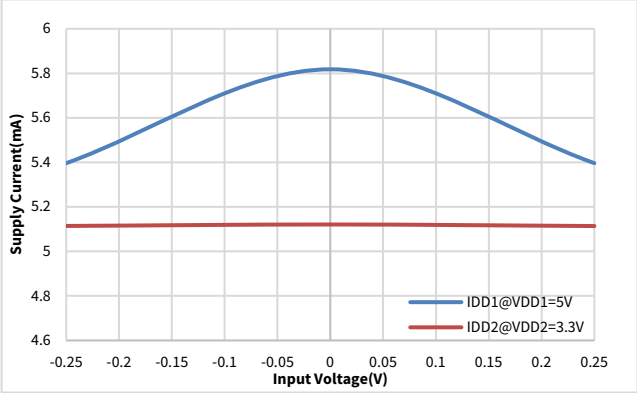

Figure 6.19 Supply Current vs Input Voltage

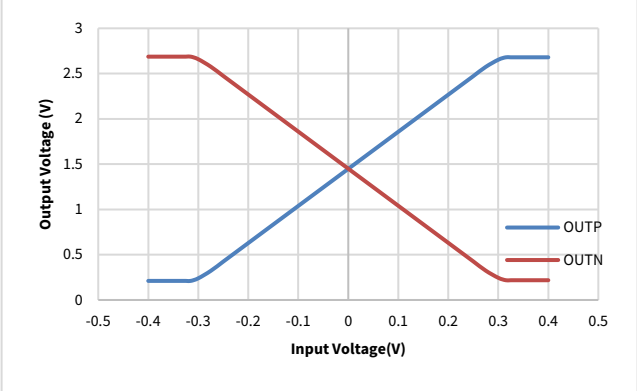

Figure 6.20 Output Voltage vs Input Voltage

6.1. Parameter Measurement Information

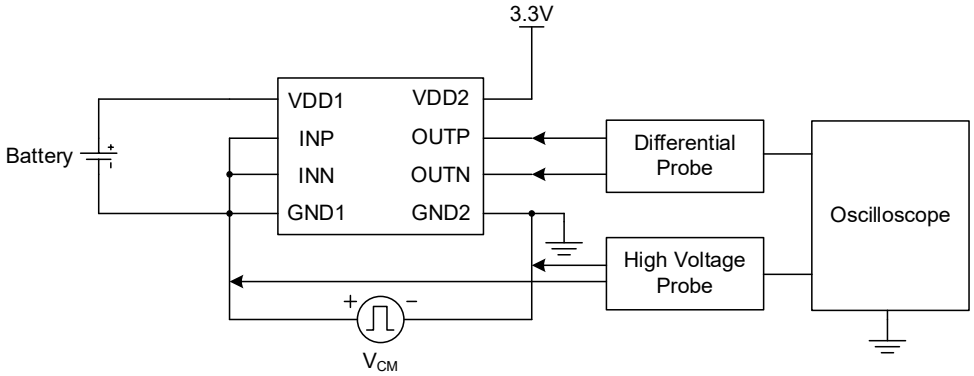

Figure 6.21 Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value			Unit	Comments
		SOP8	DUB8	SOW8		
Minimum External Clearance	CLR	4	6.5	8	mm	IEC 60664-1:2007
Minimum External Creepage	CPG	4	6.5	8	mm	IEC 60664-1:2007
Distance Through Insulation	DTI	28			μm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600			V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I				IEC 60664-1

Description	Test Condition	Value		
		SOP8	DUB8	SOW8
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	I to IV	I to IV	I to IV
	For Rated Mains Voltage ≤ 300Vrms	I to III	I to IV	I to IV
	For Rated Mains Voltage ≤ 600Vrms	I to II	I to IV	I to IV
	For Rated Mains Voltage ≤ 1000Vrms	I	I to III	I to III
Climatic Classification		40/125/21		
Pollution Degree per DIN VDE 0110		2		

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7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value			Unit
			SOP8	DUB8	SOW8	
DIN EN IEC 60747-17 (VDE 0884-17)						
Maximum repetitive isolation voltage		V_{IORM}	990	1000	2121	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	700	/	1500	V_{RMS}
	DC Voltage		990	/	2121	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, Vini=V_{IOTM}, t_{ini} = 60 s , $V_{pd(m)}$=1.2*V_{IORM}, t_m=10s.	q_{pd}	/	<5	<5	pC
	Method a, after environmental tests subgroup 1, Vini=V_{IOTM}, t_{ini}=60s ,$V_{pd(m)}$=1.6*V_{IORM}, t_m=10s					
	Method b, routine test (100% production) and preconditioning (type test);V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd\ (m)}$=1.875*V_{IORM}, t_m=1s （method b1） or $V_{pd(m)}$=Vini, t_m=t_{ini}(method b2)					
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, Vini=V_{IOTM}, t_{ini} = 60 s , $V_{pd(m)}$=1.2*V_{IORM}, t_m=10s.	q_{pd}	<5	/	/	pC
	Method a, after environmental tests subgroup 1, Vini=V_{IOTM}, t_{ini}=60s ,$V_{pd(m)}$=1.3*V_{IORM}, t_m=10s					
	Method b, routine test (100% production) and preconditioning (type test);V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd\ (m)}$=1.5*V_{IORM}, t_m=1s （method b1） or $V_{pd(m)}$=Vini, t_m=t_{ini}(method b2)					
Maximum transient isolation voltage	t = 60sec	V_{IOTM}	4242	8000	8000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50-us waveform per IEC62368-1	V_{IMP}	3000	6250	6250	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, V_{IOSM}≥V_{IMP} × 1.3	V_{IOSM}	6000	10000	10000	V_{PEAK}
Isolation resistance	V_{IO} =500V, T_{amb}=25°C	R_{IO}	>10^{12}	>10^{12}	>10^{12}	Ω

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Description	Test Condition	Symbol	Value			Unit
			SOP8	DUB8	SOW8	
	V_{IO} =500V, 100°C ≤ T_{amb} ≤ 125°C	R_{IO}	>10^{11}	>10^{11}	>10^{11}	Ω
	V_{IO} =500V, T_{amb}=T_S	R_{IO}	>10^{9}	>10^{9}	>10^{9}	Ω
Isolation capacitance	f = 1MHz	C_{IO}	1.2	1.2	1.2	pF
Safety total power dissipation	V_I = 5.5V, T_J = 150 °C, T_A = 25 °C	Ps	907	1650	1453	mW
Safety input, output, or supply current	θ_{JA} = 137.7°C/W for SOP8, V_I = 5.5V, T_J = 150 °C, T_A = 25 °C	Is	165	/	/	mA
	θ_{JA} = 76°C/W for DUB8, V_I = 5.5V, T_J = 150 °C, T_A = 25 °C		/	300	/	mA
	θ_{JA} = 86°C/W for SOW8, V_I = 5.5V, T_J = 150 °C, T_A = 25 °C		/	/	264	mA
Maximum safety temperature		Ts	150	150	150	°C
UL1577						
Insulation voltage per UL	V_{TEST} = V_{ISO}, t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO}, t = 1 s (100% production test)	V_{ISO}	3000	5000	5000	V_{RMS}

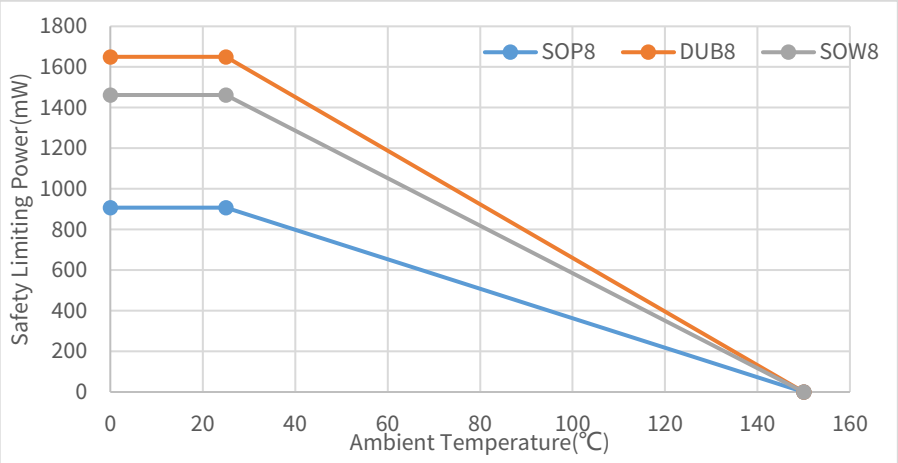

Figure 7.1 NSI1200C Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17

7.3. Regulatory Information

The NSI1200C-DSPR is approved or pending approval by the organizations listed in table.

UL		VDE	CQC	TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1

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UL		VDE	CQC	TUV
Single Protection, 3000V_{rms} Isolation voltage	Single Protection, 3000V_{rms} Isolation voltage	Basic Insulation V_{IORM}=990 V_{PEAK} V_{IOTM}=4242 V_{PEAK} V_{IOSM}=6000 V_{PEAK}	Basic insulation	3000Vrms for 1min
E500602	E500602	File (pending)	CQC20001264940	R50574061

The NSI1200C-DSWVR and NSI1200C-DDBR are approved or pending approval by the organizations listed in table.

UL		VDE	CQC	TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1
Single Protection, 5000V_{rms} Isolation voltage	Single Protection, 5000V_{rms} Isolation voltage	Reinforce Insulation V_{IORM}=2121Vpeak for SOW8/ 1000Vpeak for DUB8 V_{IOTM}=8000Vpeak, V_{IOSM}=10000Vpeak	Reinforced insulation	5000Vrms for 1min
E500602	E500602	40052820	CQC20001264938 for SOW8 CQC20001263786 for DUB8	R50574061

8. Function Description

8.1. Overview

The NSI1200C is a high-performance isolated amplifier that accepts fully-differential input. The fully-differential input is ideally suited to shunt current monitoring in high voltage applications where isolation is required. The analog input is continuously sampled by a second-order Σ-Δ modulator in the device. With the internal voltage reference and clock generator, the modulator converts the analog input signal to a digital bitstream. The output of the modulator is transferred by the drivers (called TX in the Functional Block Diagram) across the isolation barrier that separates the isolated input side and output side voltage. The received bitstream and clock are synchronized and processed, as shown in the Functional Block Diagram, by a fourth-order analog filter on the output side and has a differential output.

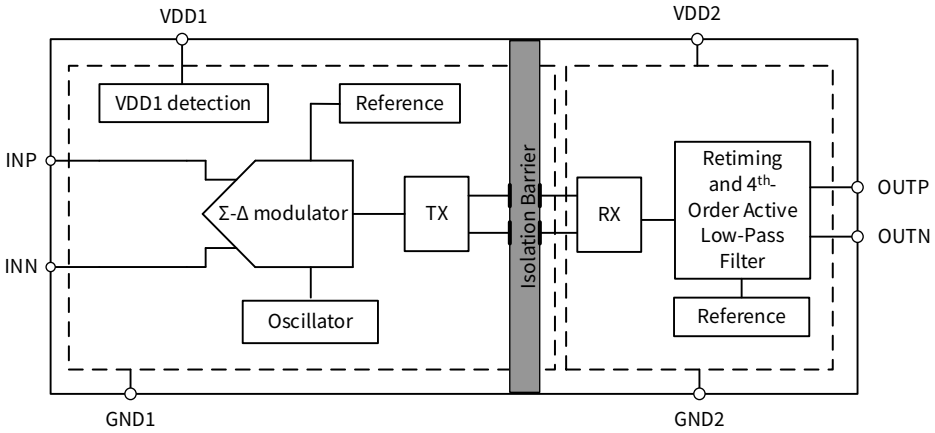

Figure 8.1 Function Block Diagram

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8.2. Analog Input

The analog input of the NSI1200C is a switched-capacitor circuit based on the second-order Σ-Δ modulator. The Equivalent circuit of analog input is shown in Figure 8.2. The internal capacitance C_{IND} is continuously charged and discharged through periodical switching action with the internal clock frequency f_{CLK} for input signal digitization. In the charging phase, the external input source must provide enough transient charge for the internal capacitance. To prevent transient voltage drop of C_{IND}, an external capacitor (C_{FLT} in Figure 8.1, also acting as filter capacitance) of more than 330pF should be placed as close as possible to the device as charge buffering, which ensures sensing accuracy.

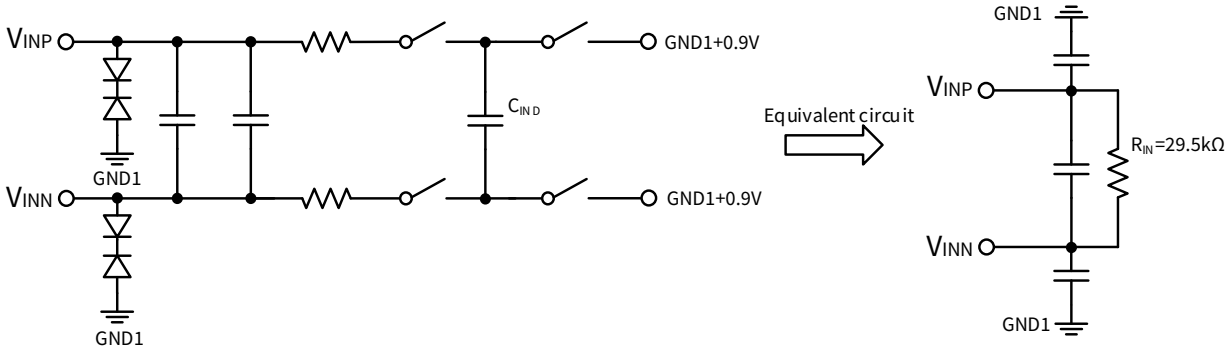

Figure 8.2 Equivalent Circuit of Analog Input

According to the equivalent circuit, the input resistance R_{IN} can be calculated as

$$R_{IND} = 1/(f_{CLK} * C_{IND})$$

There are two restrictions on the analog input signals (VINP and VINN).

- If the input voltage exceeds the range GND1 – 6 V to VDD1 + 0.5 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on.
- The linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

8.3. Analog Output

For linear input range, the analog output of NSI1200C has a fixed gain 8.0. If a full-scale input signal is applied to the NSI1200C ($V_{IN} \geq V_{Clipping}$), the analog output will be clipped (typically, 2.45V for positive clipping and -2.45V for negative clipping). The typical negative clipping output of NSI1200C is shown in Figure 8.3.

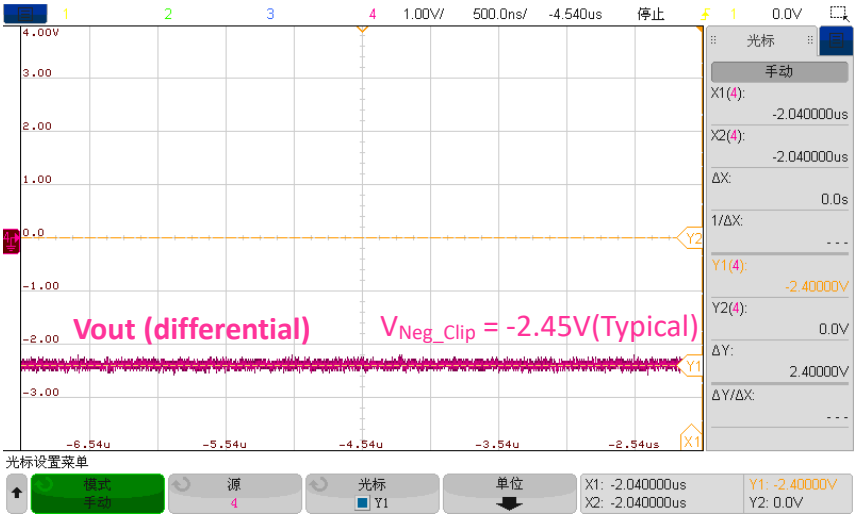

Figure 8.3 Typical negative clipping output

In addition, NSI1200C integrates some diagnostic measures and offers a fail-safe output to simplify system-level design. The fail-safe output is a negative differential output voltage that does not occur under normal device operation, and it will only be activated in following conditions:

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- When the undervoltage of VDD1 is detected (VDD1< $VDD1_{UV}$).
- When the overvoltage of common-mode input voltage is detected (V_{CM}>V_{CMov}).

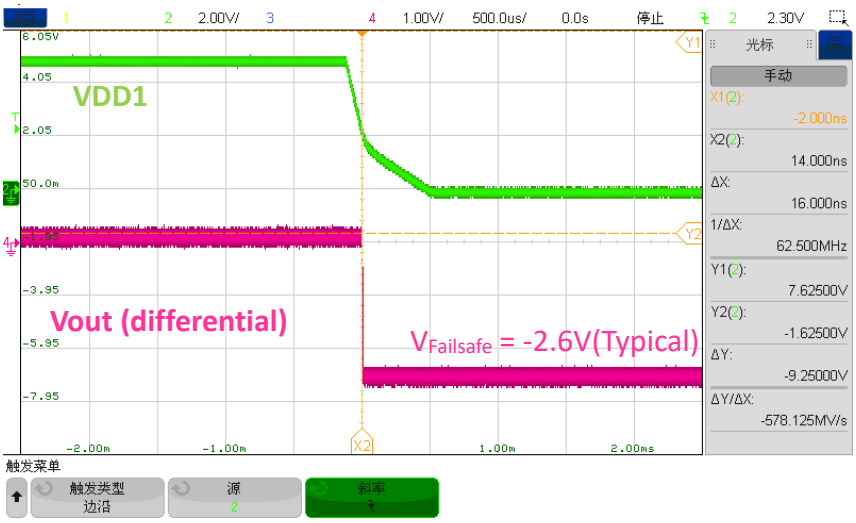

Figure 8.4 Typical Failsafe output when VDD1 undervoltage

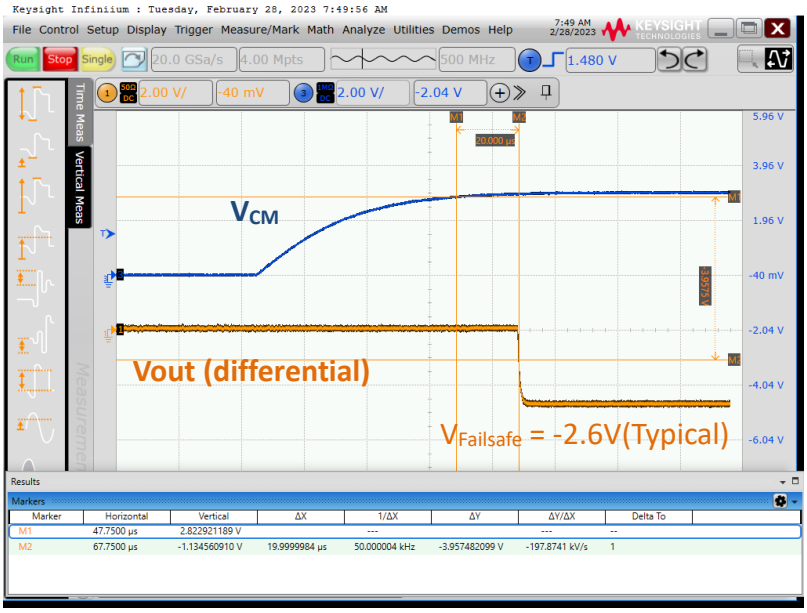

Figure 8.5 Typical Failsafe output when input common mode signal overvoltage

9. Application Note

9.1. Typical Application Circuit

NSI1200C is ideally suited to shunt resistor-based current sensing in high voltage applications such as motor drives. The typical application circuit is shown in Figure 8.1.

The voltage across the shunt resistor R_{sense} is applied to the differential input of NSI1200C through a RC filter (R_{FLT} and C_{FLT}). The filter capacitance of more than 330pF placing as close as possible to the device must be added for charge buffering of the input switched-capacitor circuit (further details in 8.2 Analog Input) and better performance in high-noise applications.

The differential output of the isolated amplifier is converted to a single-ended analog output with an operational-amplifier-based circuit. Suggest to add >1kΩ resistor on the OUTP and OUTN pin to prevent output over-current. An analog-to-digital converter usually receives the analog output and converts to digital signal for controller processing.

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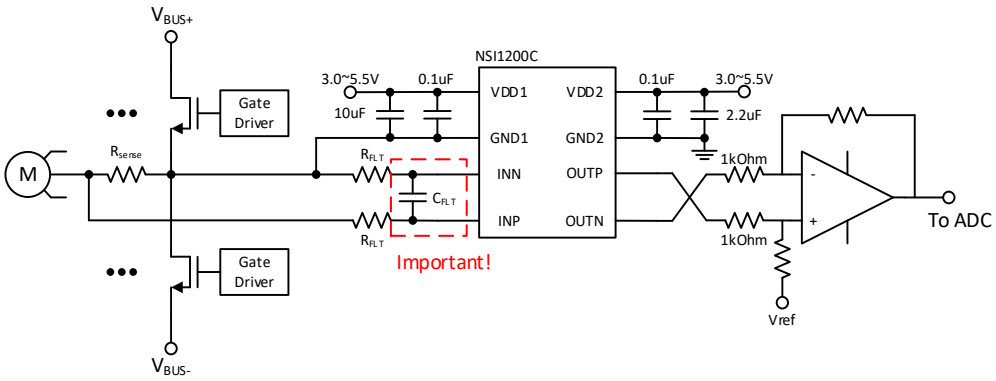

Figure 9.1 Typical application circuit in phase current sensing

9.2. Shunt Resistor Selection

Choosing a particular shunt resistor is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller sense resistor decreases power dissipation, while larger sense resistor can improve measure accuracy by utilizing the full input range of isolated amplifier.

There are two other factors should be considered when selecting the shunt resistor:

- The voltage-drop caused by the rated current range must not exceed the recommended linear input voltage range: $V_{SHUNT} \leq FSR$.
- The voltage-drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $V_{SHUNT} \leq V_{Clipping}$.

9.3. PCB Layout

There are some key guidelines or considerations for optimizing performance in PCB layout:

- Place the input filter capacitors as close as possible to the INP and INN pins for best performance.
- NSI1200C requires a 0.1μF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the VDD pin. If better filtering is required, an additional 1~10μF capacitor may be used.
- Kelvin rules is recommended for the connection between shunt resistor to NSI1200C. Because of the Kelvin connection, any voltage drops across the trace and leads should have no impact on the measured voltage.
- Place the shunt resistor close to the INP and INN inputs and keep the layout of both connections symmetrical and run very close to each other to the input of the NSI1200C. This minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal.

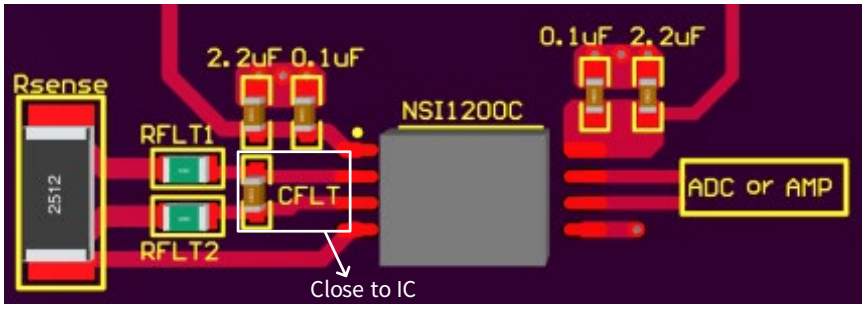

Figure 9.2 Typical application circuit in phase current sensing

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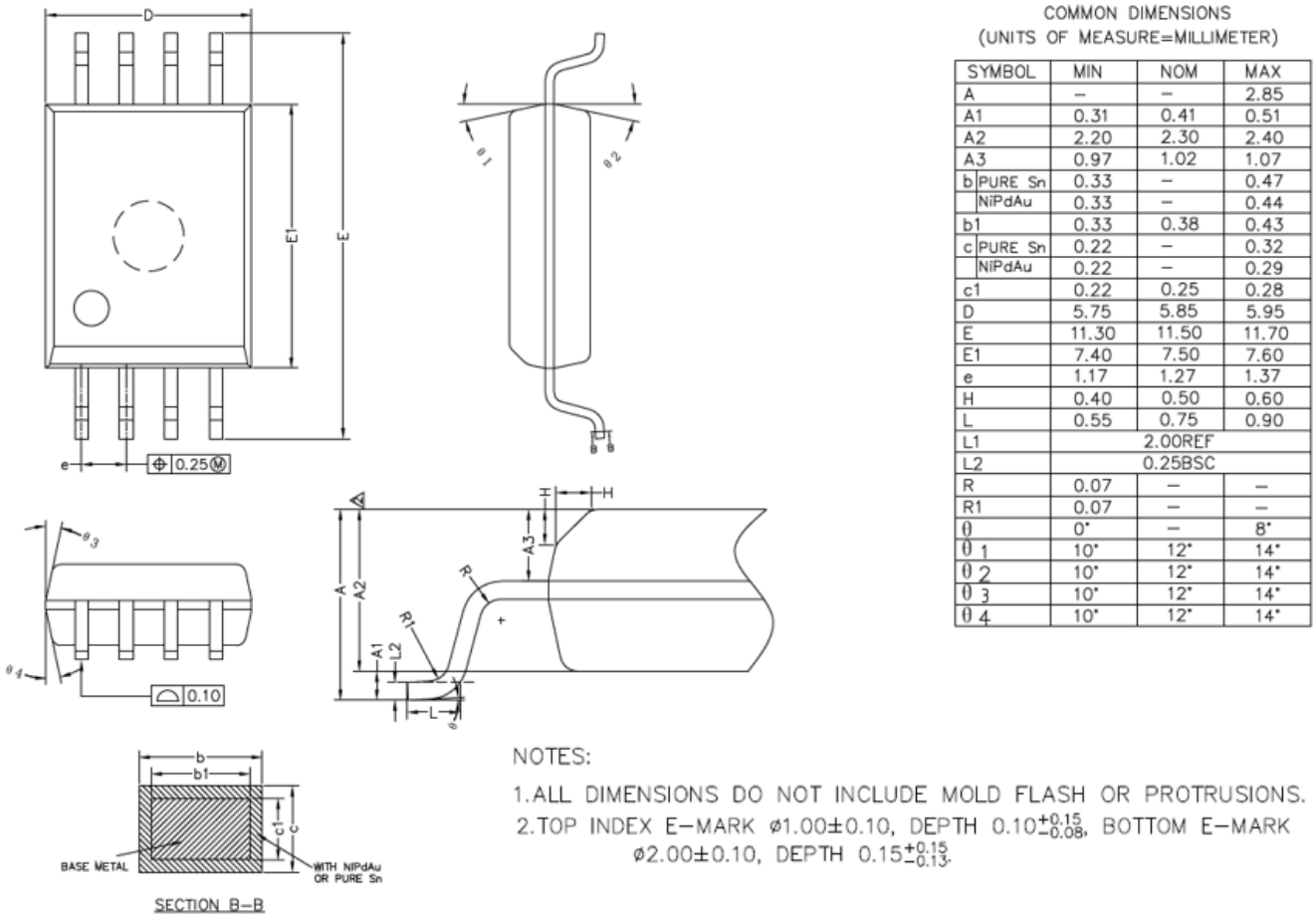
10. Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL		MIN	NOM	MAX
A		–	–	2.85
A1		0.31	0.41	0.51
A2		2.20	2.30	2.40
A3		0.97	1.02	1.07
b	PURE Sn	0.33	–	0.47
	NiPdAu	0.33	–	0.44
b1		0.33	0.38	0.43
c	PURE Sn	0.22	–	0.32
	NiPdAu	0.22	–	0.29
c1		0.22	0.25	0.28
D		5.75	5.85	5.95
E		11.30	11.50	11.70
E1		7.40	7.50	7.60
e		1.17	1.27	1.37
H		0.40	0.50	0.60
L		0.55	0.75	0.90
L1			2.00REF	
L2			0.25BSC	
R		0.07	–	–
R1		0.07	–	–
θ		0°	–	8°
θ1		10°	12°	14°
θ2		10°	12°	14°
θ3		10°	12°	14°
θ4		10°	12°	14°

NOTES:

1. ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. TOP INDEX E–MARK ø1.00±0.10, DEPTH $0.10^{+0.15}_{-0.08}$, BOTTOM E–MARK ø2.00±0.10, DEPTH $0.15^{+0.15}_{-0.13}$.

Figure 10.1 SOW8 Package Shape and Dimension in millimeters

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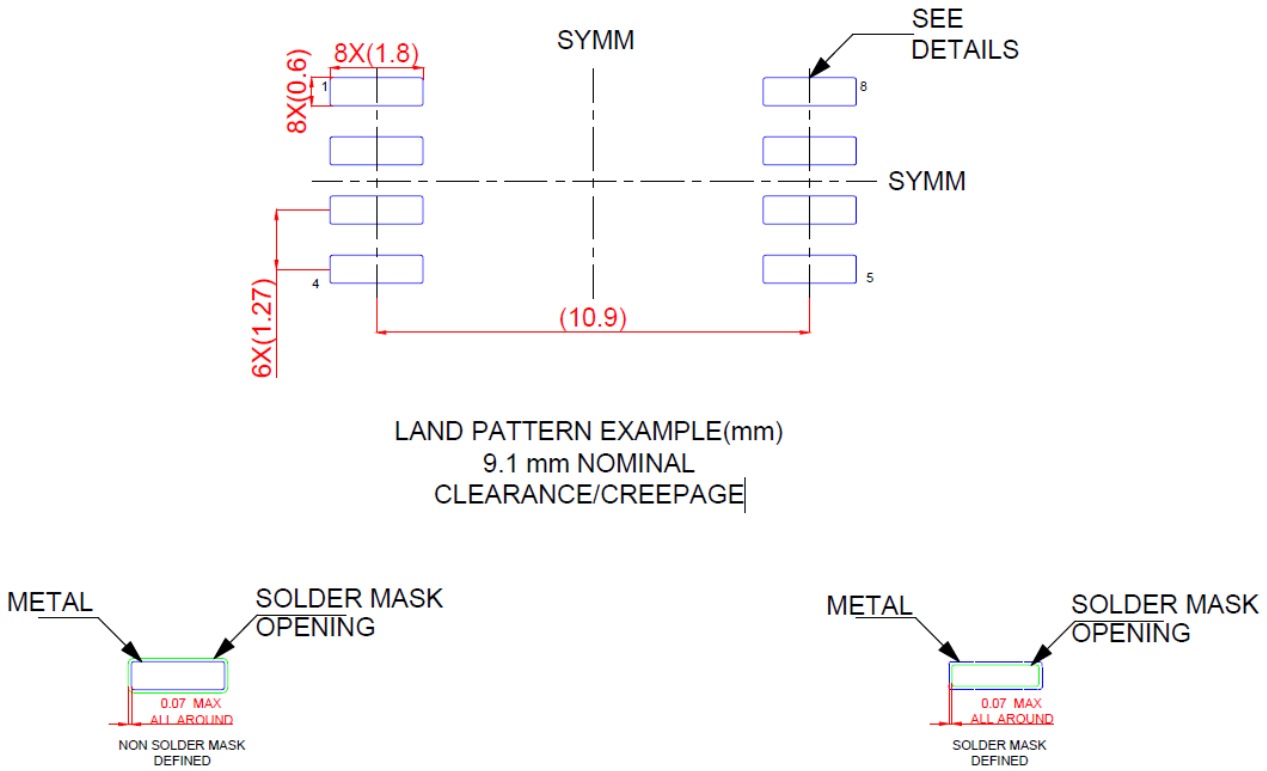
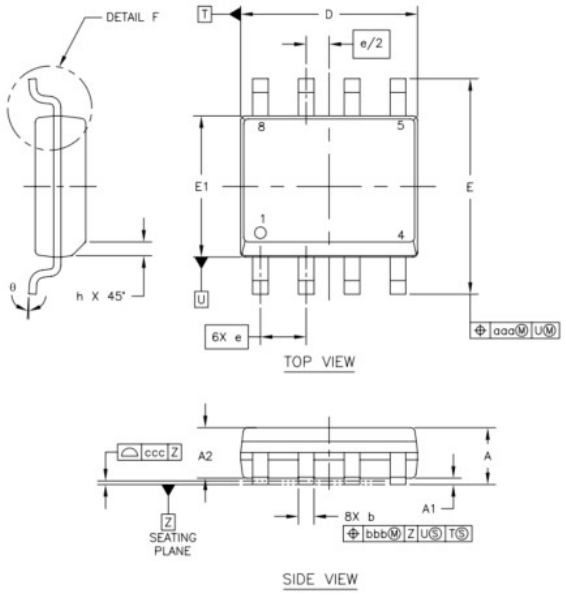


Figure 10.2 SOW8 Package Board Layout Example



DESCRIPTION	SYMBOL	INCH			MILLIMETER		
		MIN	NOM	MAX	MIN	NOM	MAX
TOTAL THICKNESS	A	.053		.069	1.35		1.75
STAND OFF	A1	.004		.010	0.10		0.25
MOLD THICKNESS	A2	.049		---	1.25		---
LEAD WIDTH	b	.014		.019	0.35		0.49
L/F THICKNESS	c	.007		.010	0.19		0.25
BODY SIZE	D	.189		.197	4.80		5.00
	E1	.150		.157	3.80		4.00
	E	.228		.244	5.80		6.20
LEAD PITCH	e	.050 BSC			1.27 BSC		
	L	.016		.049	0.40		1.25
	h	.010		.020	0.25		0.50
	θ	0°		7°	0°		7°
	θ1	5°		15°	5°		15°
	θ2	2°	7°	12°	2°	7°	12°
LEAD EDGE OFFSET	aaa	.010			0.25		
LEAD OFFSET	bbb	.010			0.25		
COPLANARITY	ccc	.004			0.10		

Figure 10.3 SOP8 package shape and dimension in millimeters

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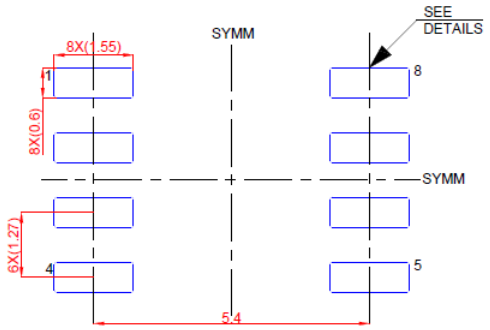
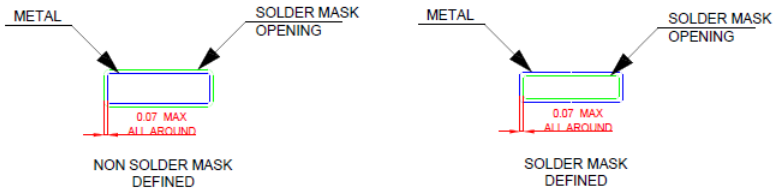
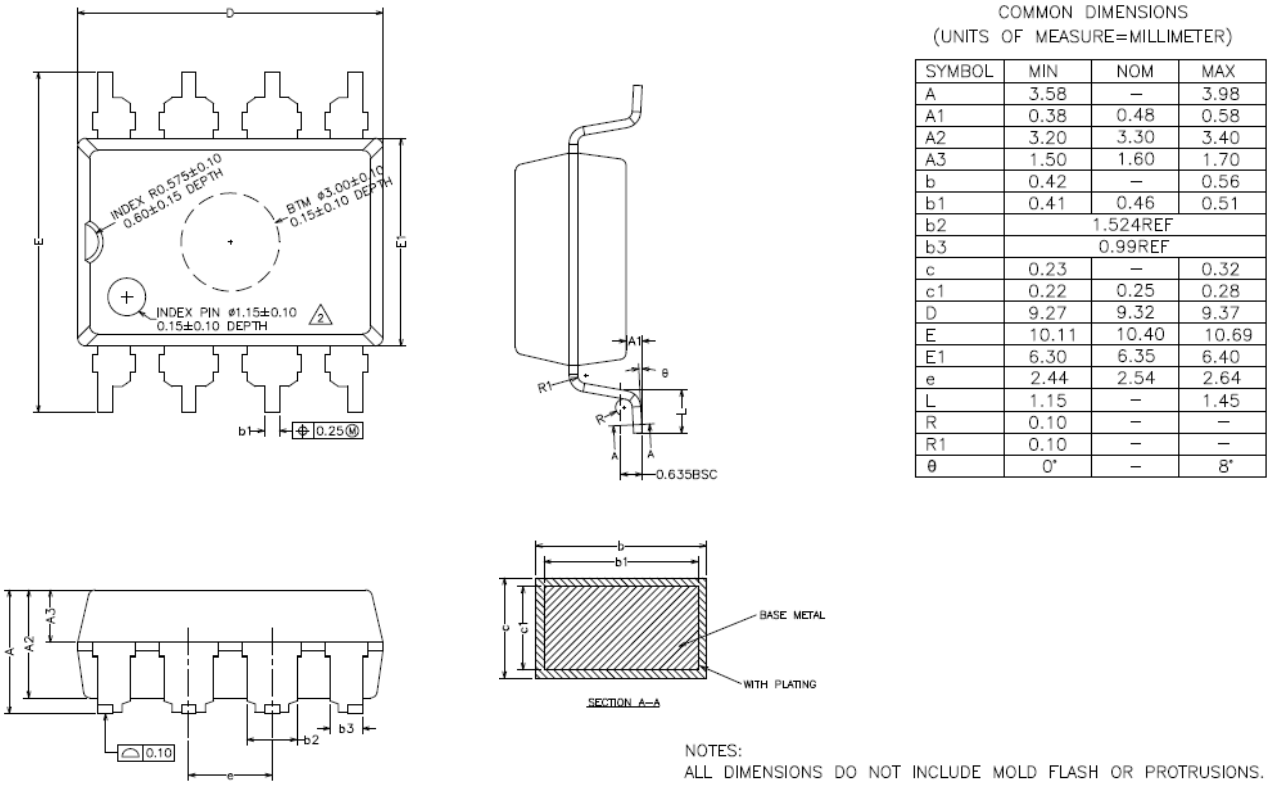


LAND PATTERN EXAMPLE(mm)



SOLDER MASK DETAILS

Figure 10.4 SOP8 Package Board Layout Example



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	3.58	–	3.98
A1	0.38	0.48	0.58
A2	3.20	3.30	3.40
A3	1.50	1.60	1.70
b	0.42	–	0.56
b1	0.41	0.46	0.51
b2	1.524REF		
b3	0.99REF		
c	0.23	–	0.32
c1	0.22	0.25	0.28
D	9.27	9.32	9.37
E	10.11	10.40	10.69
E1	6.30	6.35	6.40
e	2.44	2.54	2.64
L	1.15	–	1.45
R	0.10	–	–
R1	0.10	–	–
θ	0°	–	8°

NOTES:
ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

Figure 10.5 DUB8 Package Shape and Dimension in millimeters

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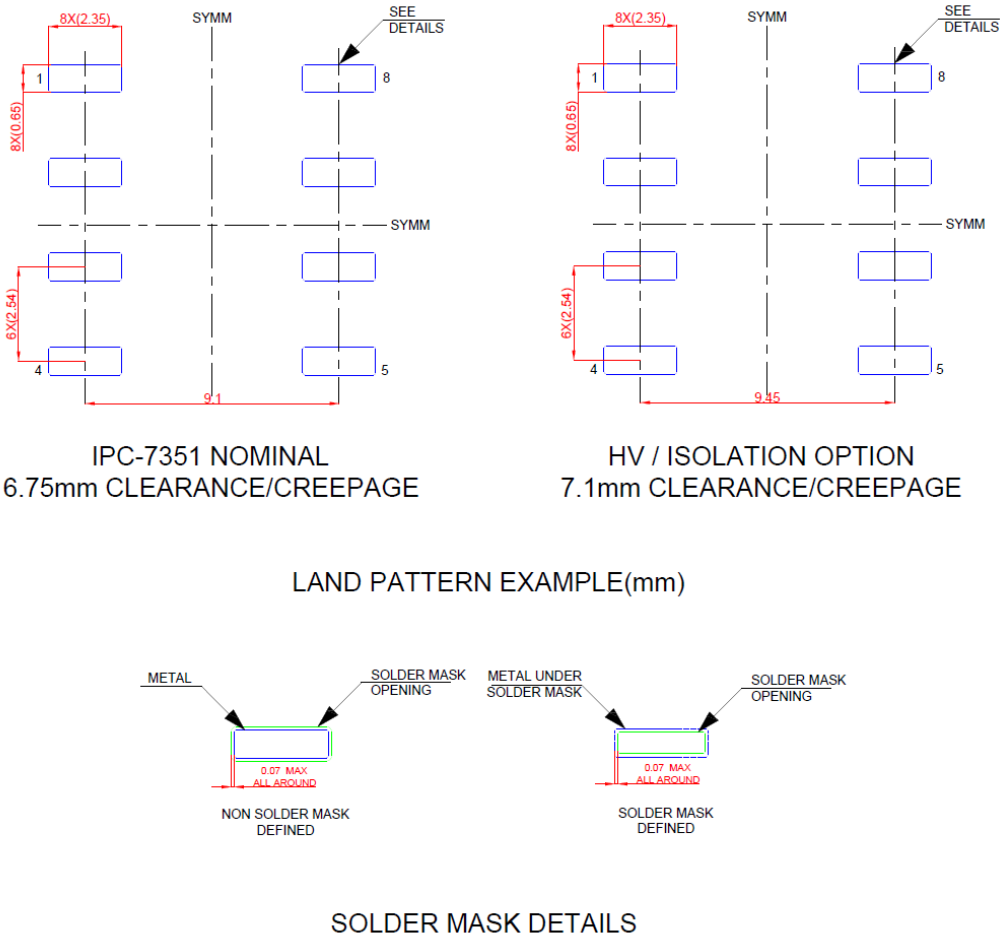

Figure 10.6 DUB8 Package Board Layout Example

11. Ordering Information

Part No.	*Isolation Rating(kV)*	*Linear Input Range(mV)*	*Moisture Sensitivity Level*	*Temperature*	*Package Type*	*Package Drawing*	*SPQ*	*Release to market*
NSI1200C-DSWVR	5	-250 ~ 250	Level-3	-40 to 125°C	SOP8 (300mil)	SOW8	1000	YES
NSI1200C-DSPR	3	-250 ~ 250	Level-3	-40 to 125°C	SOP8 (150mil)	SOP8	2500	NO
NSI1200C-DDBR	5	-250 ~ 250	Level-3	-40 to 125°C	DUB8	DUB8	800	YES

12. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
NSI1200C	Click here	Click here	Click here	Click here

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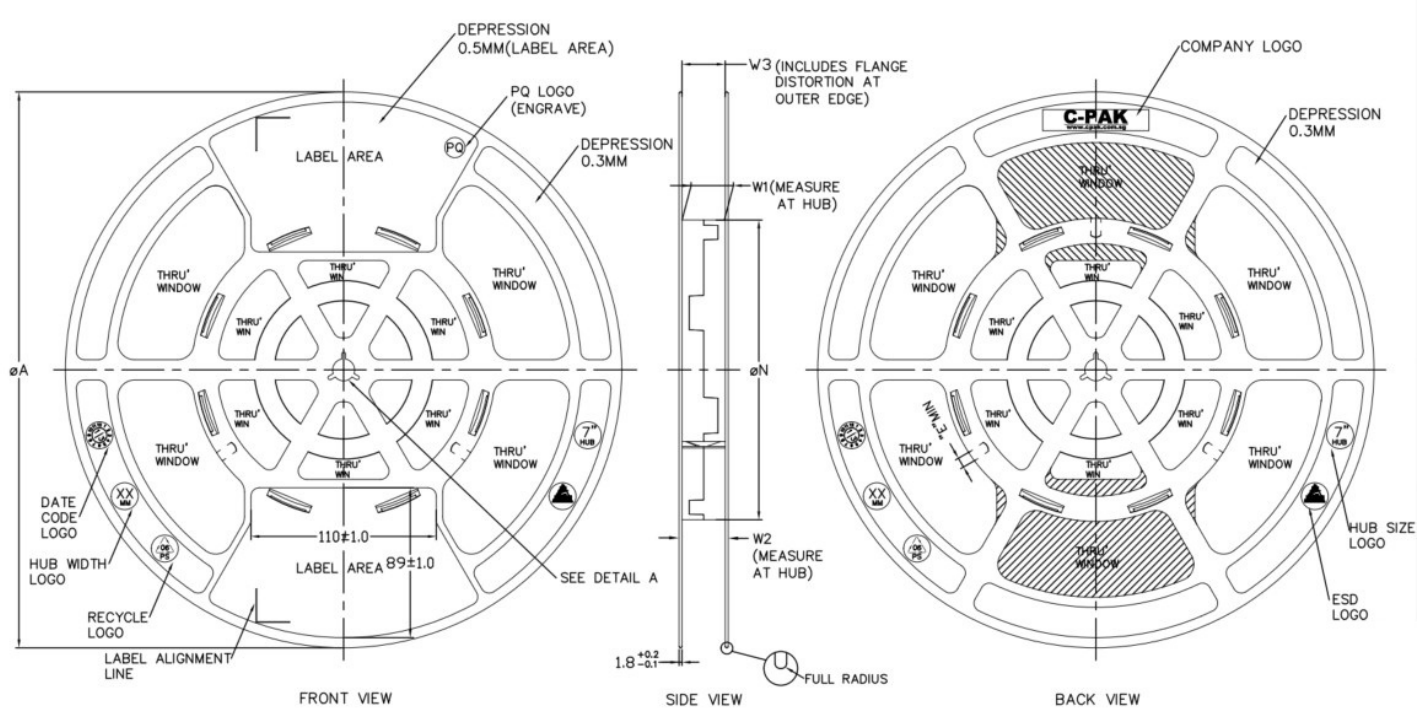
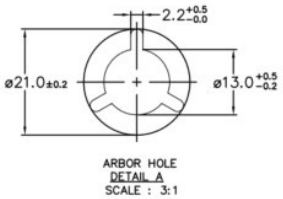
13. Tape and Reel Information





PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 −0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 −0.0	18.4		5.5
16MM	330	178	16.4 +2.0 −0.0	22.4		5.5
24MM	330	178	24.4 +2.0 −0.0	30.4		5.5
32MM	330	178	32.4 +2.0 −0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{9} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{9}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES

Figure 13.1 Reel Information of SOP8

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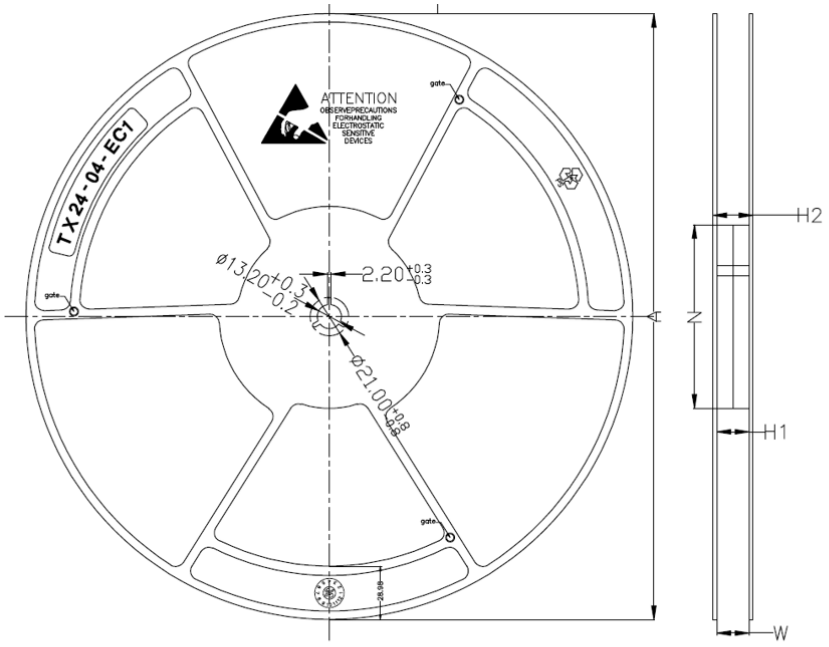
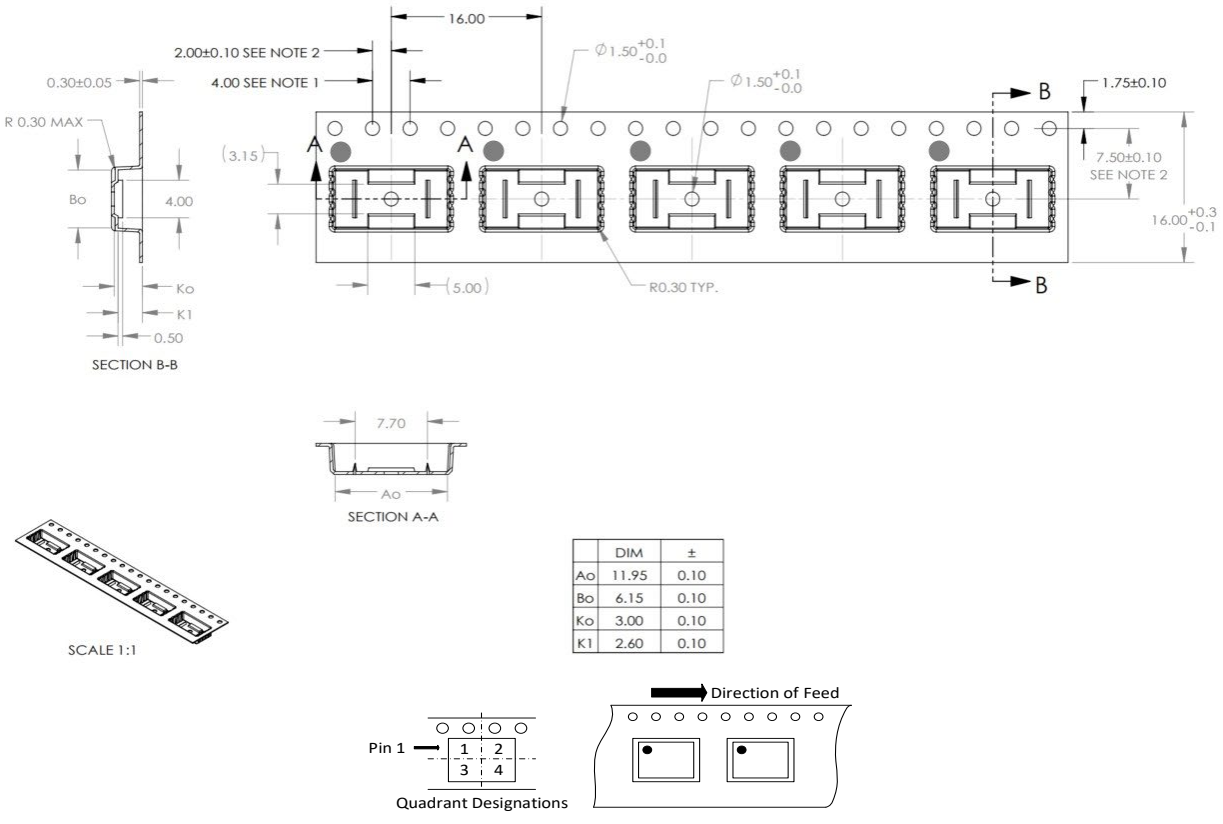


PRODUCT SPECIFICATIONS					
TAPE WIDTH	øA +2 −2	øN +2 −2	H1 +2 −0	H2 +1 −1	W +3.5 −0.2
24MM	330	100	24.4	28.6	24.4

NOTES:
1. MATERIAL: DISSIPATIVE(BLACK)
2. FLANGE WARPAGE:3 MM MAXIMUM
3. ALL DIMENSIONS ARE IN MM
4. ESD - SURFACE RESISTIVITY-10 TO 10 OHMS/SQ
5. GENERAL TOLERANCE: ±0.25 MM

Figure 13.2 Reel Information of DUB8



	DIM	±
Ao	11.95	0.10
Bo	6.15	0.10
Ko	3.00	0.10
K1	2.60	0.10

Figure 13.3 Tape Information of SOP8(300mil)

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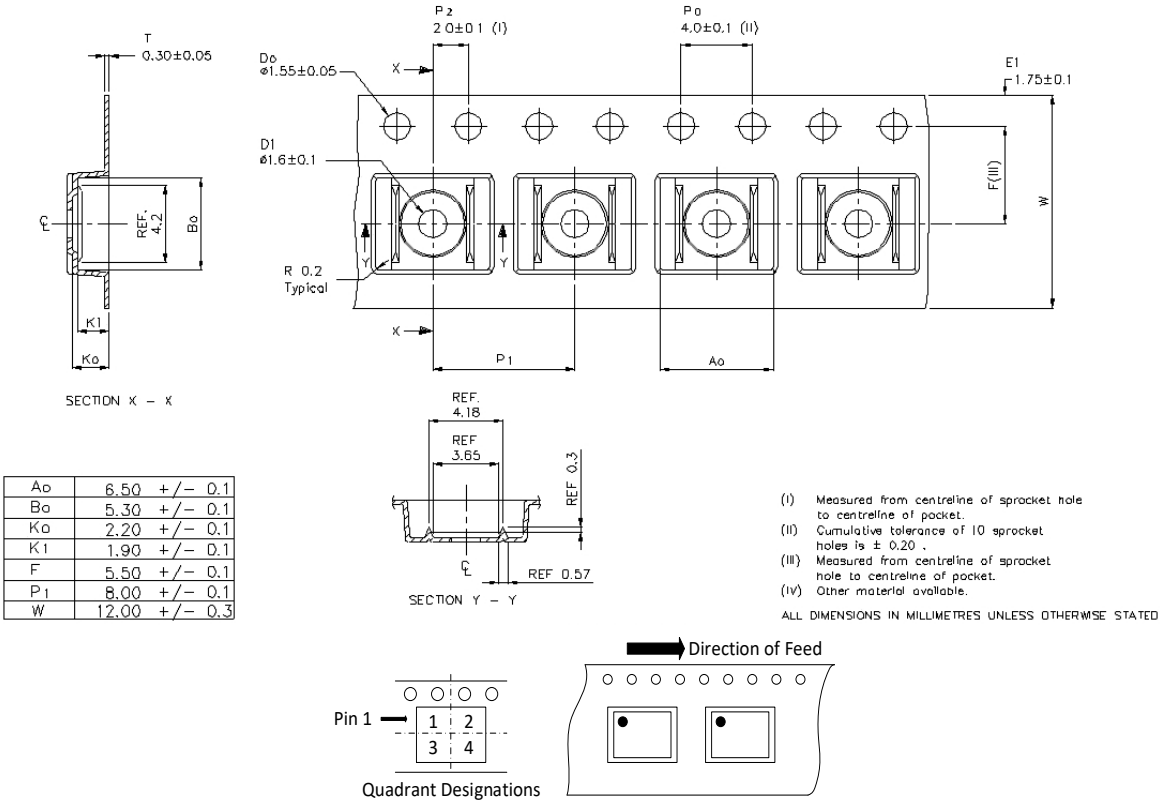
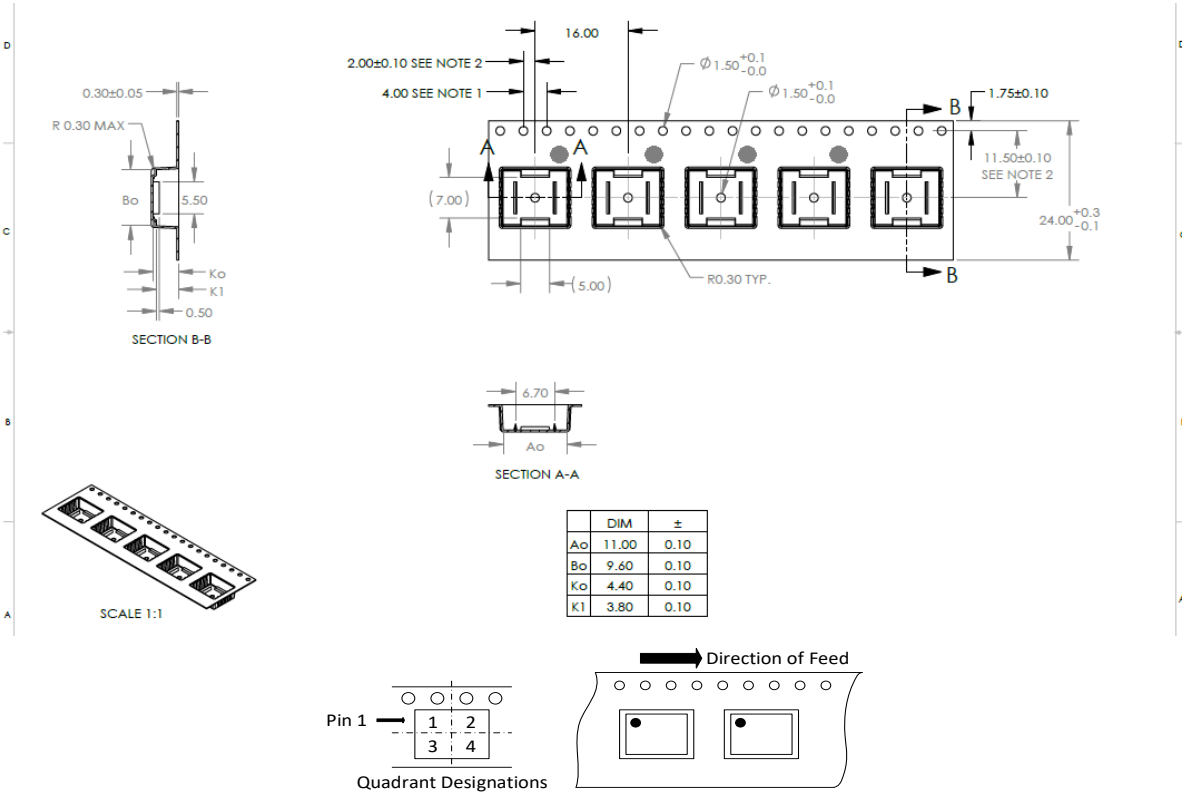


Ao	6.50 +/– 0.1
Bo	5.30 +/– 0.1
Ko	2.20 +/– 0.1
K1	1.90 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

Figure 13.4 Tape Information of SOP8(150mil)



	DIM	±
Ao	11.00	0.10
Bo	9.60	0.10
Ko	4.40	0.10
K1	3.80	0.10

Figure 13.5 Tape Information of DUB8

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14. Revision History

Revision	Description	Date
1.0	Initial release	2023/11/7
1.1	Update Regulatory Information in 7.3. Update Figure 10.1 SOW8 Package Shape and Dimension in millimeters and Figure 10.5 DUB8 Package Shape and Dimension in millimeters. Add Figure 10.6 DUB8 Package Board Layout Example and Figure 13.2 Reel Information for DUB8 Add the label of Release to market in Part 11. Update Template of datasheet.	2025/6/17

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