NOVOSENSE

NSD8381

Bipolar Stepper Motor Driver with Micro-step Dual H-Bridge or Quad Half Bridge

Datasheet (EN) 1.1

Product Overview

The NSD8381 is a bipolar stepper motor driver, supporting up to max 1.35A full-scale current, for wide range automotive applications including headlight position, projector adjustment actuator in HUD and other valves or BDC motors used in thermal management application.

The device includes current chopping regulation, internal up to 1/32 micro-step translator and multiple decay modes selection to enable stepper motor smooth motion. Furthermore, configurable full-scale current, external pin as simple STEP / DIR input and HOLD mode, all these functions easy customer management of stepper motor operation.

The device is fully protected from faults and short circuits, including undervoltage, overcurrent and overtemperature. Also, open load diagnosis and stall detection can be individually requested to perform during system running. Both SPI interface and dedicated DOUT1/DOUT2 pins are provided to indicate these fault status & alert to microcontroller.

With the different connection of half bridge outputs and HBMODE control, the device can also work as 4x independent half bridges and support other various load as BDC motor, relay etc.

The device features sleep mode with low quiescent current when EN input is low or VDD falls below POR threshold.

Applications

- Headlight adjustment
- HUD
- Actuator control in thermal management

Device information

Part Number	*Package*	*Body Size*
NSD8381-Q1QAIR	VQFN40	6mm × 6mm
NSD8381-Q1QANR	VQFN32	5mm × 5mm

Key Features

- Bipolar stepper motor driver with max 1.35A full scale current or 4x independent half bridge driver
  - Wide 4.5-V to 36-V Operating Voltage
  - 1200mΩ Typical $R_{DS(ON)}$ (HS + LS), per leg
- Programmable input IOs for STEP / DIR / HOLD or direct half bridge control
- Programmable step mode:

  Full step, half step, mini step, 1/8 micro step, 1/16 micro step, 1/32 micro step
- Programmable output stage slew rate / dead time
- Selectable decay mode:

  Slow decay, mixed decay, auto decay 1, auto decay 2
- Current regulation loop with fully integrated PWM controller and internal current sensing
  - 4bit programmable full scale current and 4-bit programmable HOLD current
  - Internal DAC for reference current generation
  - Spread spectrum function on PWM for EMC reduction
- Very low power consumption in sleep mode
- SPI Interface (24-bit, 4 MHz)
- VQFN40 or VQFN32, wettable flank with exposed pad
- AEC-Q100 Grade 1 Qualified
- Integrated Protection Features
  - VS Undervoltage Lockout (VS UV)
  - Overcurrent Protection (OCP)
  - Thermal Warning (OTW/UTW) and Shutdown (OTSD)
  - Open load detection
  - Stall detection based on BEMF sensing
  - Fault indicating (FAULT)

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1. Pin Configuration and Functions

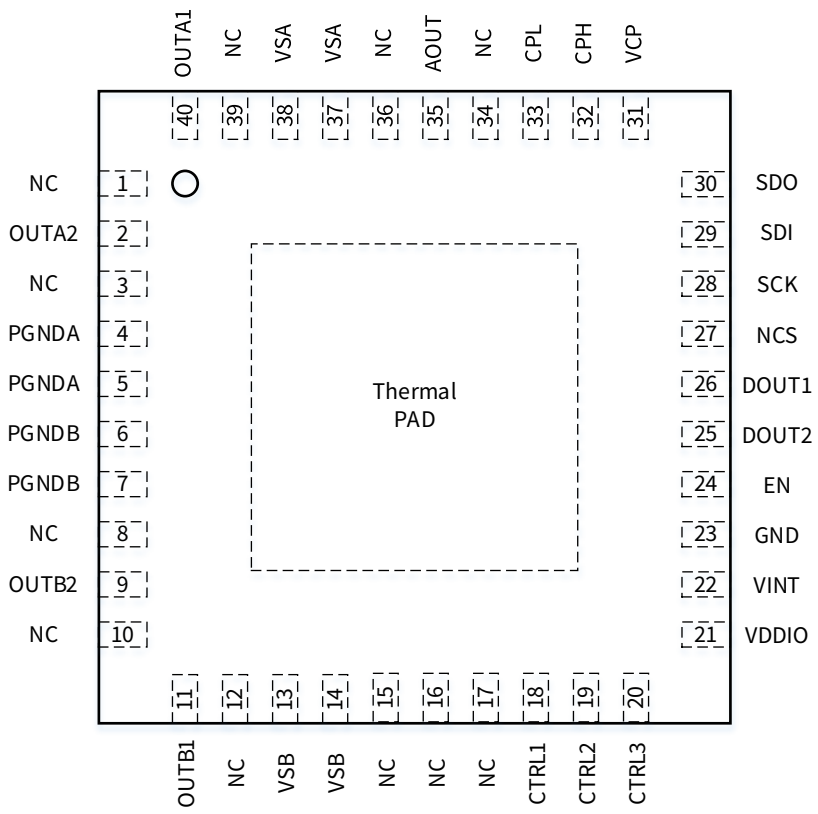


Figure 1-1 NSD8381 VQFN40 Pinout (top view)

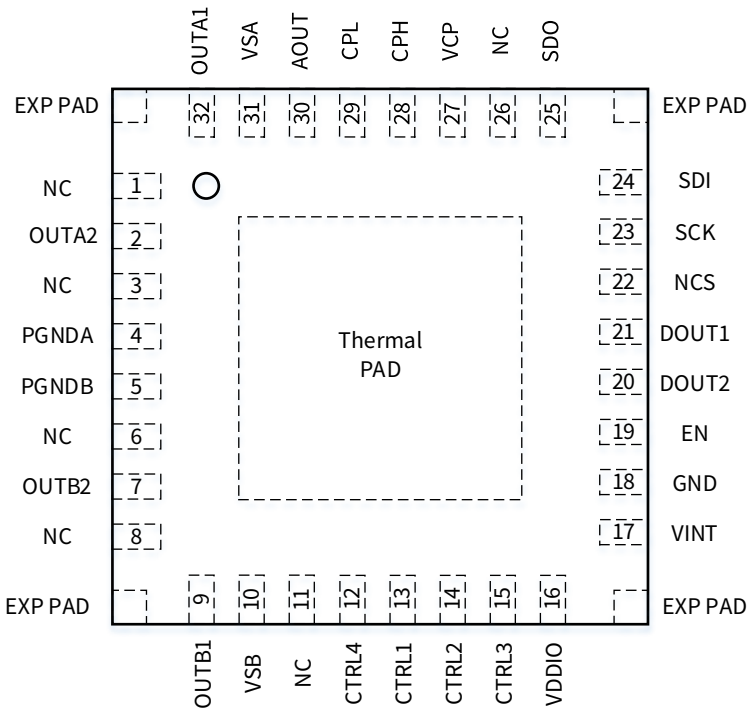


Figure 1-2 NSD8381 VQFN32 Pinout (top view)

Table 1-1. NSD8381 Pin Configuration and Description

NAME	NSD8381 PIN		TYPE	DESCRIPTION
	VQFN40 NO.	VQFN32 NO.		
CTRL4	-	12	I	Logic inputs 4. It has internal pull downs. In bipolar stepper mode, no function associated with CTRL4. In half bridge mode, CTRL4 pin controls the OUTB2 output as PWM input. CTRL4 is only available on NSD8381 -Q1QANR / VQFN32 pin out, and NOT presented in NSD8381 -Q1QAIR / VQFN40.
CTRL1	18	13	I	Logic inputs 1. It has internal pull downs. In bipolar stepper mode, CTRL1 pin are configured as STEP input function in default. In half bridge mode, CTRL1 pin controls the OUTA1 output as PWM input.
CTRL2	19	14	I	Logic inputs 2. It has internal pull downs. In bipolar stepper mode, CTRL2 pin are configured as DIR input function in default.

				In half bridge mode, CTRL2 pin controls the OUTA2 output as PWM input.
CTRL3	20	15	I	Logic inputs 3. It has internal pull downs. In bipolar stepper mode, no function associated with CTRL3 in default. HOLD or SMODE input function through CTRL3 pin can be active by SPI setting after device powers up. In half bridge mode, CTRL3 pin controls the OUTB1 output as PWM input.
VDDIO	21	16	PWR	Digital I/Os supply. Suggest 100nF X7R decoupling capacitor closed to VDDIO pin.
VINT	22	17	PWR	Internal regulator decoupling output. Connect 100nF X7R ceramic capacitor to ground, the capacitor shall be closed to VINT pin.
GND	23	18	PWR	Device ground. Connect to system ground.
EN	24	19	I	Device-enable input pin with internal pull down (active HIGH). If EN input pin is pulled low, all OUTAx/OUTBx go to tri-state and device move to low-power sleep state.
DOUT2	25	20	O	Push-pull output DOUT2 for fault indication or internal PWM signal or fault check indication, selected by SPI setting.
DOUT1	26	21	O	Push-pull output DOUT1 for coil voltage conversion status signals, selected by SPI setting.
NCS	27	22	I	SPI chip select input pin.
SCK	28	23	I	SPI clock input pin.
SDI	29	24	I	SPI data input pin.
SDO	30	25	O	SPI data output pin.
VCP	31	27	PWR	Charge pump output. Put 100nF X7R capacitor between VCP and VSx pins.
CPH	32	28	PWR	Charge pump high side pin, connect a 100nF X7R capacitor between CPH and CPL pins.
CPL	33	29	PWR	Charge pump low side pin, connect a 100nF X7R capacitor between CPH and CPL pins.
AOUT	35	30	O	Internal analog voltage or reference mux output.
VSA	37,38	31	O	5V to 36V power supply. Connect a 0.1-μF bypass capacitor to ground, as well as sufficient bulk capacitor needs to guarantee VSx pin voltage in maximum range. Put the 0.1uF and bulk capacitor (≥22uF) close to the VSx pin. Two VSA and VSB pins should be externally connected together.
OUTA1	40	32	O	Half-bridge output OUTA1 pin. Connect directly to the motor or other inductive load.

OUTA2	2	2	O	Half-bridge output OUTA2 pin. Connect directly to the motor or other inductive load.
PGNDA	4,5	4	PWR	High-current ground path. Connect PGND directly to board ground.
PGNDB	6,7	5	PWR	High-current ground path. Connect PGND directly to board ground.
OUTB2	9	7	O	Half bridge output OUTB2 pin. Connect directly to the motor or other inductive load.
OUTB1	11	9	O	Half bridge output OUTB1 pin. Connect directly to the motor or other inductive load.
VSB	13,14	10	PWR	5V to 36V power supply. Connect a 0.1-μF bypass capacitor to ground, as well as sufficient bulk capacitor needs to guarantee VSx pin voltage in maximum range. Put the 0.1uF and bulk capacitor (≥22uF) close to the VSx pin. Two VSA and VSB pins should be externally connected together.
NC	1,3,8,10, 12,15,16,17, 34,36,39	1,3,6,8, 11,26,30	-	Not connected
Thermal PAD	-	-	-	Exposed thermal pad. Connect to board ground. For good thermal dissipation, use large ground planes on multiple layers, and multiple nearby vias connecting those planes.
EXP PAD	-	-	-	Corner exposed pad pins only on VQFN32 package, which are internal electrically shorted to thermal pad in the package. Recommend to solder them toward floating or GND node for mechanical robustness.

2. Absolute Maximum Rating

ITEMS	MIN	MAX	UNIT
Power supply voltage (VSA, VSB)	–0.3	40	V
VDDIO voltage	–0.3	5.75	V
VINT voltage	–0.3	5.75	V
Logic input/ouput voltage (SDI, SDO, NCS, SCK, EN, CTRL1, CTRL2, CTRL3, CTRL4, DOUT1, DOUT2)	–0.3	VDDIO+0.3	V
Analog output (AOUT)	–0.3	40	V
VCP, CPH charge pump voltage	VS-0.3	VS+6	V
CPL, charge pump negative pin voltage	-0.3	VS	V
Output voltage (OUTA1, OUTA2, OUTB1, OUTB2) DC condition	–0.3	VS+0.3	V
Output voltage (OUTA1, OUTA2, OUTB1, OUTB2) AC condition, Iout=1A for t<500ms, voutx < VPS+1V	-1	VS+1	V

3. ESD Ratings

SYMBOL	DESCRIPTION	VALUE	UNIT
VESD_HBM	Human Body Model(HBM), all pins per ANSI/ESDA/JEDEC JS-001	±2000	V
VESD_CDM	Charged device model(CDM), Corner pin, per JEDEC specification JS-002	±750	V
	Charged device model(CDM), other pins, per JEDEC specification JS-002	±500	V

4. Recommended Operating Conditions

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VS	VSA, VSB Power supply voltage	4.5		36	V
VDDIO	VDD supply voltage	3		5.5	V
EN, NCS, SCK, SDO, SDI, CTRL1, CTRL2, CTRL3, CTRL4, DOUT1, DOUT2	Logic input / output voltage	0		5.5	V

AOUT	Analog output voltage	0		5.5	V
CTRL1	STEP signal low or high timing	2			us
IFS(1)	Motor full scale current			IFSR (MAX 1.35)	A
IRMS(1)	Motor RMS current			IFSR*0.707 (MAX 1.06)	A

(1) The maximum allowable output load current shall be also evaluated considering application scenario, for both power dissipation and thermal condition including ambient temperature, application board thermal condition etc.

5. Thermal Information

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
Ta	Ambient operating ambient temperature	-40		125	°C
Tj	Junction temperature	-40		150	°C
Tstg	Storage temperature	-65		150	°C
Rthjc	VQFN40, Thermal resistance, junction to case		5		°C/W
Rthjc	VQFN32, Thermal resistance, junction to case		5		°C/W
Rthja	VQFN40, Thermal resistance, junction to ambient, on 1S0P PCB based on JEDEC standard		56		°C/W
	VQFN40, Thermal resistance, junction to ambient, on 2S2P (4-layer) PCB based on JEDEC standard		31		°C/W
Rthja	VQFN32, Thermal resistance, junction to ambient, on 1S0P PCB based on JEDEC standard		60		°C/W
	VQFN32, Thermal resistance, junction to ambient, on 2S2P (4-layer) PCB based on JEDEC standard		32		°C/W

6. Functional description

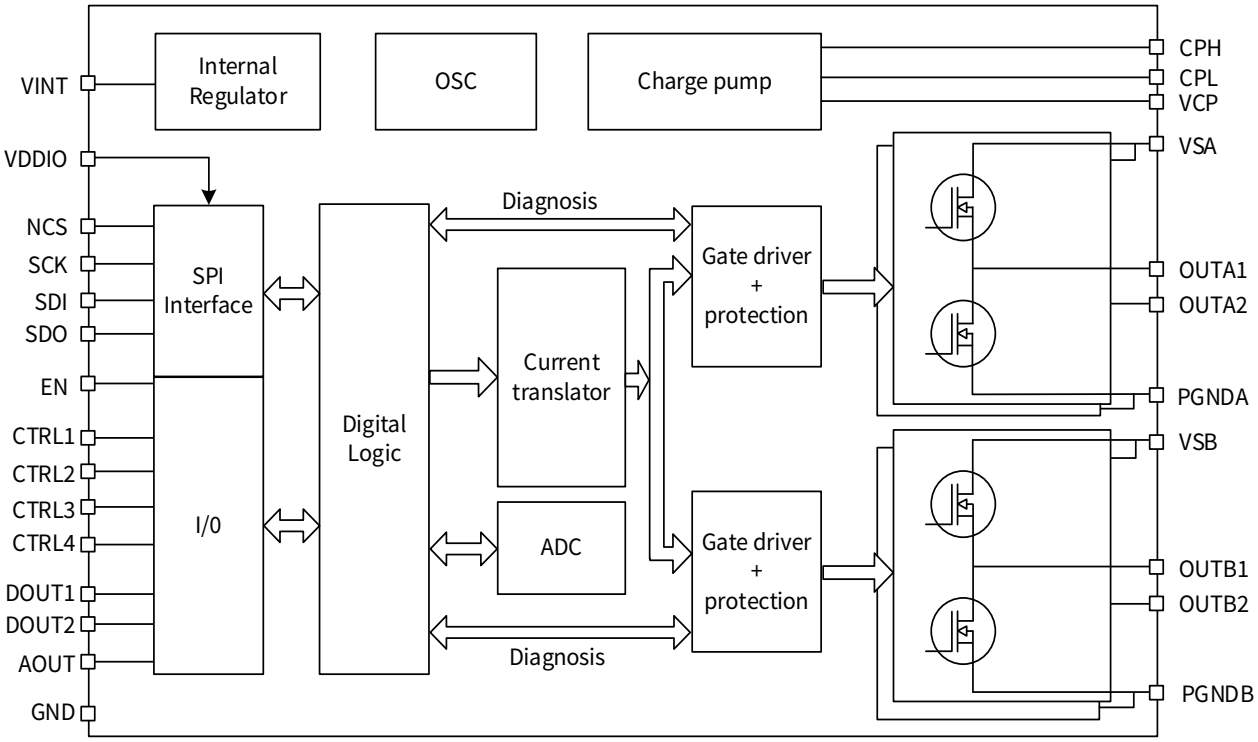


Figure 6-1. Block diagram

6.1. VSA, VSB Input

VS is the supply voltage used for internal H-bridge outputs and change pump; it ranges from 4.5v to 36v with typical case 13.5v power supply. VSA and VSB pins must be shorted together externally on PCB.

During motor operation, electrical energy is stored in the motor coils, and then fed back to the supply voltage VS once motor shut down. Thus, it is required to put at both ceramic and bulk electrolytic capacitor closed to VSA, VSB pin to avoid electrical spike / overstress on VSA and VSB pins.

6.1.1.VS UV, VS RST

When VS power supply pin voltage falls below the undervoltage threshold (VS_UV_L) over 10us typ. undervoltage deglitch time,

- The corresponding VS undervoltage flag (***VSUV bit*** in ***STA_1*** register) is set to '1';
- Half bridge outputs OUTA1, OUTA2, OUTB1, OUTB2 becomes OFF and charge pump is switched off.

When VS rise above the VS_UV_H longer than 10us typ. undervoltage deglitch time, then

- If ***FLT_LATCH*** bit = '1', device works in fault latch mode, to recovery normal operation, ***VSUV*** bit shall be read & clear to re-enable charge pump and ***DRV_EN*** bit in ***CONFIG_3*** register shall remain unchanged '1', active enable.
- If ***FLT_LATCH*** bit = '0' (default), device automatically resumes operation, when ***DRV_EN*** bit remains unchanged '1' active enable status and charge pump voltage exit CP_UV. In the meantime, the ***VSUV*** flag bit keeps '1' until read & clear command is received.

When VS power supply pin voltage falls below the undervoltage reset threshold (VS_RST_L) over 5us typ. undervoltage reset deglitch time,

- SPI unavailable.
- Half bridge outputs OUTA1, OUTA2, OUTB1, OUTB2 becomes OFF and charge pump is switched off.

When VS rise above the VS_RST_H threshold longer than 5us typ. undervoltage deglitch time, then

- Device is reset and all SPI registers are reset to default value.

6.1.2. VS OV protection

When ***OVP_DIS*** bit = '0' and VS power supply pin voltage rises above the overvoltage threshold (VS_OV_H) over 10us typ. overvoltage deglitch time,

- The corresponding VS overvoltage flag (***VSOV bit*** in ***STA_1*** register) is set to '1';
- half bridge outputs OUTA1, OUTA2, OUTB1, OUTB2 becomes OFF and charge pump is switched off.

When ***OVP_DIS*** bit = '0' and VS decrease under the VS_OV_L threshold longer than 10us typ. overvoltage deglitch time, then

- If ***FLT_LATCH*** bit = '1', device works in fault latch mode, to recovery normal operation, ***VSOV*** bit shall be read & clear and ***DRV_EN*** bit remains unchanged '1' active enable status
- If ***FLT_LATCH*** bit = '0' (default), device automatically resumes operation when ***DRV_EN*** bit in ***CONFIG_3*** register remains unchanged '1' active enable status. The ***VSOV*** bit keeps '1' until read & clear command is received.

When ***OVP_DIS*** bit = '1', overvoltage protection function is disabled, no reaction on ***VSOV*** status and ***DRV_EN*** bit, half bridge outputs OUTA1, OUTA2, OUTB1, OUTB2, charge pump; in consequence, no need for overvoltage recovery.

6.1.3.VS power supply electrical specifications

T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VSA, VSB)						
VS	VS operating voltage		4.5		36	V
I_{VS}	VS operating supply current	VSA = VSB = 13.5V, EN=HIGH, all output off		3	7	mA
		VSA = VSB = 13.5V, EN=HIGH, half bridge driver working, no load			10	mA
I_{VS_SLEEP}	VS sleep current	VSA= VSB = 13.5V, -40≤Tj≤85ºC EN=LOW, I(VSA)+I(VSB) Half bridge driver output = GND			10	μA
VS_UV_L	VS undervoltage threshold	VSx falls until VSUV triggers	4.25	4.5	4.75	V
VS_UV_H		VSx rises until operation recovers	4. 5	4.75	5	V
V_{UV_HYS}	VS undervoltage hysteresis			200		mV
t_{UV}	VS undervoltage deglitch time	Guaranteed by digital scan	7	10	13	us

VS_RST_L	VS undervoltage reset	VSx fall until reset triggers	2.9	3.3	3.7	V
VS_RST_H		VSx rise until reset	3.1	3.5	3.9	V
$V_{UV\_RST\_HYS}$	VS undervoltage reset hysteresis			200		mV
VS_OV_H	VS overvoltage	VSx increasing, OVP_DIS = '0'	28		32	V
VS_OV_L		VSx decreasing, OVP_DIS = '0'	27		31	V
V_{OV_HYS}	VS overvoltage hysteresis			1		V
t_{OV}	VS overvoltage deglitch time	Guaranteed by digital scan	7	10	13	us
C_{VS}	Capacitor on VSA, VSB pin	Application information		100		nF
C_{VS_BULK}	Bulk Capacitor on VSx pin	Application information		22		uF

6.2. VINT internal regulator

A linear voltage regulator is integrated into the device to supply internal blocks.

For proper operation, connect the VINT pin to GND using a ceramic capacitor which typical value is 100nF and min/max ranges from 47nF~470nF.

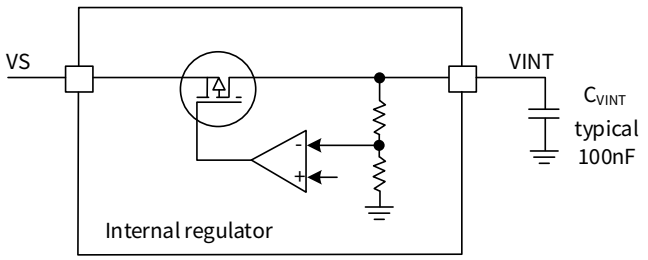


Figure 6-2. Internal regulator block diagram

During sleep state, the internal regulator is disabled.

6.2.1.VINT internal regulator electrical specifications

T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal regulator (VINT)						
V_{VINT}	VINT internal regulator voltage	Load current 0~2mA	4.65	5	5.35	V
C_{VINT}	Capacitor on VINT pin	Application information	47	100	470	nF

6.3. VDDIO Supply Input

VDDIO pin accepts wide external supply range from 3v to max 5.5v, which intends for the compatibility with both 3.3v and 5v system supply. 100nF X7R ceramic capacitor is suggested to put closed to VDDIO pin.

When VDDIO drops below VDDIO_RST_L, SPI interface, digital output will be inactive, also including charge pump and all half bridge drivers are switched off.

Once VDDIO > VDDIO_RST_H, internal digital is reset and back to normal working state.

6.3.1.VDDIO internal regulator electrical specifications

T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDDIO supply input (VDDIO)						
I_{VDDIO}	Input current of VDDIO	EN=High, outputs off			1	mA
I_{VDDIO_SLEEP}	Input current of VDDIO in sleep mode	EN=LOW, SPI inactive -40≤Tj≤85 ºC		3.5	10	uA
$V_{VDDIO\_RST\_H}$	VDDIO reset high threshold,	VDDIO increasing	2	2.5	3	V
$V_{VDDIO\_RST\_L}$	VDDIO reset low threshold	VDDIO decreasing	1.8	2.3	2.8	V

6.4. Charge pump

To drive internal high side output, a charge pump is used to generate the high side gate driving voltage which is above VS. In the meanwhile, external fly capacitor between CPH and CPL, also external tank capacitor between VS and VCP, are required.

Additionally, a built-in monitoring circuit checks if the charge pump output voltage is sufficient high. In case of VCP undervoltage ($V_{CP} < V_{CP\_UV}$), the outputs (OUTA1, OUTA2, OUTB1, OUTB2) are actively turned off and ***CPUV bit*** **in** ***STA_1*** **register** is set and latched.

- If ***FLT_LATCH*** bit = '1', device works in fault latch mode, to recovery normal operation, CPUV bit shall be read & clear and V_{CP} rise above V_{CP_UV} with t_{CP_UV}.
- If ***FLT_LATCH*** bit = '0' (default), output stage automatically resumes operation if V_{CP} rise above V_{CP_UV} with t_{CP_UV}. The CPUV bit keeps latch until read & clear command is received.

The charge pump nominal frequency is 400kHz, it also has the possibility to enable internal frequency with modulation through spread spectrum (***CP_SS_CONFIG bit*** in ***CONFIG_8*** register)

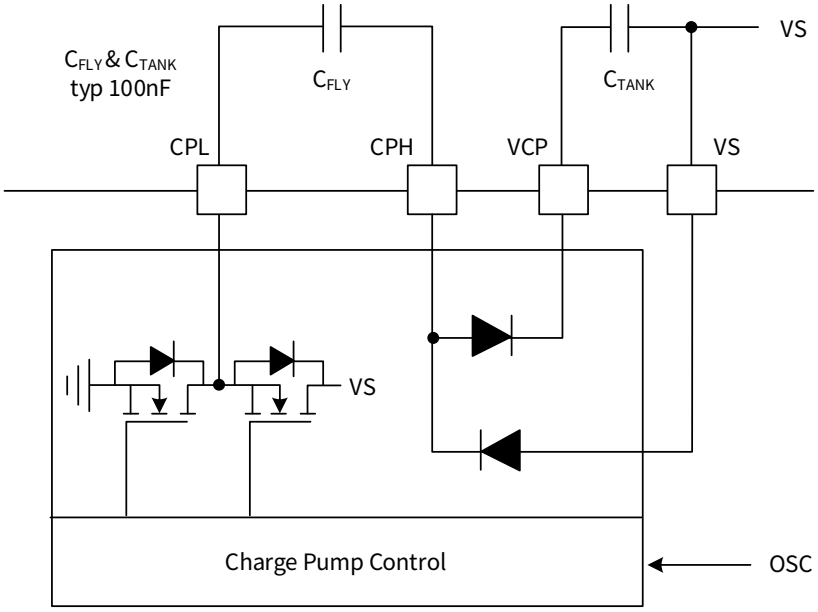


Figure 6-3. Charge pump block diagram

6.4.1.VCP charge pump electrical specifications

T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Charge pump (VCP)						
V_{CP}	Charge pump output voltage	VSx >=9V, I_{VCP}=3mA	VS+4.5	VS+5		V
		6v<VSx <9V, I_{VCP}=3mA	VS+4			V
V_{CP_UV}	Charge pump undervoltage	VCP falling		VS+3		V
$V_{CP\_UV\_HYS}$	Charge pump undervoltage hysteresis			200		mV
t_{CP_UV}	Charge pump undervoltage digital deglitch filter	Guaranteed by digital scan		10		us
F_{CP}	Charge pump frequency	spread spectrum disable		400		kHz
		spread spectrum enable		+/- 10%		kHz
C_{FLY}	Fly capacitor between CPH and CPL pin	Application information		100		nF
C_{TANK}	Tank capacitor between VS and VCP pin	Application information		100		nF

6.5. Digital Input EN & CTRL1/2/3/4 & SPI SDI/SCK/NCS

NCS / SDI / SCK is the typical CMOS schmitt trigger as SPI inputs.

EN, SCK, SDI and CTRL1/2/3/4 input pins have typ. 100kohm internal pull-down resistance, while 100kohm internal pull up is applied on NCS pin.

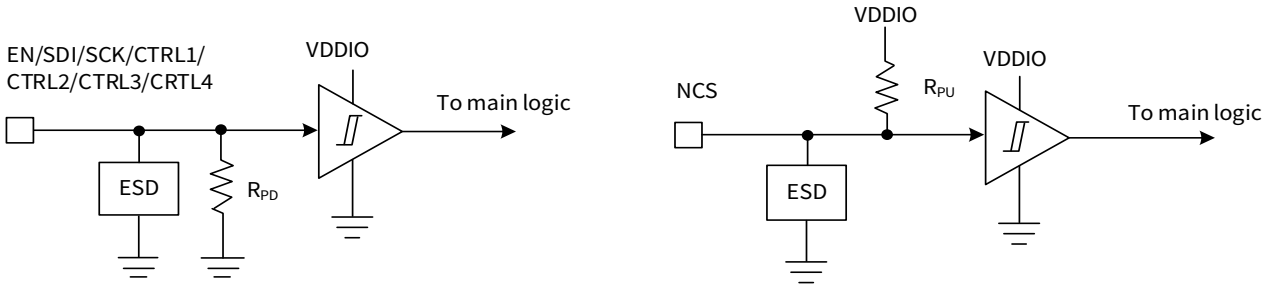


Figure 6-4. Digital input pins block diagram

6.5.1.EN Function

The EN pin is sleep / active mode control signal.

When it is driven low, internal logic / register is reset, charge pump / all outputs OUTA1/A2, OUTB1/OUTB2 are disabled, and device enter sleep mode.

After EN transition from low to high at VDDIO>$V_{VDDIO\_RST\_H}$ & VS>V_{UV_RST}, device come out sleep mode at finishing internal POR and set ***RSTB bit*** in ***global status byte*** of SDO frame.

Once device move from sleep to normal operation. a t_{WAKE} timing shall be wait, it is used to setup internal circuit / block, such as SPI, digital logic, and charge pump.

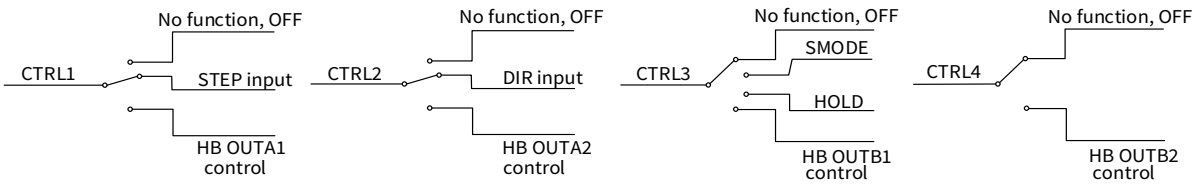
6.5.2.CTRL1/2/3/4 Function

The functions in NSD8381, such as stepper mode – STEP / DIR / HOLD input, can be directly controlled by microcontroller I/Os through the CTRL1/2/3 digital input pins or partially use I/O with the combination of SPI.

A typical example can be CTRL1 as STEP function connecting to MCU PWM function I/O, both CTRL2 and CTRL3 pins are floating, DIR and HOLD function are controlled by SPI register operation. Anyhow, so flexible is the configuration of CTRL1/2/3/4 that several combinations (ie. minimize MCU I/O numbers - CTRL1/2/3 all floating and STEP/DIR/HOLD all SPI control, general usage - 2x I/O CTRL1/2 for STEP/DIR, etc.) are feasible.

To support half bridge operation, CTRL1/2/3/4 has to be configured in order to map and control outputs (OUTA1/A2/B1/B2)

The above-mentioned CTRL1/2/3/4 different configurations are defined by selection bits (***CTRL1_SEL, CTRL2_SEL, CTLR3_SEL[1:0]***) in ***CONFIG_1*** and ***HB_MODE bit*** in ***CONFIG_8*** register.



Note: CTRL4 is only available on NSD8381 -Q1QANR / VQFN32 pin out, and NOT presented in NSD8381 -Q1QAIR / VQFN40.

CTRL1/2/3/4 pin selection function and details description are defined as Table 6-1.

Table 6-1. CTRL1/2/3/4 function summary

Pin	Function	Register configuration		Comment
		CONFIG_1	CONFIG_8	
CTRL1	Stepper mode - no function	Bit D5, ***CTRL1_SEL***='0'	Bit D3, ***HB_MODE*** ='0'	STEP signal is not related to CTRL1 under this register bits setting. STEP is controlled by writing ***PH[5:0]*** in ***CONFIG_3*** or ***APH[6:0]*** in ***CONFIG_7*** (if CONFIG_8, 1/32_STEP_EN bit =1)
	Stepper mode - STEP input	Bit D5, ***CTRL1_SEL***='1'	Bit D3, ***HB_MODE*** ='0'	**Default setting, after power up.** CTRL1 pin as stepper mode - STEP signal input. Phase counter ***PH[5:0]*** in ***CONFIG_3*** or ***APH[6:0]*** in ***CONFIG_7*** is read-only.
	Half bridge - OUTA1 control	Don't care	Bit D3, ***HB_MODE*** ='1'	See details in section '***Half bridge mode***'
CTRL2	Stepper mode - no function	Bit D3, ***CTRL2_SEL***='0'	Bit D3, ***HB_MODE*** ='0'	DIR signal is not related to CTRL2 under these register bits setting. It is controlled by SPI ***DIR*** bit in ***CONFIG_3***.
	Stepper mode - DIR input	Bit D3, ***CTRL2_SEL***='1'	Bit D3, ***HB_MODE*** ='0'	**Default setting, after power up** CTRL2 pin as stepper mode - DIR signal input.
	Half bridge – OUTA2 control	Don't care	Bit D3, ***HB_MODE*** ='1'	See details in section '***Half bridge mode***'
CTRL3	**Stepper mode - no function**	Bits D2&D1, ***CTRL3_SEL[1:0]***= '00'	Bit D3, ***HB_MODE*** ='0'	**Default setting, after power up**. Changing stepper mode or switching into HOLD are not related to CTRL3 pin under these register bits setting. Device into HOLD operation mode is controlled by ***HOLD_EN*** bit in ***CONFIG_3***.
	Stepper mode - SMODE input	Bits D2&D1, ***CTRL3_SEL[1:0]***= '01'	Bit D3, ***HB_MODE*** ='0'	CTRL3 pin controls stepper operation mode switching between ***ASM[2:0]*** and ***SM[2:0]*** under these register bits setting
	Stepper mode - HOLD input	Bits D2&D1, ***CTRL3_SEL[1:0]***= '10'	Bit D3, ***HB_MODE*** ='0'	CTRL3 pin directly controls HOLD operation mode switching under these register bits setting
	Half bridge - OUTB1 control	Don't care	Bit D3, ***HB_MODE*** ='1'	See details in section '***Half bridge mode***'
CTRL4	**Stepper mode - no function**	No bit in CONFIG_1 related CTRL4	Bit D3, ***HB_MODE*** ='0'	**Default setting, after power up**
	Half bridge - OUTB2 control	Don't care	Bit D3, ***HB_MODE*** ='1'	See details in section 'Half bridge mode'

6.5.3.Logical control input pins electrical specifications

T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic Control Input (EN, NCS, SDI, SCK, CTRL1, CTRL2, CTRL3, CTRL4)						
V_{IL}	Input logic low voltage				0.8	V
V_{IH}	Input logic high voltage		2			V
V_{HYS}	Input logic hysteresis			0.5		V
R_{PD}	Pulldown resistance	EN, SDI, SCK, CTRL1, CTRL2, CTRL3, CTRL4	50	100	150	kΩ
R_{PU}	Pullup resistance	NCS	50	100	150	kΩ
C_{IN}	Input capacitance	NCS, SDI, SCK, CTRL1, CTRL2, CTRL3, CTRL4 pin Specified by design			15	pF
$t_{Deglitch\_EN}$	Deglitch filter on EN falling and rising	Specified by design		10	20	us
t_{WAKE}	wake-up time	From EN low to high transition until SPI ready, specified by design			250	us
		From EN low to high transition until Output transition, specified by design			1.5	ms

6.6. Digital output SDO and DOUT1 / DOUT2

SDO is push-pull structure, which transfers internal register values to microcontroller. It also features SDO tristate at NCS high when device SPI interface is not selected.

The two DOUT pins, DOUT1 & DOUT2, are also push-pull structure with tristate when EN pin is low.

6.6.1.DOUT1 / DOUT2 functions

The device drives DOUT1 & DOUT2 pins upon detecting internal status or faults signals, as shown in Table 6-2 and Table 6-3.

Table 6-2. DOUT1 function table

***DOUT1_SEL[1:0]* in *CONFIG_2* register**	**DOUT1 function**
2b'00'	OFF, tri-state (EN pin low), low (EN pin high)
2b'01'	Coil voltage conversion ready signal (CVRDY) output
2b'10'	Coil voltage conversion under low limit (CVLL) output
2b'11'	Coil voltage conversion out of range (CVOOR) output

DOUT2_SEL[1:0] in *CONFIG_2* register	DOUT2 function
2b'00'	OFF, tri-state (EN pin low), low (EN pin high)
2b'01'	Internal current regulation PWM signal (PWM)
2b'10'	Fault (Fault) output, active high when fault detected, on the contrary, logic low stands for normal operation or no fault detected.
2b'11'	Fault Check Indicator (FCI)

Table 6-3. DOUT2 function table

6.6.2.Digital output pins electrical specifications

T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DOUT1, DOUT2, SDO output (push-pull)						
V_{OL}	DOUT1 & DOUT2 & SDO output low voltage	I_O = 2 mA		0.2	0.5	V
V_{OH}	DOUT1 & DOUT2 & SDO Output high	I_O = 2 mA	VDDIO -0.5			V
I_{leak_DOUT}	DOUT1 & DOUT2 & SDO Output leakage current	DOUT1, DOUT2 function selection OFF, EN=0, 0<V_{DOUT}<VDDIO NCS high, 0<V_{SDO}<VDDIO	-1		1	uA
C_{DOUT}	Digital output capacitance	Specified by design			60	pF

6.7. Analog output AOUT

The device integrates an analog output channel, which can be selectable among embedded sensor output, internal bandgap voltage reference, see ***CONFIG_1*** register ***AOUT_SEL*** bits setting.

Table 6-4. AOUT function table

AOUT_SEL[1:0] in *CONFIG_1* register	AOUT function
2b'00' or 2b'11'	Disabled
2b'01'	Voltage proportional to junction temperature
2b'10'	Bandgap voltage

6.7.1.Analog output pins electrical specifications

T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog output (Bandgap)						
V_{AOUT_BG}	V_{AOUT_BG} Bandgap output voltage			1.2		V
$V_{AOUT\_BG\_ERR}$	$V_{AOUT\_BG\_ERR}$ Bandgap output voltage accuracy		-2.5		2.5	%
Analog output (TSENSE)						
V_{AOUT_TSENSE}	Output voltage proportional to junction temperature			1.36		V
K_{AOUT_TSENSE}	Thermal coefficient of output proportional to junction temperature	Specified by design		-3.5		mv/°C
Analog output						
C_{AOUT}	Analog output capacitance	Specified by design			100	pF
I_{AOUT}	Output current	Design information			10	uA

6.8. Stepper operation

6.8.1.Stepper mode selection

Six different step modes, full step (4 steps), half step (8 steps), 1/4 mini step (16 steps), 1/8 micro step (32 steps), 1/16 micro step (64 steps), 1/32 micro step (128 steps), can be selected depending on application required step resolution.

CONFIG_3 register ***SM[2:0]*** / ***ASM[2:0]*** bits set two step modes independently among full step (4 steps) to 1/16 micro step (64 steps). In association with CTRL3 selection SMODE function, the two step mode selection bits, SM[2:0] and ASM[2:0], provide a convenient way in system to switch between two step modes. For example, SM[2:0] uses 1/16 micro step, ASM[2:0] chooses 1/4 micro step, CTRL3_SEL[1:0] is configured as SMODE switching function, CTRL3 pin sets high level to use ASM[2:0] 1/4 micro step, while moving CTRL3 pin to low level to use ASM[2:0] 1/16 micro step for more smooth operation in stepper motor.

CONFIG_8 register ***1/32 STEP_EN*** bit determines 1/32 micro step enable or not,

CONFIG_8 FULL_STEP_IFS bit selects full step mode full scale current percentage as 71% or 100%.

Note:

- ***PH[5:0]*** bits in ***CONFIG_3*** register stand for the phase counter value of full step, half step, 1/4 mini step, 1/8 micro step, 1/16 micro step, except 1/32 micro step. While ***APH[6:0]*** bits in ***CONFIG_7*** only represent the phase counter value in 1/32 micro step operation.
- Changing between 1/32 micro step and all other stepper modes (for example, 1/4 mini step, 1/16 micro step...etc.) on the fly is NOT allowed. This is due to ***DRV_EN*** bit in ***CONFIG_3*** register requires '0' or reset before 1/32 micro step enable. If different step modes changing on the fly is required, ***SM[2:0]*** related step modes (half step, 1/4 mini step, 1/8 micro step, 1/16 micro) shall be used.
- ***CONFIG_8*** register bit7~bit1, 7-bits including above mentioned ***1/32 STEP_EN*** bit, ***FULL_STEP_IFS*** bit, are lock and protected. To access and change these 7-bits setting, ***CONFIG_9*** register ***UNLOCK*** command has to be sent first.

After device POWER ON RESET (caused by VSx, EN, VDDIO), the internal step mode is reset to default (SM[2:0] 1/16 micro step) and coil current translator moves to the position 0 degree.

6.8.2.Coil current translator

Under micro step operation mode, the translator starts from position 0, and the next position is increased or decreased with 1 of the same columns. As shown in Table 6-5, the relative coil A current and coil B current vs. micro step modes / phase counter are listed.

Positive current is defined as current flowing from OUTA1 to OUTA2 or OUTB1 to OUTB2, in contrast, current from OUTA2 to OUTA1 or OUTB2 to OUTB1 is considered as negative.

Table 6-5. Step translator of micro step modes

APH[6:0]	PH[5:0]	1/32 micro step	1/16 micro step	1/8 micro step	1/4 mini step	1/2 half step	coil A % of IFS	coil B % of IFS
0000000	000000	0	0	0	0	0	0	100
0000001		1					4.91	99.88
0000010	000001	2	1				9.8	99.52
0000011		3					14.67	98.92
0000100	000010	4	2	1			19.51	98.08
0000101		5					24.3	97
0000110	000011	6	3				29.03	95.69
0000111		7					33.69	94.15
0001000	000100	8	4	2	1		38.27	92.39
0001001		9					42.76	90.4
0001010	000101	10	5				47.14	88.19
0001011		11					51.41	85.77
0001100	000110	12	6	3			55.56	83.15
0001101		13					59.57	80.32
0001110	000111	14	7				63.44	77.3
0001111		15					67.16	74.1
0010000	001000	16	8	4	2	1	70.71	70.71
0010001		17					74.1	67.16
0010010	001001	18	9				77.3	63.44
0010011		19					80.32	59.57
0010100	001010	20	10	5			83.15	55.56
0010101		21					85.77	51.41

0010110	001011	22	11				88.19	47.14
0010111		23					90.4	42.76
0011000	001100	24	12	6	3		92.39	38.27
0011001		25					94.15	33.69
0011010	001101	26	13				95.69	29.03
0011011		27					97	24.3
0011100	001110	28	14	7			98.08	19.51
0011101		29					98.92	14.67
0011110	001111	30	15				99.52	9.8
0011111		31					99.88	4.91
0100000	010000	32	16	8	4	2	100	0
0100001		33					99.88	-4.91
0100010	010001	34	17				99.52	-9.8
0100011		35					98.92	-14.67
0100100	010010	36	18	9			98.08	-19.51
0100101		37					97	-24.3
0100110	010011	38	19				95.69	-29.03
0100111		39					94.15	-33.69
0101000	010100	40	20	10	5		92.39	-38.27
0101001		41					90.4	-42.76
0101010	010101	42	21				88.19	-47.14
0101011		43					85.77	-51.41
0101100	010110	44	22	11			83.15	-55.56
0101101		45					80.32	-59.57
0101110	010111	46	23				77.3	-63.44
0101111		47					74.1	-67.16
0110000	011000	48	24	12	6	3	70.71	-70.71
0110001		49					67.16	-74.1
0110010	011001	50	25				63.44	-77.3
0110011		51					59.57	-80.32
0110100	011010	52	26	13			55.56	-83.15

0110101		53					51.41	-85.77
0110110	011011	54	27				47.14	-88.19
0110111		55					42.76	-90.4
0111000	011100	56	28	14	7		38.27	-92.39
0111001		57					33.69	-94.15
0111010	011101	58	29				29.03	-95.69
0111011		59					24.3	-97
0111100	011110	60	30	15			19.51	-98.08
0111101		61					14.67	-98.92
0111110	011111	62	31				9.8	-99.52
0111111		63					4.91	-99.88
1000000	100000	64	32	16	8	4	0	-100
1000001		65					-4.91	-99.88
1000010	100001	66	33				-9.8	-99.52
1000011		67					-14.67	-98.92
1000100	100010	68	34	17			-19.51	-98.08
1000101		69					-24.3	-97
1000110	100011	70	35				-29.03	-95.69
1000111		71					-33.69	-94.15
1001000	100100	72	36	18	9		-38.27	-92.39
1001001		73					-42.76	-90.4
1001010	100101	74	37				-47.14	-88.19
1001011		75					-51.41	-85.77
1001100	100110	76	38	19			-55.56	-83.15
1001101		77					-59.57	-80.32
1001110	100111	78	39				-63.44	-77.3
1001111		79					-67.16	-74.1
1010000	101000	80	40	20	10	5	-70.71	-70.71
1010001		81					-74.1	-67.16
1010010	101001	82	41				-77.3	-63.44
1010011		83					-80.32	-59.57

1010100	101010	84	42	21			-83.15	-55.56
1010101		85					-85.77	-51.41
1010110	101011	86	43				-88.19	-47.14
1010111		87					-90.4	-42.76
1011000	101100	88	44	22	11		-92.39	-38.27
1011001		89					-94.15	-33.69
1011010	101101	90	45				-95.69	-29.03
1011011		91					-97	-24.3
1011100	101110	92	46	23			-98.08	-19.51
1011101		93					-98.92	-14.67
1011110	101111	94	47				-99.52	-9.8
1011111		95					-99.88	-4.91
1100000	110000	96	48	24	12	6	-100	0
1100001		97					-99.88	4.91
1100010	110001	98	49				-99.52	9.8
1100011		99					-98.92	14.67
1100100	110010	100	50	25			-98.08	19.51
1100101		101					-97	24.3
1100110	110011	102	51				-95.69	29.03
1100111		103					-94.15	33.69
1101000	110100	104	52	26	13		-92.39	38.27
1101001		105					-90.4	42.76
1101010	110101	106	53				-88.19	47.14
1101011		107					-85.77	51.41
1101100	110110	108	54	27			-83.15	55.56
1101101		109					-80.32	59.57
1101110	110111	110	55				-77.3	63.44
1101111		111					-74.1	67.16
1110000	111000	112	56	28	14	7	-70.71	70.71
1110001		113					-67.16	74.1
1110010	111001	114	57				-63.44	77.3

1110011		115					-59.57	80.32
1110100	111010	116	58	29			-55.56	83.15
1110101		117					-51.41	85.77
1110110	111011	118	59				-47.14	88.19
1110111		119					-42.76	90.4
1111000	111100	120	60	30	15		-38.27	92.39
1111001		121					-33.69	94.15
1111010	111101	122	61				-29.03	95.69
1111011		123					-24.3	97
1111100	111110	124	62	31			-19.51	98.08
1111101		125					-14.67	98.92
1111110	111111	126	63				-9.8	99.52
1111111		127					-4.91	99.88

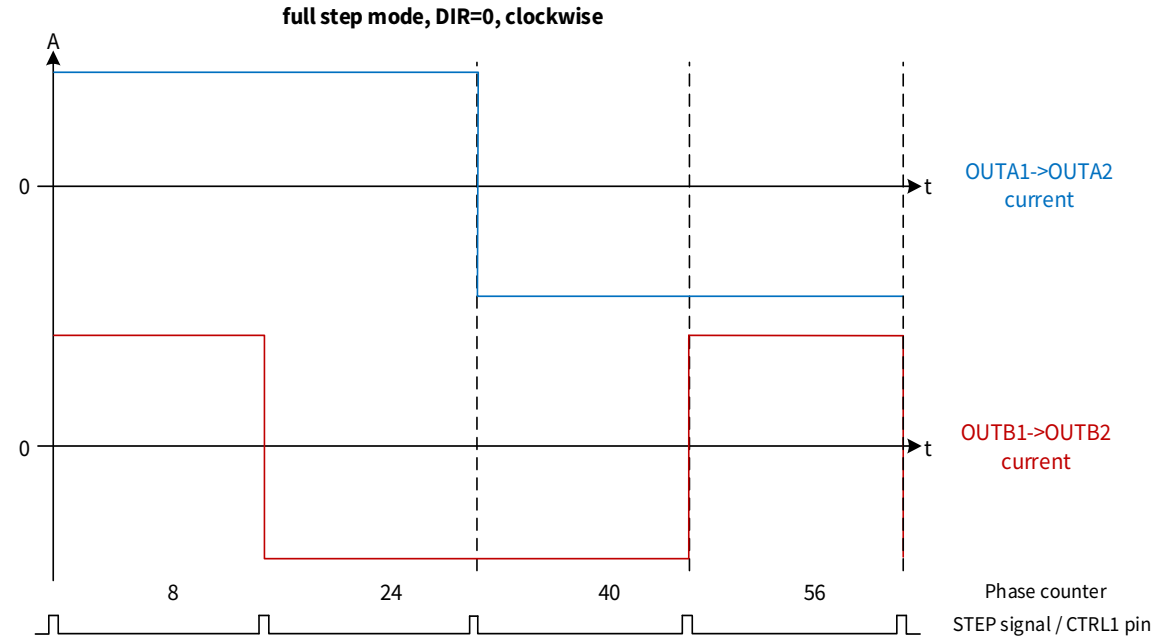
Table 6-6 shows full step operation with 100% full scale current.

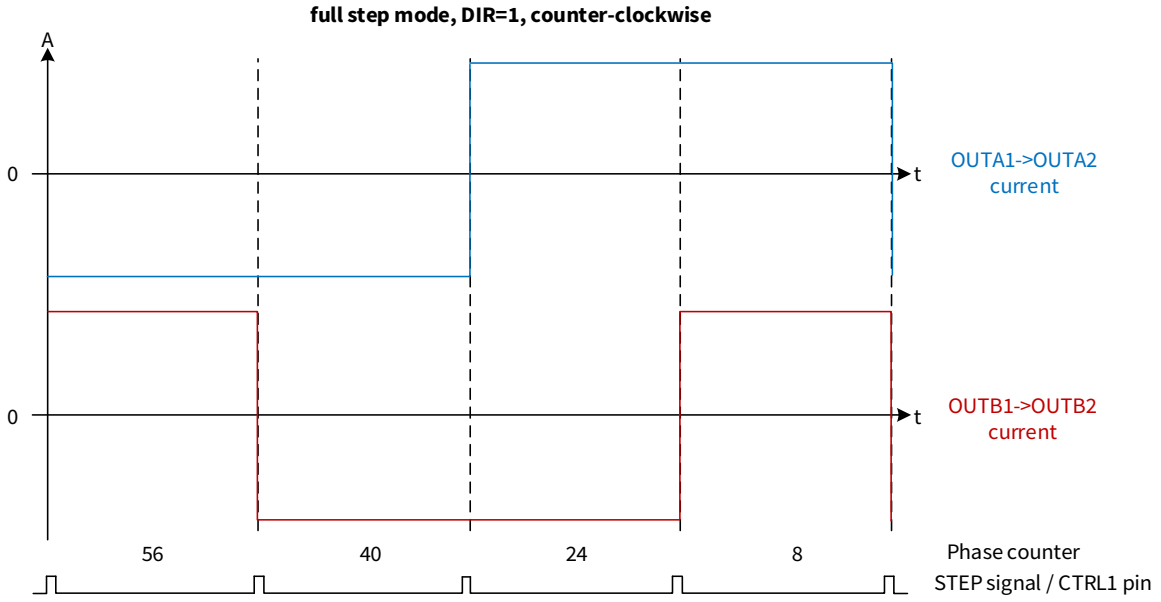
71% full scale current in full step operation is similar, difference is only coil current maxim value.

Table 6-6. Full step with 100% full scale current

PH[5:0]	Full step mode	Coil A current (% of IFS)	Coil B current (% of IFS)
001000	8	100	100
011000	24	100	-100
101000	40	-100	-100
111000	56	-100	100

6.8.3.Step update





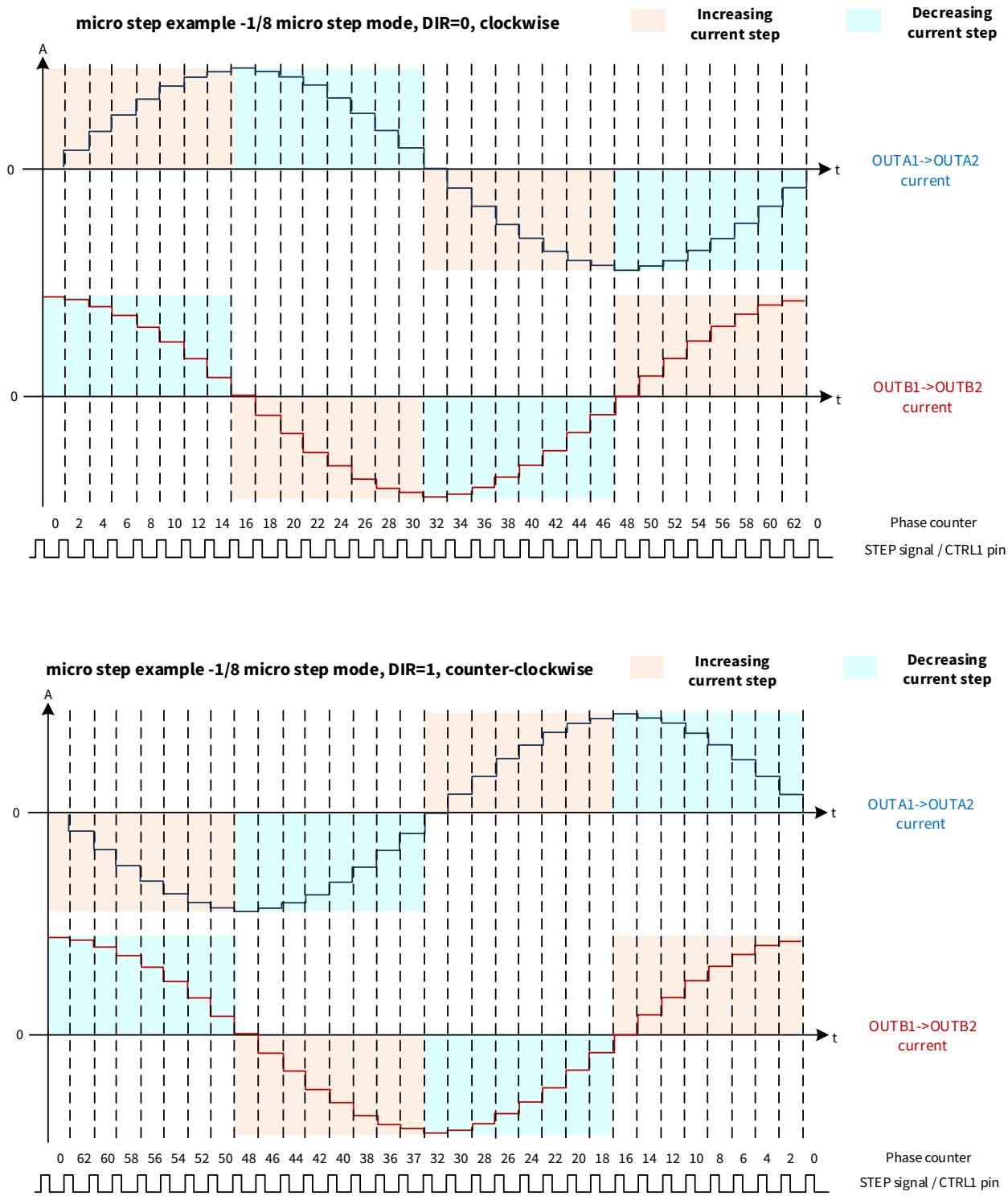


Figure 6-5. Step update example

Step operation is done by updating internal phase counter values. Two methods can be used in application to make motor step spin.

- Update the phase counter by CTRL1 pin pulse signal input, together with DIR direction control
- Directly update phase counter via SPI write ***PH[5:0]*** in ***CONFIG_3*** or ***APH[6:0]*** in ***CONFIG_7*** (if CONFIG_8, 1/32_STEP_EN bit =1) .

Note:

- CTRL1 pin pulse is recognized at rising edge with internal filter, thus min 2us high in CTRL1 pulse is suggested.
- CTRL1/CTRL2/CTRL3/CTRL4 pin function, phase counter, DIR control… etc. these settings are described in Table 6-1. CTRL1/2/3/4 function summary and Table 6-23. CONFIG_1 register description.
- Phase counter updating refers Table 6-5. Step translator of micro step modes and Table 6-6. Full step with 100% full scale current.

6.8.4.PWM current regulation

To regulate the coil current in specific level of each step, an internal current control loop is implemented. Several blocks (current monitor/ comparator / DAC / PWM clock and control logic) are including.

The current monitor of each low-side sources a current image which has a fixed ratio of the instantaneous coil current. These current images are compared with the DAC-controlled current limit in current regulation loop. This loop comparator generates the control signal which turns on or turn off the output H-bridge stage. Therefore, two phases (PWM ON and PWM OFF) of current regulation are established.

During PWM ON phase, the H-bridge output periodically switching on points are synchronized to internal PWM clock. After H-bridge turning on, the current monitor output is ignored for a programmable period (t_{BLANK}). The blanking time also sets the minimum driving ON time of PWM. The value of t_{BLANK} is related on output slew rate selection (***SR_SEL[1:0]*** bits in ***CONFIG_4*** register), and can be extended (***TBLANK_EXT*** bit in ***CONFIG_4*** register) or reduced (***TBLANK_RED*** bit in ***CONFIG_8*** register). After the blanking time, when the coil current reaches the limit, the internal regulation loop automatically moves the H-Bridge output into PWM OFF phase.

The frequency of internal PWM clock determines the H-bridge switching on timing interval, it can be select among 20khz(default), 30khz, and 40khz, through ***PWM_FREQ_SEL[1:0]*** bits in **CONFIG_4** register. High frequency means short period and helps to reduce the overall current ripple amplitude. Additional, to further reduce the PWM emission, the spread spectrum function can be enabled by ***PWM_SS*** bit in ***CONFIG_1*** register.

The current regulation loop comparator output signal is used to detect open load condition also.

6.8.5.Decay modes

During PWM ON phase, once the current limit is reached over t_{FT}, the H-bridge switch to PWM OFF state and begins current decay. It can operate in two different states, slow decay or mixed decay. If the slow decay mode is used, both low side FETs will be turn on to reduce coil current until next PWM cycle. Mixed decay is a working mode which combines fast decay and slow decay, as it runs, the H-bridge first turns on the opposite HS and LS to reduce the current in fast decay; as the load current drop and cross the limit for t_{FT}, then the bridge output stage is changed to slow decay to avoid large current ripple. Figure 6-6 shows the above two working phases.

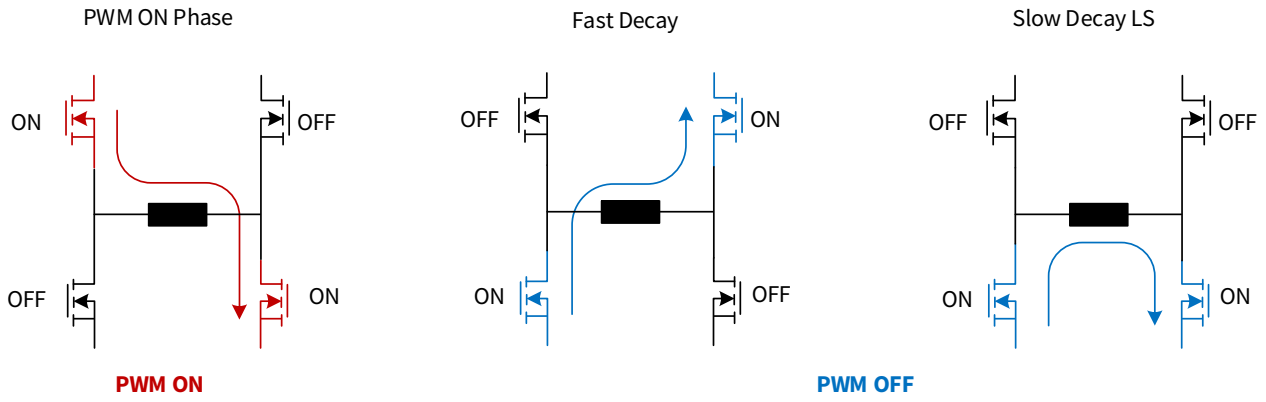


Figure 6-6. PWM ON and OFF phase

Furthermore, to provide the low current ripple of entire steps, the difference of increasing current steps and decreasing current steps has to be considered. So the device provides four decay selection (***DECAY_SEL[1:0]*** bits in ***CONFIG_4*** register) to cover the scenario, especially the auto decay 1 and auto decay 2. Table 6-7 lists the decay mode details of increasing and decreasing current step.

Table 6-7. Decay modes selection

***CONFIG_4* register *DECAY_SEL1:0]* setting**	**Increasing current steps**	**Decreasing current steps**
2b'00' auto decay 1 (default)	Slow decay	Mixed decay
2b'01' slow decay always	Slow decay	Slow decay
2b'10' mixed decay always	Mixed decay	Mixed decay
2b'11' auto decay 2	Slow decay	Slow/mixed decay combination

Note:

- Slow decay features the smallest current ripple of the decay modes. However, during decreasing current steps of slow decay, the current decreases very slowly and takes longer time to settle to the new current step. So slow decay may not properly regulate current where some cases (low coil current, but long t_{BLANK} or t_{FT} timing), this may cause a loss of current regulation, and a more aggressive decay mode (mixed decay or auto decay) is recommended.
- Mixed decay begins as fast decay for a time, followed by slow decay for the remainder. In mixed decay always mode, mixed decay occurs for both increasing and decreasing current steps. The current ripple of this mode is larger than slow decay. On decreasing current steps, mixed decay settles to the new current step faster than slow decay. In cases motor at very low stepping speeds, or low coil current, mixed decay mode allows the current level to stay in regulation.
- Auto decay1 and auto decay 2, which combine the advantage of low current ripple in slow decay and fast response in mixed decay for both increasing current steps and decreasing current steps.
- The difference between auto decay 1 and auto decay 2 is the decay mode used, when the target current limit is reached at decreasing current steps. Unlike mixed decay mode used in auto decay1 for decreasing current step, auto decay 2 first use mixed decay to fast reach new current limit, then switch to slow decay to minimize current ripple.

- All four decay modes can be selected for micro step modes (from half step, 1/4 mini step, …, to 1/32 micro step), while only two modes, slow decay always or mixed decay always, work in full step mode.

6.8.6.Full scale current - Run mode and Hold mode

The driver has two stepper modes, RUN mode and HOLD mode.

RUN mode is the major used mode to drive stepper motor, the coil current changes along with the step updating (CTRL1 pin PWM input or phase counter value update by SPI).

In HOLD mode, two options are provided by ***HOLDM_CONFIG*** bit in ***CONFIG_8*** register.

- If HOLDM_CONFIG bit = '0' (default), STEP pulse or phase counter is still active even under HOLD mode, thus it provides a lower amplitude full scale current working mode comparing with RUN mode. Some stepper motor full scale current is lower than RUN mode full scale current setting minimum value, this mode can work and drive.
- If HOLDM_CONFIG bit = '1', STEP pulse is ignored and phase counter is hold during HOLD mode, thus the motor is HOLD in place using a relatively low coil current.

Three methods allow device shift from RUN mode to HOLD mode.

- Set ***CONFIG_3*** register ***HOLD_EN*** bit = '1' to enter HOLD mode and ***HOLD_EN*** bit =0 to exit HOLD mode, if CTRL3_SEL bit NOT configured as HOLD function enable & HB_MODE bit function not active.
- Set CTRL3 pin in high status to enter HOLD mode, while CTRL3 pin in low to exit HOLD mode, if CTRL3_SEL bit configure as HOLD function enable & HB_MODE bit function not active
- If the coil voltage measurement function is enabled (***CONFIG_5*** register ***CV_EN*** bit), in the meantime, the sampled coil voltage is out of the range [CVLLA, CVUL] for the consecutive conversion number over ***CONFIG_5*** register ***CV_STALL_NUM[2:0]*** bits setting and ***CONFIG_5*** register ***STALL_HOLD_EN*** bit is also set, then the ***STALL*** flag in ***STA_1*** register is asserted and the ***HOLD_EN*** bit is also automatically asserted to enter HOLD mode. In this condition, STALL_HOLD_EN bit setting must be cleared before HOLD_EN bit can be configured or reset to 0.

Note:

- If ***CONFIG_5*** register ***STALL_HOLD_EN*** bit is set, even CTRL3 pin is configuration as HOLD function and CTRL3 is low, but coil voltage measurement and ***STALL*** bit still can trigger ***HOLD_EN*** bit automatically enable.
- The HOLD mode caused by STALL condition will freeze phase counter and ignore step input, no matter ***HOLDM_CONFIG*** bit setting.

The current regulation decay mode used in HOLD is determined by ***DECAY_SEL_HOLD*** bit in ***CONFIG_4*** register. Only slow decay and mixed decay can be selected, not same as RUN mode decay configured by ***DECAY_SEL[1:0]*** bits in ***CONFIG_4***.

The full scale current of each mode can be set by SPI (***CONFIG_6*** register, ***IFSR[3:0]*** and ***IFSH[3:0]*** bits).

The full-scale current for each register value is shown as Table 6-8 .

Table 6-8. Full scale current setting in RUN mode & HOLD mode

CONFIG_6 register *IFSR[3:0]* setting	RUN mode, full scale current (mA)	*CONFIG_6* register *IFSH[3:0]* setting	HOLD mode, full scale current (mA)
'0000'	176	'0000'	28
'0001'	198	'0001'	50
'0010'	220	'0010'	62
'0011'	302	'0011'	73
'0100'	323	'0100'	79
'0101'	329	'0101'	84
'0110'	375	'0110'	95
'0111'	396	'0111'	101
'1000'	465	'1000'	118
'1001'	571	'1001'	140
'1010'	679	'1010'	168
'1011'	812	'1011'	202
'1100'	920	'1100'	230
'1101'	1051	'1101'	264
'1110'	1160	'1110'	292
'1111'	1350	'1111'	326

6.8.7. Stepper operation electrical specifications

T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal current regulation						
F_{PWM}	Current regulation PWM frequency	PWM_FREQ_SEL[1:0] = '00' & PWM_SS bit ='0'		20		kHz
		PWM_FREQ_SEL[1:0] = '01' & PWM_SS bit = '0'		30		kHz
		PWM_FREQ_SEL[1:0] = '10' or '11' & PWM_SS bit = '0'		40		kHz
		PWM_SS bit = '1'		F_{PWM} +/- 2.5%		

t_{BLANK} (1)	Current regulation blanking time	SR_SEL[1:0] = '00' & TBLANK_EXT bit = '0' & TBLANK_RED bit = '0'		4		μs
		SR_SEL[1:0] = '01' & TBLANK_EXT bit = '0' & TBLANK_RED bit = '0'		1.8		μs
		SR_SEL[1:0] = '10' & TBLANK_EXT bit = '0' & TBLANK_RED bit = '0'		1.2		μs
		SR_SEL[1:0] = '11' & TBLANK_EXT bit = '0' & TBLANK_RED bit = '0'		1		μs
		TBLANK_EXT bit = '1' & TBLANK_RED bit = '0', no matter SR_SEL[1:0] setting		4		μs
		TBLANK_RED bit = '1', no matter SR_SEL[1:0] and TBLANK_EXT setting		0.5		μs
t_{FT} (1)	Current regulation filter timing	TFILT_SEL[1:0] = '00' & TFILT_TOC_EXT bit = '0'		0.5		μs
		TFILT_SEL[1:0] = '00' & TFILT_TOC_EXT bit = '1'		0.7		μs
		TFILT_SEL[1:0] = '01' & TFILT_TOC_EXT bit = '0'		1		μs
		TFILT_SEL[1:0] = '01' & TFILT_TOC_EXT bit = '1'		1.2		μs
		TFILT_SEL[1:0] = '10' & TFILT_TOC_EXT bit = '0'		2		μs
		TFILT_SEL[1:0] = '10' & TFILT_TOC_EXT bit = '1'		2.2		μs
		TFILT_SEL[1:0] = '11' & TFILT_TOC_EXT bit = '0'		3		μs
		TFILT_SEL[1:0] = '11' & TFILT_TOC_EXT bit = '1'		3.2		μs

(1) Guaranteed by digital scan

6.9. Half bridge mode

When ***CONFIG_8*** register ***HB_MODE*** bit is set, the device is latched into half bridge mode. This mode allows four half bridge drivers, OUTA1/OUTA2 & OUTB1/OUTB2, can be directly control for Brush DC motor loads.

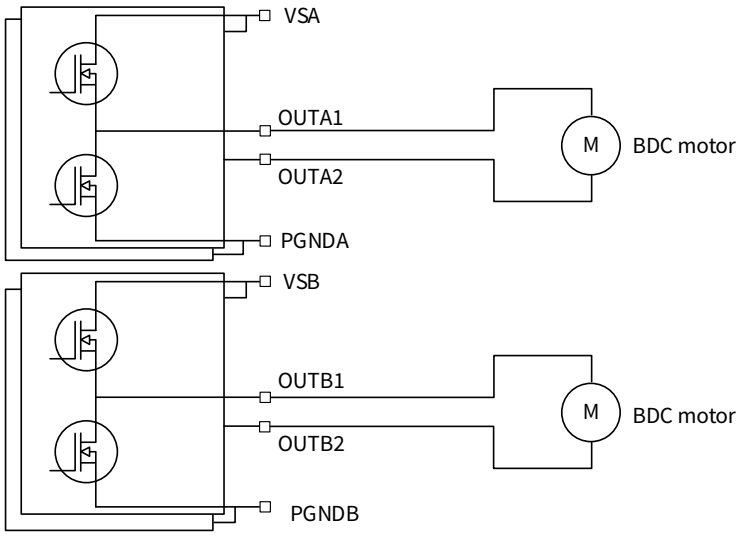


Figure 6-7. BDC motor driving using NSD8381

The CTRL1/2/3/4 & OUTA1/OUTA2/OUTB1/OUTB2 relationship is defined as section CTRL1/2/3/4 function description. And the truth table for half bridge mode is shown as table 6-9.

In half bridge mode, over current protection is still available, but internal current regulation is disabled.

CONFIG_8 register ***HB_MODE*** bit shall be cleared to exit half bridge control.

Table 6-9. Half bridge mode control table

EN pin	*DRV_EN* bit in *CONFIG_3*	*OUTxx_HIZ* bit in *CONFIG_7*	CTRLx pin	OUTx	Description
LOW	x	x	x	HIZ	Sleep, half bridge output HIZ
HIGH	‘0’	x	X	HIZ	Half bridge output not enable, HIZ
HIGH	‘1’	‘1’	x	HIZ	Half bridge output not enable, HIZ
HIGH	‘1’	‘0’	LOW	LOW	Output low side on, high side off
HIGH	‘1’	‘0’	HIGH	HIGH	Output low side off, high side on

Note:

- Half bridge mode application and corresponding connection diagram shall be fully evaluated, taking in account that OUTA1/OUTA2/OUTB1/OUTB2 pin voltage affect the leakage current in system sleep state. In general, for system with low current consumption (ie. <100uA or less) in sleep state, it is NOT suggested to connect OUTx pin to permanent battery supply of system via loads or other equivalent circuit

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6.10. output stage, OUTA1/OUTA2, OUTB1/OUTB2

Each half bridge output stage is built by an internally connected high side and a low-side FET. Due to the integrated body diodes of the HS/LS output stage, inductive loads can be directly driven without external freewheeling diodes. To reduce the power dissipation during decay condition, the internal PWM controller will switch-on the output low side as synchronous rectification.

The half bridges are cross-current protected by an internal delay timing t_{CC} which depends on slew rate configuration (***SR_SEL[1:0]*** bits in ***CONFIG_4*** register)

6.10.1. Output stage electrical specifications

T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output (OUTA1, OUTA2, OUTB1, OUTB2)						
$R_{DS(ON)}$	HS/LS FET on resistance	I = 0.5 A, Tj=25°C, NSD8381-Q1QAIR		0.7		Ω
		I = 0.5 A, Tj=25°C, NSD8381-Q1QANR		0.6		Ω
		I = 0.5 A, Tj=150°C, NSD8381-Q1QAIR			1.4	Ω
		I = 0.5 A, Tj=150°C, NSD8381-Q1QANR			1.2	Ω
I_{LEAK_HS}	HS OFF-state leakage	VS = 13.5 V, VOUT = 0V, EN=1	-50	-6	-	uA
		VS = 13.5 V, VOUT = 0V, EN=0	-50	-4	-	uA
I_{LEAK_LS}	LS OFF-state leakage	VS = 13.5 V, VOUT = 13.5V, EN=1	-	30	100	uA
		VS = 13.5 V, VOUT = 13.5V, EN=0	-	30	100	uA
t_{RISE}, t_{FALL},	Output rise time Output fall time High side or low side	VS = 13.5 V, SR_SEL[1:0]= ‘00’ resistive load 100 ohm,		10		V/µs
		VS = 13.5 V, SR_SEL[1:0]= ‘01’ resistive load 100 ohm,		40		V/µs
		VS = 13.5 V, SR_SEL[1:0]= ‘10’ resistive load 100 ohm,		70		V/µs
		VS = 13.5 V, SR_SEL[1:0]= ‘11’ resistive load 100 ohm,		100		V/µs
t_{PDLH}	Propagation delay (half bridge output low to high)	VS = 13.5 V, SR_SEL[1:0]= ‘00’ resistive load 100 ohm to GND		4		µs
		VS = 13.5 V, SR_SEL[1:0]= ‘01’ resistive load 100 ohm to GND		2.1		µs
		VS = 13.5 V, SR_SEL[1:0]= ‘10’ resistive load 100 ohm to GND		1.6		µs
		VS = 13.5 V, SR_SEL[1:0]= ‘11’ resistive load 100 ohm to GND		1.4		µs

t_{PDHL}	Propagation delay (half bridge output high to low)	VS = 13.5 V, SR_SEL[1:0]= '00' resistive load 100 ohm to GND		1.3		µs
		VS = 13.5 V, SR_SEL[1:0]= '01' resistive load 100 ohm to GND		0.8		µs
		VS = 13.5 V, SR_SEL[1:0]= '10' resistive load 100 ohm to GND		0.7		µs
		VS = 13.5 V, SR_SEL[1:0]= '11' resistive load 100 ohm to GND		0.6		µs
t_{CC}	Cross protection time, high to low / low to high. Test by digital scan	VS = 13.5 V, SR_SEL[1:0]= '00' resistive load 100 ohm,		4.8		µs
		VS = 13.5 V, SR_SEL[1:0]= '01' resistive load 100 ohm,		1.8		µs
		VS = 13.5 V, SR_SEL[1:0]= '10' resistive load 100 ohm,		1.2		µs
		VS = 13.5 V, SR_SEL[1:0]= '11' resistive load 100 ohm,		0.9		µs

6.11. Protection and diagnosis function

6.11.1. Overcurrent protection

The integrated overcurrent protection function provides the half bridge high side against short to ground or half bridge low side against short to battery.

The coil current passes the half bridge high side (VS -> highside -> OUTx) or flow into the half bridge low side (OUTx -> low side -> GND), once I_{OC} overcurrent threshold is exceeded, an overcurrent deglitch filter t_{OC} starts and internal overcurrent circuit also limits the short circuit current.

Upon the overcurrent condition last until t_{OC} expiration, overcurrent protection is triggered. Thus, the particular half bridge (including high side and low side) is disabled for half bridge mode, while device is under stepper mode, all four half bridge outputs are disabled on the same time for OC. No matter stepper or half bridge, the OC status bit shall report the corresponding HS or LS which trigger OC, see ***STA_1*** & ***STA_2*** register description. DOUT2 pin also asserts high if FAULT function is selected.

For example, if only OUTA1 LS is short to battery and detected, then ***STA_2*** register ***OC_OUTA1_LS*** bit and ***STA_1*** register ***OC*** bit is asserted, OC status bit ***OC_OUTA1_HS*** or other corresponding OUTA2/OUTB1/OUTB2 bits are not impacted, in the meantime, only OUTA1 half bridge, HS and LS, are disabled in half bridge mode while in stepper mode all OUTA1/A2/B1/B2 are disabled under this scenario.

Under overcurrent protection state, the output stage is latched off, to resume normal driving, besides the overcurrent condition disappear, it is also required to clear the ***OC*** status bit in ***STA1*** & ***STA2*** register by sending READ&CLEAR command.

Note:

- Even the half bridge output is disabled due to overcurrent protection mechanism, the ***DRV_EN*** bit in ***CONFIG_3*** register remains previous state, unless its value changed by SPI.
- Charge pump remains active during overcurrent protection.

- When device operate in high VS voltage > 28v, short t_{OC} is automatically used, even ***TOC_SEL*** bit in ***CONFIG_8*** register is set to select long filter.

Anyhow if overcurrent condition short than t_{OC} deglitch filter, the OC event is not confirmed, and Half bridge / stepper outputs keep normal status.

6.11.1.1. Overcurrent protection electrical specifications

T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overcurrent protection						
I_{OC}	Over current threshold	Half bridge low side	1.9	2.9	3.7	A
		Half bridge high side	-3.7	-2.7	-1.9	A
t_{OC}	OC deglitch filter time(1)	TOC_SEL bit = '0', TFLT_TOC_EXT bit = '0'		0.2		us
		TOC_SEL bit = '0', TFLT_TOC_EXT bit = '1'		0.4		
		TOC_SEL bit = '1', TFLT_TOC_EXT bit = '0'		3.2		
		TOC_SEL bit = '1', TFLT_TOC_EXT bit = '1'		6.4		

(1) Guaranteed by digital scan

6.11.2. Over temperature warning and shut down

To protect power stage from overheat, dedicated thermal sensor is placed close to half bridge power stage, if the temperature increases above the OT_{WARN}, a temperature warning flag (***OTWARN***) is set in SPI ***STA_1*** register, stepper / half bridge output operation is not impacted. Once the sensed temperature over the second higher OT_{SD} threshold, the corresponding ***OTSD*** flag is set and power FET channel is automatically disabled.

DOUT2 pin can be configured for OTWARN and OTSD event report, which asserted DOUT2 (configured as FAULT) to high.

If ***FLT_LATCH*** = '1', in order to reactive the output stage after OTSD and release DOUT2 pin, the temperature drops below OT_{SD}-T_{HYS_OTSD}, and the thermal shutdown ***OTSD*** bit is cleared by SPI READ&CLEAR command. In a similar way, the ***OTWARN*** flag is latched until temperature drops below OT_{WARN}-T_{HYS_OTW} and SPI READ&CLEAR command.

If ***FLT_LATCH*** = '0' (default), when the temperature drops below OT_{SD}-T_{HYS_OTSD}, the output stage is automatically recovery, while the thermal shutdown ***OTSD*** bit is latched until SPI READ&CLEAR command. For ***OTWARN*** flag, it is automatically cleared once temperature drops below OT_{WARN}-T_{HYS_OTW}.

6.11.2.1. Thermal protection electrical characteristics

T_j = -40~150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Thermal protection						
OT_{WARN}	Thermal warning temperature (1)		130	145	160	°C
T_{HYS_OTW}	Thermal warning hysteresis			20		°C
OT_{SD}	Thermal shutdown temperature (1)		155	170	185	°C
T_{HYS_OTSD}	Thermal shutdown hysteresis			20		°C

(1) OT_{WARN}, OT_{SD} threshold is not overlap.

6.11.3. Under temperature warning

If the device internal temperature falls below the under-temperature warning threshold, the ***UTWARN*** flag is set in SPI register ***CONFIG_7***. No other action is performed, and device operation is NOT impacted. When the temperature rises and exceeds the UTwarn + T_{HYS_UTW}, the UTW flag is automatically cleared.

UTW flag is not reported on ***STA_1*** register, neither on DOUT2 pin.

6.11.3.1. Under temperature warning electrical specifications

T_j = -40~150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Under temperature protection						
UT_{WARN}	Under temperature warning temperature		-30	-16	0	°C
T_{HYS_UTW}	Under temperature warning hysteresis			10		°C

6.11.4. Open load in ON state

The load current is monitored in each activated output stage for open load detection in ON state under stepper mode.

Starting from any PWM current regulation cycle, if the coil current is NOT reaching the current limit for at least t_{OL} for consecutive PWM cycles, the corresponding open load bit is set in status register (***OPL_OUTA*** or ***OPL_OUTB*** bit in STA2 register, ***OPL*** bit in ***STA1*** register). The OL status bits (***STA2*** & ***STA1*** corresponding bits) are latched until SPI READ&CLEAR command when open load condition is disappeared.

The open load is only as information flag and stepper operation not impacted. DOUT2 (FAULT output function if selected) is also asserted high once open load detected, as ***WARN*** bit in global status byte contains open load.

Note:

- For stepper application, the open load detection is not asserted in below condition
  i. Output driver disabled (DRV_EN not able, TSD, OCP, CPUV, VSUV, VSOV if VSOV_DIS=0).

ii. When the stepper motor position is 0°/ 180° (stop open load detection only in OUTA side, as OUTA coil current equals 0 in 0°/ 180°), 90°/ 270° (stop open load detection only in OUTB side, as OUTB coil current equals 0 in 90°/ 270°)

- ON state open load detection filter timing t_{OL} can be programmable (***OPL_FLT*** bit in ***CONFIG_4*** register)
- ON state open load detection can be disabled by ***OPL_DIS*** bit in ***CONFIG_8*** register, in case ON state open load not required.
- Due to ON state open load diagnosis is based on current regulation function, thus it is only available under stepper mode, not works in half bridge control.

6.11.4.1. open load electrical characteristics

T_j = -40~150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ON state open load protection						
t_{OL}	Open load filter time (1)	OPL_FLT bit = '0'	15	30	45	ms
		OPL_FLT bit = '1'	30	60	90	ms

(1) Guaranteed by digital scan

6.11.5. Stall detection in stepper mode

As figure 6-8 & 6-9 shown, there is a clear relation between the coil current and stepper motor BEMF. When the motor load increases, the BEMF shifts and cause voltage difference at coil current equals 0. The NSD8381 takes advantage of this phenomenon. When the stepper motor position is 0°/ 180 °/ 90°/ 270 °, one coil current is typically programmed at zero amps, this makes it possible to measure the induced BEMF voltage through sampling the voltage across the motor terminal.

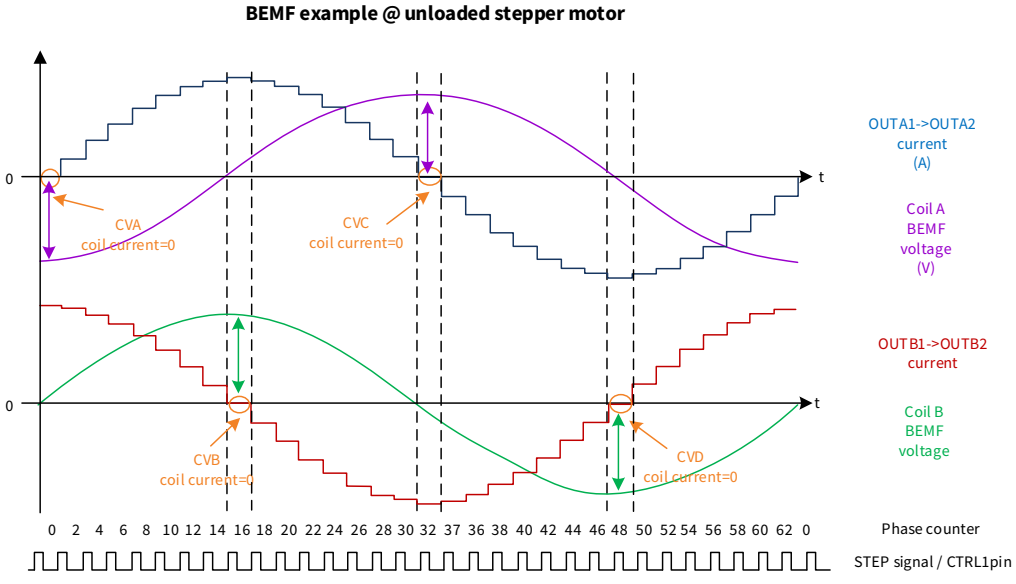


Figure 6-8. BEMF example in unloaded stepper motor

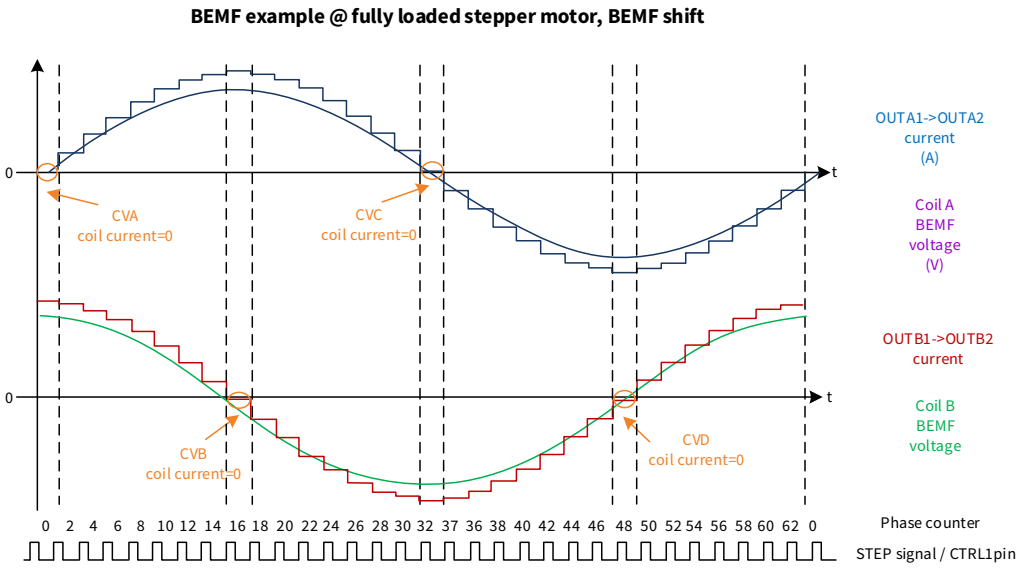


Figure 6-9. BEMF example in fully loaded stepper motor

As soon as the zero current step (0°/ 180 °/ 90°/ 270 °) starts, the half bridge PWM driving signals are switched off. If coil voltage conversion is enabled by SPI ***CONFIG_5*** register ***CV_EN*** bit, after the cross current protection timing, the opposite low side is switched on to measure the motor terminal voltage difference refer to GND. The four corresponding digital values are stored into SPI register CVA, CVB, CVC, CVD, as Table 6-10 explained.

Table 6-10. BEMF voltage conversion operation table

Step position	PHASE COUNTER APH[6:0]	PHASE COUNTER PH[5:0]	DIR=0		DIR=1		SPI store register
			Switch on low side	Sampling	Switch on low side	Sampling	
0°	0000000	000000	OUTA2	OUTA1	OUTA1	OUTA2	CVA
90°	0100000	010000	OUTB1	OUTB2	OUTB2	OUTB1	CVB
180°	1000000	100000	OUTA1	OUTA2	OUTA2	OUTA1	CVC
270°	1100000	110000	OUTB2	OUTB1	OUTB1	OUTB2	CVD

The full scale BEMF measurement is range from min 150mV to max 28v, and the converted BEMF (CVA,CVB,CVC,CVD) is defined as below formula:

$$V_{BEMF} = \frac{\text{CVA or CVB or CVC or CVD, 10bit register decimal value}}{1023} \times 28V$$

6.11.5.1. BEMF voltage measurement sample point

Motor related operating condition, like motor speed & load torque, has effect on BEMF voltage and timing. The key of right detecting the stall condition is to sample the BEMF at the proper point.

CONFIG_5 register ***CV_DELAY[4:0]*** bits allow user to adjust the BEMF sample point by the number of PWM periods after zero current step starts.

Default setting of ***CV_DELAY[4:0]*** is '00000', it is defined as sampling the BEMF at the end of zero current step. This is useful for detection at continuous movement in fast speeds. To detect the stall condition at low speed, the sample point shall be close to the beginning of zero current step, in hence, ***CV_DELAY[4:0]*** setting value shall be not too high.

In case the phase counter update command is given before the ***CV_DELAY[4:0]*** PWM periods expired, the zero current step is extended and next step movement is delayed, until coil voltage conversion ready.

6.11.5.2. BEMF voltage measurement averaging

The ***CV_AVG_SEL*** bit in ***CONFIG_8*** register determines whether the average of 8~16 times conversion or the real time ADC data is updated to the corresponding CVx register.

6.11.5.3. BEMF voltage measurement indicator CV_RDY signal / CV_REG_IND[1:0] bits

CV_REG_IND[1:0] bits in ***CONFIG_5*** register always report the last updated CVx register where the new conversion value stored.

Additionally, the device provides digital signal 'CV_RDY' output which indicates the coil voltage (BEMF) measurement is ready and available the respective CVx register. When the new conversion triggers, the CV_RDY signal goes from high to low, then it returns to high once the voltage measurement is updated.

CV_RDY signal can be mux on DOUT1 pin, when ***DOUT1_SEL[1:0]*** in ***CONFIG_2*** register is configured as CV_RDY output.

6.11.5.4. BEMF voltage measurement comparison and stall detection

Three different thresholds related to stall detection can be configured by SPI registers.

- ***CVUL*** (coil BEMF voltage upper limit)
- ***CVLLB*** (coil BEMF voltage low limit B)
- ***CVLLA*** (coil BEMF voltage low limit A) -> recommend for the lowest threshold

Depending on the comparison result between coil BEMF voltage measurement value and the three thresholds, the device asserts and reports the corresponding flag bit.

- ***CVULF*** bit in ***STA_2*** register is set if the coil conversion voltage is higher than CVUL threshold. It is automatically cleared when new value is lower.
- ***CVLLBF*** bit in ***STA_2*** register is set if the coil conversion voltage is lower than CVLLB threshold. It is automatically cleared when new value exceeds CVLLB.
- ***CVLLAF*** bit in ***STA_2*** register is set if the coil conversion voltage is lower than CVLLA threshold. It is automatically cleared when new value exceeds CVLLA.

If the conversion value is out of range [CVLLA; CVUL] for lasting over the number of consecutive conversions in zero current step, which equals the ***CV_STALL_NUM[2:0]*** bits in ***CONFIG_5*** register value, then the ***STALL*** flag bit in ***STA_1*** is set. For example, if the conversion value is quite low and below CVLLA threshold over the stall counter number, the device reports both ***CVLLAF*** and ***STALL*** flag, similar case for conversion value higher than CVUL, ***CVULF*** and ***STALL*** flag is set.

Both ***CVULF*** / ***CVLLBF*** / ***CVLLAF*** and ***STALL*** flag NOT impact device operating state.

Additionally, two digital signals related with BEMF measurement comparison, CVLL and CVOOR, can be mux on DOUT1 pin. CVOOR signals is set to high if BEMF conversion value out of range, and then return back to low once BEMF conversion value is within the two setting thresholds [CVLLA; CVUL]. In a similar way, CVLL signal is set if BEMF conversion value is below CVLLB threshold.

6.11.5.5. BEMF voltage conversion electrical specification

T_j = -40~150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BEMF voltage adc conversion						
V_{BEMF_IN}	BEMF voltage adc measurement range				28	V
V_{BEMF_RES}	BEMF voltage adc measurement resolution (LSB)	Design information		27.4		mV
V_{BEMF_ERR}	BEMF voltage adc measurement error			+/- 3		LSB

6.11.6. Fault table summary

FAULT EVENT	Condition	Configuration	ERR indicator	Output status	Charge pump	Digital logic	SPI Comm	Recovery action
VSx UV	VS < VS_UV_L	FLT_LATCH=0	a.VSUV bit in STA_1 b. DOUT2 if fault function is set	OFF	OFF	Normal	Normal	Power stage output, charge pump and internal translator automatically recover when VS>VS_UV_H rising edge. VSUV flag keeps latch until read&clear command is sent.
		FLT_LATCH=1		OFF	OFF	Normal	Normal	VSUV flag keeps latch until read&clear command is sent. Power stage output, charge pump and internal translator recover after both VS>VS_UV_H rising edge and VSUV flag cleared are met
VSx POR	VS < VS_RST_L	NA	RSTB =1 in GSB byte of SDO frame	OFF	OFF	RESET	OFF	NA
VSx OV	VS > VS_OV_H	OVP_DIS=0 & FLT_LATCH=0	a.VSOV in STA_1 b. DOUT2 if fault function is set	OFF	OFF	Normal	Normal	Power stage output and charge pump automatically recover when VS < VS_OV_L. VSOV flag keeps latch until read&clear command is sent
		OVP_DIS=0 & FLT_LATCH=1		OFF	OFF	Normal	Normal	VSOV flag keeps latch until read&clear or read command if RD_CLR_EN=1. Power stage output and charge pump also keeps latch until VS < VS_OV_L and VSOV flags clear by read&clear command
		OVP_DIS=1, FLT_LATCH= x	NA (not report)	Normal	Normal	Normal	Normal	NA
VDDIO POR	VDDIO < $V_{VDDIO\_RST\_L}$	NA	RSTB =1 in GSB byte of SDO frame	OFF	OFF	RESET	OFF	NA
CP UV	$V_{CP} < V_{CP\_UV}$	FLT_LATCH=0	a. CPUV bit in STA_1 b. DOUT2 if fault function is set	OFF	Normal	Normal	Normal	Output stage automatically recovery if $V_{CP} > V_{CP\_UV}$ with t_{CP_UV}. CPUV flag keeps latch until read&clear command is sent
		FLT_LATCH=1		OFF	Normal	Normal	Normal	CPUV flag keep latch until read&clear command is sent, and also output stage remains latch until CPUV flag clear and $V_{CP}>V_{CP\_UV}$ with t_{CP_UV}
OCP(1)	IOUT > I_{OC}	NA	a. OC bit in STA_1 b. OCP_OUTA1_HS or OCP_OUTA1_LS or OCP_OUTA2_HS or OCP_OUTA2_LS or OCP_OUTB1_HS or OCP_OUTB1_LS or OCP_OUTB2_HS or OCP_OUTB2_LS bits in STA_2 b. DOUT2 if fault function is set	HIZ	Normal	Normal	Normal	OC flags, output stages off are latched until read&clear command is sent and OC condition removed.

OPEN LOAD (ON MODE)(2)	Load open / not connected	NA	a. OPL bit in STA_1 b. OPL_OUTA or OPL_OUTB bits in STA_2 b. DOUT2 if fault function is set	Normal	Normal	Normal	Normal	NA
STALL(2)	Motor stuck	NA	a. STALL bit in STA_1 b. CVLLA or CVUL bits in STA_2 b. DOUT2 if fault function is set	Normal	Normal	Normal	Normal	STALL flag can be cleared by read&clear command, after BEMF voltage conversion value is within [CVLLA, CVUL] range.
OTSD	Tj > OT_{SD}	FLT_LATCH=0	a. OTSD bit in STA_1 b. DOUT2 if fault function is set	OFF	OFF	Normal	Normal	Automatically recovery of output and charge pump after Tj < OT_{SD} - T_{HYS_OTSD} . OTSD flag keep latch until read&clear command is sent
		FLT_LATCH=1		OFF	OFF	Normal	Normal	OTSD flag, output stage off and charge pump off are latched until read&clear command is sent after Tj < OT_{SD} - T_{HYS_OTSD}
OTWARN	Tj > OT_{WARN}	FLT_LATCH=0	a. OTWARN bit in STA_1 b. DOUT2 if fault function is set	Normal	Normal	Normal	Normal	Automatically clear of OTWARN bit when Tj < OT_{WARN} - T_{HYS_OTW}
		FLT_LATCH=1		Normal	Normal	Normal	Normal	OTWARN flag are latched until read&clear command is sent, when Tj < OT_{WARN} - T_{HYS_OTW}
UTWARN	Tj < UT_{WARN}	NA	a. UTWARN bit in CONFIG_7	Normal	Normal	Normal	Normal	Automatically clear of UTWARN bit Tj > UT_{WARN} + T_{HYS_UTW}

Note:

1. After OC triggered, the particular half bridge (including high side and low side) is disabled for half bridge mode, while device is under stepper mode, all four half bridge outputs are disabled on the same time for OC.
2. OPEN LOAD and stall detection are NOT available in half bridge mode.

6.12. SPI interface

The following table summarizes the SPI interface designed.

Table 6-11. SPI Interface quick look

Parameter	Description
Protocol	in frame
Single Frame Length	24 bit, MSB first
Frame protection	frame length & odd parity check & SDI stuck & CPOL check
Max. Frequency	4 MHz
CPOL	0
CPHA	0
Master/Slave configuration	Slave

The falling edge of NCS defines the start of the SPI frames. It samples the SDI line at the rising edge of SCK, while the output data is shifted out on SDO line at the falling edge of SCK (CPOL='0' CPHA = '0'). The end of SPI frame is defined by a rising edge of NCS.

6.12.1. SPI Frame structure

Each SDI input frame has 24 bits with the following structure:

- 2-bit operation code C1 / C0
  - '00' for write operation,
  - '01' for read operation,
  - '10' for read&clear operation
- 6-bit ADDRESS
- 16-bit DATA, including D15~D1 data + D0 odd parity bit

Table 6-12. SPI SDI frame

	MSB								LSB
BIT	23	22	21	20	19	18	17	16	[15:0]
SDI	C1	C0	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	DATA

Note:

- Bit D0 odd parity bit is calculated based on bit 23~bit 1, not only write operation, but also read operation and read&clear operation all perform SDI frame parity check. Wrong parity SDI frame will be ignored.
- In SPI read operation, SDI frame DATA[15~1] can be any value.
- Read&clear SPI command is combined by '10' operation code + address bit + particular data bit related to status flag required to clear. A given example of read&clear overcurrent OC status flag is SPI send 24-bit frame as '100000010000000000001000' (0x810080), this operation only read&clear OC flag when OC condition is removed.

- To read&clear all status bit in STA_1 register, SPI shall send '10000001111111111111111' (0x81FFFE), similar, '10000010111111111111110' (0x82FFFE) can be used to read & clear all status bit in STA_2 register.

Register frame SDO responses the selected address and register content bit values. It has with the following structure:

- 8-bit GSB (global status byte), represents global status / failure / warning
- 16-bit return data, all D15~D1 data + D0 odd parity bit

Table 6-13. SPI SDO frame

	MSB								LSB
BIT	23	22	21	20	19	18	17	16	[15:0]
SDO	Global status byte								DATA

6.12.2. Global status byte definition

Every bit of global status byte in SDO frame

Table 6-14. Global status byte definition

	Global status byte							
BIT	23	22	21	20	19	18	17	16
SDO	GSBN	RSTB	SPI_ERR	0	Function_ERR	DEVICE_ERR	WARN	0

Table 6-15. Bit description in global status byte

Bit name	Function description
GSBN	The GSBN bit is a logical NOR combination of SDO Global status byte bit 17 to bit 23. GSBN = '1' (No Error), GSBN = '0' (Error)
RSTB	The RSTB bit is set to 1 after any POR (VS POR or VDDIO POR), it is reset after first valid SPI frame
SPI_ERR	The SPI_ERR is a logical OR combination of SPI communication related error: frame length, ODD parity, SDI stuck, CPOL check.
FUNCTION_ERR	The FUNCTION_ERR is a logical OR combination of application specific function flags: • Overcurrent status bit (OC) • Stall detection (STALL)
DEVICE ERR	The DEVICE_ERR is a logical OR combination of device specific block flags: • Overvoltage status bit (VSOV)

	• Undervoltage status bit (VSUV) • Charge pump status bit (CPUV) • Overtemperature shutdown bit (OTSD)
WARN	The WARN is a logical OR combination of warning flags: • Thermal warning (OTWARN) • Open Load (OL)

6.12.3. GSBN flag

Between NCS falling edge and the first SCK rising edge, a logic OR combination between GSBN and the signal present on SDI is reported on SDO.

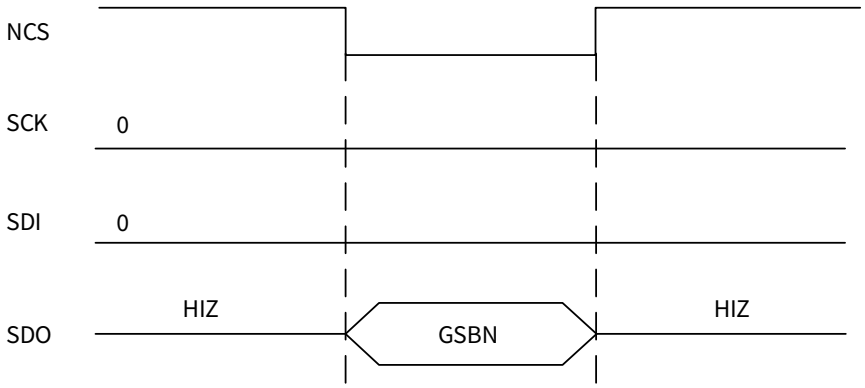


Figure 6-10. GSBN flag in SDO

GSBN is set if a fault condition is detected or if the device comes from a Power On Reset (POR). It is possible to check if the device has detected a fault by reading the GSBN without SCK clock pulse.

6.12.4. Parallel and multi-devices communication

SPI communication between microcontroller (SPI master) and multiple these devices (slave) can be operated only in parallel.

Parallel operation: several slave devices are connected to one SPI channel, which share communication lines SDI, SDO and SCK, but every slave connects dedicated own NCS.

Daisy chain operation: multi devices shared one NCS and SCK and each device SDI and SDO daisy-chain connected are NOT supported.

6.12.5. Frame Length Check

For each command received, the SPI peripheral checks the number of clock edges at SCK pin. If the total number of edges is not 16 plus a multiple of 8, which means 24, 32, 40…, the frame content is discarded and an SPI_ERR bit will be returned upon next iteration.

6.12.6. ODD parity check

An ODD parity is used in NSD8381 for SPI data consistency check. The ODD parity bit is allocated in bit0, LSB, and the value is calculated based on the number of ‘1’ from bit 23 to bit 1. If the count number is even, the LSB odd parity bit value shall be inserted using ‘1’, otherwise, ‘0’ shall be used.

6.12.7. NCS timeout

An internal timer is started when NCS pin is tied down from high to low, the SPI frame shall be within the timer window T_{NCS_TO}, as the SDO is internally set to tristate (HIZ) after the timer ends. It avoids one device abnormal occupancy on SDO, in case NCS is stuck at low of multi devices communication on the same SPI bus.

6.12.8. SDI stuck

When the 24-bit values of one SPI command are all ‘0’, it is considered as SDI stuck at low, all ‘0’ SPI frame is discarded and an SPI_ERR will be returned on next iteration. The mechanism means a SPI write command to register address ’000000’ with all data bit in ’0’ is rejected.

In the similar way, for SDI stuck at high, the frame with 24-bit all ‘1’ is also rejected and SPI_ERR flag is set.

6.12.9. SDO stuck

The GSBN bit is logic NOR of other bits in GSB. It means the normal SDO frame always contains both ‘0’ and ‘1’, therefore, SDO returns all ‘1’ can be recognized as SDO stuck at high and all ‘0’ means SDO stuck at low. This fault detection can be handled by microcontroller.

6.12.10. CPOL check

Providing the first SCK edge is falling after NCS low or last SCK edge is rising before CSN goes high, the NSD8381 detects the input SPI frame CPOL abnormal, ignores the wrong SPI frame and reports SPI_ERR on next SDO frame.

6.12.11. SPI error flag

As the above SPI protection described, the SPI_ERR diagnosis bit in GSB will be returned upon next communication iteration for the following error occurs:

- Frame Length error
- ODD parity
- SDI stuck
- CPOL check

6.12.12. SPI Physical Layer

It implements an SPI Slave with the following timing requirements:

Figure 6-11. SPI Timing Diagram

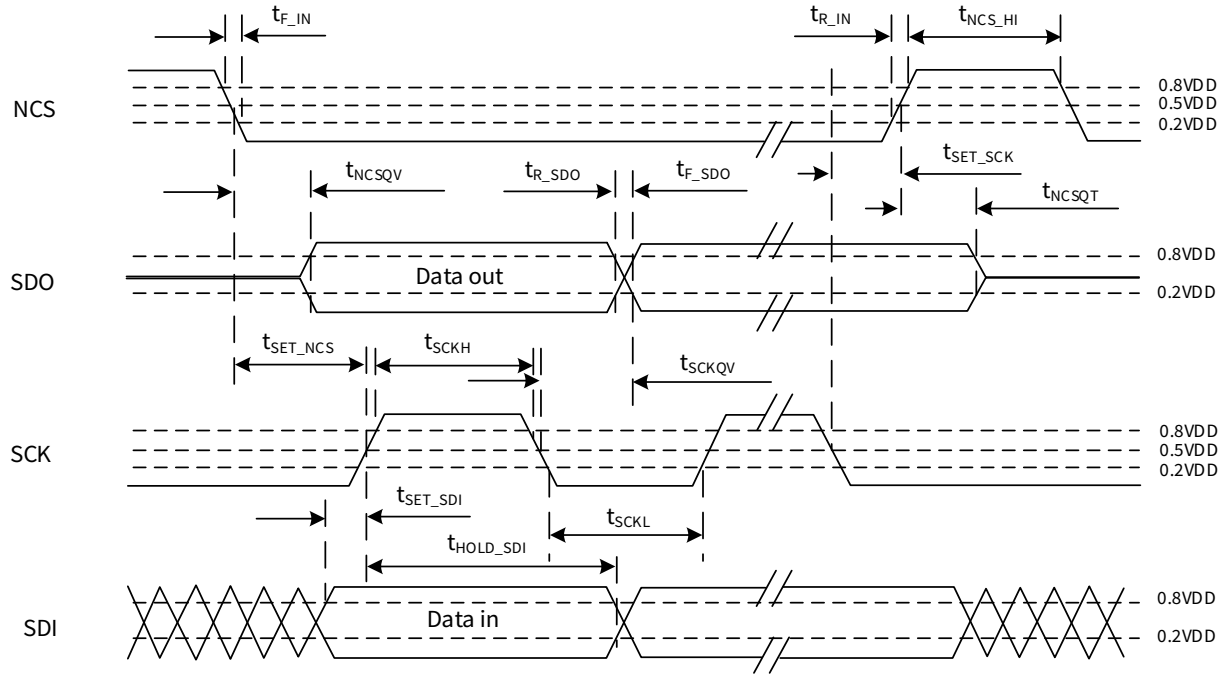


Table 6-16. SPI AC Characteristics

Symbol	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SCKL}	Minimum time CLK = LOW	Application info	100			ns
t_{SCKH}	Minimum time CLK = HIGH	Application info	100			ns
t_{NCSQV}	NCS falling until SDO valid	Cload=50pF			100	ns
t_{SET_NCS}	NCS setup timing before CLK rising	Application info	100			ns
t_{SCKQV}	SCK falling until SDO valid	Cload=50pF			60	ns
t_{SET_SDI}	SDI input setup time (SCK change low to high after SDI data valid)	Application info	25			ns
t_{HOLD_SDI}	SDI input hold time	Application info	25			ns
t_{SET_SCK}	SCK low timing before NCS rising		100			ns
t_{NCSQT}	NCS high timing to SDO tri-state	Cload=50pF			100	ns

t_{F_IN}	SCK, NCS, SDI falling timing	Application info			25	ns
t_{R_IN}	SCK, NCS, SDI rising timing	Application info			25	ns
t_{F_SDO}	SDO falling timing	Cload=50pF			25	ns
t_{R_SDO}	SDO rising timing	Cload=50pF			25	ns
t_{NCS_HI}	NCS high timing between two SPI frame		6			us
t_{NCS_TO}	NCS low time out		20	35	50	ms
F_{SCK_SPI}	SCK frequency (50% duty cycle)	Application info			4	MHz

6.12.13. Registers map

Table 6-17. Registers map table

SECT	REG_NAME	REG_ADDR	Bits															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Status register	STA_1	0x01	VSOV	VSUV	Reserved	Reserved	Reserved	CPUV	Reserved	Reserved	Reserved	OTWARN	OTSD	OPL	OC	STALL	Reserved	Parity
	STA_2	0x02	OC_OUTA1_HS	OC_OUTA1_LS	OC_OUTA2_HS	OC_OUTA2_LS	OC_OUTB1_HS	OC_OUTB1_LS	OC_OUTB2_HS	OC_OUTB2_LS	OPL_OUTA	OPL_OUTB	Reserved	Reserved	CVULF	CVLLAF	CVLLBF	Parity
Control register	CONFIG_1	0x03	CP_SS	PWM_SS	Reserved	AOUT_SEL[1:0]		Reserved	Reserved	Reserved	Reserved	Reserved	CTRL1_SEL	Reserved	CTRL2_SEL	CTRL3_SEL[1:0]		Parity
	CONFIG_2	0x04	Reserved	Reserved	Reserved	Reserved	DOUT1_SEL[1:0]		Reserved	DOUT2_SEL[1:0]		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Parity
	CONFIG_3	0x05	DRV_EN	HOLD_EN	ASM[2:0]			SM[2:0]			DIR	PH[5:0]						Parity
	CONFIG_4	0x06	PWM_FREQ_SEL[1:0]		TFILT_TOC_EXT	TBLANK_EXT	TFILT_SEL[1:0]		SR_SEL[1:0]		DECAY_SEL[1:0]		Reserved	Reserved	OPL_FILT	DECAY_SEL_HOLD	Reserved	Parity
	CONFIG_5	0x07	CV_EN	Reserved	CV_DELAY[4:0]					CV_STALL_NUM[2:0]			CV_REG_IND[1:0]		STALL_HOLD_EN	Reserved	Reserved	Parity
	CONFIG_6	0x08	IFSH[3:0]				Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	IFSR[3:0]				Parity
	CVA	0x09	Reserved	Reserved	Reserved	Reserved	Reserved	CVA[9:0]										Parity
	CVB	0x0A	Reserved	Reserved	Reserved	Reserved	Reserved	CVB[9:0]										Parity
	CVC	0x0B	Reserved	Reserved	Reserved	Reserved	Reserved	CVC[9:0]										Parity
	CVD	0x0C	Reserved	Reserved	Reserved	Reserved	Reserved	CVD[9:0]										Parity
	CVLLB	0x0D	Reserved	Reserved	Reserved	Reserved	Reserved	CVLLB[9:0]										Parity
	CVLLA	0x0E	Reserved	Reserved	Reserved	Reserved	Reserved	CVLLA[9:0]										Parity
	CVUL	0x0F	Reserved	Reserved	Reserved	Reserved	Reserved	CVUL[9:0]										Parity
	CONFIG_7	0x10	OUTA1_HIZ	OUTA2_HIZ	OUTB1_HIZ	OUTB2_HIZ	Version[1:0]		Device_ID	UTWARN	APH[6:0]							Parity
	CONFIG_8	0x11	CP_SS_CONFIG	HOLDM_CONFIG	TOC_SEL	OPL_ON_DIS	CV_AVG_SEL	TCC_INC	TCC_RED	TBLANK_RED	1/32 STEP_EN	DIS_SLOPE_BLANK	FULL_STEP_IFS	Reserved	HB_MODE	FLT_LATCH	OVP_DIS	Parity
	CONFIG_9	0x12	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Unlock	Parity

6.12.14. SPI – status and control registers

Table 6-18. STA_1 status register (REG_ADDR = 0x01)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	VSOV	VSUV	Reserved	Reserved	Reserved	CPUV	Reserved	Reserved
Operation Type	RLR	RLR	RO	RO	RO	RLR	RO	RO
Default	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	Reserved	OTWARN	OTSD	OPL	OC	STALL	Reserved	Parity
Operation Type	RO	RLR	RLR	RLR	RLR	RLR	RO	-
Default	0	0	0	0	0	0	0	-

Table 6-19. STA_1 status register description

Bit	Field Name	Description
15	VSOV	0: No VS overvoltage detected (default value). 1: VS overvoltage detected. Error flag latched.
14	VSUV	0: No VS undervoltage detected (default value). 1: VS undervoltage detected. Error flag latched.
13	Reserved	0: reversed (default value).
12	Reserved	0: reversed (default value).
11	Reserved	0: reversed (default value).
10	CPUV	0: No charge pump undervoltage detected (default value). 1: Charge pump undervoltage detected. Error flag latched.
9	Reserved	0: reversed (default value).
8	Reserved	0: reversed (default value).
7	Reserved	0: reversed (default value).
6	OTWARN	0: No over temperature warning (default value). 1: Over temperature warning detected. Error flag latched if FLT_LATCH= ‘1’, in the contrary, automatically clear if FLT_LATCH = ‘0’.
5	OTSD	0: No over temperature shut down (default value). 1: Over temperature shut down detected. Error flag latched.
4	OPL	0: No open load in OUTA / OUTB detected (default value). 1: Open load detected. Error flag latched.
3	OC	0: No overcurrent in OUTA / OUTB high/low side detected (default value). 1: overcurrent detected in OUTA/OUTB. Error flag latched.
2	STALL	0: No stall detected at OUTA/OUTB running (default value). 1: Stall detected. Error latched.
1	Reserved	0: reversed (default value).
0	Parity	Bit 0 parity bit, ODD parity check. If the number of occurrences of '1' is odd from bit 23~bit 1, the value of last bit shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

Table 6-20. STA_2 status register (REG_ADDR = 0x02)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	OC_OUTA1_HS	OC_OUTA1_LS	OC_OUTA2_HS	OC_OUTA2_LS	OC_OUTB1_HS	OC_OUTB1_LS	OC_OUTB2_HS	OC_OUTB2_LS
Operation Type	RLR	RLR	RLR	RLR	RLR	RLR	RLR	RLR
Default	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	OPL_OUTA	OPL_OUTB	Reserved	Reserved	CVULF	CVLLAF	CVLLBF	Parity
Operation Type	RLR	RLR	RO	RO	RO	RO	RO	-
Default	0	0	0	0	0	0	0	-

Table 6-21. STA_2 status register description

Bit	Field Name	Description
15	OC_OUTA1_HS	0: No overcurrent in OUTA1 high side detected (default value). 1: Overcurrent detected in OUTA1 high side. Error flag latched.
14	OC_OUTA1_LS	0: No overcurrent in OUTA1 low side detected (default value). 1: Overcurrent detected in OUTA1 low side. Error flag latched.
13	OC_OUTA2_HS	0: No overcurrent in OUTA2 high side detected (default value). 1: Overcurrent detected in OUTA2 high side. Error flag latched.
12	OC_OUTA2_LS	0: No overcurrent in OUTA2 low side detected (default value). 1: Overcurrent detected in OUTA2 low side. Error flag latched.
11	OC_OUTB1_HS	0: No overcurrent in OUTB1 high side detected (default value). 1: Overcurrent detected in OUTB1 high side. Error flag latched.
10	OC_OUTB1_LS	0: No overcurrent in OUTB1 low side detected (default value). 1: Overcurrent detected in OUTB1 low side. Error flag latched.
9	OC_OUTB2_HS	0: No overcurrent in OUTB2 high side detected (default value). 1: Overcurrent detected in OUTB2 high side. Error flag latched.
8	OC_OUTB2_LS	0: No overcurrent in OUTB2 low side detected (default value). 1: Overcurrent detected in OUTB2 low side. Error flag latched.
7	OPL_OUTA	0: No open load in OUTA detected (default value). 1: Open load in OUTA detected. Error flag latched.
6	OPL_OUTB	0: No open load in OUTB detected (default value). 1: Open load in OUTB detected. Error flag latched.
5	Reserved	0: Reversed (default value).
4	Reserved	0: Reversed (default value).
3	CVULF	0: No conversion voltage CVA / CVB / CVC / CVD over CVUL upper limit detected (default value). 1: Conversion voltage CVA or CVB or CVC or CVD, one or multiple, over CVUL upper limit detected.
2	CVLLAF	0: No conversion voltage CVA / CVB / CVC / CVD under CVLLA low limit A detected (default value). 1: Conversion voltage CVA or CVB or CVC or CVD, one or multiple, under CVLLA low limit A detected.
1	CVLLBF	0: No conversion voltage CVA / CVB / CVC / CVD under CVLLB low limit B detected (default value). 1: Conversion voltage CVA or CVB or CVC or CVD, one or multiple, under CVLLB low limit detected.
0	PARITY	Bit 0 parity bit, ODD parity check. If the number of occurrences of '1' is odd from bit 23~bit 1, the value of last bit shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

Table 6-22. CONFIG_1 control register (REG_ADDR = 0x03)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	CP_SS	PWM_SS	Reserved	AOUT_SEL[1:0]		Reserved	Reserved	Reserved
Operation Type	RW	RW	RO	RW	RW	RW	RO	RO
Default	0	0	0	0	0	1	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	Reserved	Reserved	CTRL1_SEL	Reserved	CTRL2_SEL	CTRL3_SEL[1:0]		Parity
Operation Type	RO	RO	RW	RO	RW	RW	RW	-
Default	0	0	1	0	1	0	0	-

Table 6-23. CONFIG_1 register description

Bit	Field Name	Description
15	CP_SS	0: Fix charge pump frequency (default value). 1: Enable charge pump spread spectrum function.
14	PWM_SS	0: Fix current regulation PWM frequency (default value). 1: Enable current regulation PWM spread spectrum function.
13	Reserved	0: Reversed (default value).
12 11	AOUT_SEL[1:0]	00: Disabled (default value) 01: Voltage proportional to junction temperature 10: Bandgap voltage 11: Disabled
10	Reserved	1: Reversed (default value).
9	Reserved	0: Reversed (default value).
8	Reserved	0: Reversed (default value).
7	Reserved	0: Reversed (default value).
6	Reserved	0: Reversed (default value).
5	CTRL1_SEL	0: No function selected on CTRL1 pin, stepper mode phase counter PH[5:0] or APH[6:0] updated only by SPI. 1: CTRL1 as stepper mode STEP input control signal (default value), a rising edge on CTRL1 pin cause phase counter updated, while PH[5:0] or APH[6:0] bits can only be read.
4	Reserved	0: Reversed (default value).
3	CTRL2_SEL	0: No function selected on CTRL2 pin, stepper mode DIR signal updated by SPI CONFIG_3 register DIR bit. 1: CTRL2 as stepper mode DIR input control signal (default value), CTRL2 pin status LOW, DIR bit '0', phase counter increment, while CTRL2 pin status HIGH, DIR bit '1', phase counter decrement.
2 1	CTRL3_SEL[1:0]	00: No function selected on CTRL3 pin (default value), stepper mode HOLD or SMODE selection are achieved by CONFIG3 HOLD bit and SM[2:0] bits. 01: CTRL3 as stepper mode SMODE (ASM[2:0] / SM[2:0]) select pin. 10: CTRL3 as stepper mode HOLD select pin. 11: No function selected on CTRL3 pin， stepper mode HOLD or SMODE selection are achieved by CONFIG3 HOLD bit and SM[2:0] bits.
0	PARITY	Bit 0 parity bit, ODD parity check. If the number of occurrences of '1' is odd from bit 23~bit 1, the value of last bit shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

Table 6-24. CONFIG_2 control register (REG_ADDR = 0x04)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	Reserved	Reserved	Reserved	Reserved	DOUT1_SEL[1:0]		Reserved	DOUT2_SEL1
Operation Type	RO	RO	RO	RO	RW	RW	RO	RW
Default	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	DOUT2_SEL0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Parity
Operation Type	RW	RO	RO	RO	RO	RO	RO	-
Default	0	0	0	0	0	0	0	-

Table 6-25. CONFIG_2 register description

Bit	Field Name	Description
15	Reserved	0: Reversed (default value).
14	Reserved	0: Reversed (default value).
13	Reserved	0: Reversed (default value).
12	Reserved	0: Reversed (default value).
11	DOUT1_SEL1	00: No function available on DOUT1 pin, tristate (EN pin low) or low state (EN pin high). (default value). 01: Coil voltage conversion ready signal (CVRDY) output on DOUT1 pin. 10: Coil voltage conversion under low limit (CVLL) output on DOUT1 pin. 11: Coil voltage conversion out of range (CVOOR) output on DOUT1 pin.
10	DOUT1_SEL0	
9	Reserved	0: Reversed (default value).
8	DOUT2_SEL1	00: No function available on DOUT2 pin, tristate (EN pin low) or low state (EN pin high). (default value). 01: Internal current regulation PWM signal output on DOUT2 pin. 10: Fault output on DOUT2 pin. 11: Fault check indicator on DOUT2 pin.
7	DOUT2_SEL0	
6	Reserved	0: Reversed (default value).
5	Reserved	0: Reversed (default value).
4	Reserved	0: Reversed (default value).
3	Reserved	0: Reversed (default value).
2	Reserved	0: Reversed (default value).
1	Reserved	0: Reversed (default value).
0	PARITY	Bit 0 parity bit, ODD parity check. If the number of occurrences of '1' is odd from bit 23~bit 1, the value of last bit shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

Table 6-26. CONFIG_3 control register (REG_ADDR = 0x05)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	DRV_EN	HOLD_EN	ASM[2:0]			SM[2:0]		
Operation Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	DIR	PH[5:0]						Parity
Operation Type	RW	RW	RW	RW	RW	RW	RW	-
Default	0	0	0	0	0	0	0	-

Table 6-27. CONFIG_3 register description

Bit	Field Name	Description
15	DRV_EN	0: Output stage disable, HIZ state (default value). 1: Enable output OUTA, OUTB power stage.
14	HOLD_EN	0: HOLD mode disabled (default value). 1: HOLD mode enable. Note: if CTRL3_SEL[1:0] = 2b'10' & stepper mode, the bit is read only and reflects CTRL3 pin status, HOLD_EN bit is set to '0' in this setting when CTRL3 pin is low , on the contrary, HOLD_EN bit is asserted to '1' while CTRL3 pin is high.
13 12 11	ASM[2:0]	Alternative step mode, used only when CTRL3_SEL bits = 2b'01' && CTRL3 = HIGH && HB_MODE=0 000,101, 110, 111: 1/16th microstep 001: 1/8 th microstep 010: ministep 011: half step 100: full step Default value is ‘000’
10 9 8	SM[2:0]	Default step mode, used in stepper mode CTRL3_SEL bits = 2b'01' && CTRL3 = LOW && HB_MODE=0 or CTRL3_SEL bits != 2b'01' && HB_MODE=0 000,101, 110, 111: 1/16th microstep 001: 1/8 th microstep 010: ministep 011: half step 100: full step Default value is ‘000’
7	DIR	0: Increment phase counter, clockwise (default value). 1: decrement phase counter, counter-clockwise.
6 5 4 3 2 1	PH[5:0]	Phase counter values in stepper mode, it determines the current profile applied on OUTA / OUTB and reports the step position. If CTRL1_SEL is '0', the phase counter bits PH[5:0] can be read and write with fully SPI step position control, no matter CTRL1 /CTRL2 pin status and DIR bit. While CTRL1_SEL is '1', the phase counter bits PH[5:0] is read only, CTRL1 pin rise edge cause phase counter updated according to DIR bit status, after new PWM period begins. Default value is ‘000000’ after POR.
0	PARITY	Bit 0 parity bit, ODD parity check. If the number of occurrences of '1' is odd from bit 23~bit 1, the value of last bit shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

Table 6-28. CONFIG_4 control register (REG_ADDR = 0x06)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	PWM_FREQ_SEL[1:0]		TFILT_TOC_EXT	TBLANK_EXT	TFILT_SEL[1:0]		SR_SEL[1:0]	
Operation Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	1	1	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	DECAY_SEL[1:0]		Reserved	Reserved	OPL_FILT	DECAY_SEL_HOLD	Reserved	Parity
Operation Type	RW	RW	RW	RW	RW	RW	RW	-
Default	0	0	0	0	0	0	0	-

Table 6-29. CONFIG_4 register description

Bit	Field Name	Description
15 14	PWM_FREQ_SEL [1:0]	Current regulation PWM frequency selection 00: 20khz (default value). 01: 30khz 10: 40khz 11: 40khz
13	TFILT_TOC_EXT	Current regulation t_{FILTER} and overcurrent t_{OC} filter timing extended selection 0: No extended timing on t_{FILTER} and t_{OC}, default value. 1: Extend with additional two system clock cycles (200ns)
12	TBLANK_EXT	Current regulation t_{BLANK} timing extended selection 0: No extended on t_{BLANK} timing. 1: Extend t_{BLANK} to 4us independently from SR_SEL[1:0] settings.
11 10	TFILT_SEL[1:0]	Current regulation t_{FILTER} selection 00: 0.5us 01: 1us 10: 2us 11: 3us (default value).
9 8	SR_SEL[1:0]	OUTA, OUTB slew rate selection 00: 10v/us (default value). 01: 40v/us 10: 70v/us 11: 100v/us
7 6	DECAY_SEL[1:0]	Decay mode selection 00: auto decay mode 1 (default value). 01: slow decay always 10: mixed decay 11: auto decay mode 2
5	Reserved	0: Reversed (default value).
4	Reserved	0: Reversed (default value).
3	OPL_FILT	Open load detection filter timing 0: 30ms (default value). 1: 60ms
2	DECAY_SEL_HOLD	Decay mode selection during HOLD mode 0: Slow decay used in HOLD mode (default value). 1: Mix decay used in HOLD mode
1	Reserved	0: Reversed (default value).
0	PARITY	Bit 0 parity bit, ODD parity check. If the number of occurrences of '1' is odd from bit 23~bit 1, the value of last bit shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

Table 6-30. CONFIG_5 control register (REG_ADDR = 0x07)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	CV_EN	Reserved	CV_DELAY[4:0]					CV_STALL_NUM BIT2
Operation Type	RW	RO	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	CV_STALL_NUM BIT1	CV_STALL_NUM BIT0	CV_REG_IND[1:0]		STALL_HOLD_EN	Reserved	Reserved	Parity
Operation Type	RW	RW	RO	RO	RW	RO	RO	-
Default	0	0	0	0	0	0	0	-

Table 6-31. CONFIG_5 register description

Bit	Field Name	Description
15	CV_EN	Coil BEMF voltage conversion enable 0: Coil BEMF voltage conversion not enable (default value). 1: Coil BEMF voltage starts according to trigger sequence.
14	Reserved	0: Reversed (default value).
13	CV_DELAY[4:0]	Coil BEMF voltage conversion delay timing configuration For the value from 1 to max 31, it sets the number of PWM periods between the beginning of zero current step and coil BEMF voltage conversion starts. If the value is 0, it samples the coil voltage at the end of zero current step
12		
11		
10		
9		
8	CV_STALL_NUM[2:0]	Coil BEMF voltage stall number configuration for stall detection It sets the required number of coil BEMF voltage consecutive conversion which out of range [CVLLA, CVUL], until stall detection asserted. The minimum value is 1, even CV_STALL_NUM[2:0] is configured to 0.
7		
6		
5	CV_REG_IND[1:0]	Last coil BEMF voltage conversion store register 00: CVA 01: CVB 10: CVC 11: CVD
4		
3	STALL_HOLD_EN	Automatic hold mode enable configuration during stall event detected 0: Device doesn't automatically enter HOLD mode when stall event detected (default value). 1: Device automatically enter HOLD mode when stall event is detected
2	Reserved	0: Reversed (default value).
1	Reserved	0: Reversed (default value).
0	PARITY	Bit 0 parity bit, ODD parity check. If the number of occurrences of '1' is odd from bit 23~bit 1, the value of last bit shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

Table 6-32. CONFIG_6 control register (REG_ADDR = 0x08)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	IFSH[3:0]				Reserved	Reserved	Reserved	Reserved
Operation Type	RW	RW	RW	RW	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	Reserved	Reserved	Reserved	IFSR[3:0]				Parity
Operation Type	RO	RO	RO	RW	RW	RW	RW	-
Default	0	0	0	0	0	0	0	-

Table 6-33. CONFIG_6 register description

Bit	Field Name	Description
15 14 13 12	IFSH[3:0]	Full scale current setting in HOLD mode 1111: typ 326mA 1110: typ 292mA 1101: typ 264mA 1100: typ 230mA 1011: typ 202mA 1010: typ 168mA 1001: typ 140mA 1000; typ 118mA 0111: typ 101mA 0110: typ 95mA 0101: typ 84mA 0100: typ 79mA 0011: typ 73mA 0010: typ 62mA 0001: typ 50mA 0000: typ 28mA (default value)
11	Reserved	0: Reversed (default value).
10	Reserved	0: Reversed (default value).
9	Reserved	0: Reversed (default value).
8	Reserved	0: Reversed (default value).
7	Reserved	0: Reversed (default value).
6	Reserved	0: Reversed (default value).
5	Reserved	0: Reversed (default value).
4 3 2 1	IFSR[3:0]	Full scale current setting in normal running mode 1111: typ 1353mA 1110: typ 1160mA 1101: typ 1051mA 1100: typ 920mA 1011: typ 812mA 1010: typ 679mA 1001: typ 571mA 1000; typ 465mA 0111: typ 396mA 0110: typ 375mA 0101: typ 329mA 0100: typ 323mA 0011: typ 302mA 0010: typ 220mA 0001: typ 198mA 0000: typ 176mA
0	PARITY	Bit 0 parity bit, ODD parity check. If the number of occurrences of '1' is odd from bit 23~bit 1, the value of last bit shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

Table 6-34. CVA register (REG_ADDR = 0x09)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	Reserved	Reserved	Reserved	Reserved	Reserved	CVA[9:7]		
Operation Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	CVA[6:0]							Parity
Operation Type	RO	RO	RO	RO	RO	RO	RO	-
Default	0	0	0	0	0	0	0	-

Table 6-35. CVA register description

Bit	Field Name	Description
15	Reserved	0: Reversed (default value).
14	Reserved	0: Reversed (default value).
13	Reserved	0: Reversed (default value).
12	Reserved	0: Reversed (default value).
11	Reserved	0: Reversed (default value).
10	CVA[9:0]	Coil BEMF voltage conversion digital value at phase counter 0° $V_{BEMF} = \frac{10\text{bit register decimal value}}{1023} \times 28V$
9		
8		
7		
6		
5		
4		
3		
2		
1		
0	PARITY	Bit 0 parity bit, ODD parity check. If the number of occurrences of '1' is odd from bit 23~bit 1, the value of last bit shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

Table 6-36. CVB register (REG_ADDR = 0x0A)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	Reserved	Reserved	Reserved	Reserved	Reserved	CVB[9:7]		
Operation Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	CVB[6:0]							Parity
Operation Type	RO	RO	RO	RO	RO	RO	RO	-
Default	0	0	0	0	0	0	0	-

Table 6-37. CVB register description

Bit	Field Name	Description
15	Reserved	0: Reversed (default value).
14	Reserved	0: Reversed (default value).
13	Reserved	0: Reversed (default value).

12	Reserved	0: Reversed (default value).
11	Reserved	0: Reversed (default value).
10	CVB[9:0]	Coil BEMF voltage conversion digital value at phase counter 90° $V_{BEMF} = \frac{10bit\ register\ decimal\ value}{1023} \times 28V$
9		
8		
7		
6		
5		
4		
3		
2		
1		
0	PARITY	Bit 0 parity bit, ODD parity check. If the number of occurrences of '1' is odd from bit 23~bit 1, the value of last bit shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

Table 6-38. CVC register (REG_ADDR = 0x0B)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	Reserved	Reserved	Reserved	Reserved	Reserved	CVC[9:7]		
Operation Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	CVC[6:0]							Parity
Operation Type	RO	RO	RO	RO	RO	RO	RO	-
Default	0	0	0	0	0	0	0	-

Table 6-39. CVC register description

Bit	Field Name	Description
15	Reserved	0: Reversed (default value).
14	Reserved	0: Reversed (default value).
13	Reserved	0: Reversed (default value).
12	Reserved	0: Reversed (default value).
11	Reserved	0: Reversed (default value).
10	CVC[9:0]	Coil BEMF voltage conversion digital value at phase counter 180° $V_{BEMF} = \frac{10bit\ register\ decimal\ value}{1023} \times 28V$
9		
8		
7		
6		
5		
4		
3		
2		
1		
0	PARITY	Bit 0 parity bit, ODD parity check. If the number of occurrences of '1' is odd from bit 23~bit 1, the value of last bit shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

Table 6-40. CVD register (REG_ADDR = 0x0C)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	Reserved	Reserved	Reserved	Reserved	Reserved	CVD[9:7]		
Operation Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	CVD[6:0]							Parity
Operation Type	RO	RO	RO	RO	RO	RO	RO	-
Default	0	0	0	0	0	0	0	-

Table 6-41. CVD register description

Bit	Field Name	Description
15	Reserved	0: Reversed (default value).
14	Reserved	0: Reversed (default value).
13	Reserved	0: Reversed (default value).
12	Reserved	0: Reversed (default value).
11	Reserved	0: Reversed (default value).
10	CVD[9:0]	Coil BEMF voltage conversion digital value at phase counter 270° $V_{BEMF} = \frac{10\text{bit register decimal value}}{1023} \times 28V$
9		
8		
7		
6		
5		
4		
3		
2		
1		
0	PARITY	Bit 0 parity bit, ODD parity check. If the number of occurrences of '1' is odd from bit 23~bit 1, the value of last bit shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

Table 6-42. CVLLB register (REG_ADDR = 0x0D)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	Reserved	Reserved	Reserved	Reserved	Reserved	CVLLB[9:7]		
Operation Type	RO	RO	RO	RO	RO	RW	RW	RW
Default	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	CVLLB[6:0]							Parity
Operation Type	RW	RW	RW	RW	RW	RW	RW	-
Default	0	0	0	0	0	0	0	-

Table 6-43. CVLLB register description

Bit	Field Name	Description
15	Reserved	0: Reversed (default value).
14	Reserved	0: Reversed (default value).
13	Reserved	0: Reversed (default value).

12	Reserved	0: Reversed (default value).
11	Reserved	0: Reversed (default value).
10	CVLLB[9:0]	Coil BEMF voltage low limit B threshold setting CVLLBF flag is asserted, if the last BEMF conversion voltage below CVLLB[9:0] setting. otherwise, CVLLBF flag is cleared
9		
8		
7		
6		
5		
4		
3		
2		
1		
0	PARITY	Bit 0 parity bit, ODD parity check. If the number of occurrences of '1' is odd from bit 23~bit 1, the value of last bit shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

Table 6-44. CVLLA register (REG_ADDR = 0x0E)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	Reserved	Reserved	Reserved	Reserved	Reserved	CVLLA[9:7]		
Operation Type	RO	RO	RO	RO	RO	RW	RW	RW
Default	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	CVLLA[6:0]							Parity
Operation Type	RW	RW	RW	RW	RW	RW	RW	-
Default	0	0	0	0	0	0	0	-

Table 6-45. CVLLA register description

Bit	Field Name	Description
15	Reserved	0: Reversed (default value).
14	Reserved	0: Reversed (default value).
13	Reserved	0: Reversed (default value).
12	Reserved	0: Reversed (default value).
11	Reserved	0: Reversed (default value).
10	CVLLA[9:0]	Coil BEMF voltage low limit A threshold setting CVLLAF flag is asserted, if the last BEMF conversion voltage below CVLLA[9:0] setting. otherwise, CVLLAF flag is cleared
9		
8		
7		
6		
5		
4		
3		
2		
1		
0	PARITY	Bit 0 parity bit, ODD parity check. If the number of occurrences of '1' is odd from bit 23~bit 1, the value of last bit shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

Table 6-46. CVUL register (REG_ADDR = 0x0F)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	Reserved	Reserved	Reserved	Reserved	Reserved	CVUL[9:7]		
Operation Type	RO	RO	RO	RO	RO	RW	RW	RW
Default	0	0	0	0	0	1	1	1
	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	CVUL[6:0]							Parity
Operation Type	RW	RW	RW	RW	RW	RW	RW	-
Default	1	1	1	1	1	1	1	-

Table 6-47. CVUL register description

Bit	Field Name	Description
15	Reserved	0: Reversed (default value).
14	Reserved	0: Reversed (default value).
13	Reserved	0: Reversed (default value).
12	Reserved	0: Reversed (default value).
11	Reserved	0: Reversed (default value).
10	CVUL9:0]	Coil voltage upper limit threshold setting CVULF flag is asserted, if the last BEMF conversion voltage over CVUL[9:0] setting. otherwise, CVULF flag is cleared
9		
8		
7		
6		
5		
4		
3		
2		
1		
0	PARITY	Bit 0 parity bit, ODD parity check. If the number of occurrences of '1' is odd from bit 23~bit 1, the value of last bit shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

Table 6-48. CONFIG_7 control register (REG_ADDR = 0x10)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	OUTA1_HIZ	OUTA2_HIZ	OUTB1_HIZ	OUTB2_HIZ	Version[1:0]		Device_ID	UTWARN
Operation Type	RW	RW	RW	RW	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	APH[6:0]							Parity
Operation Type	RW	RW	RW	RW	RW	RW	RW	-
Default	0	0	0	0	0	0	0	-

Table 6-49. CONFIG_7 register description

Bit	Field Name	Description
15	OUTA1_HIZ	Half bridge HIZ control, only valid under half bridge mode 0: half bridge OUTA1 enable (default value) 1: half bridge OUTA1 disable (HIZ)
14	OUTA2_HIZ	Half bridge HIZ control, only valid under half bridge mode 0: half bridge OUTA2 enable (default value) 1: half bridge OUTA2 disable (HIZ)
13	OUTB1_HIZ	Half bridge HIZ control, only valid under half bridge mode 0: half bridge OUTB1 enable (default value) 1: half bridge OUTB1 disable (HIZ)
12	OUTB2_HIZ	Half bridge HIZ control, only valid under half bridge mode 0: half bridge OUTB2 enable (default value) 1: half bridge OUTB2 disable (HIZ)
11 10	Version[1:0]	00: Reversed (default value).
9	Device_ID	0: Reversed (default value).
8	UTWARN	0: Under low temperature not happen (default value). 1: Under low temperature happens.
7 6 5 4 3 2 1	APH[6:0]	Phase counter values only for stepper mode 1/32 stepper mode. Similar as PH[5:0] bit, if CTRL1_SEL bit is '0', the phase counter bits APH[6:0] can be read and write with fully SPI step position control, no matter CTRL1 /CTRL2 pin status and DIR bit. While CTRL1_SEL bit is '1', the phase counter bits APH[6:0] is read only, CTRL1 pin rise edge cause phase counter updated according to DIR bit status.
0	PARITY	Bit 0 parity bit, ODD parity check. If the number of occurrences of '1' is odd from bit 23~bit 1, the value of last bit shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

Table 6-50. CONFIG_8 control register (REG_ADDR = 0x11)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	CP_SS_CONFIG	HOLDM_CONFIG	TOC_SEL	OPL_ON_DIS	CV_AVG_SEL	TCC_INC	TCC_RED	TBLANK_RED
Operation Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	1/32 STEP_EN	DIS_SLOPE_BLANK	FULL_STEP_IFS	Reserved	HB_MODE	FLT_LATCH	OVP_DIS	Parity
Operation Type	RW	RW	RW	RW	RW	RW	RW	-
Default	0	0	0	0	0	0	0	-

Table 6-51. CONFIG_8 register description

Bit	Field Name	Description
15	CP_SS_CONFIG	Charge pump spread spectrum modulation frequency selection 0: 16.5khz (default value). 1: 33khz
14	HOLDM_CONFIG	HOLD mode function selection 0: STEP pulse or phase counter is still active even under HOLD mode (default value). 1: STEP pulse is ignored and phase counter is hold during HOLD mode
13	TOC_SEL	Over current protection filter timing 0: Short OC filter, 0.2us if $t_{FIT\_OC\_EX}$ = 0; 0.4us if $t_{FIT\_OC\_EX}$ = 1 (default value). 1: Long OC filter, 3.2us if $t_{FIT\_OC\_EX}$ = 0; 6.4us if $t_{FIT\_OC\_EX}$ = 1
12	OPL_ON_DIS	ON state OPL function disable selection 0: ON state OPL for stepper detection is available (default value). 1: ON state OPL function is disabled
11	CV_AVG_SEL	0: average (8~16 times) for ADC data of BEMF voltage conversion (default value). 1: Real time ADC data of BEMF voltage conversion stored in CVA/CVB/CVC/CVD registers
10	TCC_INC	0: Tcc, cross current protection timing no change (default value). 1: Tcc, cross current protection timing increase by adding tfilter
9	TCC_RED	0: Tcc, cross current protection timing no change (default value). 1: Tcc, cross current protection timing reduce as down to 1/2 ratio
8	TBLANK_RED	Current regulation t_{BLANK} timing reduction selection 0: no change on t_{BLANK} (default value) 1: Reduce t_{BLANK} to 0.5us and ignore SR_SEL[1:0] settings
7	1/32 STEP_EN	1/32 microstep mode enable 0: 1/32 microstep is not active (default value). 1: Enable 1/32 microstep
6	DIS_SLOPE_BLANK	Internal slope & blank compensation control 0: Slope & blank compensation active under mixed decay (default value). 1: Disable slope & blank in mixed decay
5	FULL_STEP_IFS	0: Full step 100% full scale current (default value). 1: Full step 71% full scale current
4	Reserved	0: reversed (default value).
3	HB_MODE	Half bridge mode enable 0: default stepper mode (default value). 1: Enable independent 4x half bridge mode (OUTA1, OUTA2, OUTB1, OUTB2).
2	FLT_LATCH	FAULT latch configuration, details as fault table summary 0: Auto recovery for VSUV, VSOV, CPUV, OTSD, OTWARN (default value). 1: For VSUV, VSOV, CPUV, OTSD fault recovery, specific procedure is required to clear and reactive.
1	OVP_DIS	OVP protection disable configuration 0: Overvoltage protection is enabled (default value). 1: Overvoltage protection is disabled.
0	PARITY	Bit 0 parity bit, ODD parity check. If the number of occurrences of '1' is odd from bit 23~bit 1, the value of last bit shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

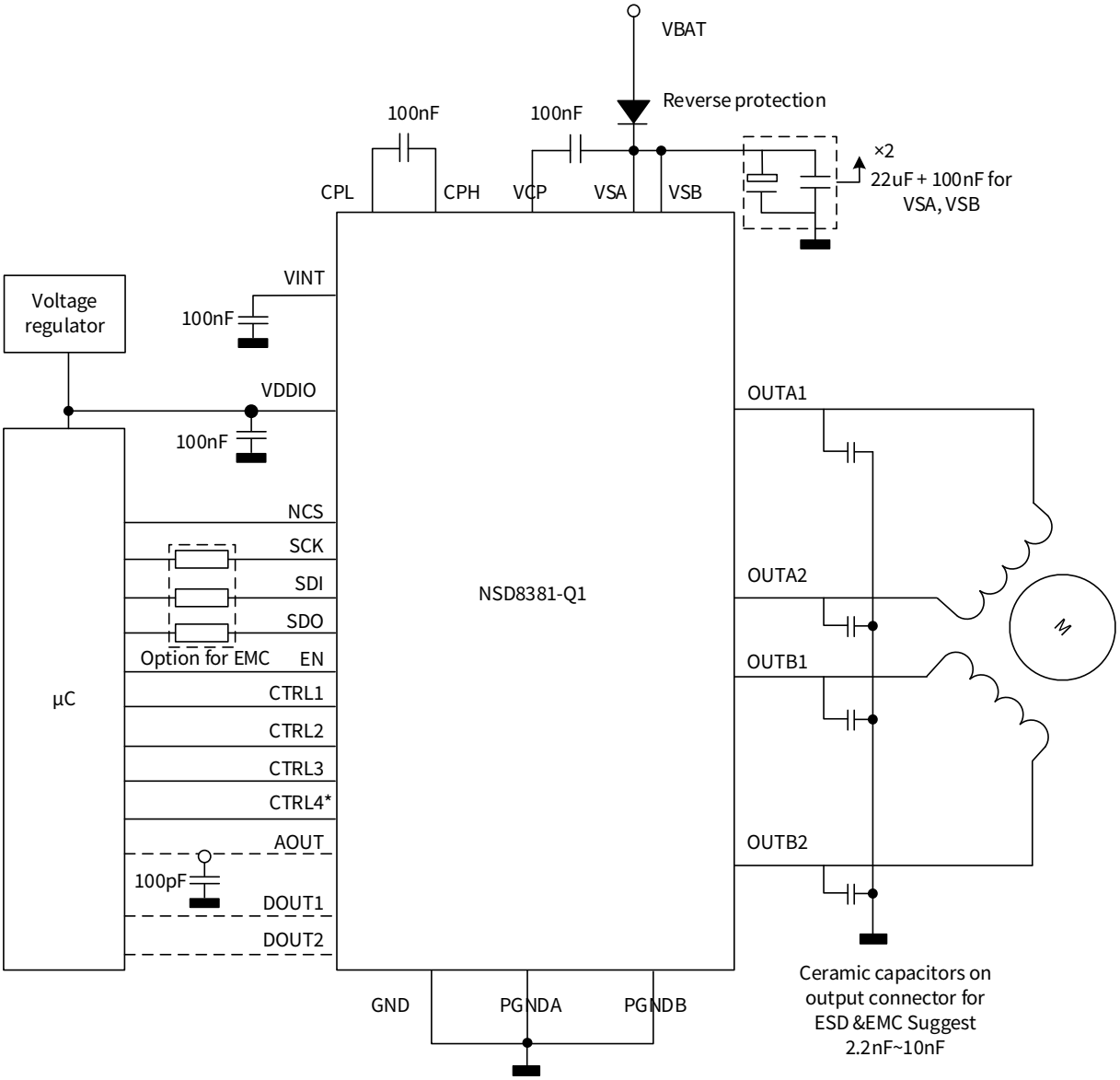
Table 6-52. CONFIG_9 register (REG_ADDR = 0x12)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Operation Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	UNLOCK	Parity
Operation Type	RO	RO	RO	RO	RO	RO	RW	-
Default	0	0	0	0	0	0	0	-

Table 6-53. CONFIG_9 register description

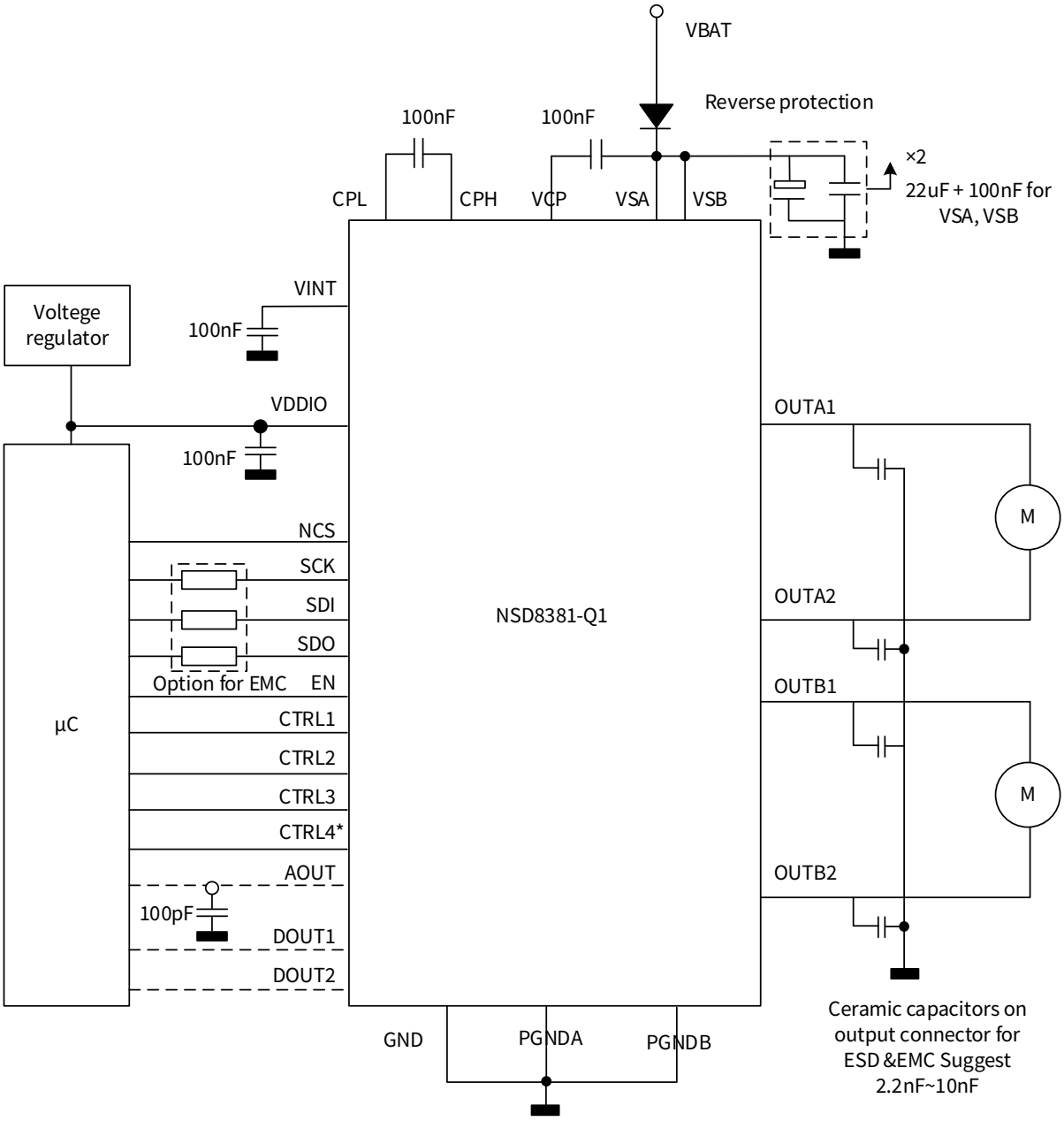
Bit	Field Name	Description
15	Reserved	0: reversed (default value).
14	Reserved	0: reversed (default value).
13	Reserved	0: reversed (default value).
12	Reserved	0: reversed (default value).
11	Reserved	0: reversed (default value).
10	Reserved	0: reversed (default value).
9	Reserved	0: reversed (default value).
8	Reserved	0: reversed (default value).
7	Reserved	0: reversed (default value).
6	Reserved	0: reversed (default value).
5	Reserved	0: reversed (default value).
4	Reserved	0: reversed (default value).
3	Reserved	0: reversed (default value).
2	Reserved	0: reversed (default value).
1	UNLOCK	0: CONFIG_8 register bit1~bit7 (OVP_DIS, FLT_LATCH, HB_MODE, RD_CLR_EN, Full_Step_IFS, DIS_SLOPE_BLANK, 1/32 STEP_EN) is lock, write command ignore. (default value). 1: Set ‘1’ to unlock the SPI write of CONFIG_8 register bit1~bit7 (OVP_DIS, FLT_LATCH, HB_MODE, RD_CLR_EN, Full_Step_IFS, DIS_SLOPE_BLANK, 1/32 STEP_EN).
0	PARITY	Bit 0 parity bit, ODD parity check. If the number of occurrences of '1' is odd from bit 23~bit 1, the value of last bit shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

7. Application diagram



Note: * CTRL4 pin is only available in VQFN32 package pinout

Figure 7-1. Typical application connection for stepper motor

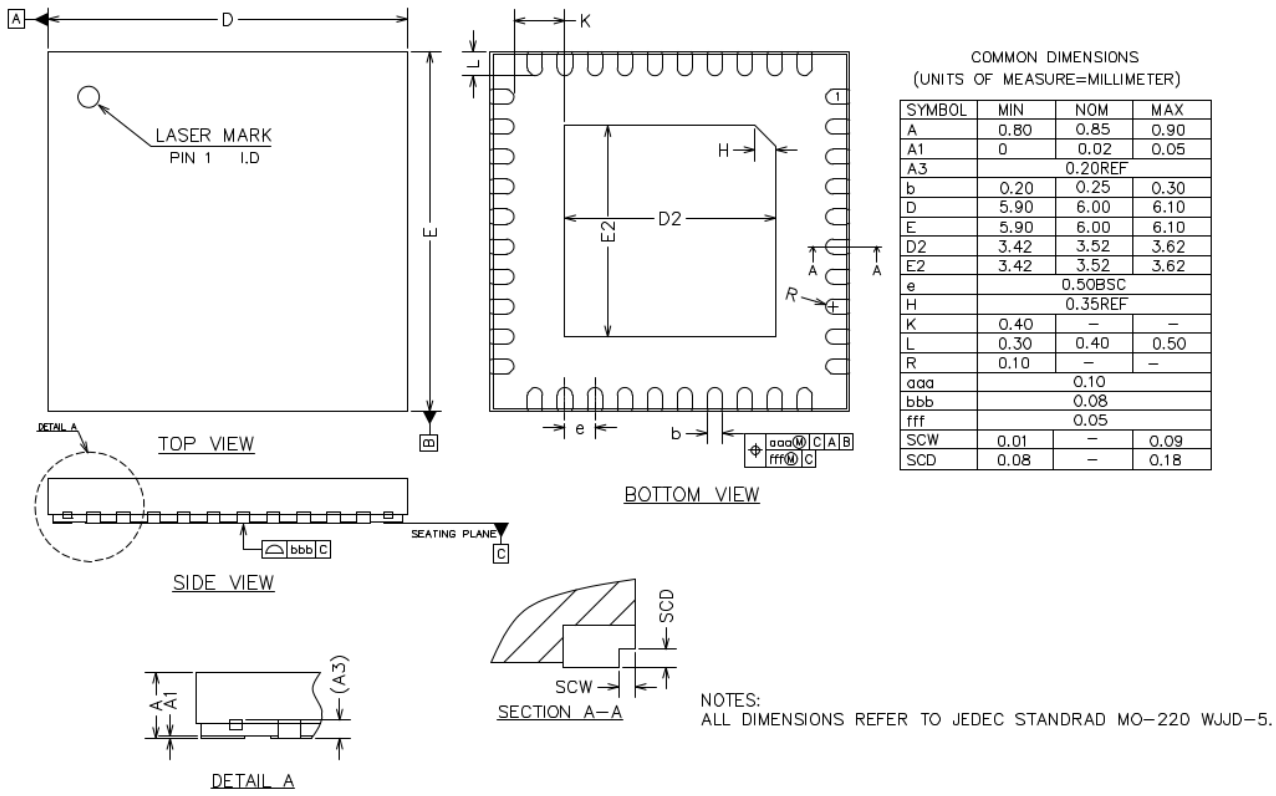


Note: * CTRL4 pin is only available in VQFN32 package pinout

Figure 7-2. Typical application connection for BDC motor

8. Package information

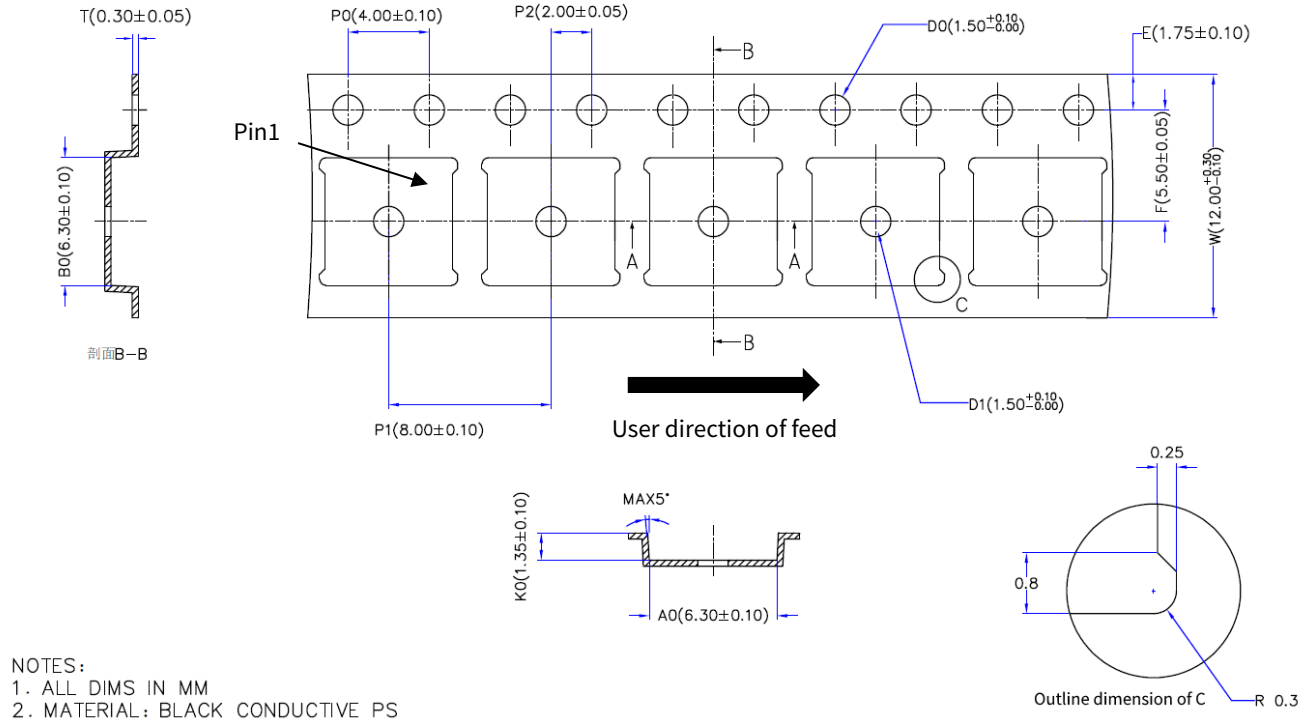
8.1. VQFN40 package information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

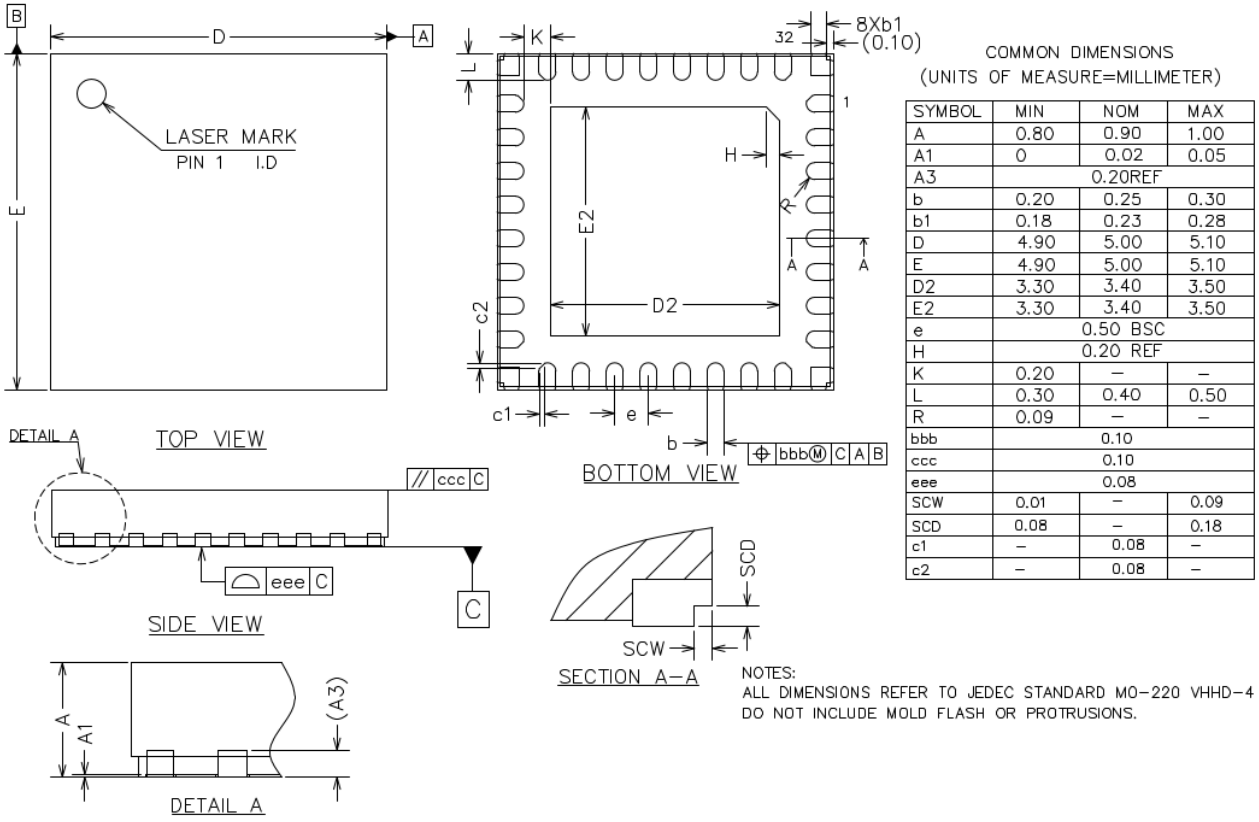
SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
A3		0.20REF	
b	0.20	0.25	0.30
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	3.42	3.52	3.62
E2	3.42	3.52	3.62
e		0.50BSC	
H		0.35REF	
K	0.40	–	–
L	0.30	0.40	0.50
R	0.10	–	–
aaa		0.10	
bbb		0.08	
fff		0.05	
SCW	0.01	–	0.09
SCD	0.08	–	0.18

8.2. VQFN40 packing information



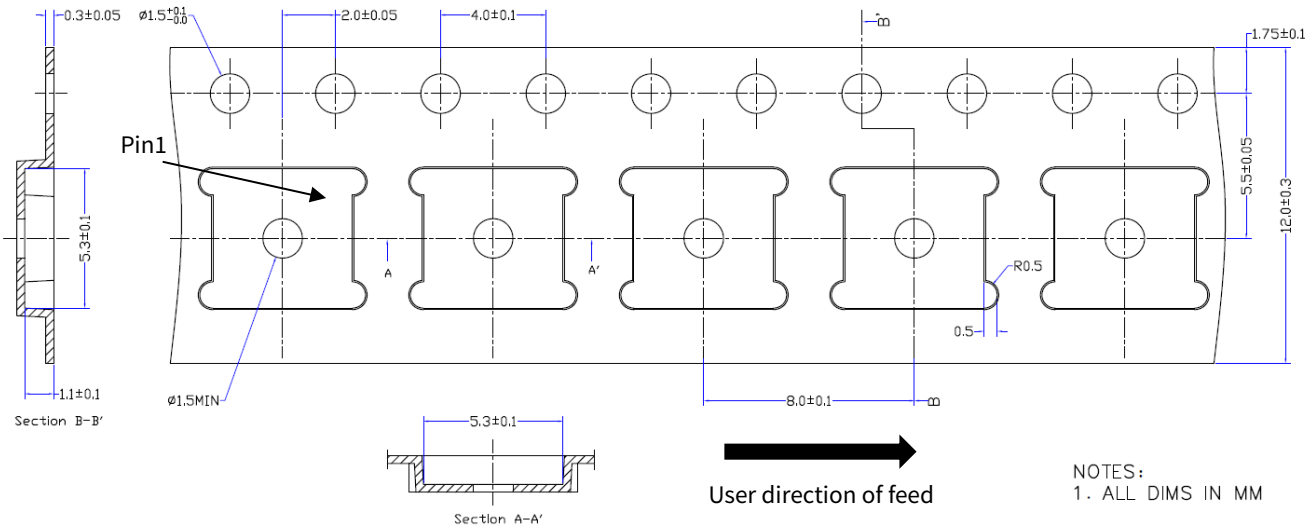
NOTES:
1. ALL DIMS IN MM
2. MATERIAL: BLACK CONDUCTIVE PS

8.3. VQFN32 package information



SYMBOL	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20REF	
b	0.20	0.25	0.30
b1	0.18	0.23	0.28
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.30	3.40	3.50
E2	3.30	3.40	3.50
e		0.50 BSC	
H		0.20 REF	
K	0.20	–	–
L	0.30	0.40	0.50
R	0.09	–	–
bbb		0.10	
ccc		0.10	
eee		0.08	
SCW	0.01	–	0.09
SCD	0.08	–	0.18
c1	–	0.08	–
c2	–	0.08	–

8.4. VQFN32 packing information



9. Ordering Information

Part Number	Automotive / Industrial	Package Type	MSL
NSD8381-Q1QAIR	Automotive	VQFN40	MSL3
NSD8381-Q1QANR	Automotive	VQFN32	MSL3
Note: All packages are ROHS compliant with peak reflow temperature of 260°C according to the JEDEC industry standard classifications and peak solder temperature.			

10. Revision History

Revision	Description	Date
0.1	Initial version	2023/4/5
0.2	Revise the description of CTRL1/2/3/4 pin function and fault table summary.	2023/6/25
0.3	Update TBD parameter values, Add and correct description in stepper operation, half bridge, diagnosis, SPI, registers, application diagram & package.	2024/2/8
0.4	Update figures as vector graphics. Insert index page information Revise UTW parameter value and the note for half bridge mode	2024/4/25
1.0	Release to 1.0 version	2024/4/30
1.1	Revise and remove ‘read command if RD_CLR_EN bit’ description. Revise datasheet format	2025/6/10

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