NOVOSENSE

NSD1015xT

Non-ISO Gate Driver with DESAT Protection

Datasheet (EN) 1.0

Product Overview

The NSD1015XT is a single-channel gate driver for driving IGBT and SiC MOSFETs. It can provide 5A source current and 5A sink current. It has a wide voltage supply range, the maximum power supply voltage is 32V, the chip provides an effective solution for solar inverters, uninterruptible power supplies, DC-DC systems.

NSD1015xT provide DESAT protection, UVLO protection and active open-drain fault report. NSD1015T has negative power-supply ability, and NSD1015MT supports Miller clamp to ensure reliable shutdown. To simplified the power-supply set in the application, accurate 5.0V reference output is provided.

The NSD1015xT device is available in SOP8 package with operating temperature range from -40°C to 125°C. In order to prevent over temperature, internal thermal shutdown at 175°C is provided.

Key Features

- Wide power supply: 14V~32V
- 5A peak source current and 5A peak sink current
- 80ns max propagation delay
- Accepts minimum input pulse width 40ns
- VREF 5V/20mA output
- Miller clamp peak current 1.5A
- DESAT protection with threshold 6.5V(typ) and mute time 35us
- Fault report when DESAT and TSD trigger
- Operation temperature: -40°C ~125 °C
- Reach RoHS compliance

Applications

- DC-to-AC solar inverters
- Motor drives and EV charging
- UPS and battery chargers
- Isolated DC/DC or DC/AC with iso components

Device Information

Part Number	Package	Body Size
NSD1015T-DSPR	SOP8	3.9mm*4.9mm
NSD1015MT-DSPR	SOP8	3.9mm*4.9mm

Simplified Application Diagram

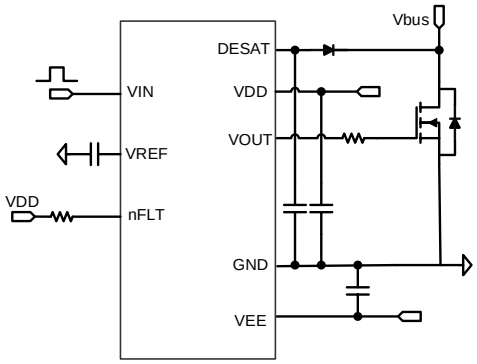

Figure 1. NSD1015T Block Diagram

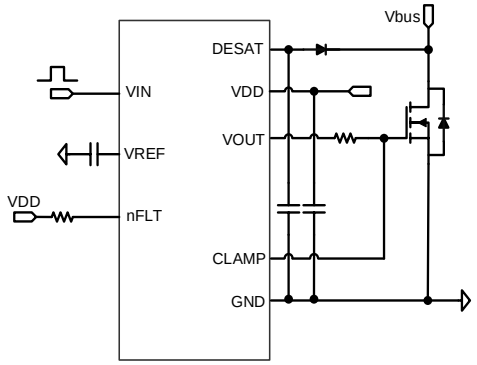

Figure 2. NSD1015MT Block Diagram

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1. Pin Configuration and Functions

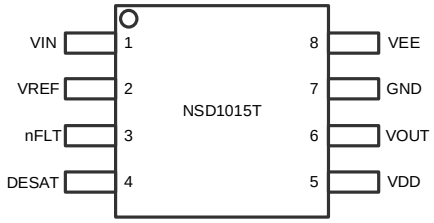


Figure 1.1 NSD1015T SOP8 Package

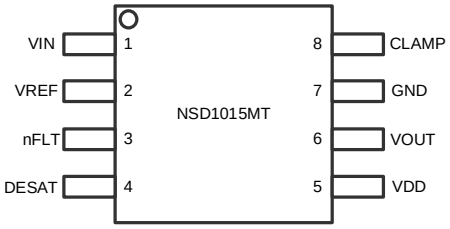


Figure 1.2 NSD1015MT SOP8 Package

Table 1.1 NSD1015xT Pin Configuration and Description

NSD1015xT SYMBOL	***NSD1015T PIN NO.***	***NSD1015MT PIN NO.***	***FUNCTION***
VIN	1	1	Input Pin
VREF	2	2	5V/20mA Output Pin for External Circuits
nFLT	3	3	Fault Open-drain Output.
DESAT	4	4	Input Pin of Desaturation Detection
VDD	5	5	Power Supply.
VOUT	6	6	Drive Output to Gate of MOS or IGBT
GND	7	7	Ground Pin
VEE	8	/	Negative Power Supply
CLAMP	/	8	Miller Clamp Pin

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit	Comments
Differential Side Supply Voltage	V_{DD} - V_{EE}	0	36	V	
Positive Power Supply	V_{DD} - GND	-0.3	36	V	
Negative Power Supply	V_{EE} - GND	-18	0.3	V	Only for NSD1015T
OUT Voltage	V_{OUT}	-0.3	VDD+0.3	V	
CLAMP	V_{CLAMP}	-0.3	VDD+0.3	V	Only for NSD1015MT
DESAT	V_{DESAT}	-0.3	14	V	
IN	V_{IN}	-0.3	5.5	V	
nFLT	V_{nFLT}	-0.3	VDD+0.3	V	
nFLT Current	I_{FLT}		20	mA	
Junction Temperature	T_j		150	°C	
Storage Temperature	T_{stg}	-65	150	°C	

3. ESD Ratings

		Symbol	Value	Unit
Electrostatic Discharge	Human-body model (HBM), per AEC Q100-002[1)]	V_{ESD_HBM}	±2500	V
	Charged-device model (CDM), per AEC Q100-011	V_{ESD_CDM}	±2000	V

1) ACE Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit	Comments
Differential Side Supply Voltage	V_{DD} - V_{EE}	14	32	V	
Positive Power Supply	V_{DD} - GND	14	32	V	VEE=0V
Negative Power Supply	V_{EE} - GND	-15	0	V	Only for NSD1015T
Input Voltage	V_{IN}	0	5	V	
Operation Ambient Temperature	T_A	-40	125	°C	

5. Thermal Information

Parameters	Symbol	SOP8	Unit
Junction-to-Ambient Thermal Resistance[1)]	$R_{\theta JA}$	101	°C/W
Junction-to-Top Characterization Parameter[2)]	Ψ_{JT}	8	°C/W
Junction-to-Board Characterization Parameter[2)]	Ψ_{JB}	51	°C/W

1) Tested using High Effective Thermal Conductivity Test Board (2S2P) described in JESD51-7.

2) Tested following the environment described in JESD51-2a.

6. Specifications

6.1. Electrical Characteristics

VDD=15V, VEE = 0V. TA = -40°C to 125°C, unless otherwise noted, Typical values are at TA=25°C.

Parameters	Symbol	Min	Norm	Max	Unit	Comments
Bias Current						
VDD Supply Quiescent Current	I_{VDDQ}		0.9	1.5	mA	
VEE Supply Quiescent Current	I_{VEEQ}		0.5		mA	VEE=-15V
VDD Supply Operation Current	I_{VDDO}		16		mA	VIN=500kHz, load:1.8nF
Under Voltage Lockout (UVLO)						
VDD UVLO Rising Threshold	V_{VDD_ON}	12.9	13.5	13.9	V	
VDD UVLO Falling Threshold	V_{VDD_OFF}	11.7	12.3	12.9	V	
VDD UVLO Hysteresis	V_{VDD_HYS}		1.2		V	
Input Pin Characteristics						
Logic High Input Threshold	V_{IN_H}	3.5	3.9		V	
Logic Low Input Threshold	V_{IN_L}		1.0	1.2	V	
Input Hysteresis Voltage	V_{HYS_IN}		2.9		V	
Input High Logic Bias Current	I_{IN_H}		5.6	10	uA	VIN =5.0V
Input Low Logic Bias Current	I_{IN_L}		0.5	1	uA	VIN = 0.5V
nFLT Pin						
nFLT Signal High State	V_{nFLT_H}			VDD	V	(I_{FLT_SINK} = 15 mA) External pull−up
nFLT Signal Low State	V_{nFLT_L}		0.5		V	
Output Pin Characteristic						
High Level Output Voltage	V_{DD}-V_{OUT}		0.1	0.25	V	Iout =-100mA
Low Level Output Voltage	V_{OUT}		0.05	0.2	V	Iout =100mA
Output Pull-Up Resistance	R_{OUTH}		1	2.5	Ω	
Output Pull-Down Resistance	R_{OUTL}		0.5	2	Ω	
High Level Peak Output Current[1)]	I_{OUTH}		5		A	Rg = 0.1Ω, C_load = 1uF
Low Level Peak Output Current[1)]	I_{OUTL}		5		A	Rg= 0.1Ω, C_load = 1uF
Active Miller Clamp (Only for NSD1015MT)						
Low Level Clamp Voltage	V_{CLAMP}		0.2		V	I_clamp = 100 mA;
Clamp Low-level Current	I_{CLAMPA}		1.5		A	
Clamp Threshold Voltage	V_{CLAMP_TH}		1.8		V	
DESAT PROTECTION						
DESAT Threshold Voltage	V_{DESAT_TH}	6	6.5	7	V	
Blanking Charge Current	I_{DESAT_CHG}	0.19	0.24	0.3	mA	
Blanking Discharge Current	I_{DESAT_DIS}		20		mA	
Blanking Time	T_{DESAT_BLK}		150		ns	
Mute Time	T_{DESAT_MUTE}		35		us	
VREF						
Voltage Reference	V_{REF}	4.85	5	5.20	V	
Reference Output Current	I_{REF}		20		mA	
Recommended Capacitance	C_{REF}	100	1000		nF	
THERMAL SHUTDOWN						

Thermal Shutdown Temperature[1)]	TSD		175		°C	
Thermal Shutdown Hysteresis[1)]	TSH		15		°C	

1) Not test covered, guaranteed by design.

6.2. Switching Characteristics

VDD=15V, VEE = 0V. TA = -40°C to 125°C, unless otherwise noted, Typical values are at TA=25°C.

Parameters	*Symbol*	*Min.*	*Norm.*	*Max.*	*Unit*	*Comments*
Minimum Pulse Width	T_{PWmin}		19	40	ns	No Load
Output Rise Time	T_R		15		ns	C_load = 1.8nF, (10% to 90%)
Output Fall Time	T_F		14		ns	C_load = 1.8nF, (90% to 10%)
Propagation Delay	T_{PDLH}	45	60	80	ns	No Load
	T_{PDHL}	45	60	80	ns	No Load
Delay Matching from ON to OFF	$T_{DM\_ON\_OFF}$		5		ns	
Delay from UVLO to VOUTL	$T_{UVLO\_VOUT\_DLY}$	17	19	23	us	
Delay from DESAT to VOUTL	$T_{DESAT\_VOUT\_DLY}$		130	250	ns	
Delay from DESAT to nFLT	$T_{DESAT\_nFLT\_DLY}$		110	250	ns	

6.3. Typical Performance Characteristics

VDD=15V, VEE = 0V. TA = -40°C to 125°C, unless otherwise noted, Typical values are at TA=25°C.

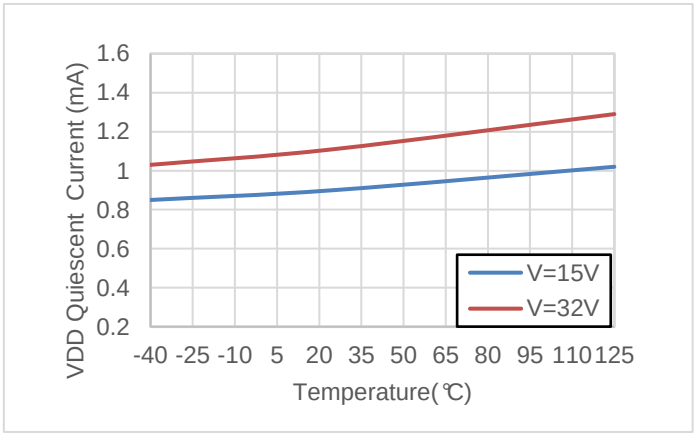


Figure 6.1 VDD Quiescent Current vs Temperature

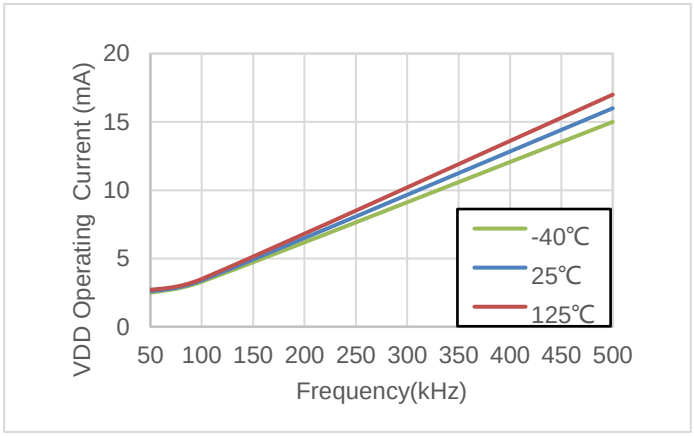


Figure 6.2 VDD Operating Current vs Frequency

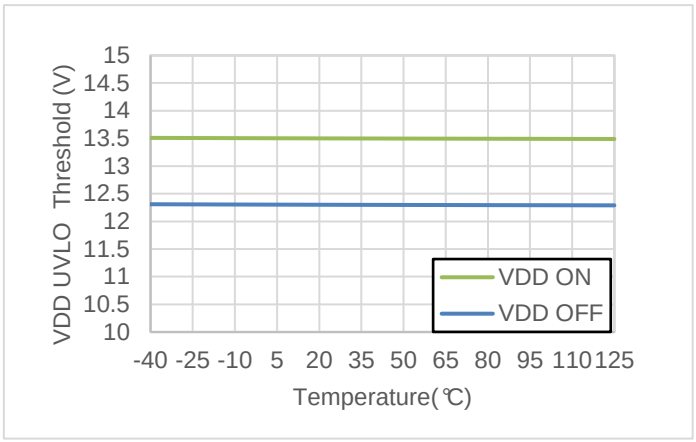


Figure 6.3 VDD UVLO Threshold vs Temperature

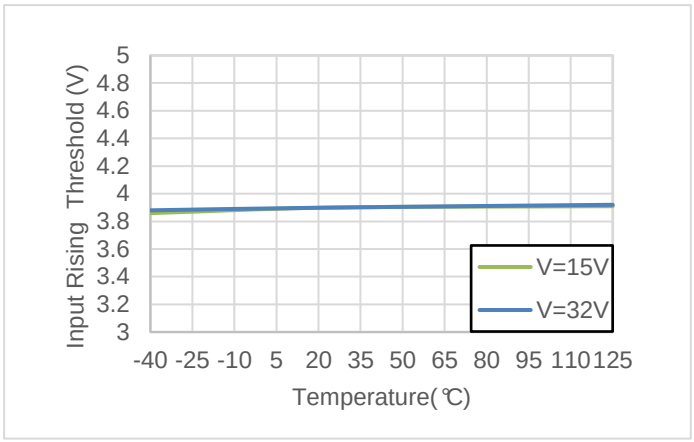


Figure 6.4 VIN Rising Threshold vs Temperature

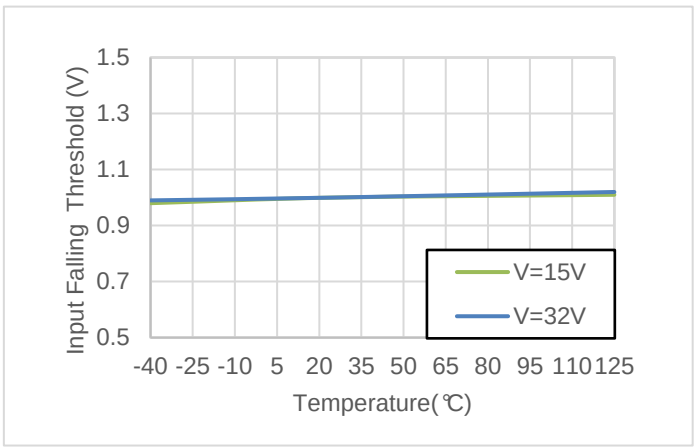


Figure 6.5 VIN Falling Threshold vs Temperature

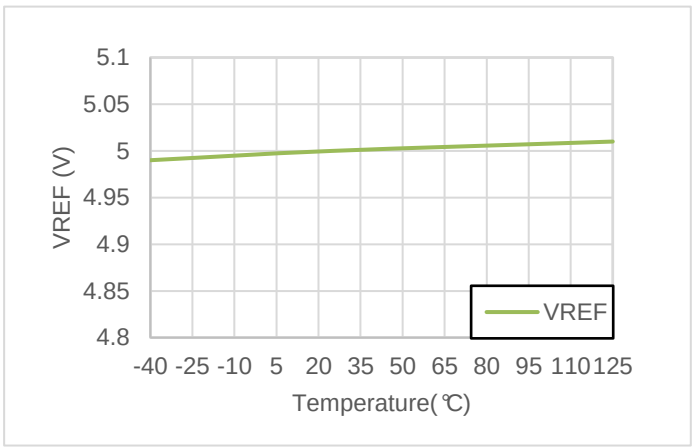


Figure 6.6 VREF vs Temperature

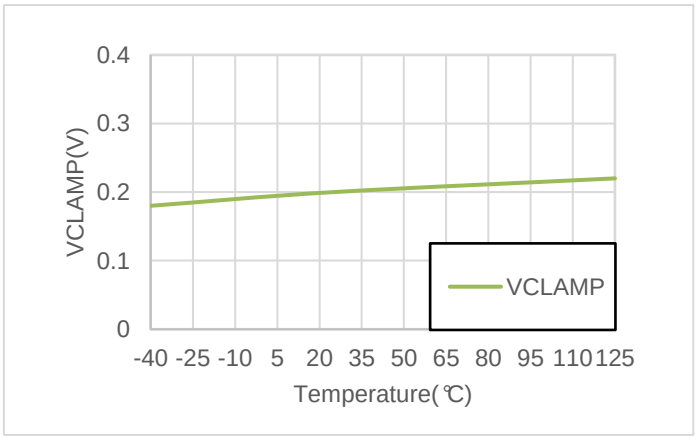


Figure 6.7 VCLAMP vs Temperature

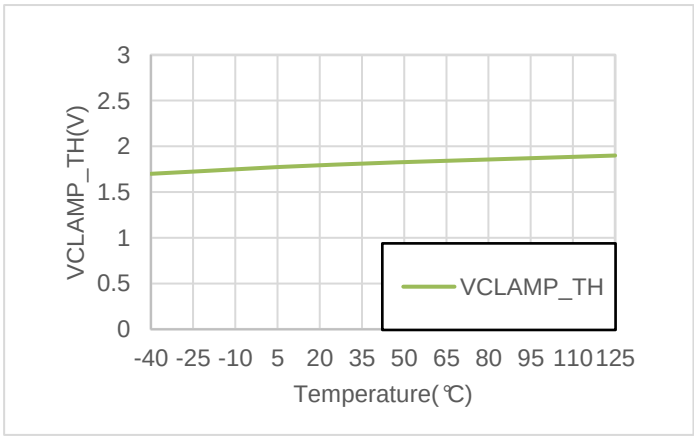


Figure 6.8 VCLAMP_TH vs Temperature

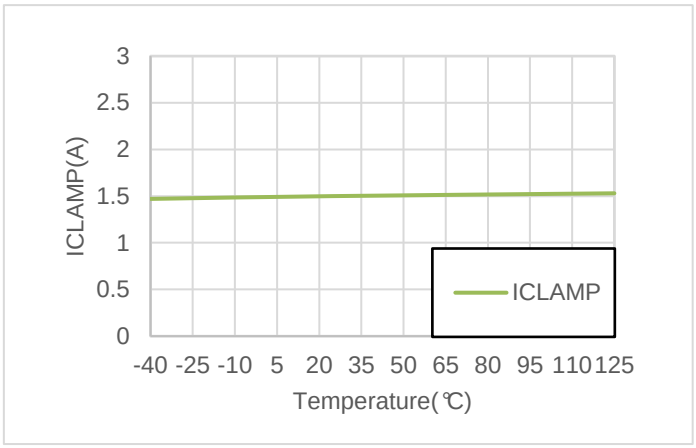


Figure 6.9 ICLAMP vs Temperature

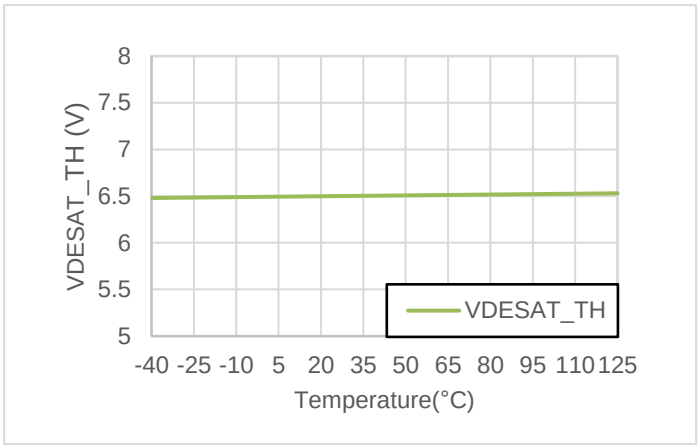


Figure 6.10 VDESAT_TH vs Temperature

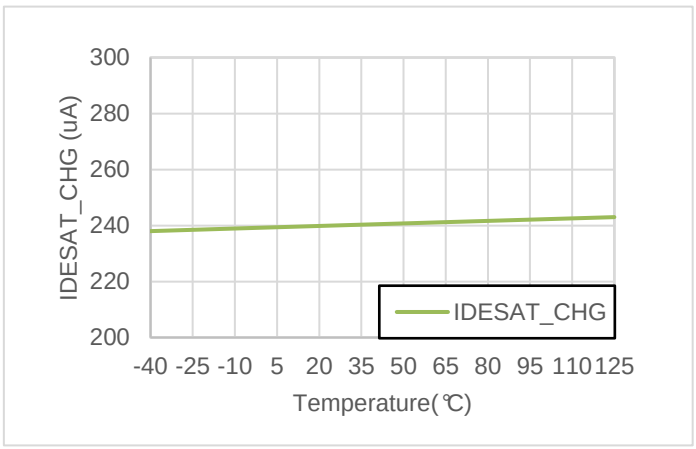


Figure 6.11 IDESAT_CHG vs Temperature

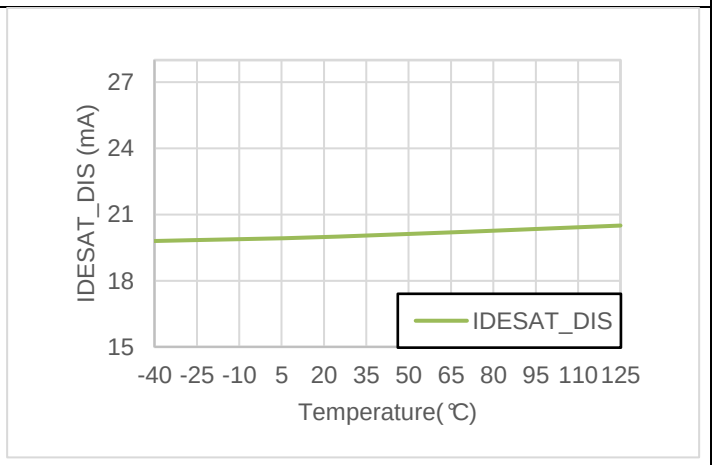


Figure 6.12 IDESAT_DIS vs Temperature

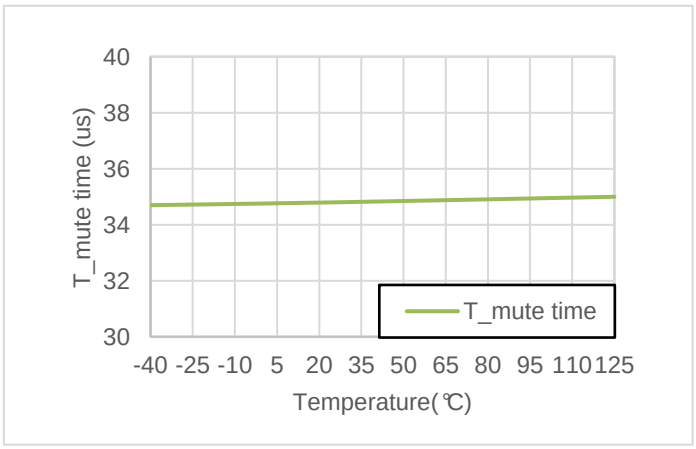


Figure 6.13 T_mute time vs Temperature

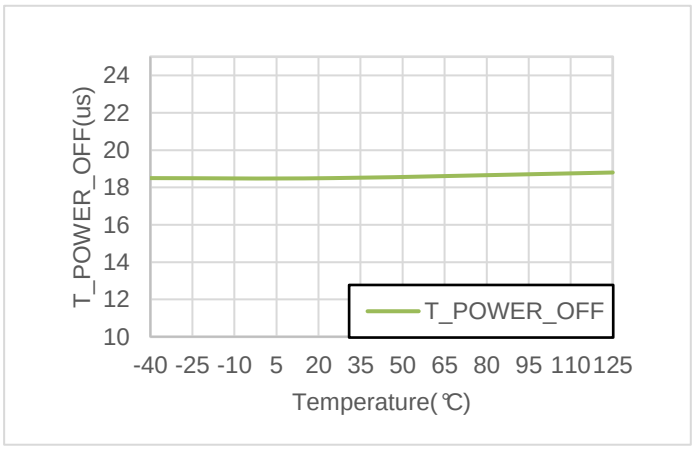


Figure 6.14 T_POWER_OFF vs Temperature

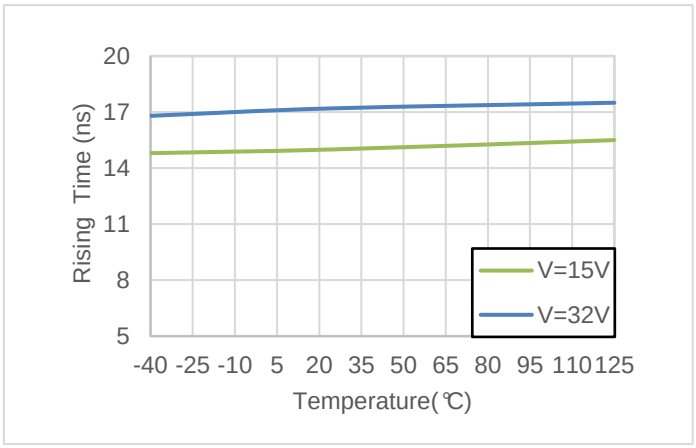


Figure 6.15 T_R vs Temperature

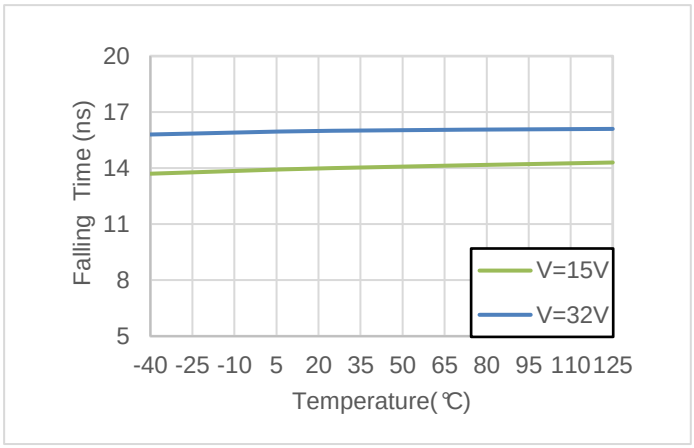


Figure 6.16 T_F vs Temperature

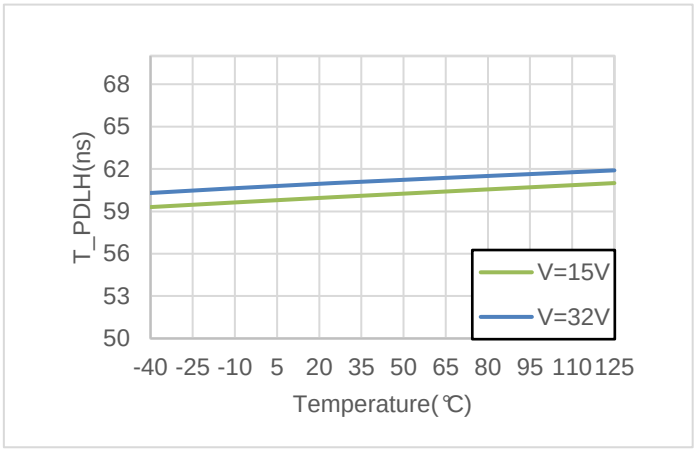


Figure 6.17 T_PDLH vs Temperature

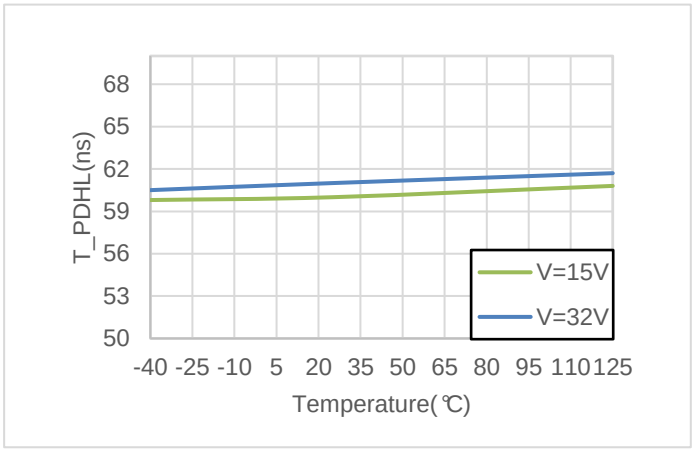


Figure 6.18 T_PDHL vs Temperature

7. Function Description

7.1. Overview

NSD1015xT is a wide supply, single-channel, high speed, low side gate driver for both MOSFET and IGBT. It has capability to deliver 5A sink and source current to the capacitive load along with rail-to-rail output to reduce the Miller effect during MOSFET's switching transition. Fast rise and fall times as well as matched propagation delay of both output channels enable the NSD1015xT be suitable for high frequency power converter application.

To promote the robust of power electronic converter, the overcurrent of power semiconductor should be considered, therefor, the NSD1015xT can provide DESAT protection. The drain-source or collector-emitter voltage is proportional to the current, when this voltage is over the VDESAT_TH, NSD1015xT could immediately to turn off the power semiconductors. The output VOUT would response input Vin again after mute time T_{DESAT_MUTE} until the rise edge on the Vin pin could be detected.

In order to make MCU achieve the fault information from NSD1015xT, the Fault pin is provided, which is open-drain to paralleled connection with multi fault signals easily. The Fault pin could active low when DESAT and TSD occurs.

The NSD1015xT operates with a maximum supply voltage of 32V which is from VDD to GND for NSD1015MT and is from VDD to VEE for NSD1015T. In addition, the maximum negative supply voltage could be -15V for NSD1015T.

The NSD1015xT device is available in SOP8 package with operating temperature range from -40°C to 125°C. In order to prevent over temperature, internal thermal shutdown at 175°C is provided.

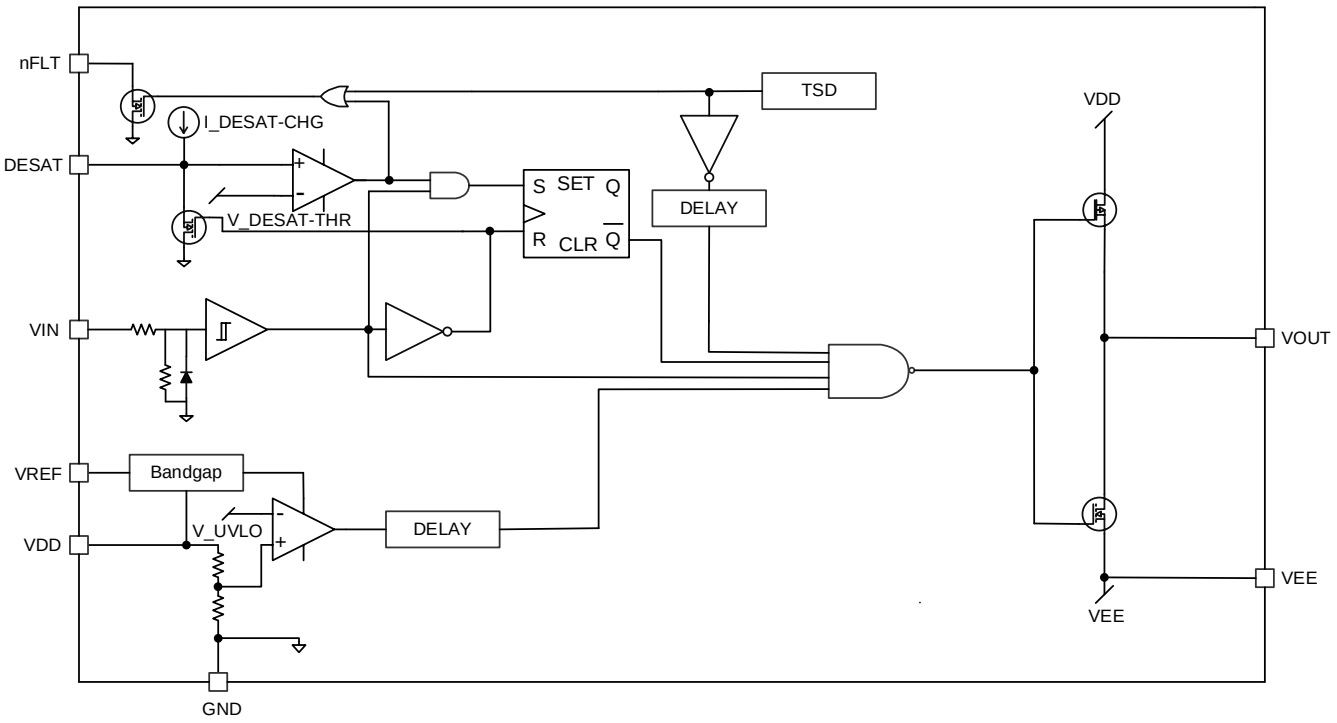


Figure 7.1 NSD1015T Functional Block Diagram

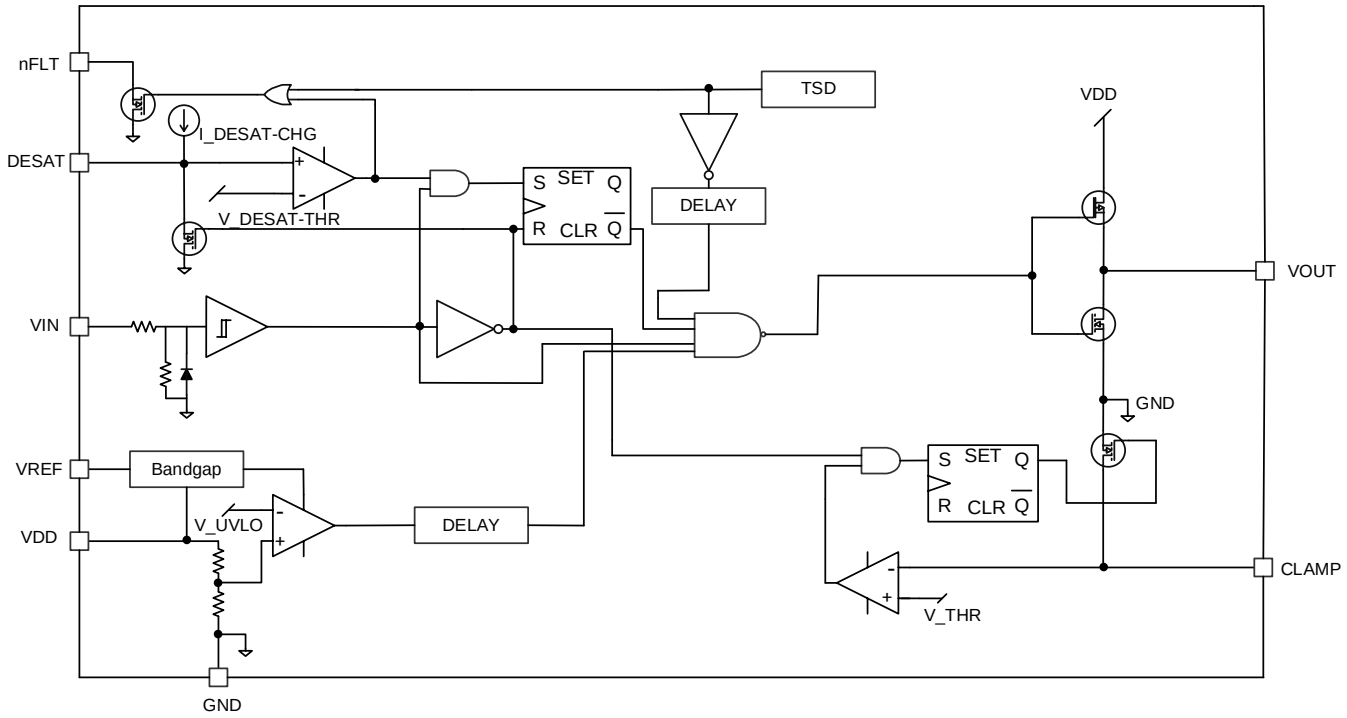


Figure 7.2 NSD1015MT Functional Block Diagram

7.2. Under Voltage Lock Out (UVLO)

NSD1015xT under voltage-lockout rising threshold is typically 13.5V with 1.2V typical hysteresis. This hysteresis prevents output bouncing when low VDD supply voltage have noise from power supply. It also prevents sags in the VDD cause by sudden increase in VDD current while system commences switching. When VDD is below the UVLO threshold the circuit holds the outputs low regardless of the status of the inputs.

7.3. Input and Output Logic Table

The input of NSD1015xT is compatible to both TTL and CMOS logic threshold that is independent of the supply voltage. The typical value of high input threshold (V_{INH} =3.9V) whereas the low threshold (V_{INL} =1.0V). NSD1015xT also feature tight control of the input pin threshold voltage levels which ease system design consideration and ensure stable operation across temperature.

Table 7.1 NSD1015xT Device Logic

VIN	*UVLO*	*DESAT*	*Internal TSD*	*VOUT*	*nFLT*
H	Inactive	L	Inactive	H	Open drain
L	Inactive	L	Inactive	L	Open drain
Any	Inactive	H	Any	L	L
Any	Inactive	Any	Active	L	L
Any	Active	Any	Inactive	L	Open drain

7.4. DESAT Protection

Desaturation protection is used to prevent the power transistor from short circuit. The DESAT pin has a typical 6.5V threshold, which means the output will be driven low if DESAT pin reaches 6.5V. By default, the DESAT pin is pulled down by internal MOSFET. The internal 240μA current source is designed to work only when the output is high level. There is a 150ns(typ) leading edge blanking time to filter the overshoot when the external power transistor is turned on. The current source begins

to charge after the internal leading-edge blanking time. Figure 7.3 shows the DESAT protection diagram. Figure 7.4 shows the DESAT protection timing diagram.

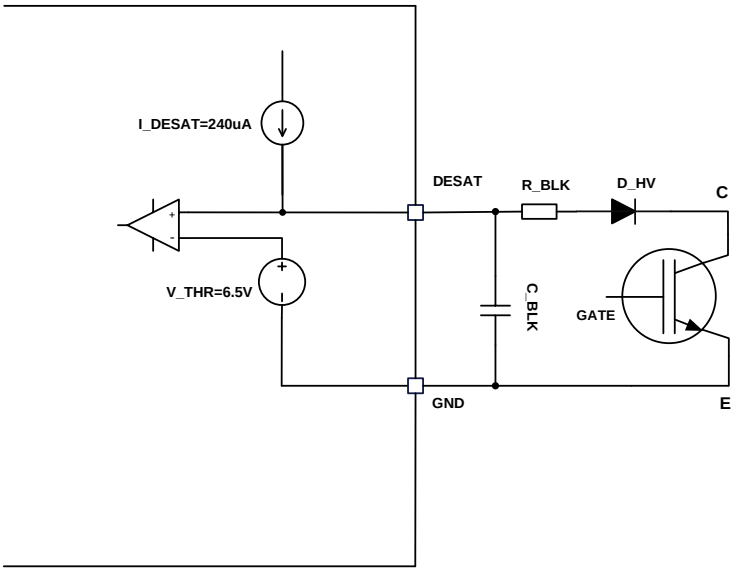


Figure 7.3 DESAT Protection Diagram

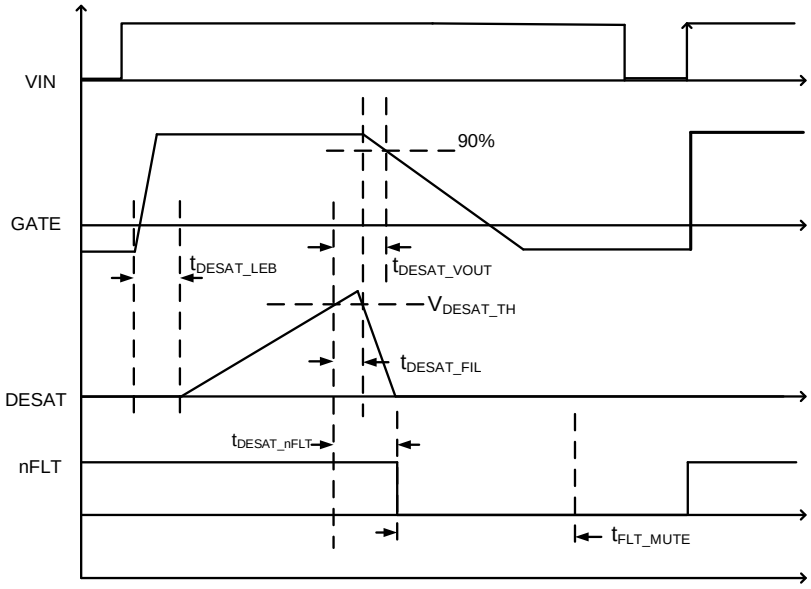


Figure 7.4 DESAT Protected timing Diagram

7.5. Active Miller Clamp Protection

Active miller clamp is used to prevent false turn on. After the external power transistor is turned off, the opposite side is turned on. The voltage of the drain-source or collector-emitter rises instantly. The dv/dt will cause a high current on miller parasitic capacitor. The voltage drops on the gate resistor possibly turn on the external power transistor unintentionally, which will cause a catastrophic damage. To deal with that, NSD1015MT is equipped with a miller clamp pin. The clamp pin detects the gate voltage of IGBT or MOSFET. When the gate voltage is decreasing and reaches the VCLAMP_TH, the clamp pin will be pulled down by the internal MOSFET, providing a low impedance path to avoid the false turn on.

7.6. VREF

The VREF pin of the NSD1015xT has the ability to supply a voltage of 5V. This pin for external bypassing and for powering low bias circuits (such as digital isolators). A capacitor of 1.0uF surface mount ceramic should be placed as close as possible to the VREF-GND pins.

7.7. FAULT Report

The nFLT pin of NSD1015xT is used to report a warning signal if the fault is detected on DESAT and TSD. If the fault occurs, the nFLT pin will be pulled down and held in low state for a mute time. During the mute time, NSD1015xT ignores any reset signal. After that, the nFLT pin will be reset to high level status if the reset signal is checked.

7.8. TSD Protection

The NSD1015xT device has the function of thermal protection. The operating range of the device is -40°C ~125°C When the device temperature reaches 175°C, the pin of the nFLT is pulled down, making the output low.

8. Application Note

8.1. Typical Application Circuit

The following is a typical application diagram of NSD1015xT.During most half-bridge application, the voltage between gate and source of the low-side power semiconductor would have positive spike when the up-side power semiconductor turns on. So, NSD1015xT provides two solutions to overcome above problem, the first one is that NSD1015T provides negative gate bias voltage, and the second one is that NSD1015MT provides miller clamp function. Both above solutions could effectively to prevent the misleading turning on. For NSD1015T, the negative voltage is recommended to be not below -15V. For NSD1015MT, although it only has positive power-supply ability, the miller clamp is provided to prevent the gate-source voltage spike. When the voltage positive spike is over the V_{CLAMP_TH}, the miller clamp would be triggered to make the VOUT voltage be below V_{CLAMP}.

In most isolation application, the NSD1015xT could work with digital isolation chips to replace the iso-driver IC solution, which could achieve the low-cost benefit. During above low-cost solution, the additional power supply for second side is necessary. Fortunately, the 5.0V reference with typical source current 20mA is provided by NSD1015xT. It is helpful to power supply design.

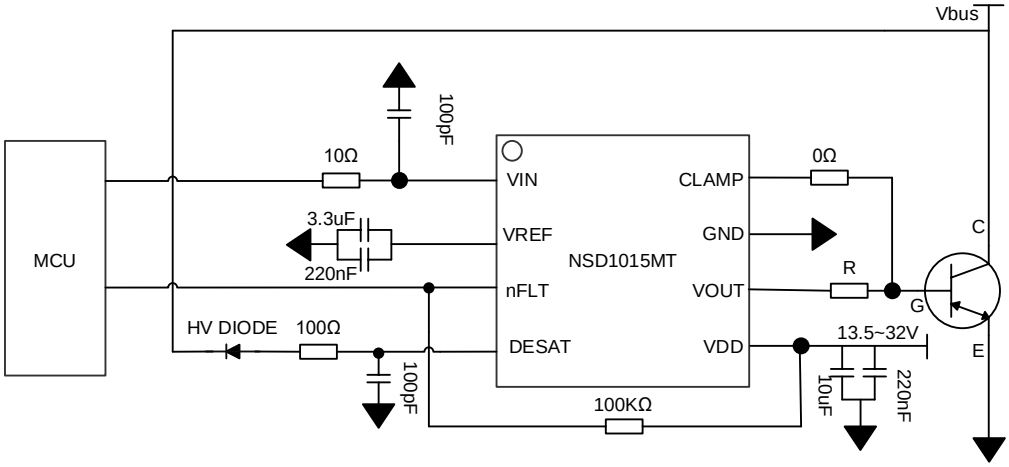


Figure 8.1 NSD1015MT Simplified Application Schematic

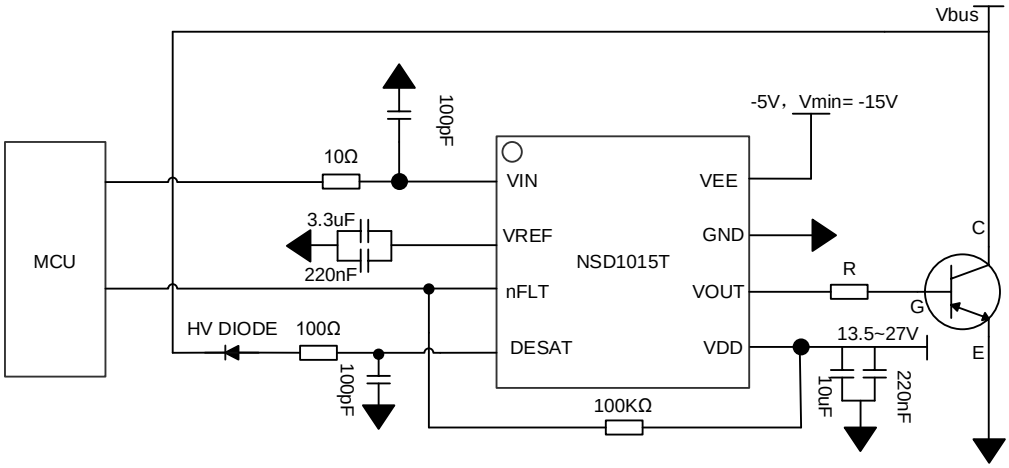
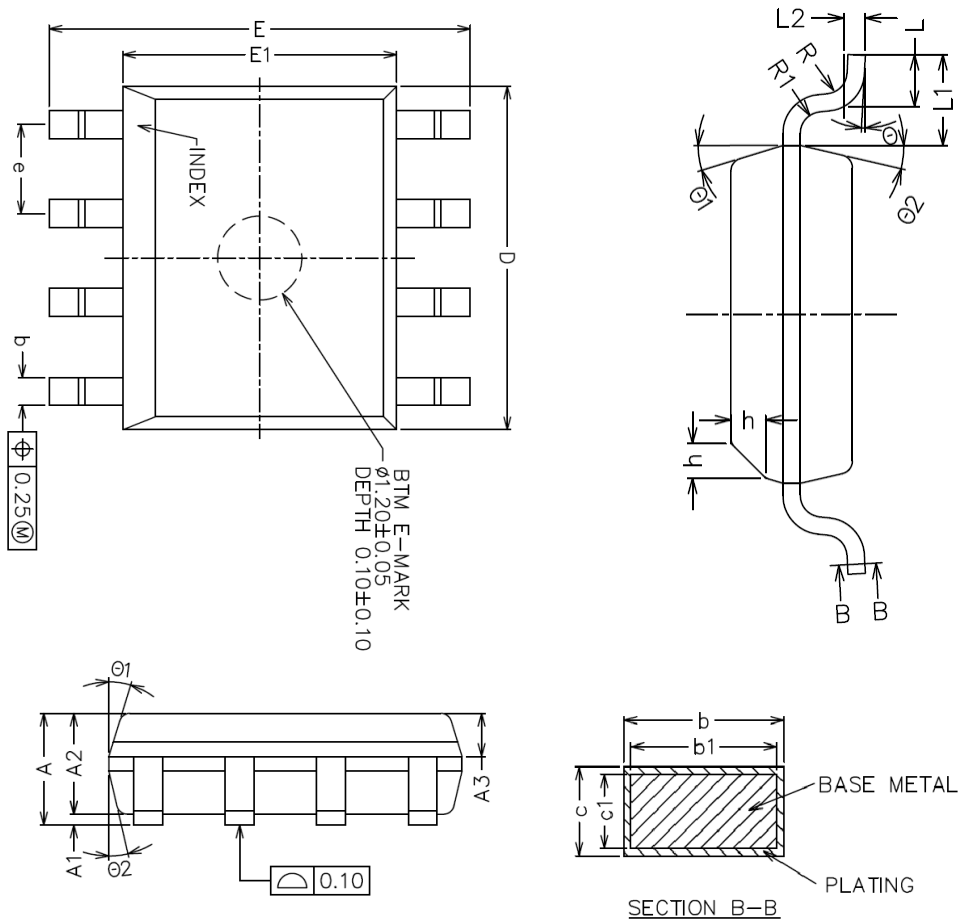


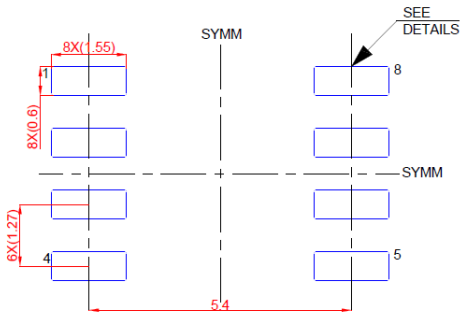
Figure 8.2 NSD1015T Simplified Application Schematic

9. Package information

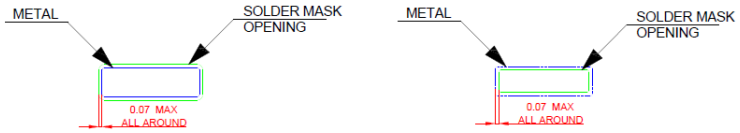


SYMBOL	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.05	–	0.25
A2	1.30	1.40	1.50
A3	0.50	0.60	0.70
b	0.38	–	0.47
b1	0.37	0.40	0.43
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.17	1.27	1.37
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
Θ	0°	–	8°
Θ1	15°	17°	19°
Θ2	11°	13°	15°

Figure 9.1 SOP8 Package Shape and Dimension



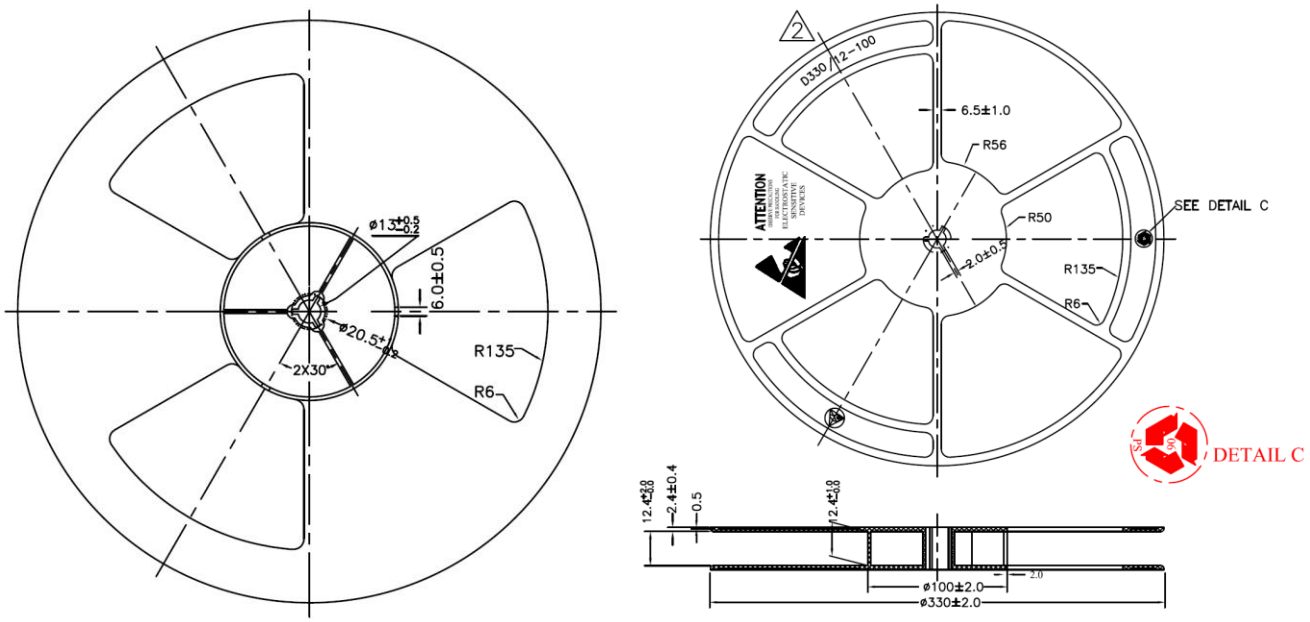
LAND PATTERN EXAMPLE(mm)



SOLDER MASK DETAILS

Figure 9.2 SOP8 Package Board Layout Example

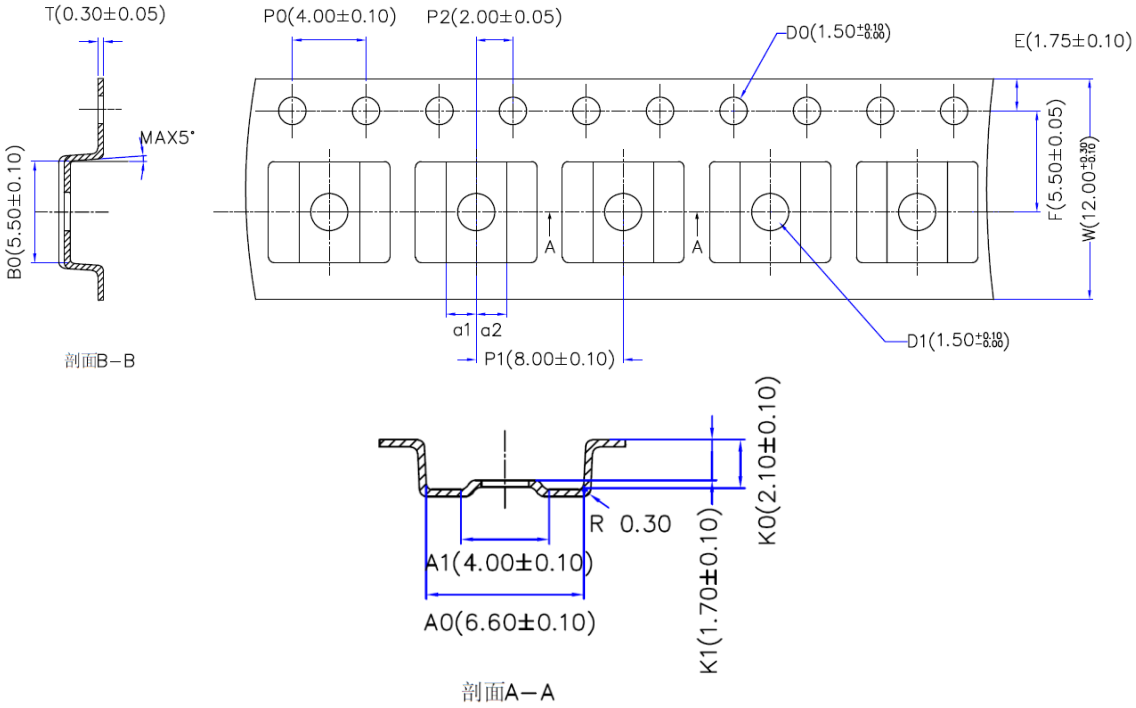
10.Tape and Reel Information



NOTES：

1. Material: Polystyrene (black);
2. Flatness: Maximum allowable 3mm;
3. All dimensions are in millimeters;
4. Surface resistance:10^5 to 10^{11} OHMS/SQ;
5. All unlabeled tolerances ±0.25；

Figure 10.1 Reel Information



NOTES：

1. ALL DIMS IN MM;
2. MATERIAL: BLACK CONDUCTIVE PS;
3. The other tolerance not indicated are ±0.10mm;
4. 10 sprocket hole pitch cumulative tolerance ±0.20mm;
5. Carrier camber is within 1mm in 250mm;
6. There must not be foreign body adhesion and the state of the surface must be excellent;
7. Surface resistance 1×10E5≤Rs < 1×10E9 OHMS;

Figure 10.2 Tape Information

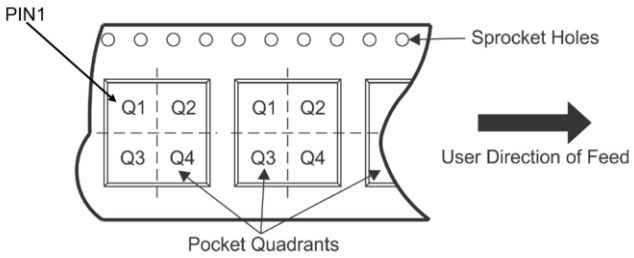


Figure 10.3 Quadrant Designation for Pin1 Orientation in Tape

11.Ordering Information

Part No.	*Temperature*	*Qualification*	*Package Type*	*MSL*	*SPQ*
NSD1015T-DSPR	-40 to 125 °C	Industrial	SOP8	3	2500
NSD1015MT-DSPR	-40 to 125 °C	Industrial	SOP8	3	2500

12.Revision History

Revision	Description	Date
1.0	Initial Version.	2025/02/25

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