NOVOSENSE

NSD10159-DSTAR
Single-Channel, High-Speed, Low-Side Gate Driver
Datasheet (EN) 1.1

Product Overview

The NSD10159 is a single-channel, high-speed gate driver specifically engineered to efficiently drive MOSFET and IGBT power switches. Featuring a symmetrical drive architecture capable of delivering up to 3.5 A source and 4 A sink currents, combined with rail-to-rail drive capability, the device ensures robust and precise switching performance. With an exceptionally low propagation delay of 25 ns (typical), the NSD10159 is optimized for high-speed applications, making it an ideal solution for driving MOSFET and IGBT power switches in demanding power electronics systems.

Key Features

- Offering optimal solution for driving FET and IGBTs
- Wide VDD range from 4.7 V to 32 V
- High peak drive currents: 3.5 A (source) and 4 A (sink)
- Fast propagation delays: 25ns (typical)
- Fast rise and fall times: 9ns and 8ns (typical with 1.8nF load)
- Operation temperature: -40°C ~125°C
- Reach RoHS compliance

Applications

- PTC heaters
- Switch-mode power supplies
- Solar inverters, motor control, UPS
- HEV and EV chargers
- Home appliances
- Renewable energy power conversion
- SiC FET converters

Device Information

Part Number	*Package*	*Body Size*
NSD10159-DSTAR	SOT23-5	2.9mm × 1.6mm

Functional Block Diagrams

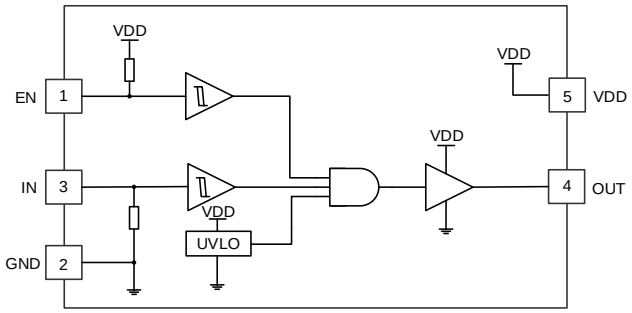


Figure 1. NSD10159 Block Diagram

INDEX

1. Pin Configuration and Functions

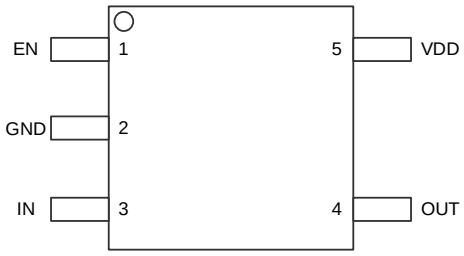


Figure 1.1 NSD10159 Pin Configuration

Table 1.1 NSD10159 Pin Configuration and Description

SYMBOL	*PIN NO.*	*FUNCTION*
EN	1	Enable pin
GND	2	Ground pin
IN	3	Input pin
OUT	4	Driver output
VDD	5	Power supply

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit	Comments
Power Supply Voltage	VDD	-0.3	35	V	
Input and Enable Pins Voltage	V_{IN}, V_{EN}	-10	35	V	
Output Voltage	V_{OUT}	-0.3	VDD+0.3	V	
		-2	VDD+0.3	V	Pulse＜200ns
Junction Temperature	T_J	-40	150	°C	
Storage Temperature	T_{stg}	-40	150	°C	

3. ESD Ratings

		Symbol	Value	Unit
Electrostatic Discharge	Human-body model (HBM), per AEC Q100-002[1)]	V_{ESD_HBM}	±2000	V
	Charged-device model (CDM), per AEC Q100-011	V_{ESD_CDM}	±2000	V

1) ACE Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit	Comments
Power Supply Voltage	VDD	4.7	32	V	
Input Pin Voltage	V_{IN}	-5	32	V	
Enable Pin Voltage	V_{EN}	-5	32	V	

5. Thermal Information

Parameters	Symbol	SOT23-5	Unit
Junction-to-Ambient Thermal Resistance[1)]	$R_{\theta JA}$	168	°C/W
Junction-to-Case(top) Thermal Resistance[1)]	$R_{\theta JC\ (top)}$	102	°C/W

1) Tested using high effective thermal conductivity test board (2S2P) described in JESD51-7.

6. Specifications

6.1. Electrical Characteristics

VDD=12V, TA = -40°C to 125°C, unless otherwise noted, typical values are at TA=25°C.

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Bias Current						
VDD Supply Start-up Current	I_{VDDSTR}	50	100	150	uA	VDD=3.4V, V_{IN} =VDD
		50	100	150	uA	VDD=3.4V, V_{IN} =GND
VDD Supply Quiescent Current	I_{VDDQ}	200	350	500	uA	V_{EN} =VDD, V_{IN} =VDD
		150	300	450	uA	V_{EN} =GND, V_{IN} =GND
VDD Supply Operating Current	I_{VDDO}		4.3		mA	F=200KHz,1.8nF
Under Voltage Lockout (UVLO)						
VDD UVLO Rising Threshold	V_{VDD_ON}	3.8	4.2	4.6	V	
VDD UVLO Falling Threshold	V_{VDD_OFF}	3.5	3.9	4.3	V	
VDD UVLO Hysteresis	V_{VDD_HYS}		0.3		V	
Input Pin Characteristics						
Logic High Input Threshold	V_{IN_H}		2.2	2.6	V	
Logic Low Input Threshold	V_{IN_L}		1.3	1.6	V	
Input Hysteresis Voltage	V_{IN_HYS}		0.9		V	
Input Pull Down Resistance	R_{IN}	200	260	300	KΩ	
Enable Signal High Threshold	V_{EN_H}		2.2	2.6	V	
Enable Signal Low Threshold	V_{EN_L}		1.3	1.6	V	
Enable Signal Hysteresis	V_{EN_HYS}		0.9		V	
Enable Pull Up Resistance	R_{EN}	100	260	300	KΩ	
Output Pin Characteristic						
High Level Output Voltage	VDD - V_{OUT}		165	290	mV	Inject -100mA From Out
Low Level Output Voltage	V_{OUT}		95	180	mV	Inject +100mA From Out
Output Pull-Up Resistance	R_{OUTH}		1.65	2.9	Ω	
Output Pull-Down Resistance	R_{OUTL}		0.95	1.8	Ω	
High Level Peak Output Current[1)]	I_{OUTH}		3.5		A	Load=1uF

Low Level Peak Output Current[1)]	I_{OUTL}		4		A	Load=1uF

1) Not test covered, guaranteed by design.

6.2. Switching Characteristics

VDD=12V, TA = -40°C to 125°C, load=1.8nF, unless otherwise noted, typical values are at TA=25°C.

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Minimum Pulse Width	T_{PWmin}		10	18	ns	
Output Rise Time	T_R		9	15	ns	
Output Fall Time	T_F		8	15	ns	
Propagation Delay	T_{PDLH}	15	25	40	ns	
	T_{PDHL}	15	25	40	ns	
Time to enable the driver once the EN pin is pulled high	$T_{Delay\_ON\_EN}$	15	28	40	ns	
Time to disable the driver once the EN pin is pulled low	$T_{Delay\_OFF\_EN}$	15	28	40	ns	

6.3. Typical Performance Characteristics

VDD=12V, TA = -40°C to 125°C, unless otherwise noted, typical values are at TA=25°C.

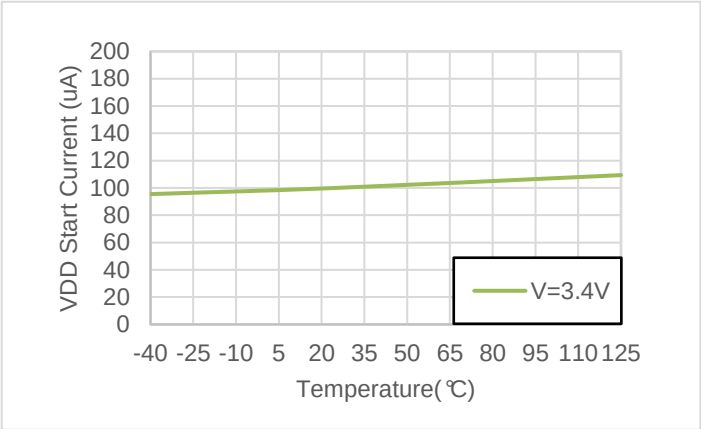


Figure 6.1 VDD(VIN=VDD) Start Current vs Temperature

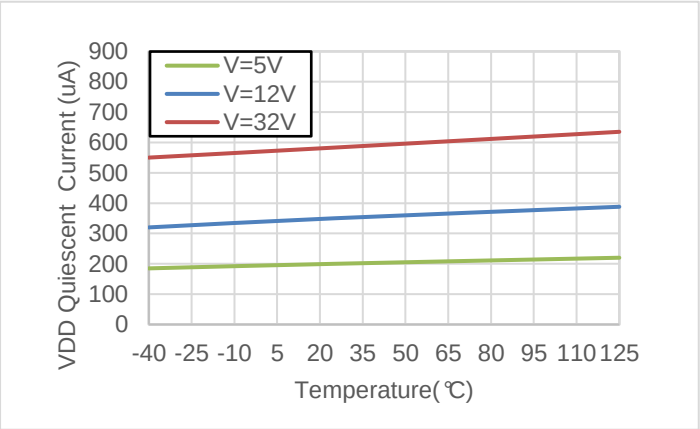


Figure 6.2 VDD(VIN=VDD) Quiescent Current vs Temperature

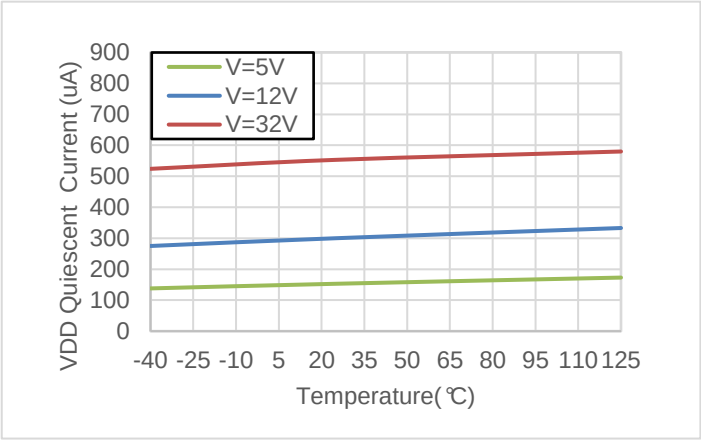


Figure 6.3 VDD(VIN=GND) Quiescent Current vs Temperature

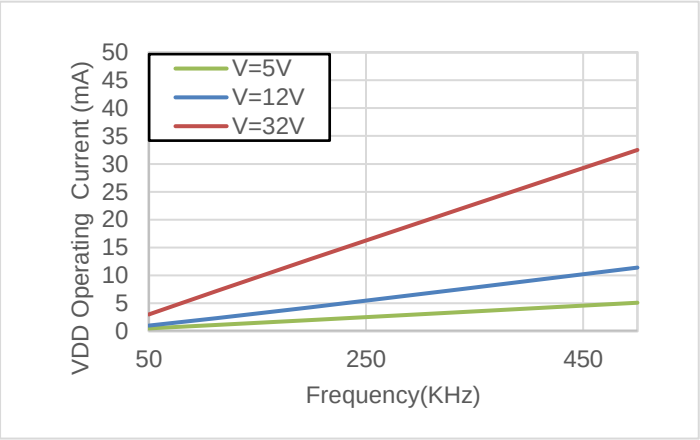


Figure 6.4 VDD Operating Current vs Frequency

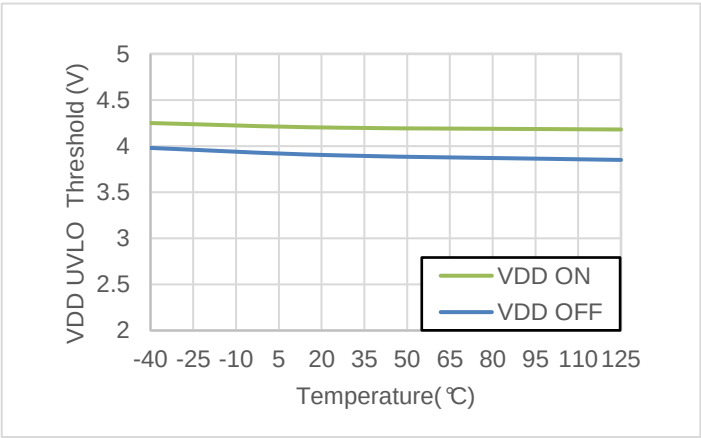


Figure 6.5 VDD UVLO Threshold vs Temperature

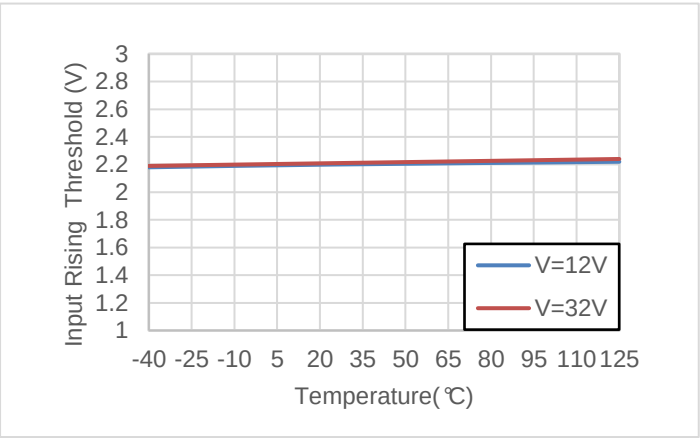


Figure 6.6 Input Rising vs Temperature

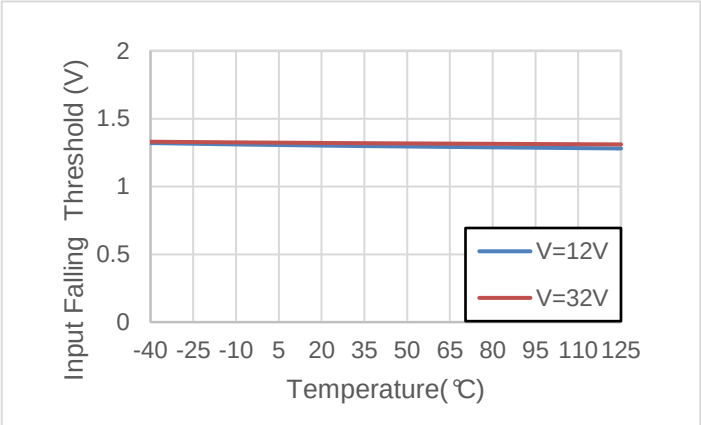


Figure 6.7 Input Falling vs Temperature

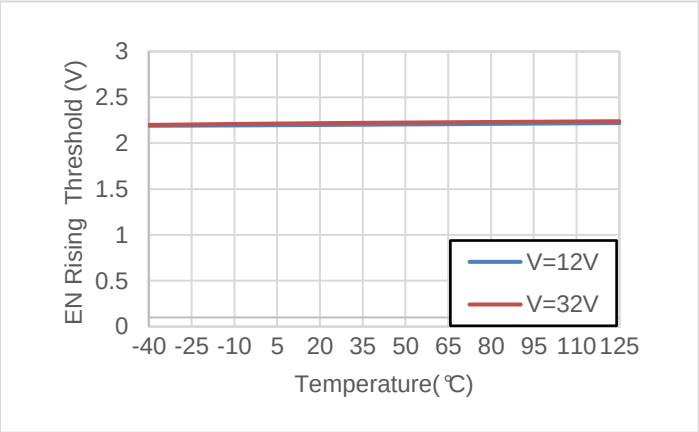


Figure 6.8 EN Rising vs Temperature

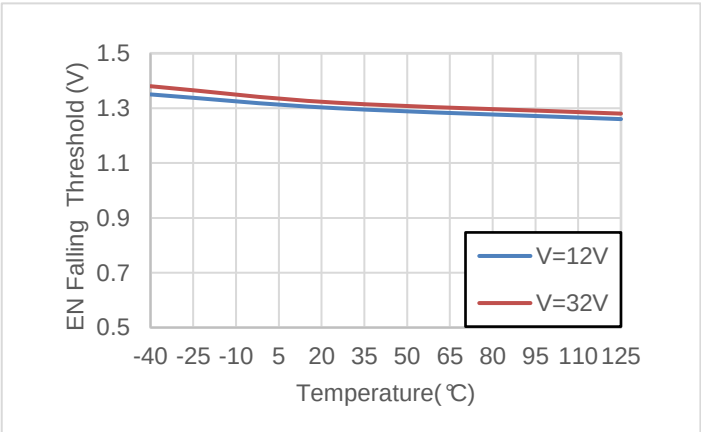


Figure 6.9 EN Falling vs Temperature

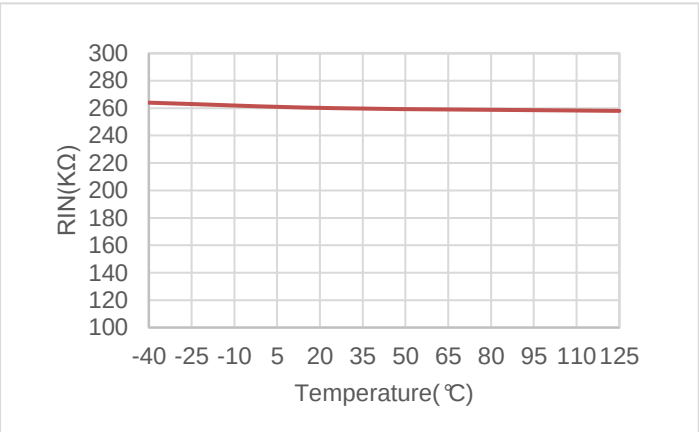


Figure 6.10 RIN vs Temperature

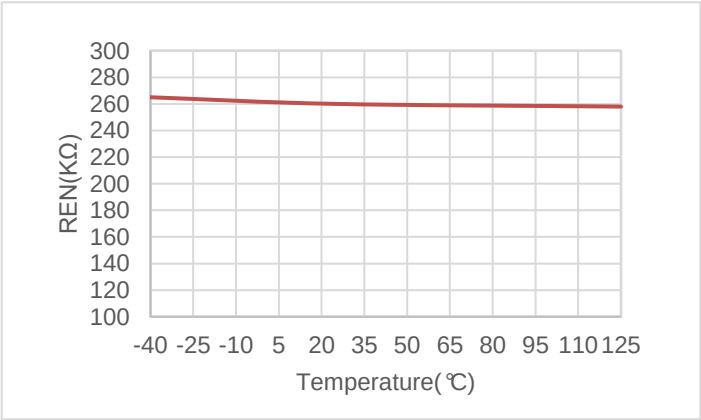


Figure 6.11 REN vs Temperature

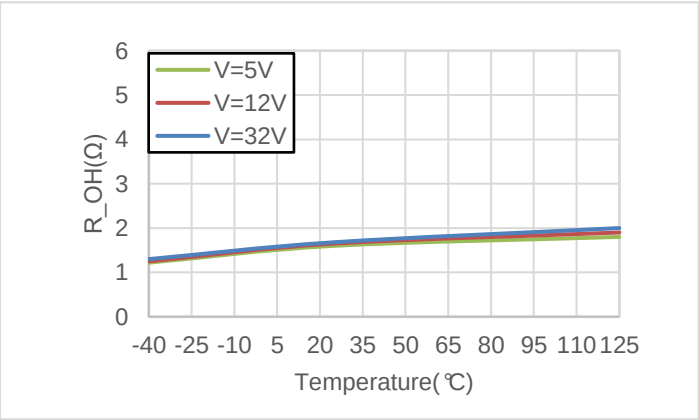


Figure 6.12 R_OH vs Temperature

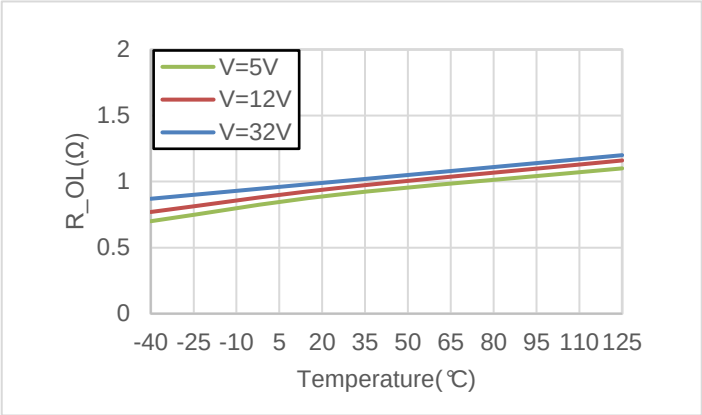


Figure 6.13 R_OL vs Temperature

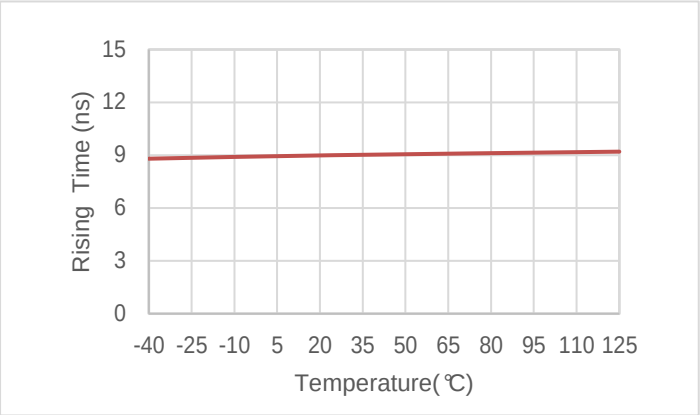


Figure 6.14 OUTPUT Rising vs Temperature

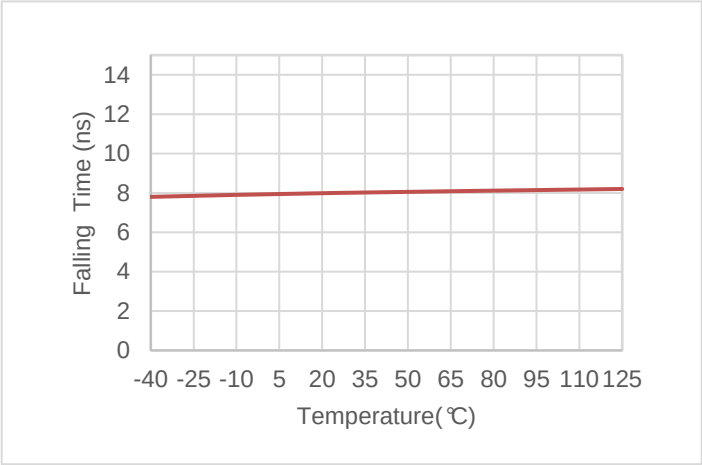


Figure 6.15 OUTPUT Falling vs Temperature

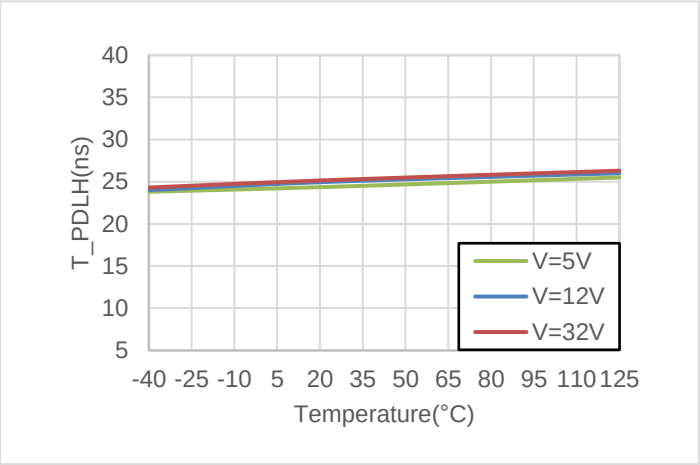


Figure 6.16 T_PDLH vs Temperature

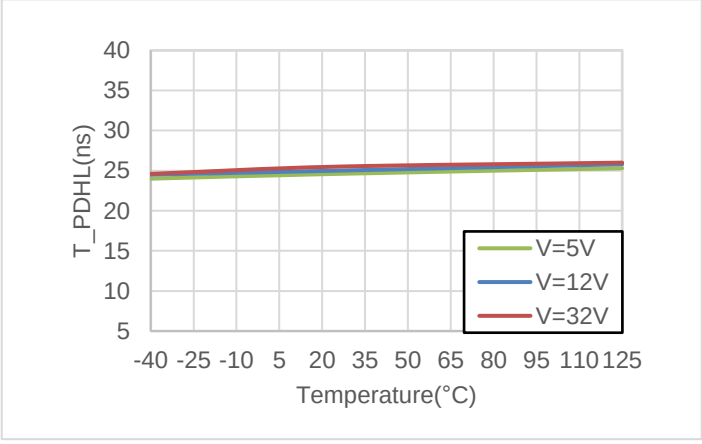


Figure 6.17 T_PDHL vs Temperature

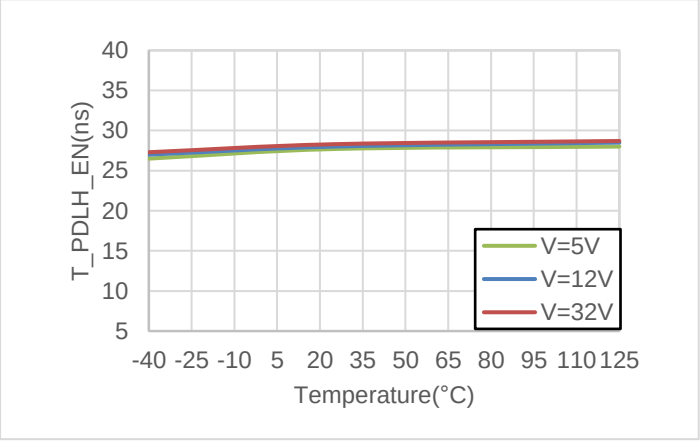


Figure 6.18 T_PDLH_EN vs Temperature

7. Function Description

7.1. Overview

NSD10159 is a single-channel, high-speed, gate driver capable of effectively driving MOSFET and IGBT power switches by up to 3.5A source and 4A sink (symmetrical drive) peak current. The driver has rail-to-rail drive capability and extremely small propagation delay, typically 25ns.

The input pin of NSD10159 device is based on TTL and CMOS compatible input threshold logic. With typical high threshold = 2.2 V and typical low threshold = 1.3 V, the logic level thresholds can be conveniently driven with PWM control signals derived from 3.3V or 5V logic. Wider hysteresis (typically 0.9V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. This device also features tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The device features an important safety function wherein, whenever the input pin is in a floating condition, the output is held in the low state. This is achieved using pull-up or pull-down resistors on the input pins as shown in the block diagrams.

7.2. Enable Function

The Enable (EN) pin of the NSD10159 has an internal pull-up resistor to an internal reference voltage so leaving Enable floating turns on the driver and allows it to send output signals properly. If desired, the Enable can also be driven by low-voltage logic to enable and disable the driver. EN pin is recommended to pull up to VDD.

7.3. Input Stage

The input pin threshold voltage level of the NSD10159 is influenced by the bias voltage applied to the VDD pin. When the VDD supply voltage is greater than the threshold and less than 7V, the threshold voltage of VIN is linearly related to the VDD voltage. when the VDD supply voltage is greater than 7V and less than or equal to the recommended maximum value, the threshold voltage of VIN remains constant and is not affected by the VDD voltage. The reason for the threshold being affected is the internal use of a Schmitt trigger. In addition, the input threshold of the chip has a relatively wide hysteresis, which enables the chip to have good noise immunity.

7.4. Output Stage

The output of NSD10159 is composed of P-Channel MOSFET and N-Channel MOSFET. The P-Channel MOSFET has a low impedance on-resistance of 1.65Ω (typ), and the N-Channel MOSFET also has a low impedance on-resistance of 0.95Ω (TYP). The NSD10159 can deliver 3.5A source, and up to 4A sink at VDD=12V. Strong sink capability results in a very low pull-down impedance in the driver output stage which boosts immunity against the parasitic Miller turn on (high slew rate dV/dt turn on) effect that is seen in both IGBT and FET power switches.

8. Application Note

8.1. Application Information

High-current gate driver devices are required in switching power applications for a variety of reasons. To enable fast switching of power devices and reduce associated switching power losses, a powerful gate driver can be employed between the PWM output of controllers or signal isolation devices and the gates of the power semiconductor devices. Further, gate drivers are indispensable when sometimes it is just not feasible to have the PWM controller directly drive the gates of the switching devices. The situation will be often encountered because the PWM signal from a digital controller or signal isolation device is often a 3.3V or 5V logic signal which is not capable of effectively turning on a power switch. A level-shifting circuitry is needed to boost the logic-level signal to the gate-drive voltage in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar, (or P-N-channel MOSFET), transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate for this because they lack level-shifting capability and low-drive voltage protection. Gate drivers effectively combine both the level-shifting, buffer drive and UVLO functions. Gate drivers also find other needs such as minimizing the effect of switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself.

The NSD10159 is very flexible in this role with a strong current drive capability and wide supply voltage range up to 32 V. This allows the driver to be used in 12V Si MOSFET applications, 20V and -5V (relative to Source) SiC FET applications, 15V and -15V (relative to Emitter) IGBT applications and many others. As a single channel driver, the NSD10159 can be used as a low-side or high-side driver. To use as a low-side driver, the switch ground is usually the system ground so it can be connected directly to the gate driver. These requirements coupled with the need for low propagation delays and availability in compact, low inductance packages with good thermal capability makes gate driver devices such as the NSD10159 extremely important components in switching power combining benefits of high-performance, low cost, component count and board space reduction and simplified system design.

8.2. Typical Application Circuit

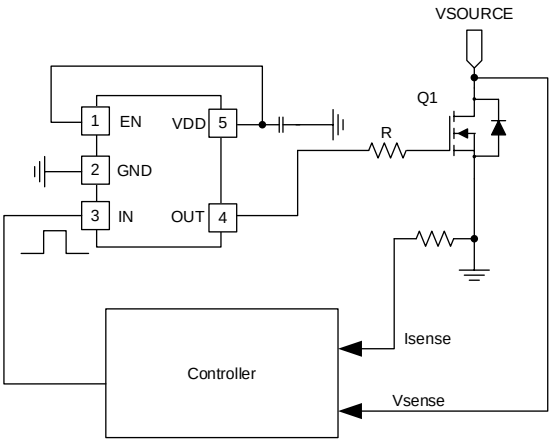
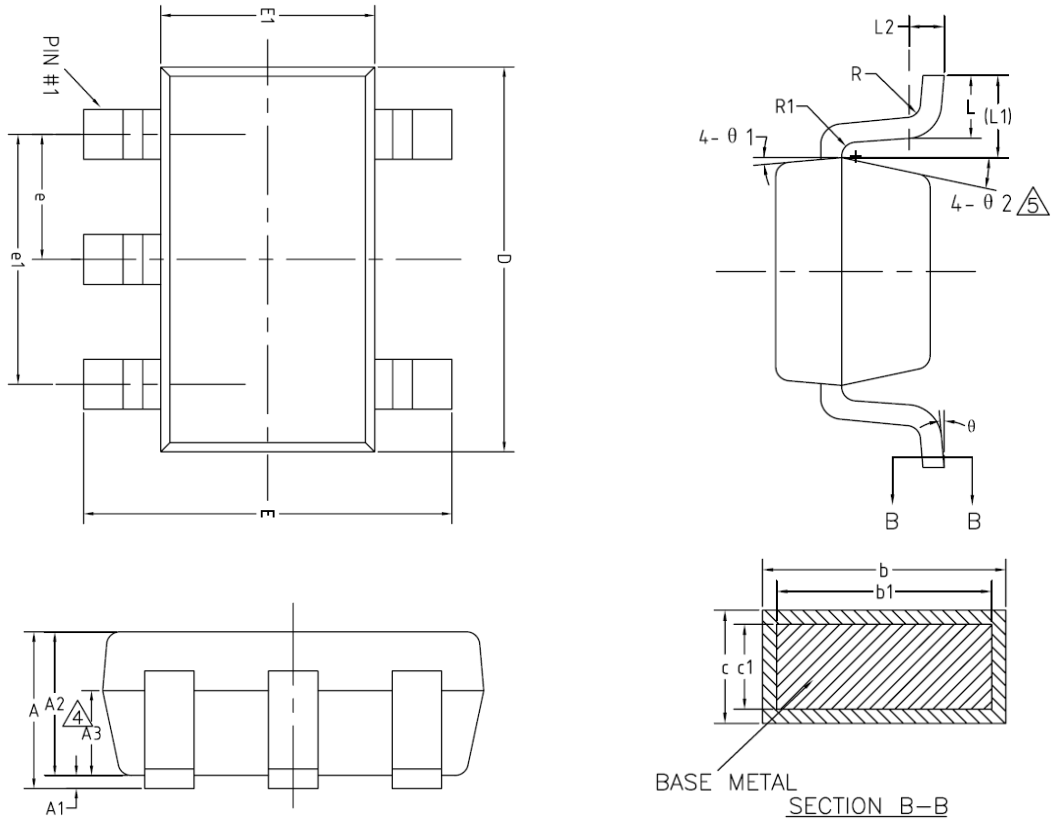


Figure 8.1 NSD10159 typical application circuit

9. Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

	SYMBOL	MIN	NOM	MAX
	A	–	–	1.25
3	A1	0	–	0.15
	A2	1.00	1.10	1.20
	A3	0.60	0.65	0.70
	b	0.36	–	0.50
	b1	0.36	0.38	0.45
	c	0.14	–	0.20
	c1	0.14	0.15	0.16
	D	2.826	2.926	3.026
	E	2.60	2.80	3.00
	E1	1.526	1.626	1.726
5	e	0.90	0.95	1.00
5	e1	1.80	1.90	2.00
	L	0.35	0.45	0.60
	L1	0.59REF		
	L2	0.25BSC		
	R	0.10	–	–
	R1	0.10	–	0.25
	θ	0°	–	8°
	θ 1	3°	5°	7°
5	θ 2	6°	–	14°

Figure 9.1 SOT23-5 Package Shape and Dimension

10. Tape and Reel Information

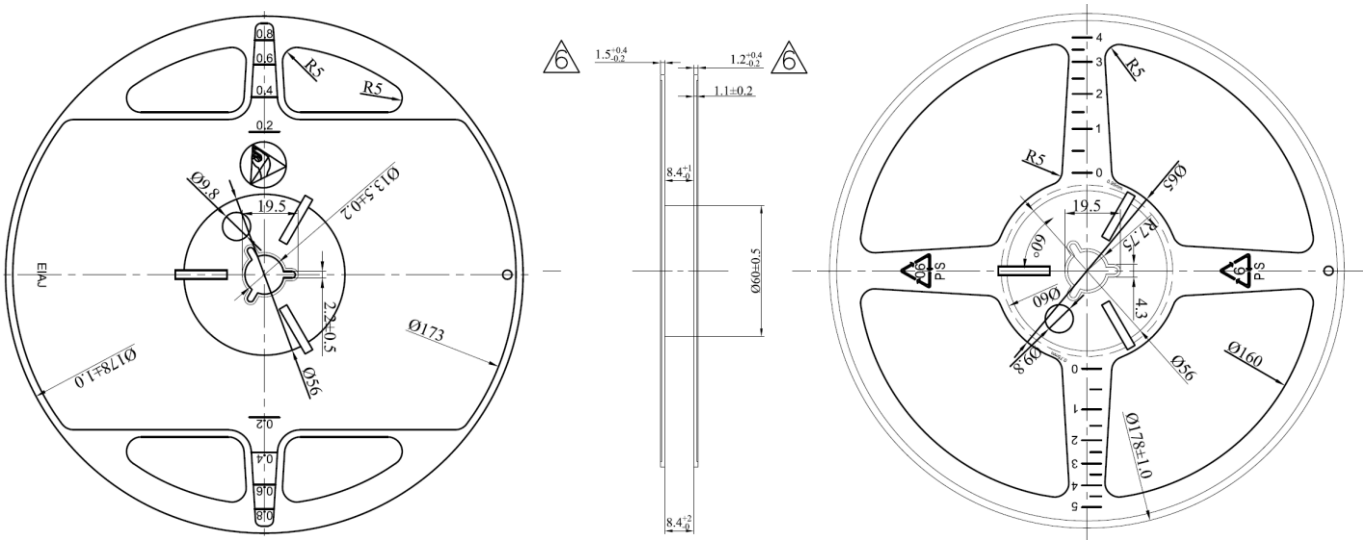
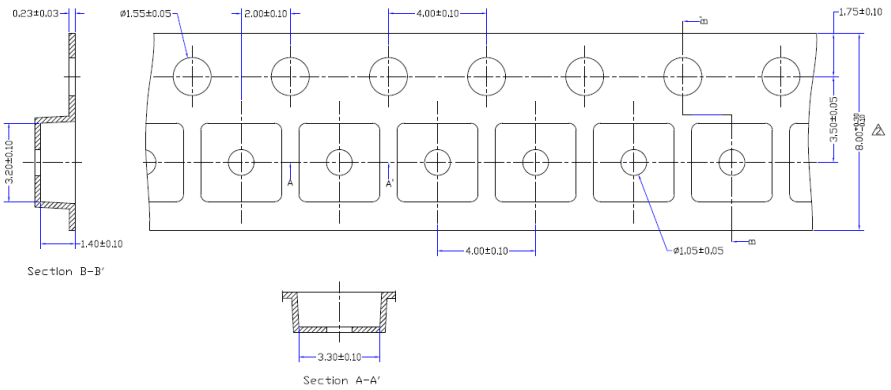


Figure 10.1 Reel Information



NOTES：

1. MATERIAL: CONDUCTIVE PS
2. ALL DIMS IN MM
3. There must not be foreign body adhesion and the state of the surface must be excellent
4. A permissible difference of the accumulation pitch of the sending hole is assumed to be ±0.2 up to 10 pitches
5. Ø560 PAPER-Reel,255000pockets(1020m)
6. Surface resistance 1×10E5~1×10E9 OHMS/SQ

Figure 10.2 Tape Information

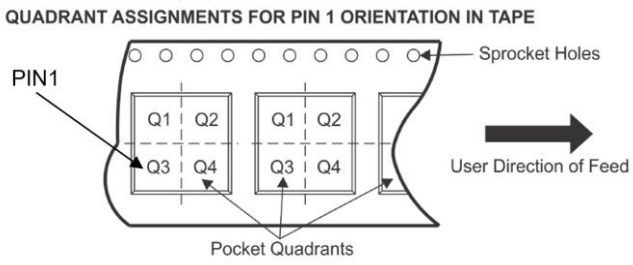


Figure 10.3 Quadrant Designation for Pin1 Orientation in Tape

11. Ordering Information

Part No.	Temperature	Qualification	Package Type	MSL	SPQ
NSD10159-DSTAR	-40 to 125°C	Industrial	SOT23-5	3	3000

12. Revision History

Revision	Description	Date
1.0	Initial Version.	2025/02/25
1.1	1、Add RoHS Standard; 2、Change Thermal Information; 3、Change parameters Measurement Information;	2025/04/11

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