NOVOSENSE

NSD1012C
Single channel low side driver with OCP function
Datasheet (EN) 1.0

Product Overview

NSD1012C is a low-side gate driver capable of delivering 3A source and 4A sink peak currents to drive power MOSFETs or IGBTs. The logic input is compatible with TTL and CMOS output. The NSD1012C has OCP pin to provide over current protection with negative voltage detected across switching current sensing resistor. The NSD1012C has a multiple purpose pin EN/nFLT which serves as both an Enable (EN) input to activate the output and a Fault (nFLT) output by being pulled low by an internal switch. The fault recovery time can be programmable by time constant set of resistance and capacitance connected to EN/nFLT pin. Internal VDD circuitry provides an under−voltage lockout function by holding the output low until the supply voltage reaches the operating range. The NSD1012C is available in SOT23-6 package with operating temperature range from -40°C to 125°C.

Key Features

- Over-current detection threshold: -0.242V negative voltage
- Single pin for fault output and enable control
- Programmable fault clear time
- 3.3 V, 5 V and 15 V input logic compatible
- Under-voltage lockout for VDD
- OCP pin withstands -10V DC voltage
- 3.5 kV ESD HBM
- RoHS compliant
- Operation temperature: -40 °C~125 °C

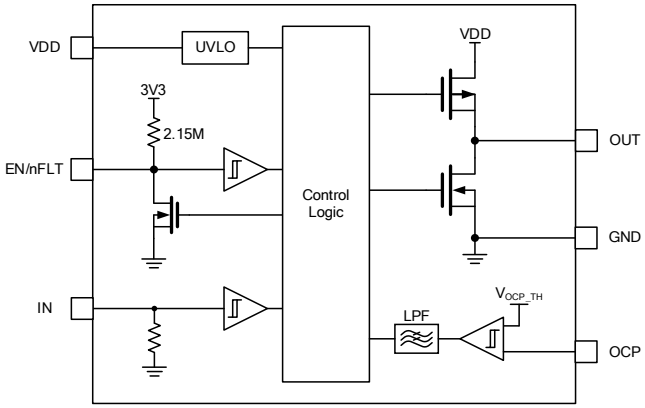
Applications

- General purpose low-side gate driver for single-ended topologies
- Switch−mode power supplies
- Industrial applications
- Home appliances
- Air conditioner
- Motor control

Device Information

Part Number	Package	Body Size
NSD1012C-DSTCR	SOT23-6	2.90 × 1.60mm

Functional Block Diagrams



NSD1012C Block Diagram

INDEX

1. Pin Configuration and Functions

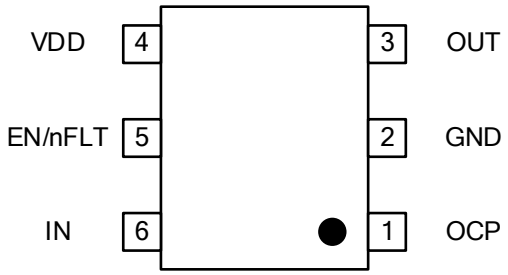


Figure 1.1 SOT23-6 Package

NSD1012C PIN NO.	*SYMBOL*	*FUNCTION*
1	OCP	Current sensor input
2	GND	Ground
3	OUT	Gate drive output
4	VDD	Supply voltage
5	EN/nFLT	Enable control and fault report pin: 1. Used as an enable pin: turn off the drive output when it is low. 2. Used as a fault report pin: when an over-current or under-voltage lockout event occurs, the pin outputs a low level. This pin requires an external pull-up resistor and capacitor for configuration. The resistor and capacitor determine the fault clear time.
6	IN	Logic input for gate driver output (OUT)

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
Maximum Supply Voltage	V_{DD}	-0.3	25	V
Maximum Output Voltage	V_{OUT}	-0.3	VDD+0.3	V
Maximum Voltage at OCP Pin	V_{OCP}	-10	VDD+0.3	V
Maximum Voltage at EN/nFLT Pin	$V_{EN/nFLT}$	-0.3	VDD+0.3	V
Maximum Input Voltage	V_{IN}	-10	VDD+0.3	V
Package Power Dissipation @ TA ⩽ 25°C	P_D		0.5	W
Thermal Resistance, Junction to Ambient	Rth_{JA}		250	°C/W
Junction Temperature	T_J	-40	150	°C
Storage Temperature	T_S	-55	150	°C
Lead Temperature (soldering, 10 seconds)	T_L		260	°C

3. ESD Ratings

Ratings		Value	Unit
Electrostatic Discharge	Human Body Model (HBM), per AEC-Q100-002-RevD	±3.5	kV
	Charged Device Model (CDM), per AEC-Q100-011-RevB	±2	kV

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
Power Supply Voltage	V_{DD}	12.7	20	V
Output Voltage	V_{OUT}	0	V_{DD}	V
Voltage at OCP Pin	V_{OCP}	-5	V_{DD}	V
Voltage at EN/nFLT Pin	$V_{EN/nFLT}$	0	V_{DD}	V
Input Voltage	V_{IN}	-5	V_{DD}	V
Ambient Temperature	T_A	-40	125	°C

5. Specifications

5.1. Electrical Characteristics

Parameters	Symbol	Min	Typ	Max	Unit	Test Conditions
VDD Quiescent Current	I_{VDD_Q}		500	700	uA	VDD=15V, VIN=0V or 5V
UVLO+	V_{UVLO+}	11.2	11.9	12.5	V	
UVLO-	V_{UVLO-}	10.3	11.0	11.6	V	
UVLOH	V_{UVH}		0.9		V	
V_{IN} High Threshold Voltage	V_{INH}	1.9	2.1	2.3	V	
V_{IN} Low Threshold Voltage	V_{INL}	0.8	1.0	1.2	V	
V_{EN} High Threshold Voltage	V_{ENH}	1.9	2.1	2.3	V	
V_{EN} Low Threshold Voltage	V_{ENL}	0.8	1.0	1.2	V	
Logic High Bias Current	I_{IN+}	35	50	70	uA	VDD = 15V, VIN = 5V
Logic Low Bias Current	I_{IN-}		-1		uA	VDD = 15V, VIN = 0V
Output Low Voltage	V_{OL}		15	50	mV	I_O = 20mA
Output High Voltage	$V_{DD} - V_{OH}$		25	60	mV	I_O = 20mA
Peak Source Current	I_{OH}	2	3		A	VDD = 15V
Peak Sink Current	I_{OL}	3	4		A	VDD = 15V
OCP Threshold Voltage	V_{OCP_TH}	-258	-242	-225	mV	
EN/nFLT Pull Down Sinking Current	I_{N_FLT}	17			mA	
EN/nFLT Leakage Current	$I_{N\_FLT\_LEAK}$		-2		uA	VDD = 15V
Active Shutdown Voltage	V_{ACTSD}		2.2	2.6	V	VDD = Floating, I_O = 260mA

5.2. Switching Characteristics

VDD=15 V, Ta=25 °C

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Propagation Delay(Turn-On)	t_{on}		50	60	ns	
Propagation Delay(Turn-Off)	t_{off}		50	60	ns	
Output Rise Time	t_r		15		ns	R_g = 0Ω, C_{load} = 1nF
Output Fall Time	t_f		10		ns	R_g = 0Ω, C_{load} = 1nF
Minimum Input Filter	$t_{\min\_p}$		24		ns	
Disable Propagation Delay	t_{DISA}		50	60	ns	V_{EN} Pulse = 5V
OCP to V_{out} Low Propagation Delay	t_{OCPDEL}		240	310	ns	V_{ocp} Pulse = -0.5V

OCP to nFLT Active Propagation Delay	t_{OCPFLT}		220	290	ns	V_{ocp} Pulse = -0.5V
FAULT Clear Time(1)	t_{FLTC}		117		us	R_{FLTC} = 1MR, C_{FLTC} = 150pF
OCP Blanking Time(2)	t_{BLK}	100	150	200	ns	R_{FLT} = 0R,C_{FLTC} = NC V_{ocp} Pulse = -0.5V
VDD Supply UVLO Filter Time	t_{VDDUV}		2		us	

(1)Parameter depends on R_{FLTC} and C_{FLTC}, not tested in production;

(2)Parameter verified by design, not tested in production;

5.3. Typical Performance Characteristics

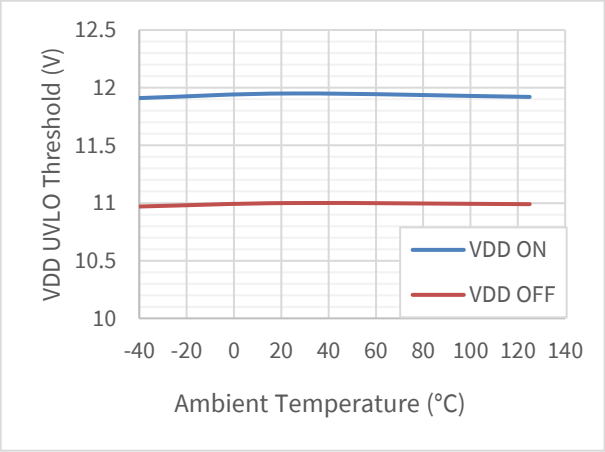


Figure 5.1 VDD UVLO Threshold vs Temperature

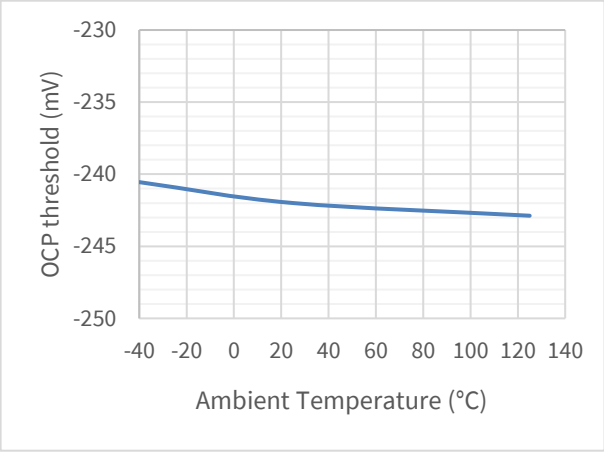


Figure 5.2 OCP Threshold vs. Temperature

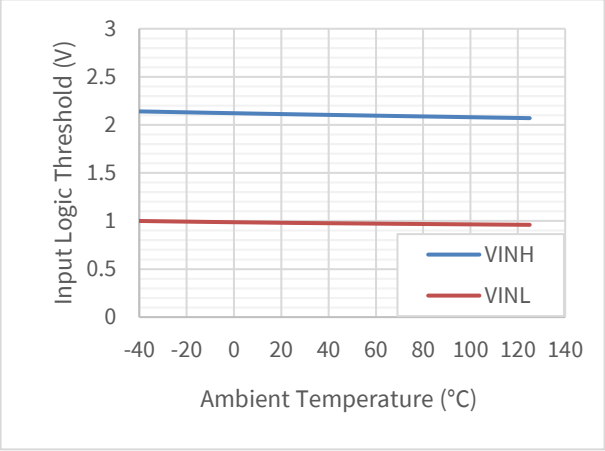


Figure 5.3 Input Logic Threshold vs Temperature

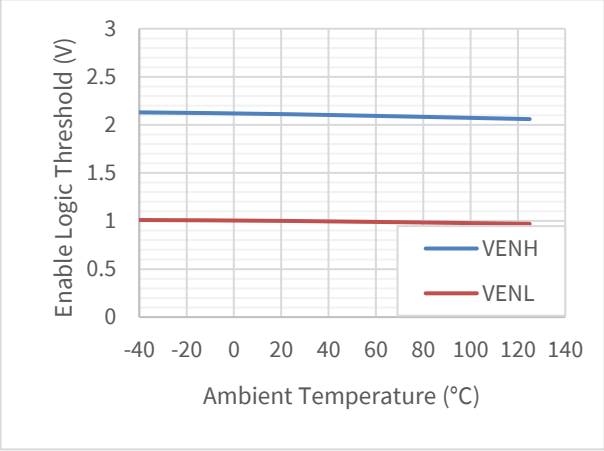


Figure 5.4 Enable Logic Threshold vs Temperature

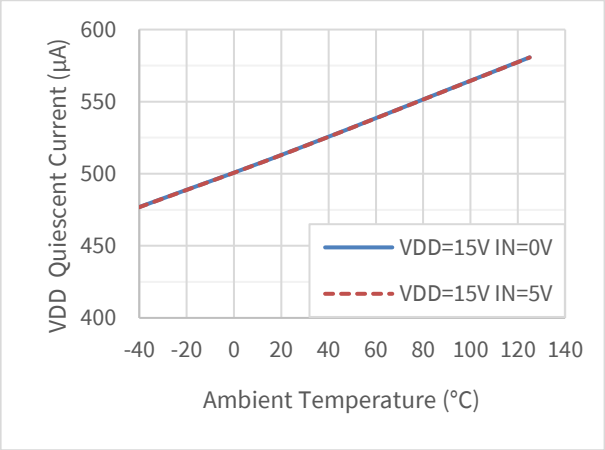


Figure 5.5 VDD Quiescent Current vs Temperature

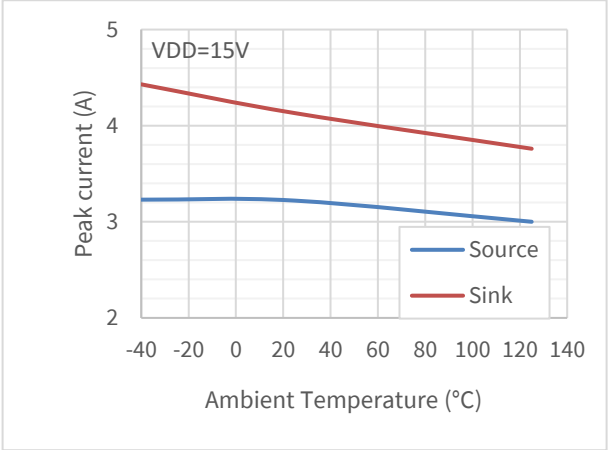


Figure 5.6 Peak Current vs Temperature

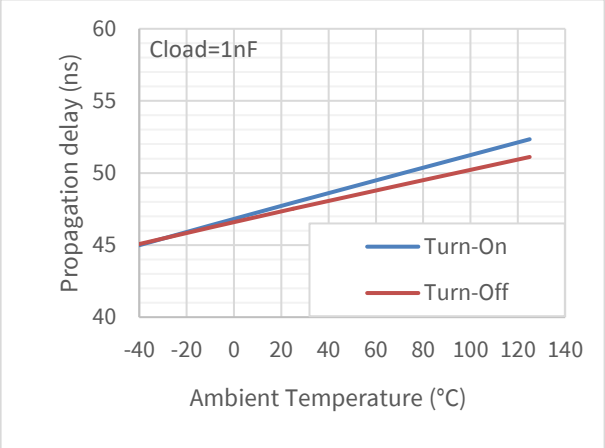


Figure 5.7 Turn-on/Turn-off Delay vs Temperature

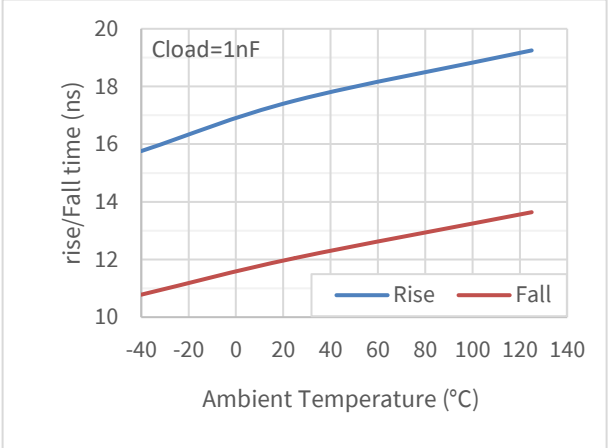


Figure 5.8 Output Rise/Fall Time vs Temperature

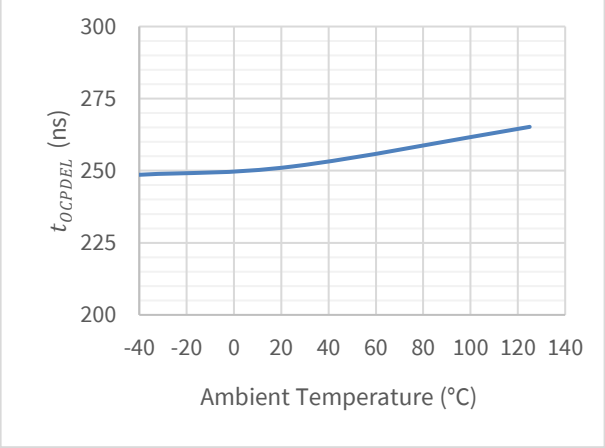


Figure 5.9 t_{OCPDEL} vs Temperature

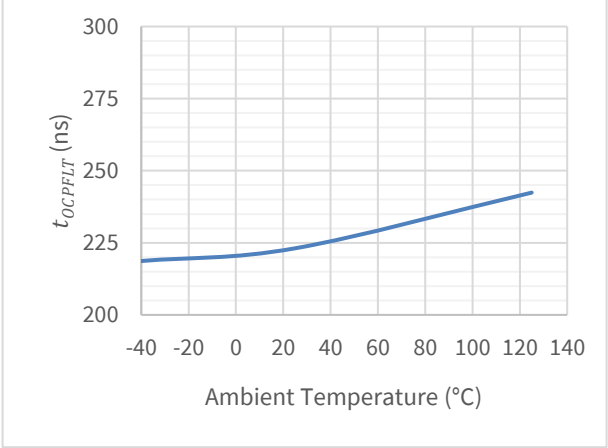


Figure 5.10 t_{OCPFLT} vs Temperature

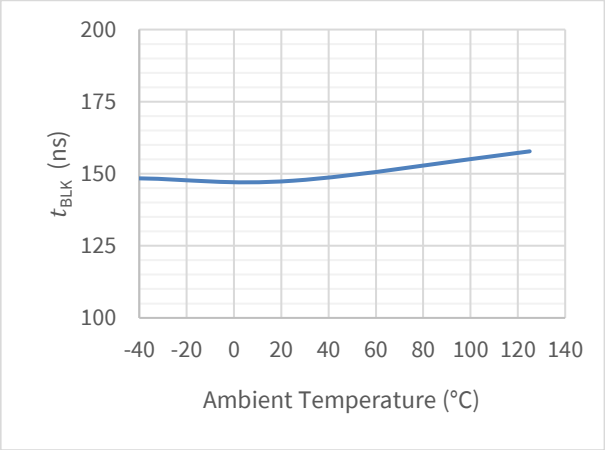


Figure 5.11 t_{BLK} vs Temperature

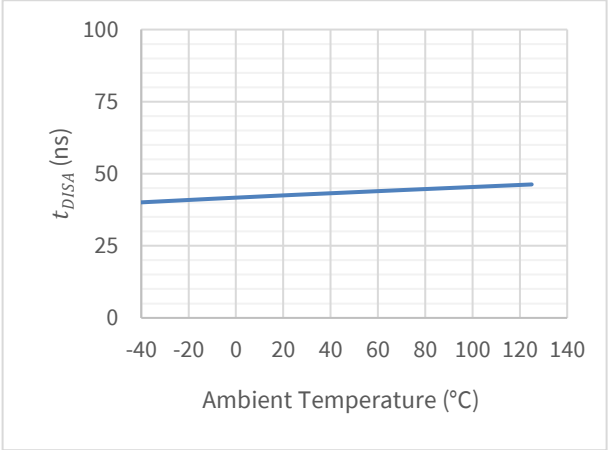


Figure 5.12 t_{DISA} vs Temperature

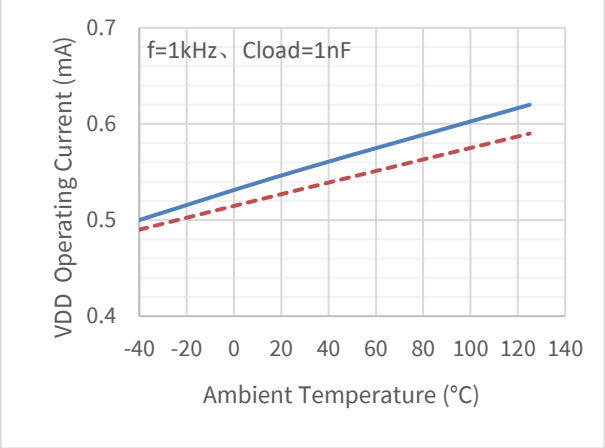


Figure 5.13 VDD Operating Current vs Temperature

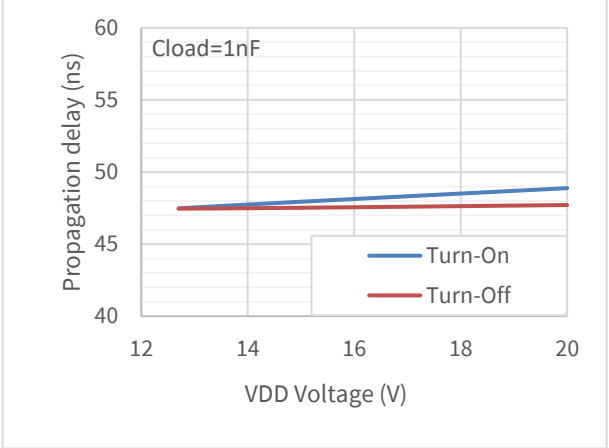


Figure 5.14 Turn-on/Turn-off Delay vs Voltage

5.4. Parameter Measurement Information

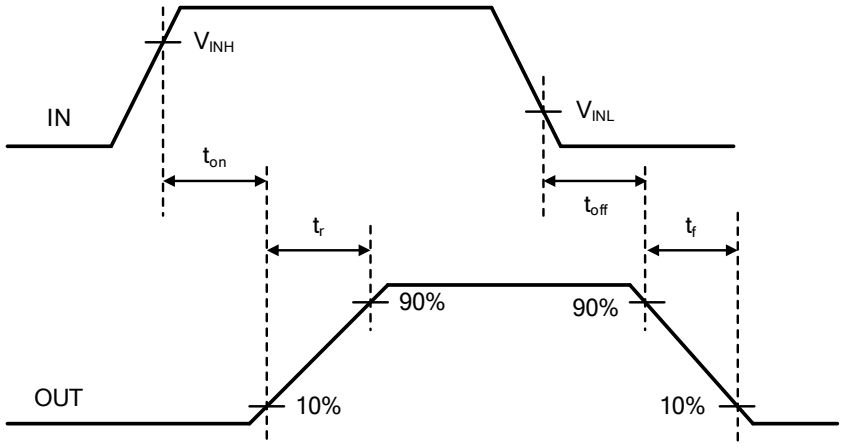


Figure 5.15 Switching Time Waveforms

6. General Description

6.1. Overview

NSD1012C is the single channel low side gate driver designed to drive Power MOSFET and IGBT with 3A source and 4A sink peak current capability. The logic threshold is compatible with both TTL and CMOS output and has about 1.1V hysteresis for strong noise immunity. The over current of power devices can be detected through OCP pin by sensing negative voltage and the information for abnormal operation conditions can be provided by changing EN/nFLT pin voltage level. When over current or UVLO conditions are detected, EN/nFLT pin voltage is pulled down by turning on internal NMOSFET while the voltage is recovered to certain voltage levels via resistor connected with the internal or external voltage sources as long as fault conditions are disappeared. Internal circuitries provide an under−voltage lockout function holding the output low and allow the fault clear time to be programmable with external component values.

6.2. VDD and Under-Voltage Lockout (UVLO)

NSD1012C has internal UVLO protection circuit which monitors the VDD supply voltage. The function of the UVLO circuits is to ensure that the gate of external power devices is driven at an optimum voltage. The UVLO circuits have hysteresis that helps to avoid VDD chattering when noise is present from the switching power supply and when VDD bias voltage is dropped by IDD increased suddenly once switching operation begins. If the VDD is below the V_{UVLO-} for more than t_{VDDUV}, driver output is kept low regardless of the IN input status and EN/nFLT pin is pulled down to GND by turning on internal NMOSFET.

EN/nFLT pin is charged by external voltage supply as long as VDD is higher than V_{UVLO+} for longer than the fault clear time, which is determined by capacitance and resistance connected externally at VDD and EN pins. Driver out is also generated when IN high signal is applied after EN/nFLT voltage is higher than V_{ENH}.

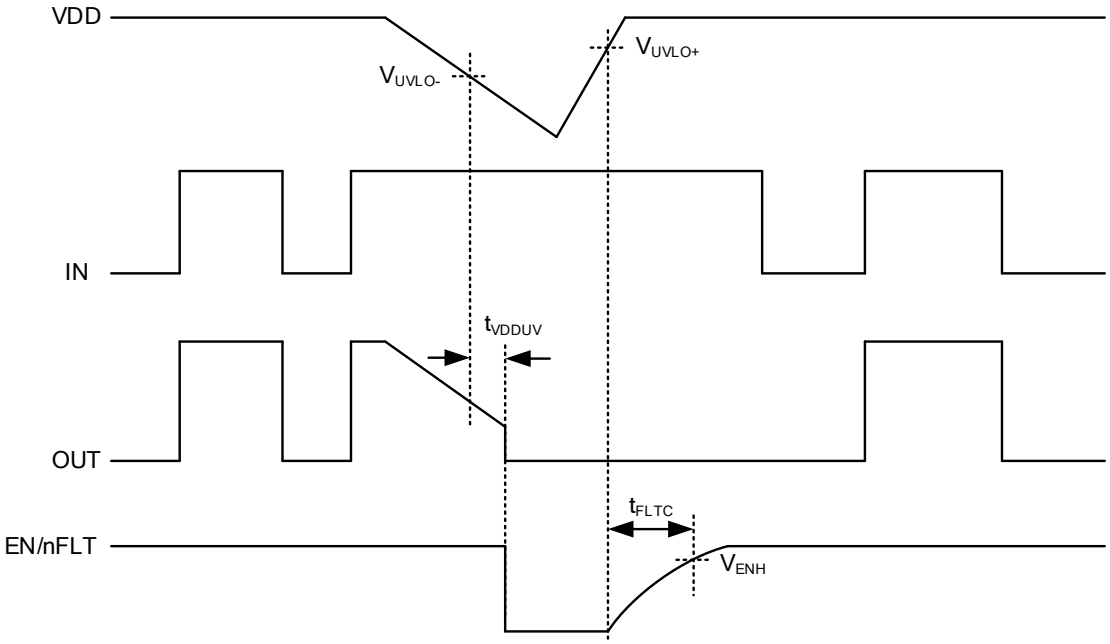


Figure 6.1 VDD UVLO Protection Timing Diagram

6.3. Over Current Protection

NSD1012C incorporates overcurrent protection functionality through the detection of negative voltage at the OCP pin. To avoid false tripping from turn-on transients caused by parasitic capacitances during IGBT activation, a blanking interval is implemented—during which overcurrent detection remains disabled for the duration of t_{BLK}. After t_{BLK} and the voltage of OCP pin is over V_{OCP_TH}, NSD1012C triggers a fault shutdown sequence. This sequence begins by generating a fault signal: an internal NMOSFET turns on, pulling the EN/nFLT pin low. At the same time the NSD1012C terminates the present cycle, and the gate output is immediately pulled down with internal propagation delay (t_{OCPDEL}). If the OCP fault condition is removed, the internal pull down NMOSFET of EN/nFLT is released and EN/nFLT will be pulled up again with VDD, but the output still keeps low until the next input signal IN is high.

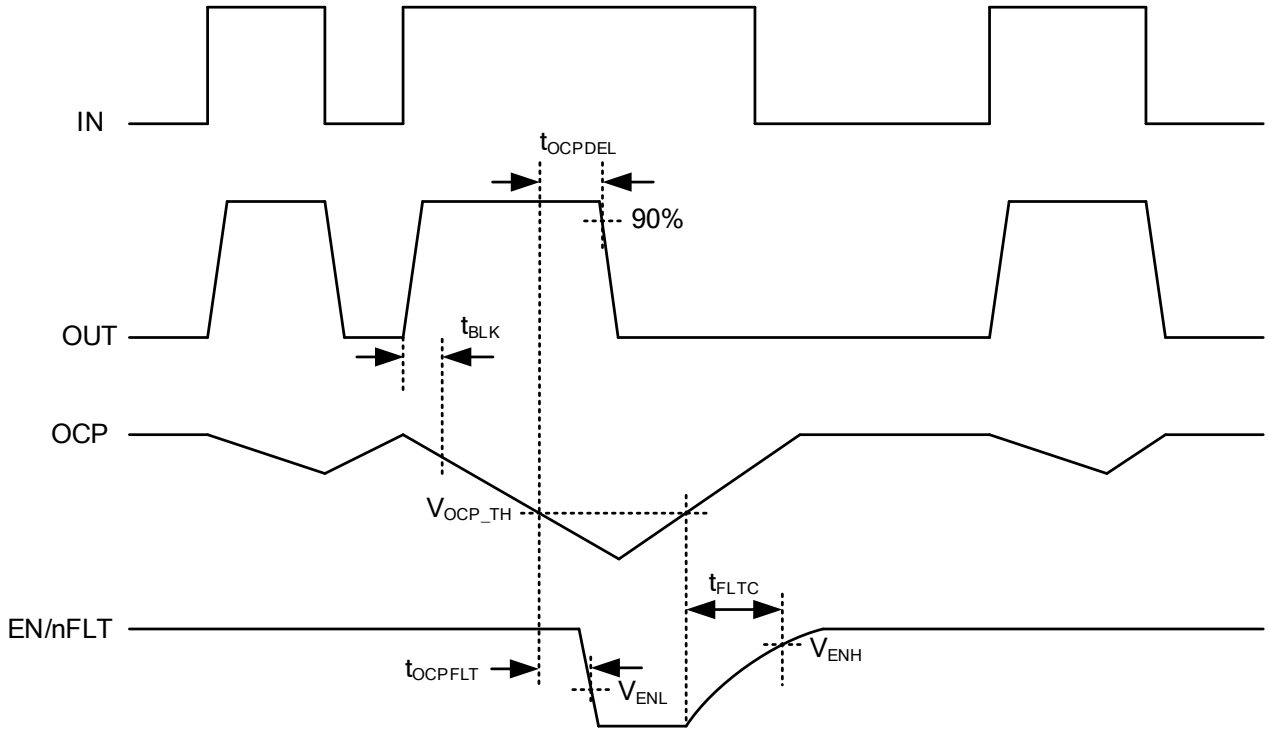


Figure 6.2 OCP Fault Detection and Fault Clear Waveforms

6.4. Fault Reporting and Clear Time

The NSD1012C features integrated fault reporting with a controlled clear timer. The driver reports faults through the EN/nFLT pin under two conditions: VDD undervoltage or OCP fault detection. When a fault occurs, the EN/nFLT pin is internally pulled down to GND. It remains low until the fault condition clears and the internal pull-down NMOS turns off, allowing the EN/nFLT pin capacitor to recharge through the combined internal and external pull-up resistors. An external controller can thus monitor the EN/nFLT pin voltage to determine the status. The recharge time, denoted as t_{FLTC}, is set by the time constant formed by R_{FLTC} and C_{FLTC}. This duration also depends on the VDD level and can be calculated using the following equation:

$$t_{FLTC} = -\left(\frac{R_{FLTC} \times 2.15M}{R_{FLTC} + 2.15M}\right) \times C_{FLTC} \times \ln\left(1 - V_{ENH} \times \frac{R_{FLTC} + 2.15M}{2.15M \times VDD + 3.3V \times R_{FLTC}}\right)$$

6.5. Enable Input

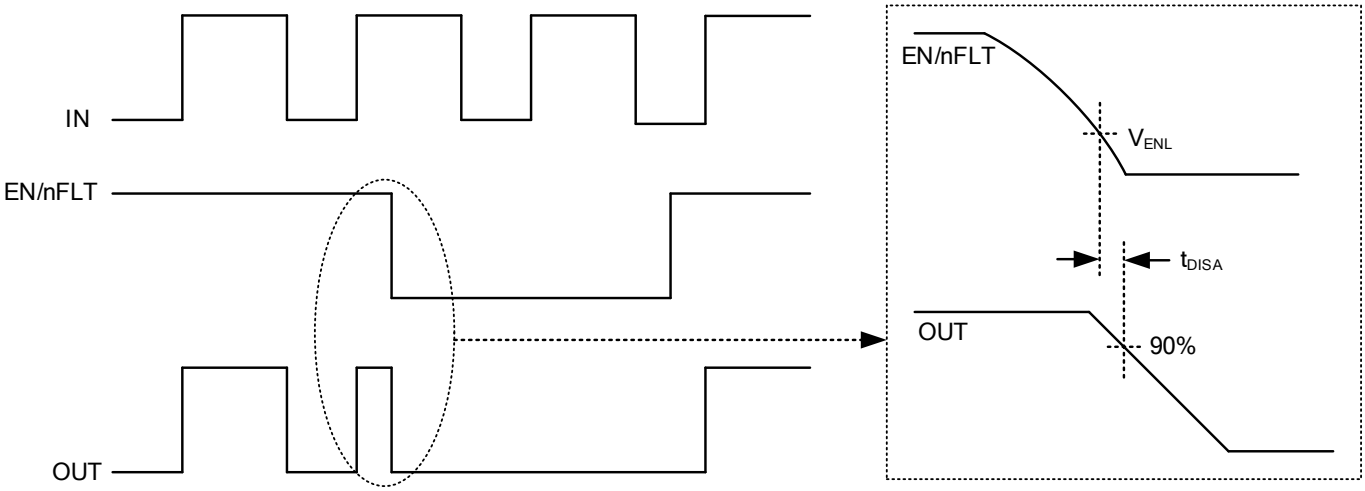


Figure 6.3 IN、OUT、EN/nFLT Pins Timing Diagrams and EN/nFLT Pin Switching Time Waveform

NSD1012C features an enable function to control the output state. When the EN/nFLT pin voltage exceeds VENH, the output becomes active; if it falls below VENL or is pulled to GND, the output remains low. A floating EN/nFLT pin can enable the output in the absence of faults. However, for reliable operation in noisy environments (e.g., switch-mode power supplies), the EN/nFLT pin should be connected to VDD via an external pull-up resistor and a small capacitor for noise immunity.

6.6. Input Stage

The input pin of the NSD1012C is compatible with industry-standard TTL and CMOS logic levels regardless of its VDD supply voltage. It features a wide hysteresis voltage of 1.1V, which provides excellent noise immunity. With a typical high-level input threshold of 2.2V and a low-level threshold of 1.1V, the NSD1012C can directly interface with PWM signals from various sources, such as MCUs and standalone PWM controllers commonly used in switching power supplies.

6.7. Output Stage

The NSD1012C is a single-channel gate driver capable of delivering 3A (typical) source and 4A (typical) sink peak currents with a 15V supply, driving 1nF loads. A high input signal turns on the internal high-side switch, charging the gate capacitance (C_g) of the external power device. A low input activates the low-side switch, discharging C_g. Due to parasitic inductance in the charge and discharge paths, ringing may occur on the VDD and OUT pins.

6.8. Input/output logic truth table

IN	*UVLO(1)*	*OCP(2)*	*EN/nFLT(3)*	*OUT*	*Description*
L	**H**	**L**	**H**	**L**	OUT = L
H	H	L	H	H	OUT = H
X	L	X	L	L	OUT = L、EN/nFLT= L
X	H	H	L	L	OUT = L、EN/nFLT= L
X	H	X	L	L	OUT = L(Pulling EN/nFLT low)

(1) UVLO “L” state is under-voltage protection.

(2) OCP “H” state is over-current protection.

(3) EN/nFLT “H” state is EN/nFLT pin externally pulling up and internally pull-down NMOSFET is off.

7. Application Note

7.1. Typical Application Circuit

Figure 7.1 presents a typical application circuit of the NSD1012C in an active PFC stage. Key elements include:

- Current detection via resistor (RCS) for OCP and SCP functionality
- RC filtering to suppress high-frequency disturbances
- Programmable fault blanking duration set by an RC network
- Microcontroller-compatible signal interface for system control and monitoring

Note: Avoid connecting EN/nFLT directly to VDD. The EN/nFLT pin is default low before power-up, and a direct connection to VDD may cause high inrush current through the EN/nFLT pin during power-on, leading to internal NMOSFET failure.

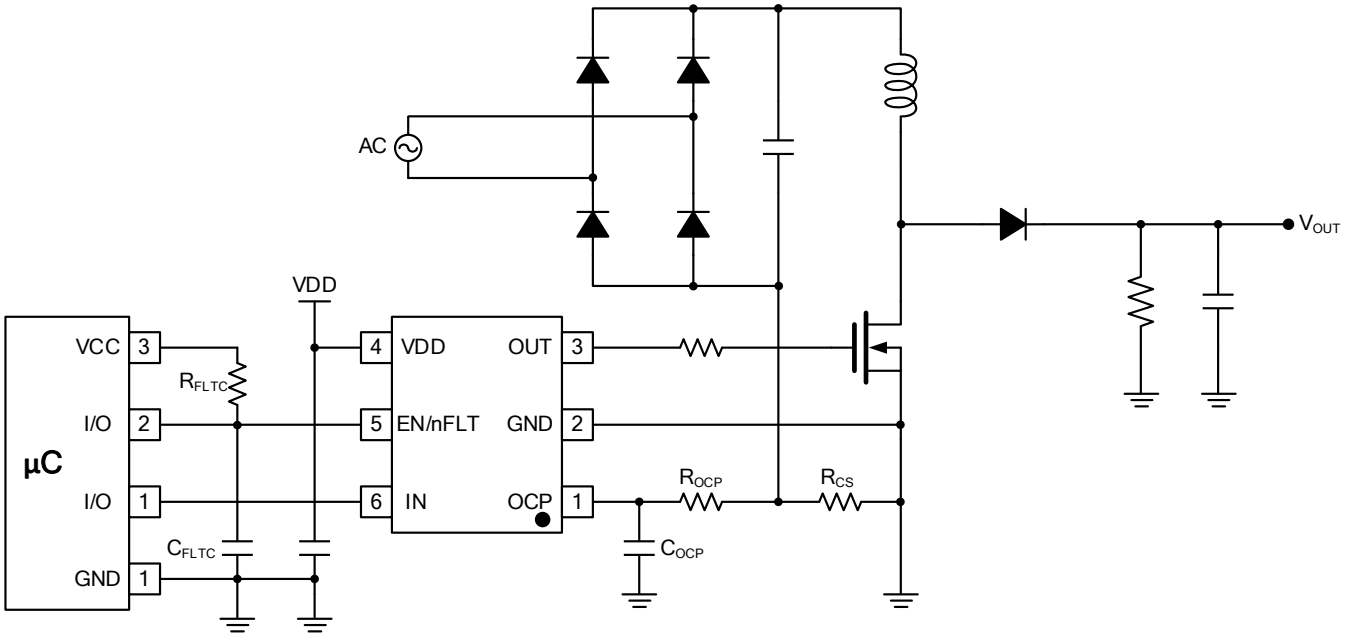


Figure 7.1 Simplified PFC Schematic

7.2. ESD Structure

Figure.7.2 illustrates the multiple parasitic diodes involved in the ESD protection components of NSD1012C device.

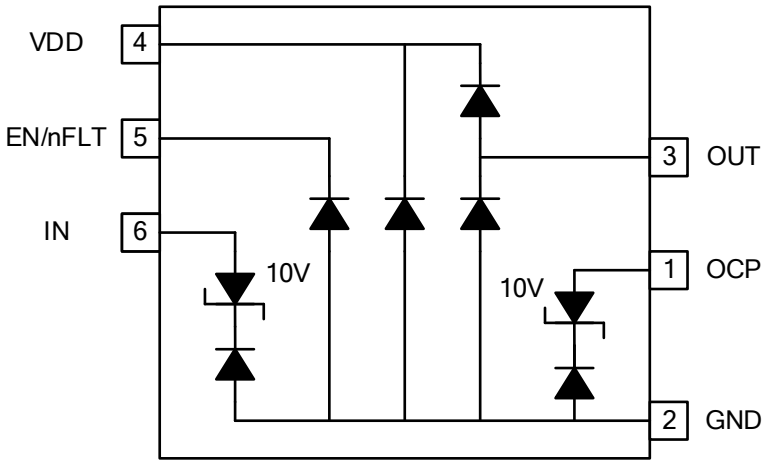


Figure 7.2 ESD Structure

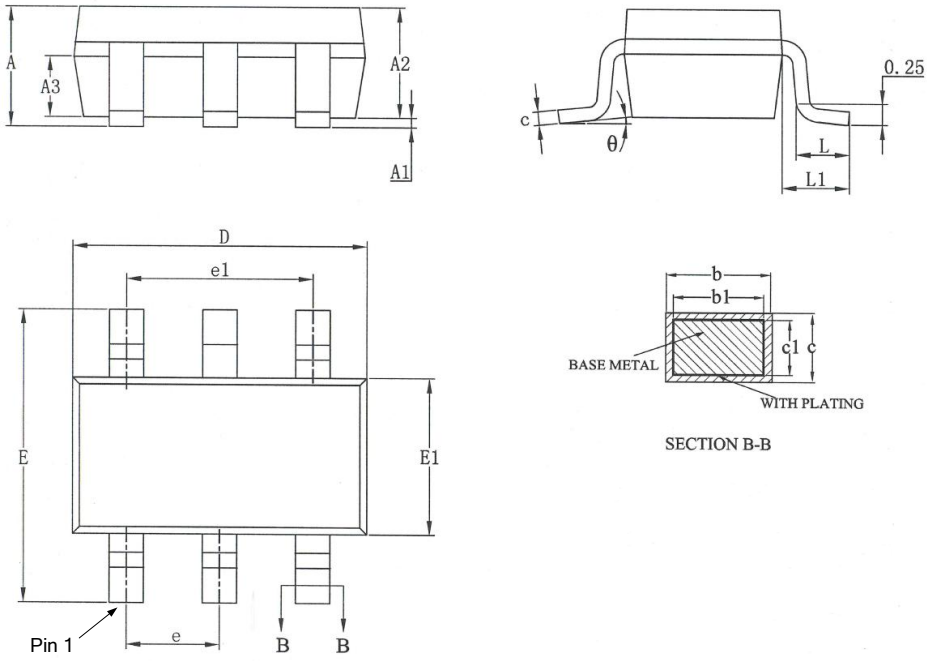
7.3. Layout Recommendations

The NSD1012C is a high-speed gate driver optimized for mid-power to high-power applications. In high-current, fast-switching environments, a carefully engineered PCB layout is crucial to maintain signal integrity, operational reliability, and system robustness. Poor layout practices can result in unintended switching behavior, significant voltage ringing, or latch-up failure.

Recommended layout practices:

- Minimize high-current loop area and parasitic inductance.
  - Place the NSD1012C in close proximity to the power switches (IGBTs/MOSFETs);
  - Mount the bypass capacitor adjacent to the VDD and COM pins;
  - Implement an extensive ground copper pour under the NSD1012C to minimize parasitic inductance;
- The ground plane serves to attenuate radiated noise and enhance thermal performance.

8. Package Information



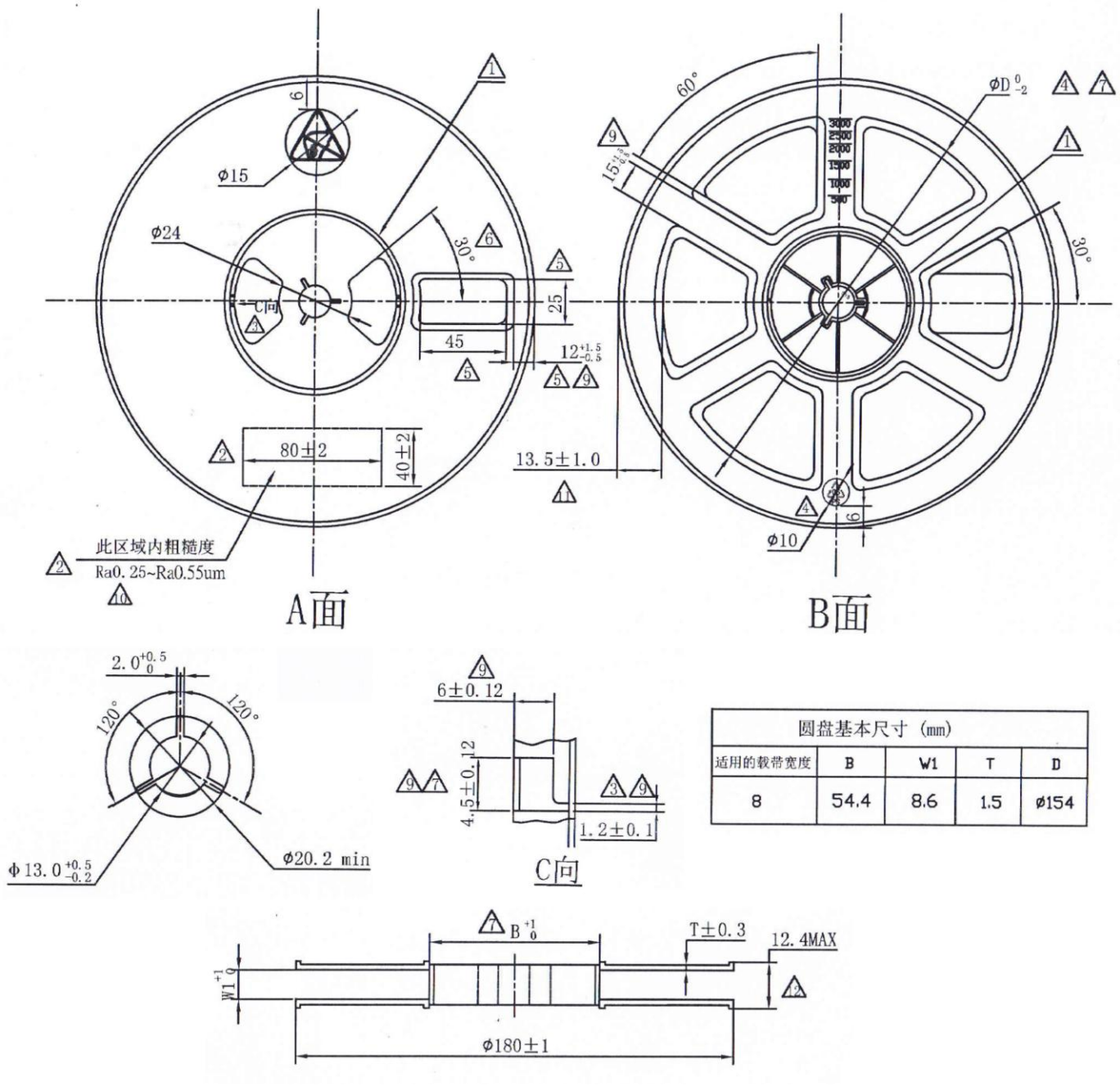
	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
	A	—	—	1.25
	A1	0.04	—	0.10
	A2	1.00	1.10	1.20
1	A3	0.60	0.65	0.70
1	b	0.33	—	0.41
	b1	0.32	0.35	0.38
1	c	0.15	—	0.19
1	c1	0.14	0.15	0.16
	D	2.82	2.92	3.02
	E	2.60	2.80	3.00
2	E1	1.50	1.60	1.70
	e	0.95BSC		
	e1	1.90BSC		
	L	0.30	—	0.60
3	L1	0.60REF		
	θ	0	—	8°

Figure 8.1 SOT23-6 Package Shape and Dimension in millimeters

9. Ordering Information

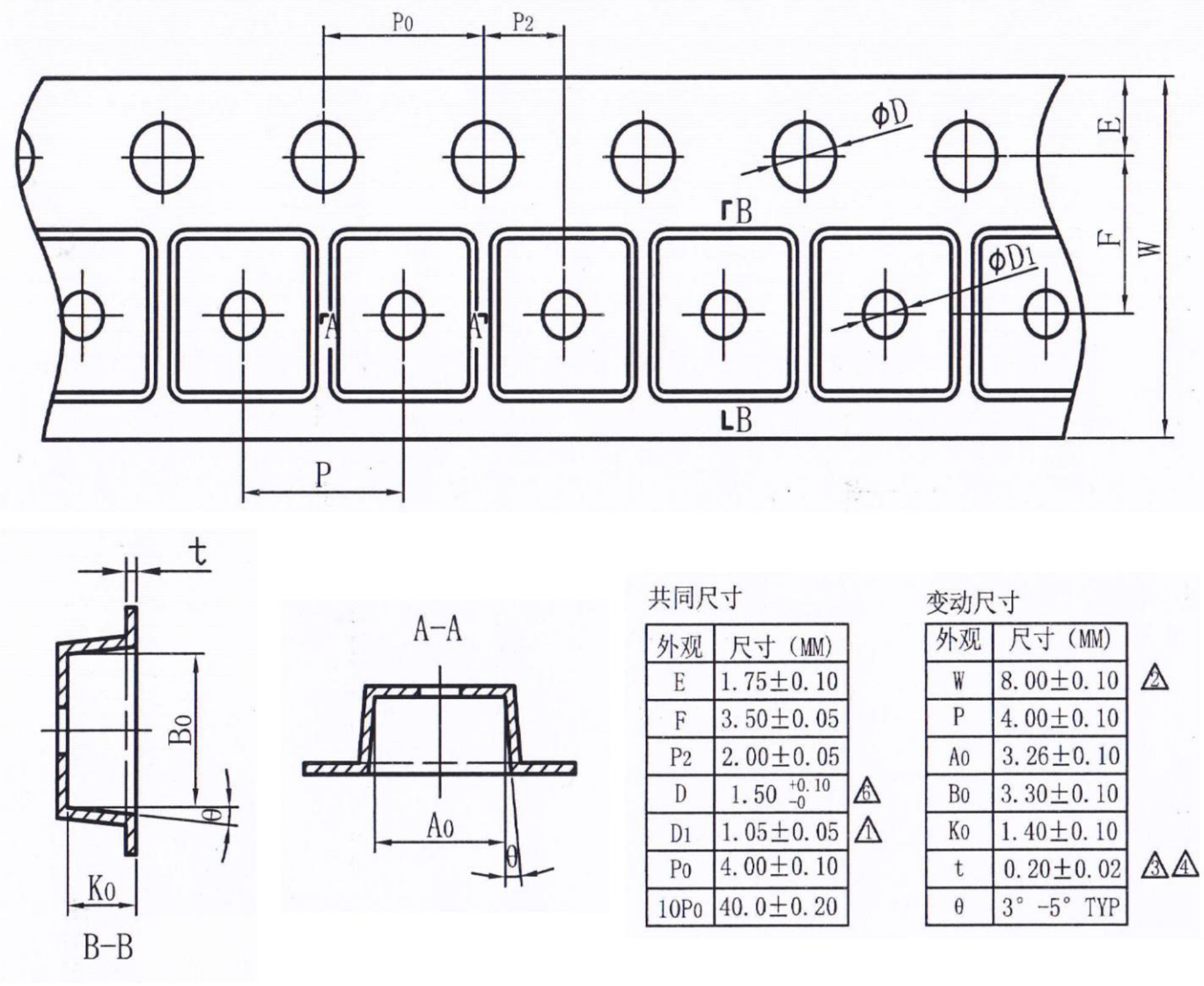
Part Number	*Temperature*	*MSL*	*Package Drawing*	*SPQ*
NSD1012C-DSTCR	-40 to 125°C	3	SOT23-6	3000

10. Tape and Reel Information



圆盘基本尺寸（mm）				
适用的载带宽度	B	W1	T	D
8	54.4	8.6	1.5	φ154

Figure 10.1 Tape Information



共同尺寸

外观	尺寸（MM）	
E	1.75±0.10	
F	3.50±0.05	
P2	2.00±0.05	
D	$1.50^{+0.10}_{-0}$	5
D1	1.05±0.05	1
P0	4.00±0.10	
10P0	40.0±0.20	

变动尺寸

外观	尺寸（MM）	
W	8.00±0.10	2
P	4.00±0.10	
A0	3.26±0.10	
B0	3.30±0.10	
K0	1.40±0.10	
t	0.20±0.02	3 4
θ	3° -5° TYP	

Figure 10.2 Reel information

11. Revision History

Revision	Description	Date
1.0	Initial Version.	2025/09/19

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