NOVOSENSE

NSR28C42, NSR28C43, NSR28C44, NSR28C45

High Performance Fixed Frequency Low Power Current Mode PWM Controllers

Datasheet (EN) 1.0

Product Overview

The NSR28C4x series are high performance fixed frequency current mode controllers. They are designed for off-line and DC-DC applications with minimal external components. The integrated circuits include an oscillator, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output for driving an N-channel MOSFET.

The NSR28C4x series have built in features such as undervoltage lockout (UVLO) for input and reference, cycle−by−cycle current limiting. NSR28C42 and NSR28C44 feature a higher VCC turn-on or turn-off hysteresis suitable for off-line power supplies while NSR28C43 and NSR28C45 are suitable for DC-DC applications with narrower hysteresis range. An 8−pin surface mount (SOP8) plastic package is available.

Key Features

- Optimized for off-line and DC-DC converters
- Low start-up current (< 0.1 mA)
- Oscillator for precise frequency control
- Peak current mode operation
- Up to 500 kHz output switching frequency
- Cycle−by−Cycle current limiting
- High-current totem-pole output
- Optional VCC UVLO threshold and hysteresis
- Optional maximum duty cycle limit
- SOP8 RoHS-compliant package
- -40 ~ 125°C operating ambient temperature

Applications

- Common-used Flyback Converters
- Auxiliary Power Supply
- Off-line Power Supply

Device Information

Part Number	*UVLO ON/OFF Threshold*	*Max Duty Cycle*
NSR28C42	15.5V / 9.5V	Up to 100%
NSR28C43	8.2V / 7.5V	Up to 100%
NSR28C44	15.5V / 9.5V	Up to 50%
NSR28C45	8.2V / 7.5V	Up to 50%

Typical Application Circuits

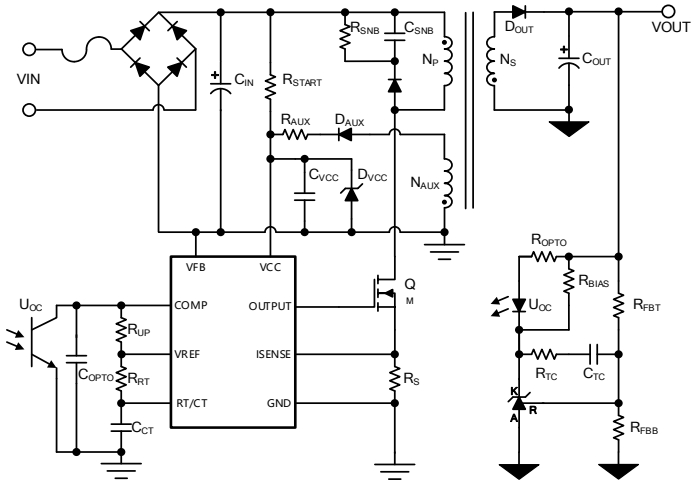


Figure 1 NSR28C4x Typical Flyback Application Circuits

INDEX

1. Pin Configuration and Functions

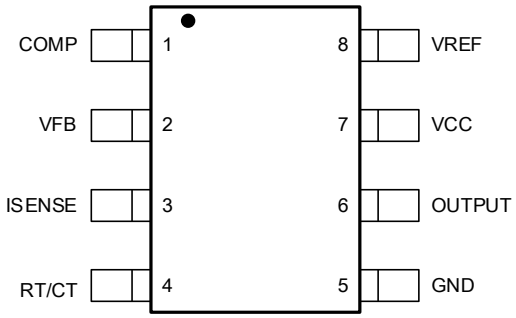


Figure 2 NSR28C4x Pin Configuration

PIN NO.	SYMBOL	FUNCTION
1	COMP	Error amplifier output. Connect to an external compensation network to the feedback for primary winding feedback. Connect to optocoupler for secondary optocoupler feedback.
2	VFB	Feedback voltage input. Connect to an external resistor divider from output to GND to regulate output voltage for primary winding feedback. Connect to GND for secondary optocoupler feedback.
3	ISENSE	Current sense amplifier input. Connect this pin with RC filter to a sense resistor which connected between source of external power MOSFET and GND.
4	RT/CT	The Oscillator frequency setting pin. Connect a resistor R_T to VREF and a timing capacitor to GND. The resistor and capacitor determine oscillator frequency. The frequency of the OUTPUT gate drive of the NSR28C42 and NSR28C43 is equal to oscillator frequency at up to 100% duty cycle; the frequency of the NSR28C44 and NSR28C45 is equal to half of the oscillator frequency at up to 50% duty cycle.
5	GND	Ground reference.
6	OUTPUT	Gate driver output. The gate of the external MOSFET should be connected to this pin.
7	VCC	Power supply of the control IC.
8	VREF	Reference voltage output. It provides charging current for capacitor C_{CT} through resistor R_{CT}.

2. Absolute Maximum Ratings

Description	Min	Max	Units
VCC to GND	-0.3	24	V
COMP to GND	-0.3	5.5	V
VFB to GND	-0.3	5.5	V
ISENSE to GND	-0.3	5.5	V
VREF to GND	-0.3	5.5	V
RT/CT to GND	-0.3	5.5	V
OUTPUT to GND	-0.3	24	V
Operating junction temperature	-40	150	℃
Storage temperature	-65	150	℃

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to conditions on Absolute Maximum Ratings for extended periods may affect device reliability.

3. ESD Ratings

Parameters	Symbol	Value	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), per AEC-Q100-002-RevD	±2000	V
	Charged device model (CDM), per AEC-Q100-011-RevB	±750	V

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}			20	V
Operating Ambient Temperature	T_A	-40		125	°C

5. Thermal Information

Parameters	Symbol	SOP8	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	115	°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	57	°C/W

(1) The thermal data is based on the JEDEC standard high-K profile, JESD 51-7, four layers board.

6. Specifications

6.1. Electrical Characteristics

V_{CC} = 15 V, C_{VCC} = 0.1 μF, R_{RT} = 10 kΩ, C_{CT} = 3.3 nF, T_J = –40°C to 125°C. (unless otherwise noted)

Parameters	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Under-voltage Lockout & Quiescent Current					
START Threshold	7.4	8.2	9.1	V	NSR28C43/28C45
START Threshold	13.3	15.5	17.2	V	NSR28C42/28C44
STOP Threshold	6.8	7.5	8.3	V	NSR28C43/28C45
STOP Threshold	8.2	9.5	10.5	V	NSR28C42/28C44
Startup Current, IDD		36	100	μA	
Operating Supply Current, IDD		1	2	mA	V_{FB} = V_{ISENSE}= 0 V
VREF Voltage					
VREF Voltage	4.92	5.08	5.21	V	I_{VREF} = 1 mA, T_A = 25°C
Line regulation		0.5	10	mV	12 ≤ V_{CC} ≤ 20 V
Load regulation		3	20	mV	1 mA to 20 mA
Temperature stability		0.2	0.4	mV/°C	Specified by design
Total output variation	4.88		5.28	V	
Long term stability		5		mV	1000 hours, T_A = 125°C
VREF noise voltage		50		μV	F_{OSC}: 10 Hz to 10 kHz, T_A = 25°C
Short Current limit - sourcing	-100	-40	-25	mA	
Error Amplifier					
Reference Voltage	2.39	2.5	2.63	V	V_{COMP} = 2.5V
FB Input Bias Current		0	1	μA	
Open Loop Voltage Gain	65	90		dB	2 ≤ V_{COMP} ≤ 4 V
Unity Gain Bandwidth	0.7	1		MHz	Specified by design
COMP Sink Current	2	6		mA	V_{FB} = 2.7 V, V_{COMP} = 1.1 V
COMP Source Current		-0.8	-0.5	mA	V_{FB} = 2.3 V, V_{COMP} = 5 V
COMP VOH	4.5	5		V	V_{FB} = 2.3 V, R_L = 15-kΩ COMP to GROUND
COMP VOL		0.1	0.7	V	V_{FB} = 2.7 V, R_L = 15-kΩ COMP to VREF
PSRR	60	70		dB	12 ≤ V_{CC} ≤ 20 V
Current Sense					
Input Bias Current	-1	-0.2		μA	

Parameters	Min	Typ	Max	Unit	Comments
Input Signal, Maximum	0.9	1	1.1	V	V_{COMP} = 5 V
Gain, ACS = ΔVCOMP/ΔVISENSE		3		V/V	
PSRR		70		dB	12 V ≤ V_{CC} ≤ 20 V, Specified by design
ISENSE to OUTPUT delay		80	200	ns	V_{ISENSE} stepped from 0 V to 2 V, Specified by design
Oscillator					
Frequency Accuracy	47	52	58	kHz	T_J = 25°C
Voltage stability		0.2	1	%	12 ≤ V_{CC} ≤ 20 V
Temperature stability		5		%	-40°C ≤ T_A ≤ 125°C
Amplitude		1.7		V	RT/CT pin peak-to-peak voltage
Discharge Current		7.8		mA	
Maximum Duty Cycle	46	48	50	%	NSR28C44/28C45
Maximum Duty Cycle	95	97	100	%	NSR28C42/28C43
Minimum Duty Cycle	0			%	
Driver Output					
Gate VOH	14	14.8		V	I_{SOURCE} = 20 mA
Gate VOH	11.6	13.3		V	I_{SOURCE} = 200 mA
Gate VOL		0.1	0.2	V	I_{SINK} = 20 mA
Gate VOL		1.3	3	V	I_{SINK} = 200 mA
Peak Output Current		1		A	
Rise Time		40	80	ns	C_{OUTPUT} = 1 nF, T_J = 25°C
Fall Time		30	71	ns	C_{OUTPUT} = 1 nF, T_J = 25°C

6.2. Typical Performance Characteristics

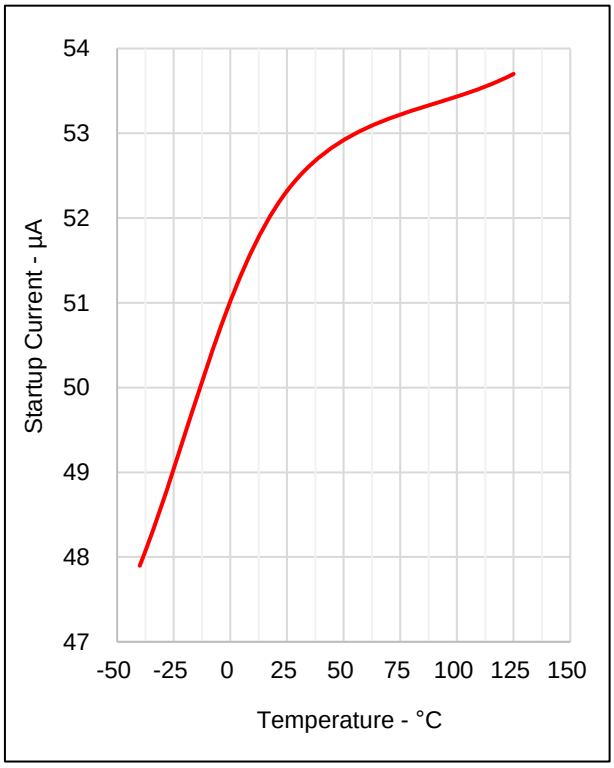


Figure 3 Startup Current vs Temperature

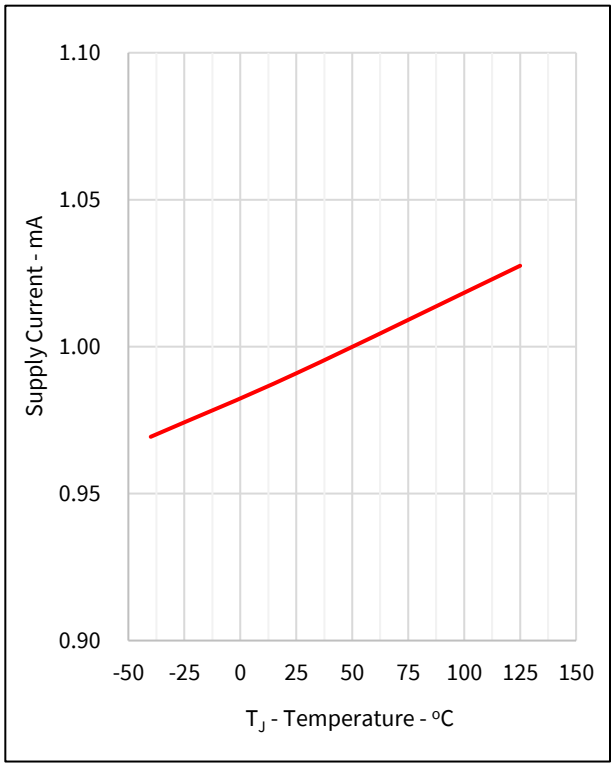


Figure 4 Supply Current vs Temperature

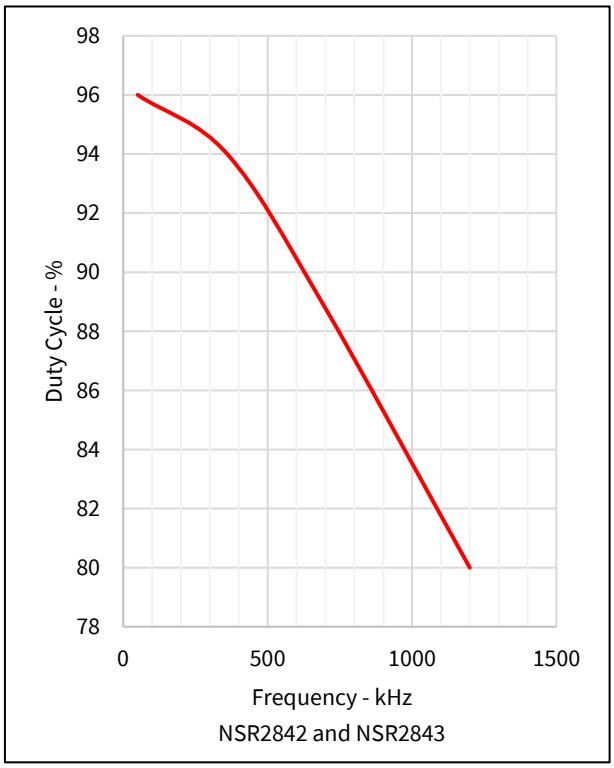


Figure 5 Maximum Duty Cycle vs Oscillator Frequency

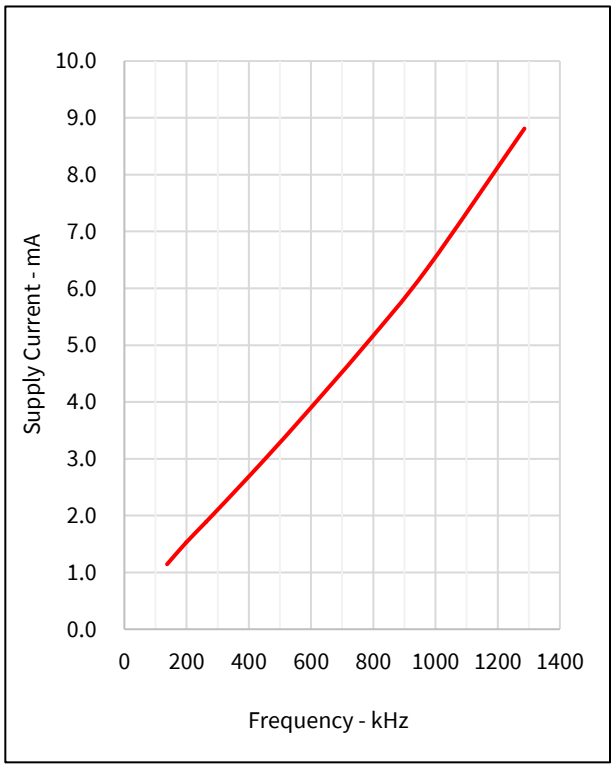


Figure 6 Supply Current vs Oscillator Frequency

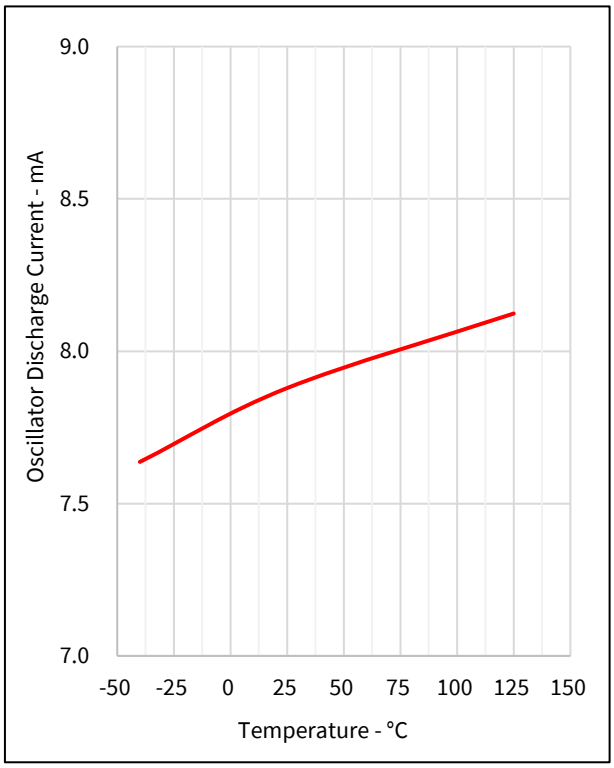


Figure 7 Oscillator Discharge Current vs Temperature

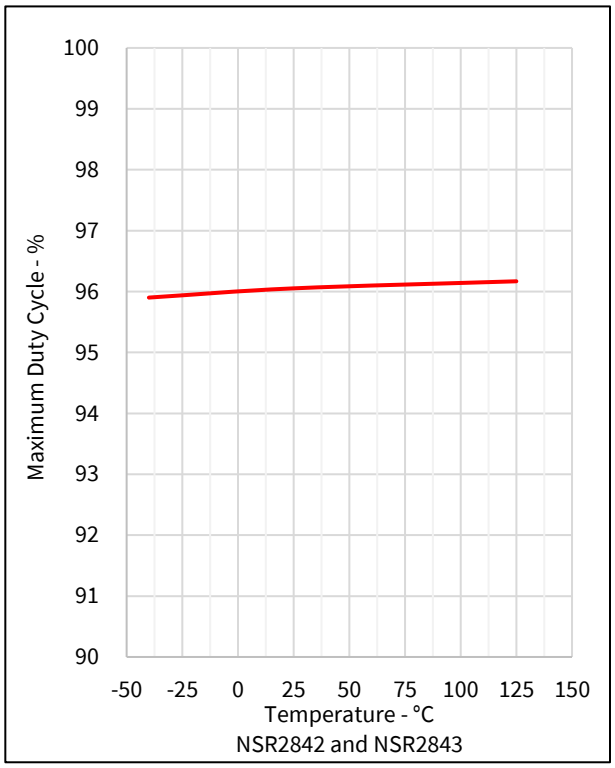


Figure 8 Maximum Duty Cycle vs Temperature

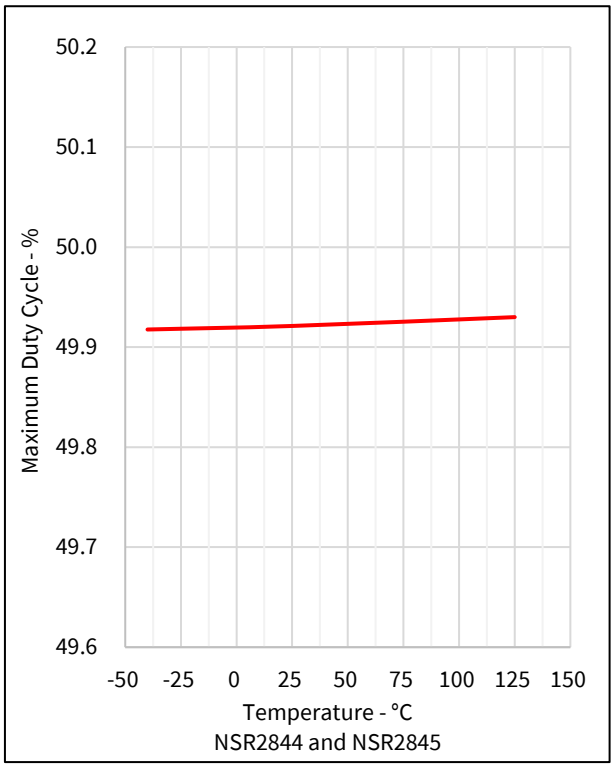


Figure 9 Maximum Duty Cycle vs Temperature

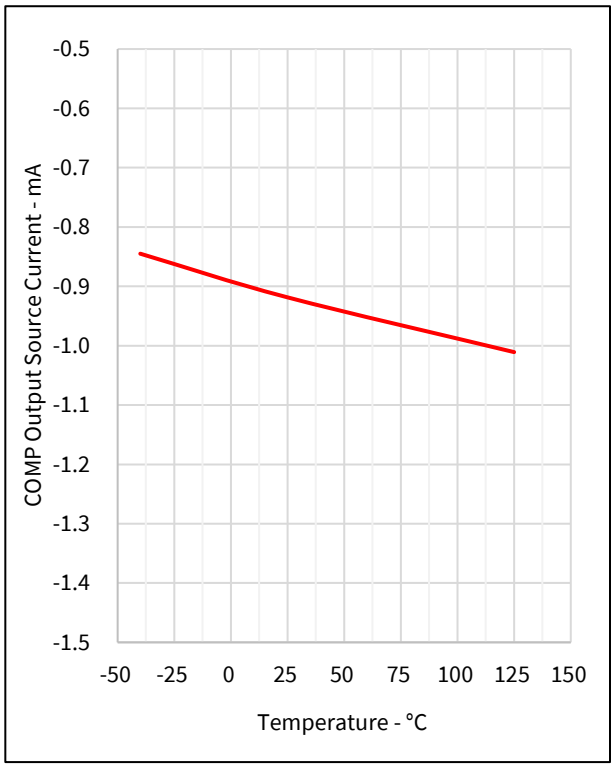


Figure 10 COMP Output Source Current vs Temperature

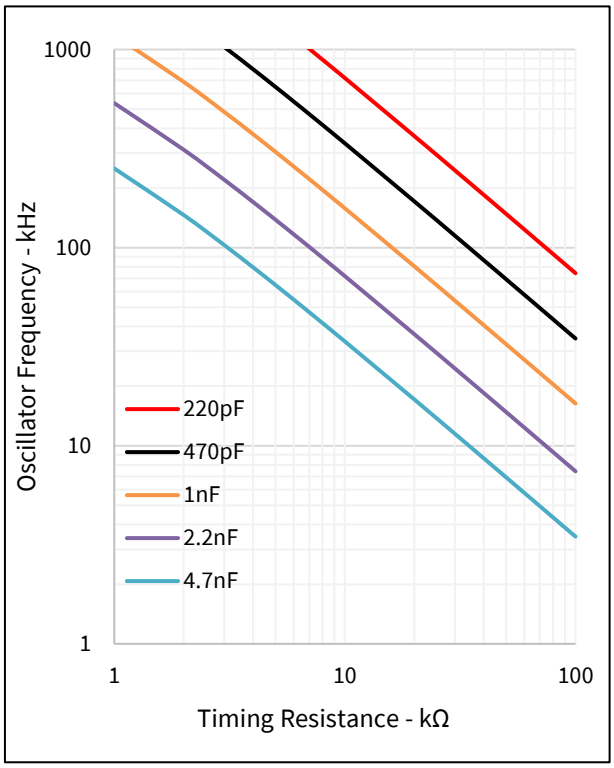


Figure 11 Frequency vs Timing Resistance and Capacitance

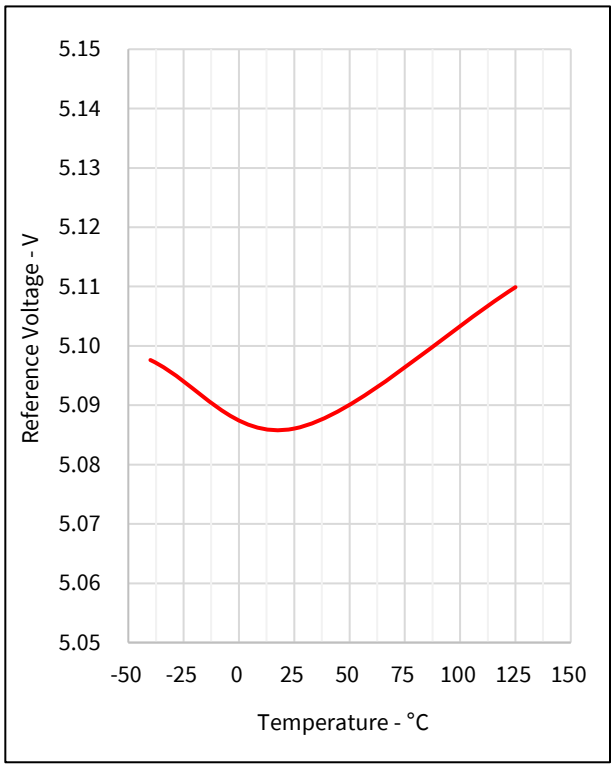


Figure 12 Reference Voltage vs Temperature

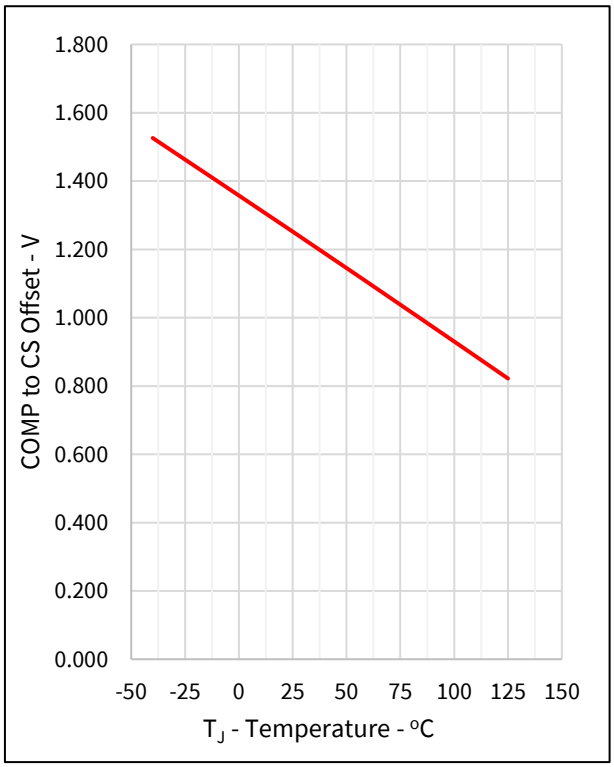


Figure 13 COMP to ISENSE Offset Voltage vs Temperature

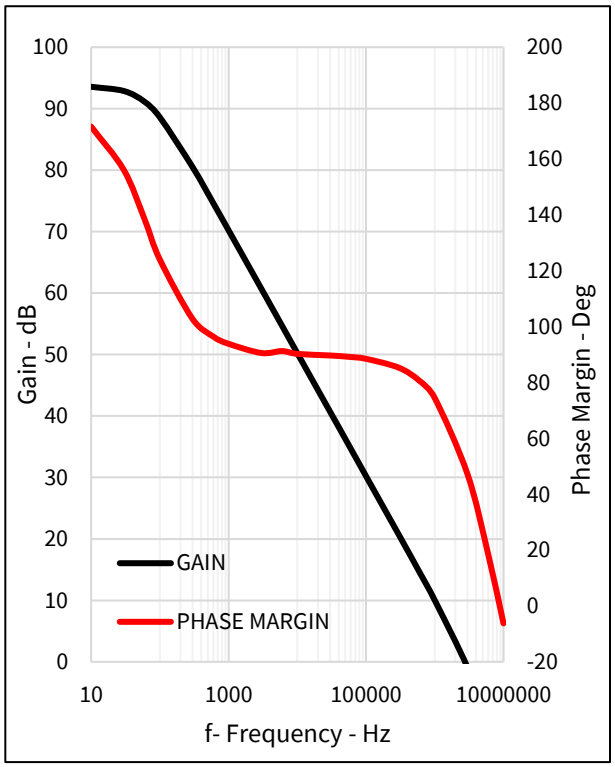


Figure 14 Error Amplifier Frequency Response

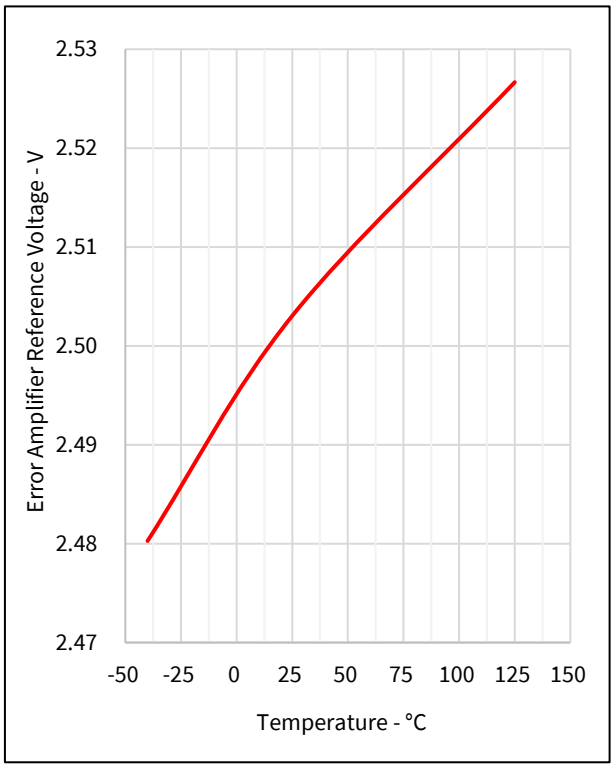


Figure 15 Error Amplifier Reference Voltage vs Temperature

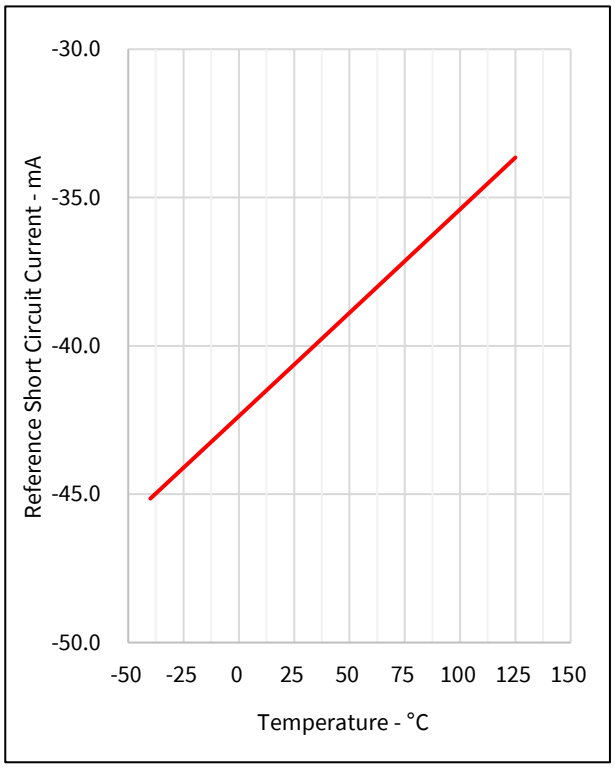


Figure 16 Reference Short-Circuit Current vs Temperature

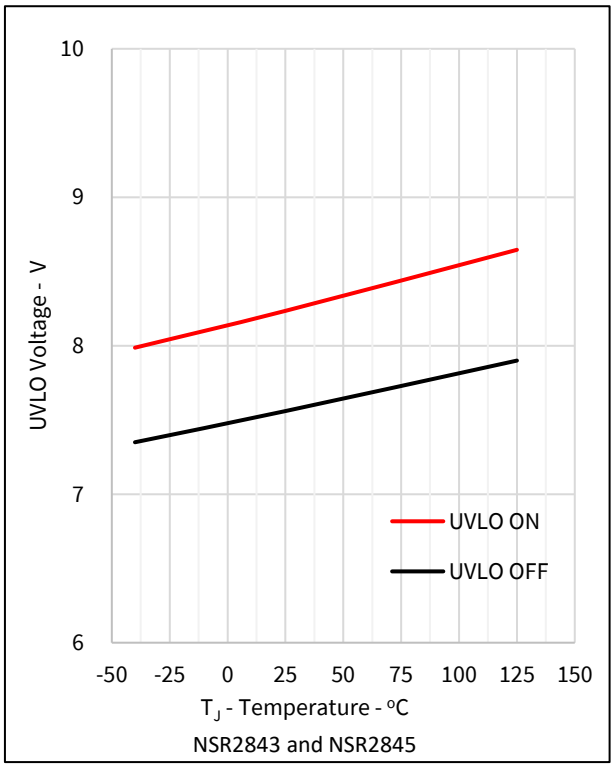


Figure 17 Undervoltage Lockout vs Temperature

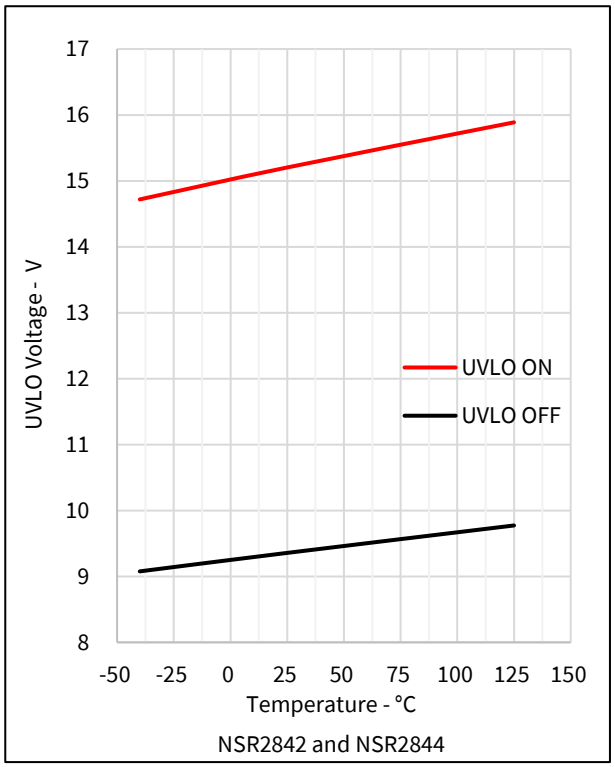


Figure 18 Undervoltage Lockout vs Temperature

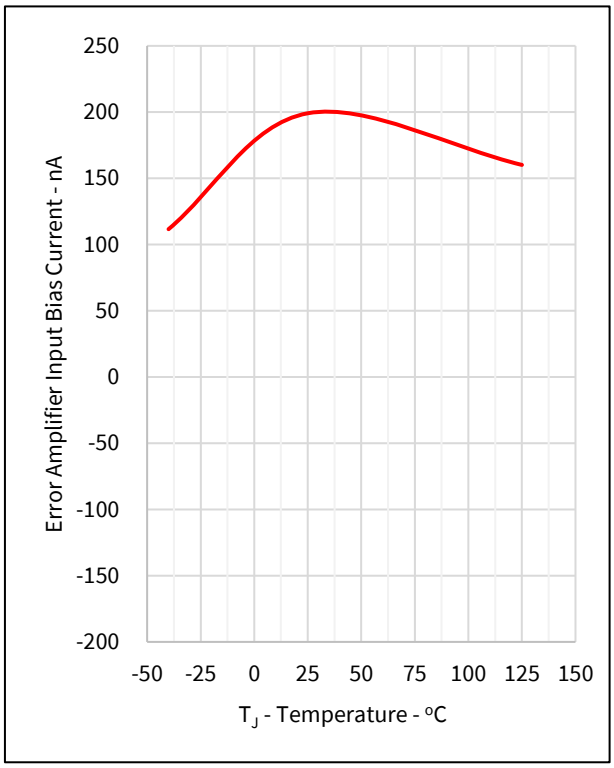


Figure 19 Error Amplifier Input Bias Current vs Temperature

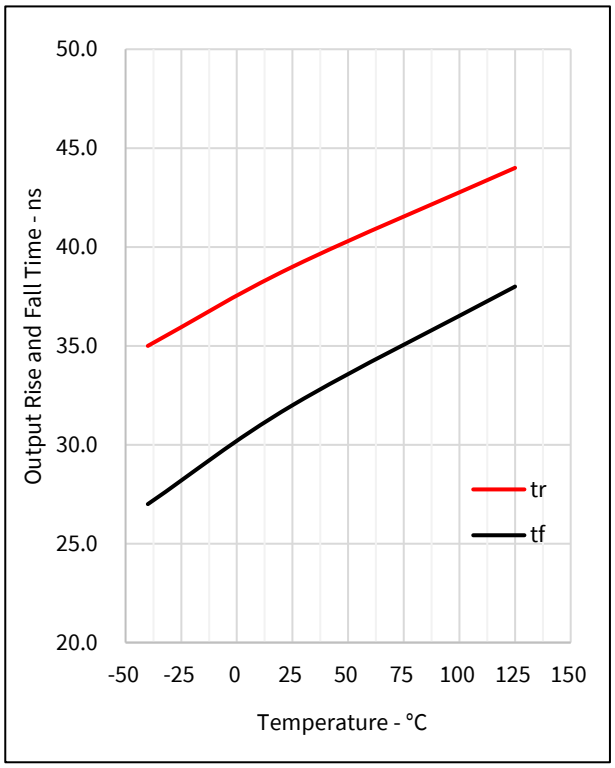


Figure 20 Output Rise Time and Fall Time vs Temperature

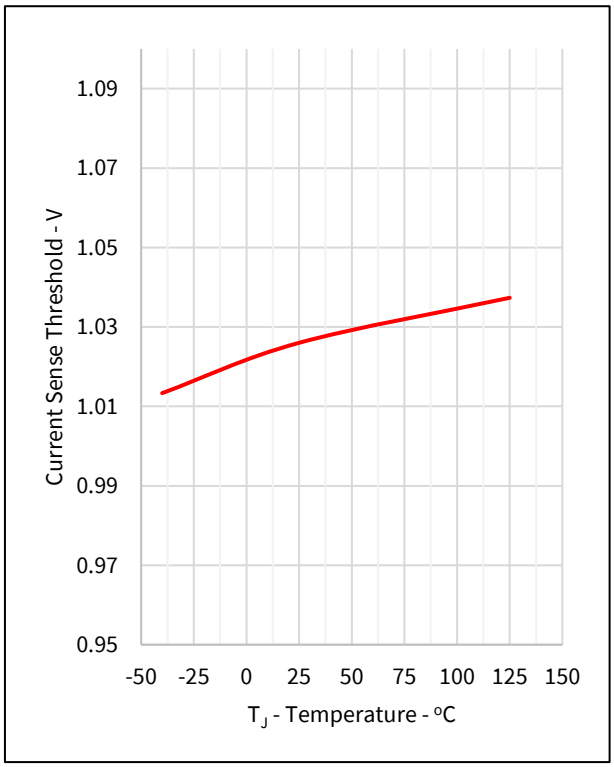


Figure 21 Current Sense Threshold Voltage vs Temperature

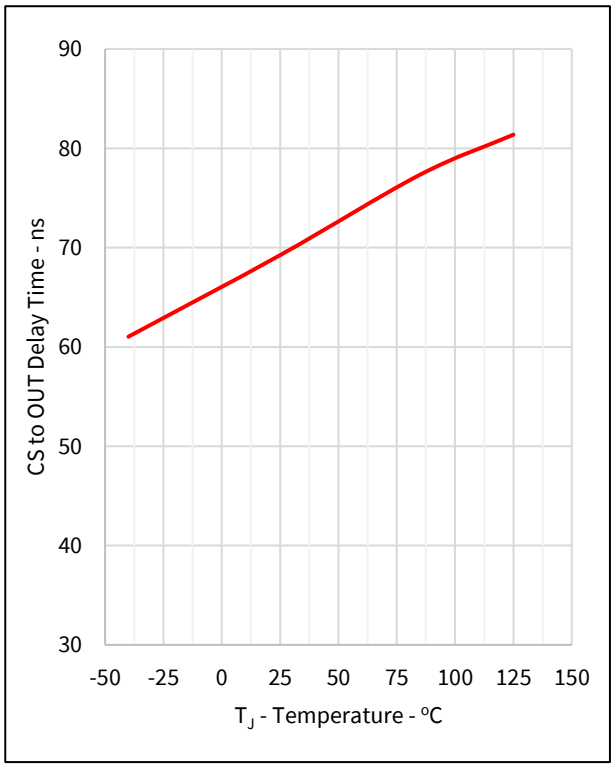


Figure 22 Current Sense Delay Time vs Temperature

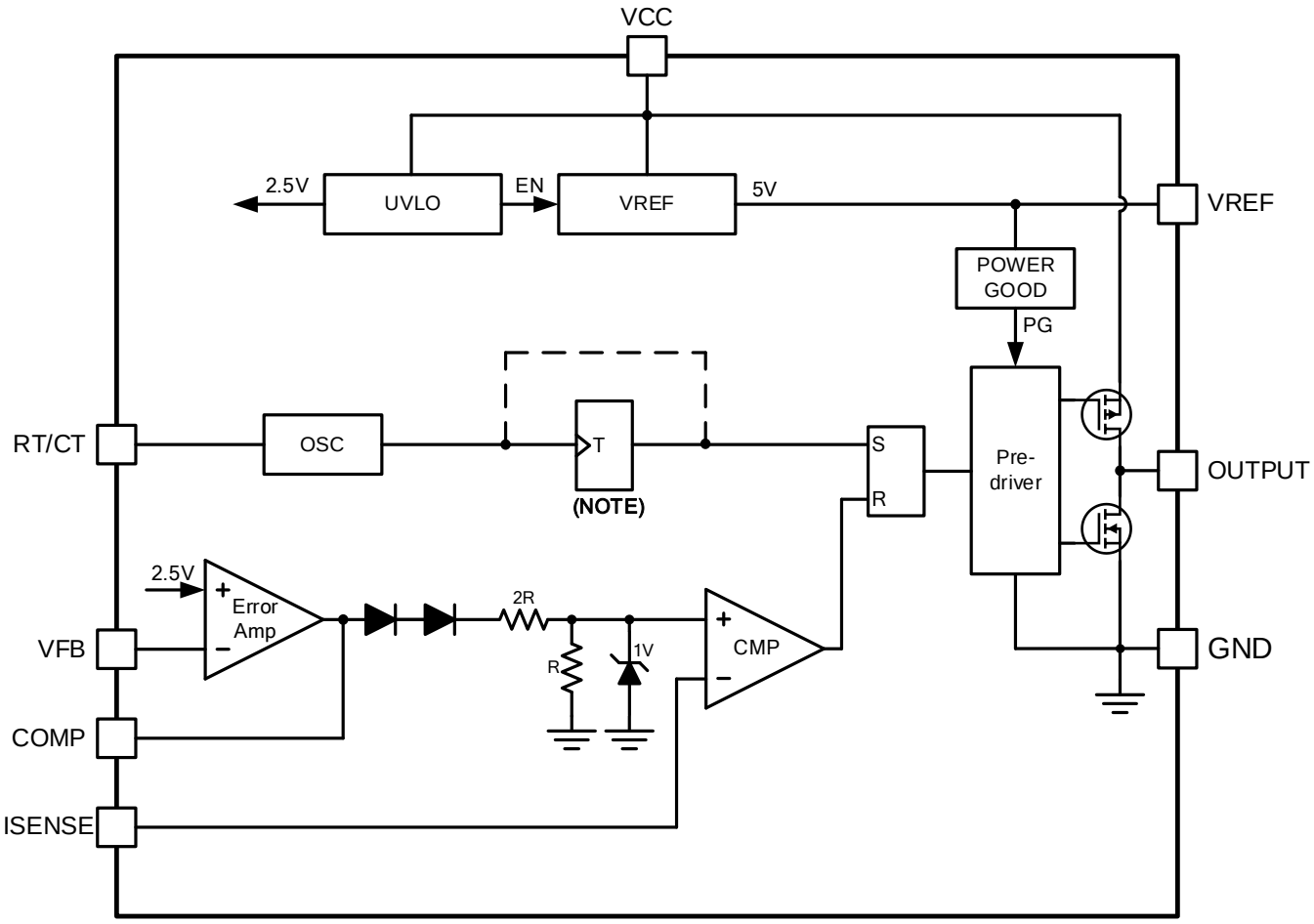
7. Detailed Description

7.1. Overview

The NSR28C4x series are high performance fixed frequency peak current mode controllers. They are designed for off-line and DC-DC applications with minimal external components. The integrated circuits include an oscillator, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output for driving an N-channel MOSFET.

The NSR28C4x series have built in features such as undervoltage lockout (UVLO) for input and reference, cycle−by−cycle current limiting. NSR28C42 and NSR28C44 feature a higher VCC turn-on or turn-off hysteresis suitable for off-line power supplies while NSR28C43 and NSR28C45 are suitable for DC-DC applications with narrower hysteresis range. An 8−pin surface mount SOP8 plastic package is available.

7.2. Block Diagram



Note: The T flip-flop only used in NSR28C44 and NSR28C45.

Figure 23 NSR28C4x Simplified Block Diagram

7.3. Feature Description

7.3.1. Under-voltage Lockout

The NSR28C4x series have a recommended input voltage up to 20V. When in low-voltage condition, the device integrates an under-voltage lock-out function to shut down the device when the input voltage falls below an internal threshold (STOP Threshold). This function ensures a proper supply voltage for internal circuits. There is also a lock-out

threshold hysteresis during under-voltage shutdown and re-start to avoid noise trigger for a well-designed system. Therefore, the startup voltage (START Threshold) will be slightly higher than the shutdown voltage (STOP Threshold).

It is worth noting that there are two types of UVLO voltage combinations for the NSR28C4x series. Among them, NSR28C43 and NSR28C45 have lower on/off voltage thresholds, while NSR28C42 and NSR28C44 have higher on/off voltage thresholds. It is necessary to select the chip version reasonably based on the input voltage range of specific application.

Table 1 NSR28C4x UVLO Options

Part Number	UVLO ON (Typ.)	UVLO OFF (Typ.)	Unit
NSR28C43/28C45	8.2	7.5	V
NSR28C42/28C44	15.5	9.5	V

7.3.2. Quiescent Current

When the device Vcc is power on but not up to START Threshold, the Vcc supply current is Startup Current, which is very important for the design of the high-voltage starting circuit of Flyback. Reasonable C_{VCC} capacitor and R_{START} resistance must be configured to ensure that the chips in applications can obtain sufficient energy to complete the conversion from the resistor start-up to auxiliary winding power supply.

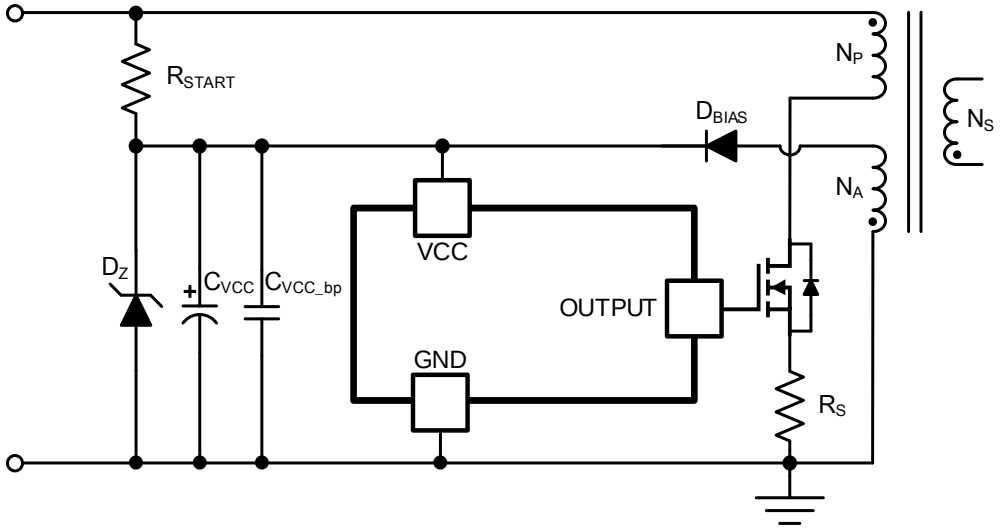


Figure 24 High Voltage Startup Circuit in Flyback Applications

It is worth noting that the chip periodically discharges the C_{CT} capacitor on the RT/CT in order to output a specific switching frequency driving. This part of the current will also manifest as the quiescent current of the chip. Therefore, the conditions in the EC table header are crucial.

When working in switching condition, the supply current is higher as internal driver works to charge and discharge external MOSFETs. Total Vcc current is the sum of quiescent current and the average driver output current. Knowing the operating frequency and the MOSFET gate charge (Q_g), average OUTPUT current can be calculated from below equation:

$$I_{Qg} = Q_g \times f_{SW} \quad (1)$$

7.3.3. VREF Voltage

VREF is supply voltage for many internal circuits in the IC, which is 5.1V reference voltage for the NSR28C4x family typically. Its primary purpose is to supply charging current to the oscillator timing capacitor C_{CT}. For the peripheral circuits of the chip, VREF functions similar to an LDO, providing necessary power for the peripheral circuits. To avoid excessive power consumption, the output short-circuit current is set to 40 mA (typical). To prevent device over-heating and damage, do not connect VREF to ground to stop switching. To ensure reference stability and avoid noise issues with high-speed switching transients, use a ceramic capacitor to bypass VREF to GND near the IC pinout. A ceramic capacitor of at least 0.1μF is needed and more VREF bypassing is needed for external loads on the VREF. In order to achieve better dynamic

response and stability, it is important to use ceramic capacitors and electrolytic capacitors in combination, while avoiding the use of only electrolytic capacitors.

7.3.4. Error Amplifier

There is a universal voltage-mode operational amplifier within the NSR28C4x family for error amplification. The positive input of the operational amplifier is connected to the internal 2.5V reference voltage, and the negative input is routed to the VFB pin. The output of the operational amplifier is routed to the COMP pin and connected to the internal PWM generation circuit, as shown in the figure below.

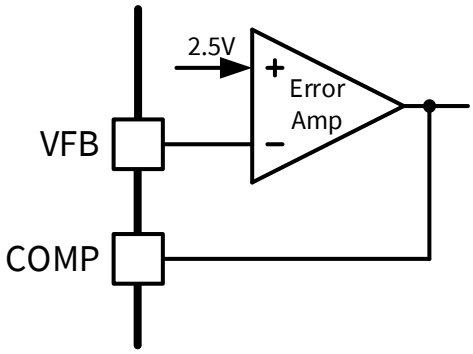


Figure 25 Error amplifier connection diagram

Error amplifier features a typical dc voltage gain of 90dB, and a unity gain bandwidth of 1.0MHz. The output of the error amplifier (COMP) has high sink and source current capabilities, as well as high voltage clamping of 5V typically.

7.3.5. Current Sense

The following figure shows the PWM generation logic in the peak current control mode. When the ISENSE voltage is greater than (COMP-Offset)/ACS, the PWM comparator is set low. The typical value of offset is 1.15V, and the typical value of ACS is 3.

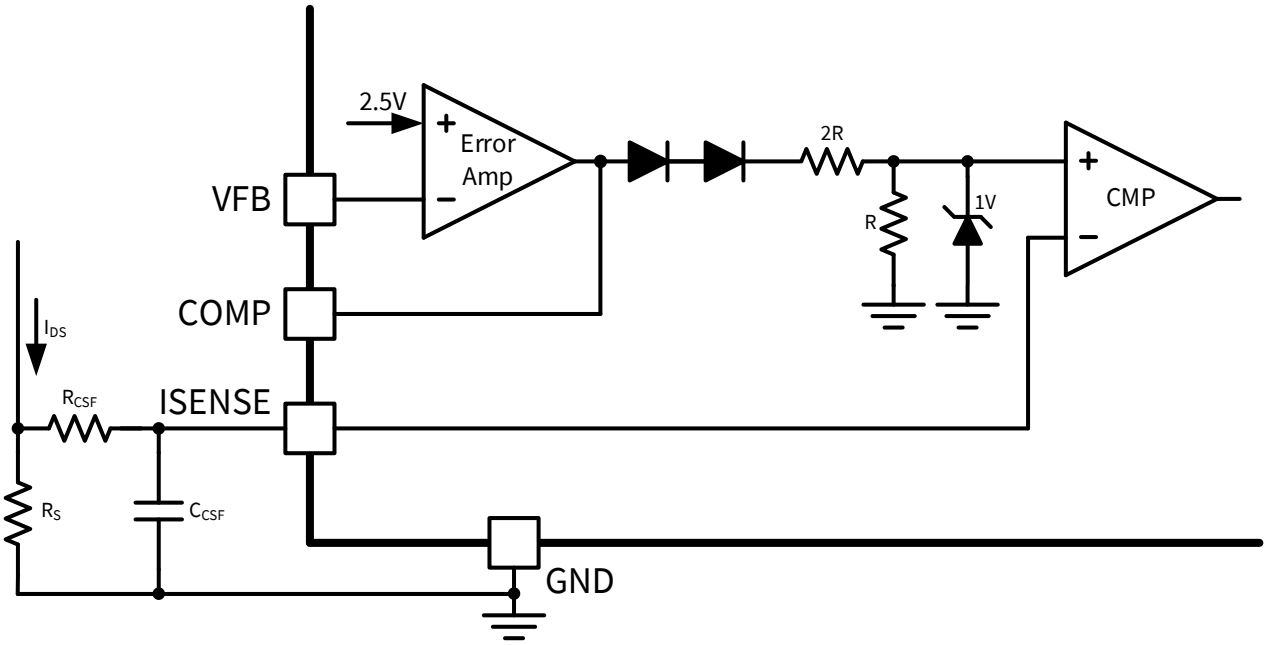


Figure 26 Current-Sense Circuit

NSR28C4x series have a cycle-by-cycle current limit function. When the ISENSE voltage exceeds 1V (Typ.), OUTPUT will be set low after ISENSE to OUTPUT delay until the next switching period arrives. Cycle-by-cycle current limit is built to limit inductor and MOSFET current when normal work. The specific peak current limit can be calculated using the following formula.

$$I_{peak} = \frac{1\ V\ (Typ.)}{R_S} \quad (2)$$

The 1V zener diode connected to the input of the PWM comparator is not an actual diode in the device design, but is only a schematic of a maximum ISENSE voltage input amplitude of 1V (Typ.). When ISENSE voltage reaches this threshold, cycle-by-cycle current limiting occurs regardless of the output voltage of the error amplifier, and the output pulse width is within 80ns (typical).

A small RC filter (R_{CSF} and C_{CSF}) is needed to suppress the switching transient noise on the sampling resistor R_S. The time constant of the filter should be about 5 to 10 times the OUTPUT rising time of the converter to avoid distortion of the current sampling waveform.

7.3.6. Oscillator

The NSR28C4x series oscillator design integrates a precise discharge current for operational frequency. In its primary function, the capacitor C_{CT} undergoes charging through a current source, established by the timing resistor R_{RT} connected to the device's reference voltage.

After power-on, VREF charges C_{CT} through R_{RT}. When the internal monitor detects that the RT/CT pin voltage reaches V_{CTH} (2.8V Typ.), it will start the internal current source to discharge C_{CT} at a current of 7.8mA (typical). During discharge, the oscillator outputs a low level. When the RT/CT pin voltage drops to V_{CTL} (1.1V Typ.), the internal current source will be turned off, and the oscillator will output a high level. After that, VREF recharges C_{CT} through R_{RT}, and the timing circuit starts a new cycle as shown in the figure below.

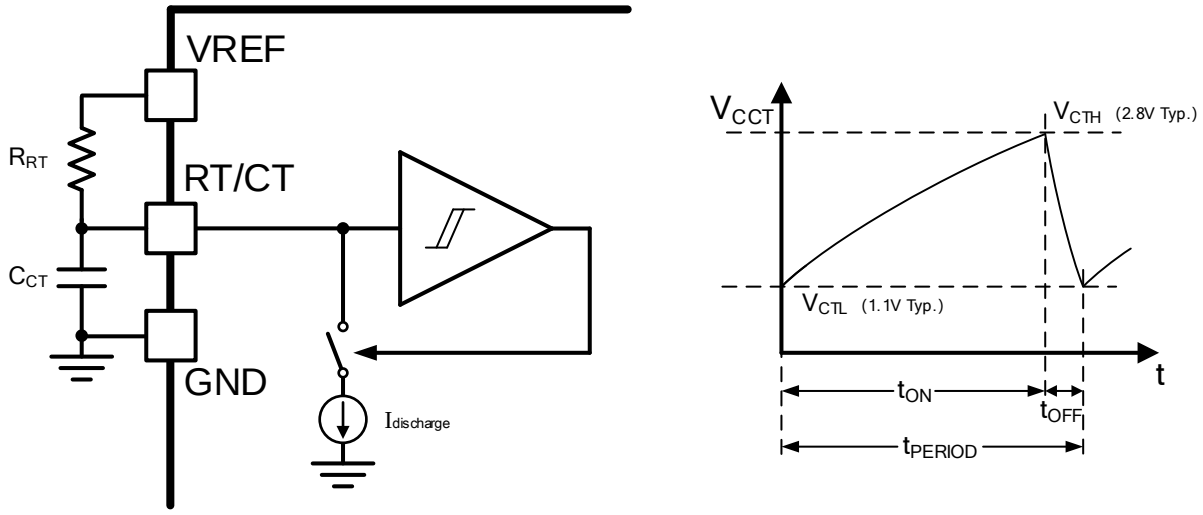


Figure 27 Oscillator Circuit

As can be seen from the above figure, while the internal current source discharges the C_{CT}, VREF also attempts to charge the C_{CT} at the same time. Therefore, the final discharge time of the C_{CT} is also affected by the R_{RT} resistance. In addition, it is worth noting that in order to provide a default 50% maximum duty cycle limit for the NSR28C44 and NSR28C45, the waveform output by the oscillator here also passes through a frequency-halving circuit. The estimation formula for switching frequency is $f_{SW} = f_{osc}$ for NSR28C42 and NSR28C43 and $f_{SW} = 0.5 * f_{osc}$ for NSR28C44 and NSR28C45.

$$f_{osc} = \frac{1}{t_{ON} + t_{OFF}} \quad (3)$$

In which

$$t_{ON} = -R_{RT} \cdot C_{CT} \cdot \ln\left(\frac{VREF - V_{CTH}}{VREF - V_{CTL}}\right) \quad (4)$$

$$t_{OFF} \approx \frac{C_{CT} \cdot (V_{CTH} - V_{CTL})}{I_{discharge} - \left(\frac{VREF - 0.5 \cdot (V_{CTH} + V_{CTL})}{R_{RT}}\right)} \quad (5)$$

7.3.7. Driver Output

Peak output current capability of NSR28C4x series is up to 1A. The internal driver resistance for both high-side and low-side is low to offer a quick transition for external MOSFET which helps with lower switching power loss.
NSR28C4x series contain a single totem pole output stage that was specifically designed for direct drive of power MOSFETs. It has a typical rise time of 40ns and fall time of 30ns with a 1.0nF capacitor load. Due to the high-side PMOS in the chip drive output being pulled up to VCC, the drive pulse high voltage of the OUTPUT equals to the VCC voltage, which enriches the application of chip drives for various power transistors.

7.3.8. Enable and Disable

Due to the lack of an EN pin on the chip, it is not possible to enable and disable the NSR28C4x series using general methods. However, there are some special methods that can achieve similar effects. For example:
1. Pull down the COMP to ground pin through the MOSFET. In fact, when the COMP voltage is less than $2*V_{BE}$, the chip will internally pull OUTPUT to ground to achieve the purpose of disabling the chip.
2. By supplying ISENSE with a continuous voltage of more than 1.1V. Due to the cycle-by-cycle current limit protection, when the ISENSE voltage exceeds 1V, after ISENSE to OUTPUT Delay, the chip will also internally ground OUTPUT.

8. Typical Application

NSR28C4x series are designed for boost, Flyback and other switching DC-DC topologies suitable for peak current mode control with low-side switches.

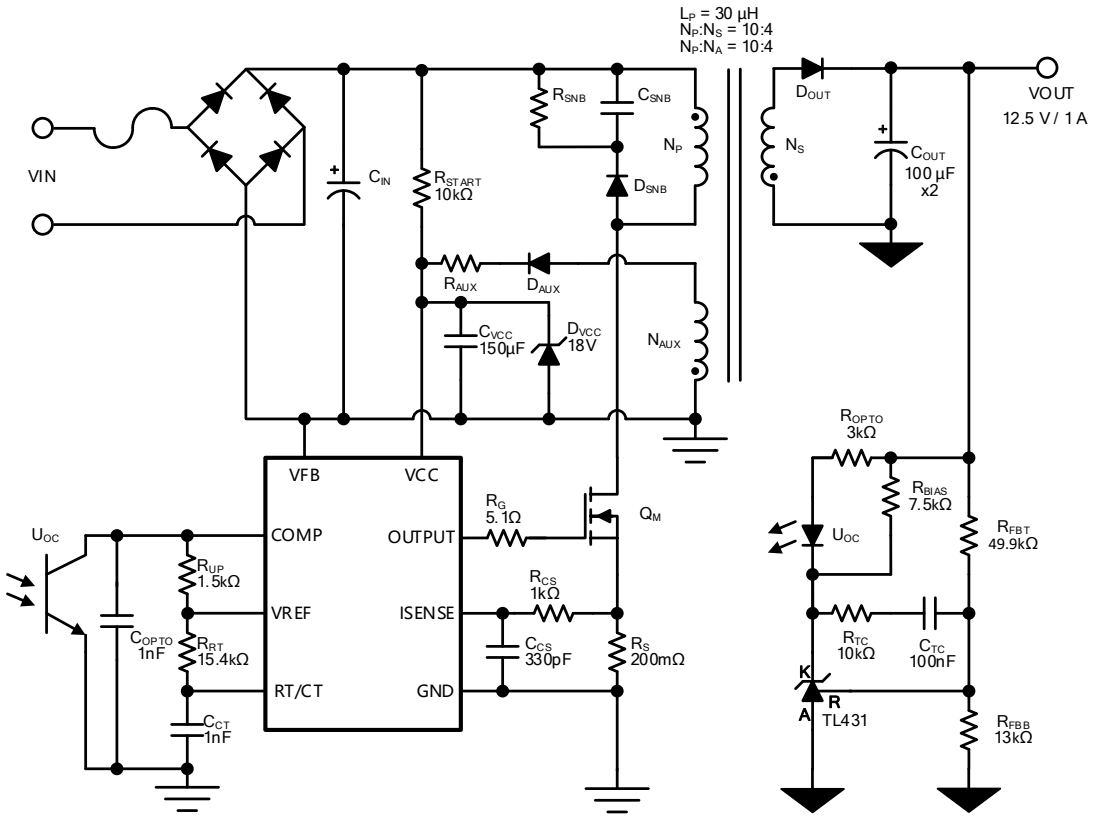


Figure 28 Typical Flyback Converter Connection with NSR28C4x

8.1. Transfer Function Basis

A DC-DC converter in application is a typical closed-loop control system which can be described as below flow chart:

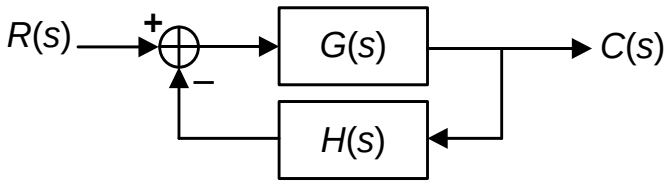


Figure 29 Closed-loop Control Flow Chart

Where G(s) can be considered as the transfer function of power stage while H(s) is the compensation section. As loop stability performance of small signal is directly determined by closed-loop transfer function expressed as below:

$$G_{\mathrm{CLOSED}}(s) = \frac{G(s)}{1 + G(s)H(s)} \tag{6}$$

The most straightforward method to check response caused by certain distributing is calculation with closed-loop transfer function from s-domain to time-domain. Frequency stability criterion is a more simple way which is equivalent to Nyquist stability criterion. The frequency stability criterion checks gain and phase curves versus frequency, which is commonly called Bode plot of open-loop transfer function

$$G_{\mathrm{OPEN}}(s) = G(s)H(s) \tag{7}$$

8.2. Overall Control Block Diagram

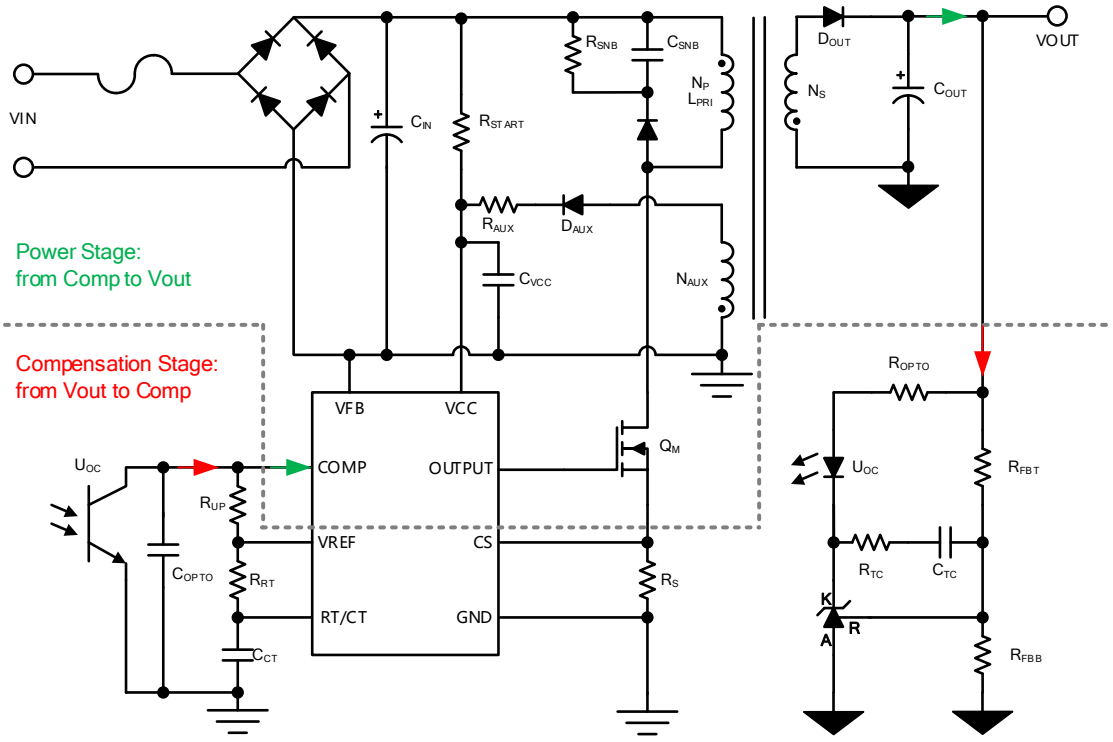


Figure 30 Flyback Converter Overall Control Block Diagram

8.3. Transfer Function and Pole-zero Location of Power Stage

In a DCM Flyback converter with peak-current-mode control and an operational transconductance amplifier (OTA) as major control component, when feedback signal come from resistance divider of auxiliary winding output which share common ground with primary winding, the power stage transfer function can be derived as below:

$$G(s) = A_{VCD} \frac{\left(1 - \frac{s}{\omega_R}\right) \cdot \left(1 + \frac{s}{\omega_{\mathrm{ESR}}}\right)}{\left(1 + \frac{s}{\omega_P}\right) \cdot \left(1 + \frac{s}{\omega_L}\right)} \tag{8}$$

Where:

$$A_{VCD} = \frac{V_{\mathrm{IN}}}{S_N + S_A} \cdot \sqrt{\frac{f_{SW} \cdot R_{LOAD}}{2 \cdot L_{PRI}}} \tag{9}$$

V_{IN} is input voltage of power stage, f_{SW} is working frequency of Flyback converter, R_{LOAD} is equivalent load resistance of output rails, L_{PRI} is primary inductance of transformer， S_A is voltage slope of internal compensation. S_N is voltage slope between current sense resistor when MOSFET is ON and primary current rises:

$$S_N = R_S \frac{V_{\mathrm{IN}}}{L_{\mathrm{PRI}}} \tag{10}$$

The angular frequency of pole from main power is:

$$\omega_P = \frac{2}{R_{LOAD} \cdot C_{\mathrm{OUT}}} \tag{11}$$

In a DCM Flyback converter with PCM control, there is a high-frequency pole from primary inductance and slop compensation:

$$\omega_L = \frac{2 \cdot f_{SW} \cdot M_R}{(M_R + 1) \cdot \text{Duty}} \quad (12)$$

Where M_R is voltage transition ratio from primary input voltage to secondary output voltage:

$$M_R = \frac{N_P \cdot V_{OUT}}{N_S \cdot V_{IN}} \quad (4)$$

When output capacitor has a equivalent series resistance (ESR), there is a zero lays at below angular frequency:

$$\omega_{\text{ESR}} = \frac{1}{C_{\text{OUT}} \cdot R_{ESR}} \quad (14)$$

There is also a right half plane zero (RHPZ) in a current-loop Flyback:

$$\omega_R = \frac{R_{LOAD} \cdot {N_P}^2}{(1 + M_R) \cdot M_R \cdot L_{\text{PRI}} \cdot {N_S}^2} \quad (15)$$

8.4. Transfer Function and Pole-zero Location of Compensation Stage

For transfer function of compensation section it can be expressed when C_C >> C_{HF} and output resistance of amplifier >> R_C:

$$H(s) = \frac{\text{CTR} \cdot R_{UP}}{A_{CS} \cdot R_{\text{OPTO}} \cdot C_{\text{TC}} \cdot R_{\text{FBT}}} \cdot \frac{1 + \frac{s}{\omega_{COMPZ}}}{s \cdot \left(1 + \frac{s}{\omega_{COMPP}}\right)} \quad (16)$$

Where ACS = 3 in NSR28C4x series.

$$\omega_{\text{COMPZ}} = \frac{1}{(R_{\text{TC}} + R_{FBT}) \cdot C_{\text{TC}}} \quad (17)$$

$$\omega_{\text{COMPP}} = \frac{1}{R_{\text{UP}} \cdot C_{\text{OPTO}}} \quad (5)$$

8.5. Loop Stability Analysis

From above equations, any change of some components could cause significant changes to loop stability. In a typically designed CCM flyback converter, when component changed, influential changes on loop stability is summarized in below table:

Table 2 Loop Stability Analysis

Component Changes	Influence on Transfer Function	Typical Influence on Bode Plot
Increase L_{PRI}	Higher A_{VCD}	Wider bandwidth
Increase C_{OUT}	Lower ω_P	Lower bandwidth
Increase ESR of C_{OUT}	Lower ω_{ESR}	Earlier boost on phase at high frequency
Increase R_S	Lower A_{VCD}	Lower bandwidth
Increase R_{TC}	Lower ω_{COMPZ}	Earlier boost on gain and phase at low frequency
Increase C_{TC}	Lower ω_{COMPZ}	Earlier boost on gain and phase at low frequency

8.6. Layout Guide

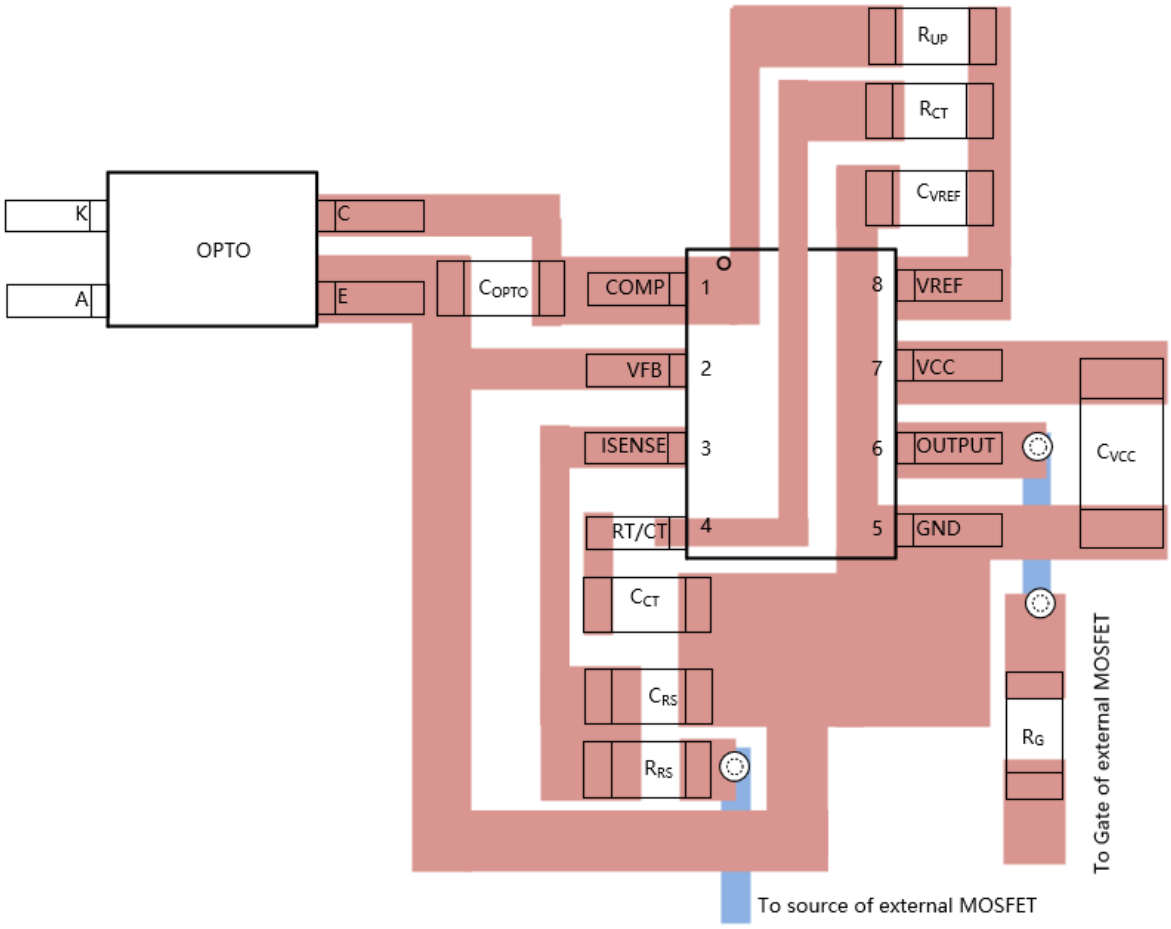
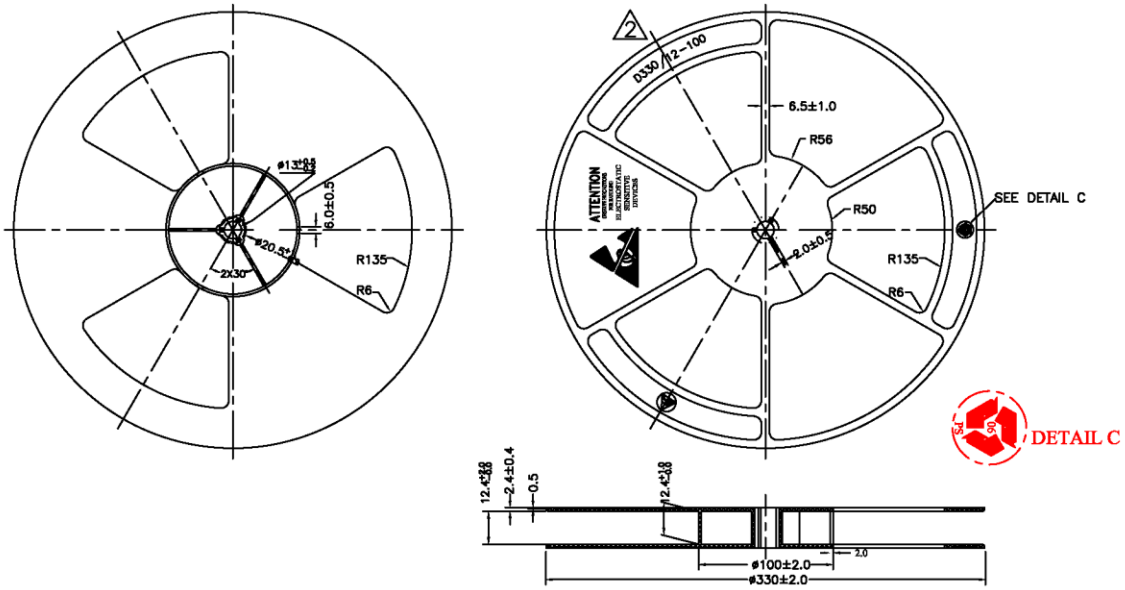


Figure 31 Layout Reference for NSR28C4x Typical Application Circuits

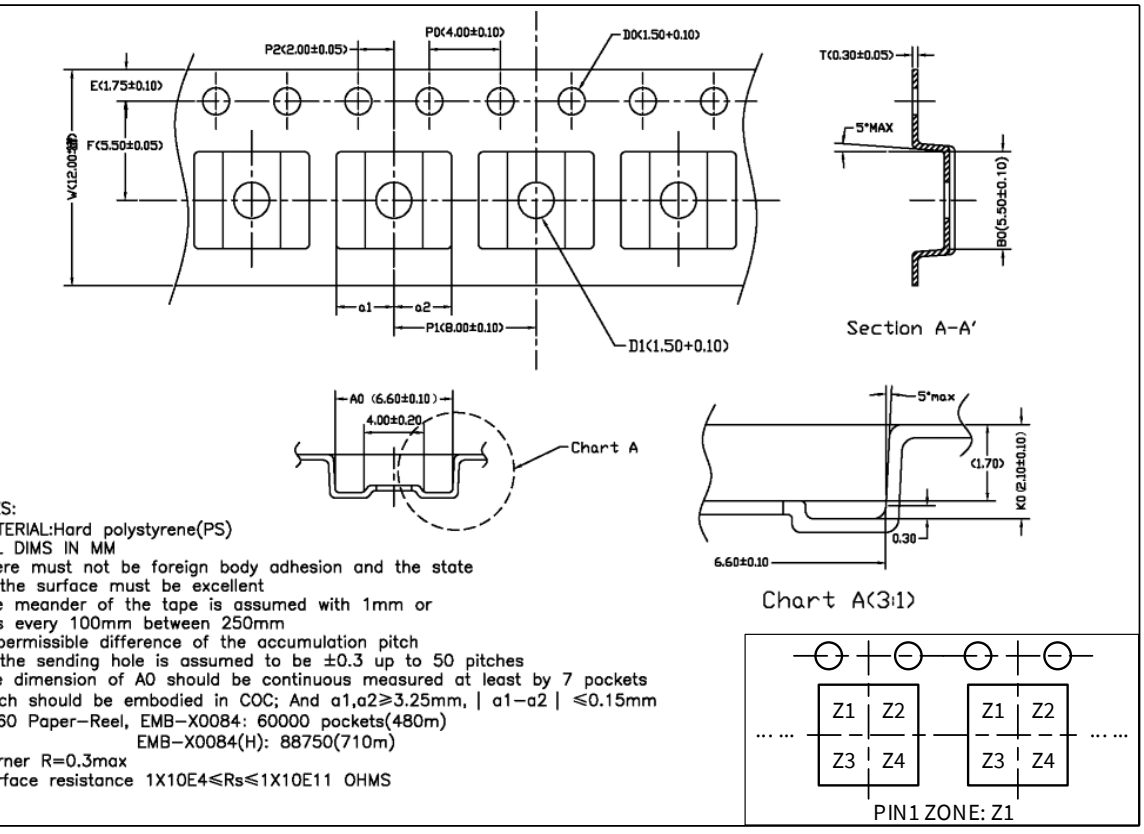
9. Package Information

9.1. SOP8

9.1.1. Tape and Reel

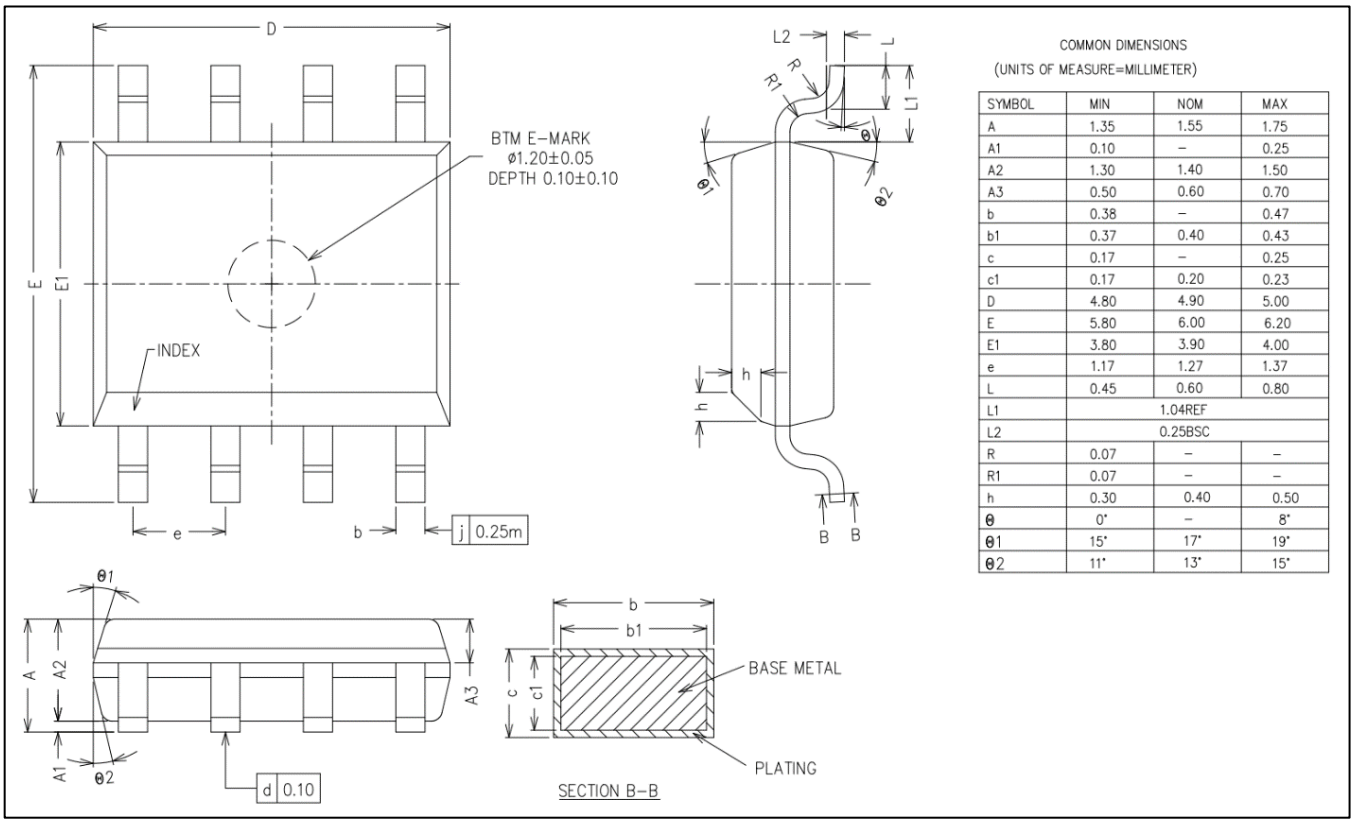


NOTES:
1. MATERIAL: POLYSTYRENE (BLACK).
2. ALL DIMENSIONS NOTED ARE IN MILLIMETERS.
3. TOLERANCE ON ALL DIMENSIONS (NOT OTHERWISE NOTED) IS ±0.25.



NOTES:
1.MATERIAL:Hard polystyrene(PS)
2.ALL DIMS IN MM
3.There must not be foreign body adhesion and the state of the surface must be excellent
4.The meander of the tape is assumed with 1mm or less every 100mm between 250mm
5.A permissible difference of the accumulation pitch of the sending hole is assumed to be ±0.3 up to 50 pitches
6.The dimension of A0 should be continuous measured at least by 7 pockets which should be embodied in COC; And a1,a2≥3.25mm, | a1−a2 | ≤0.15mm
3 7.ø560 Paper−Reel, EMB−X0084: 60000 pockets(480m)
EMB−X0084(H): 88750(710m)
8.Corner R=0.3max
4 9.Surface resistance 1X10E4≤Rs≤1X10E11 OHMS

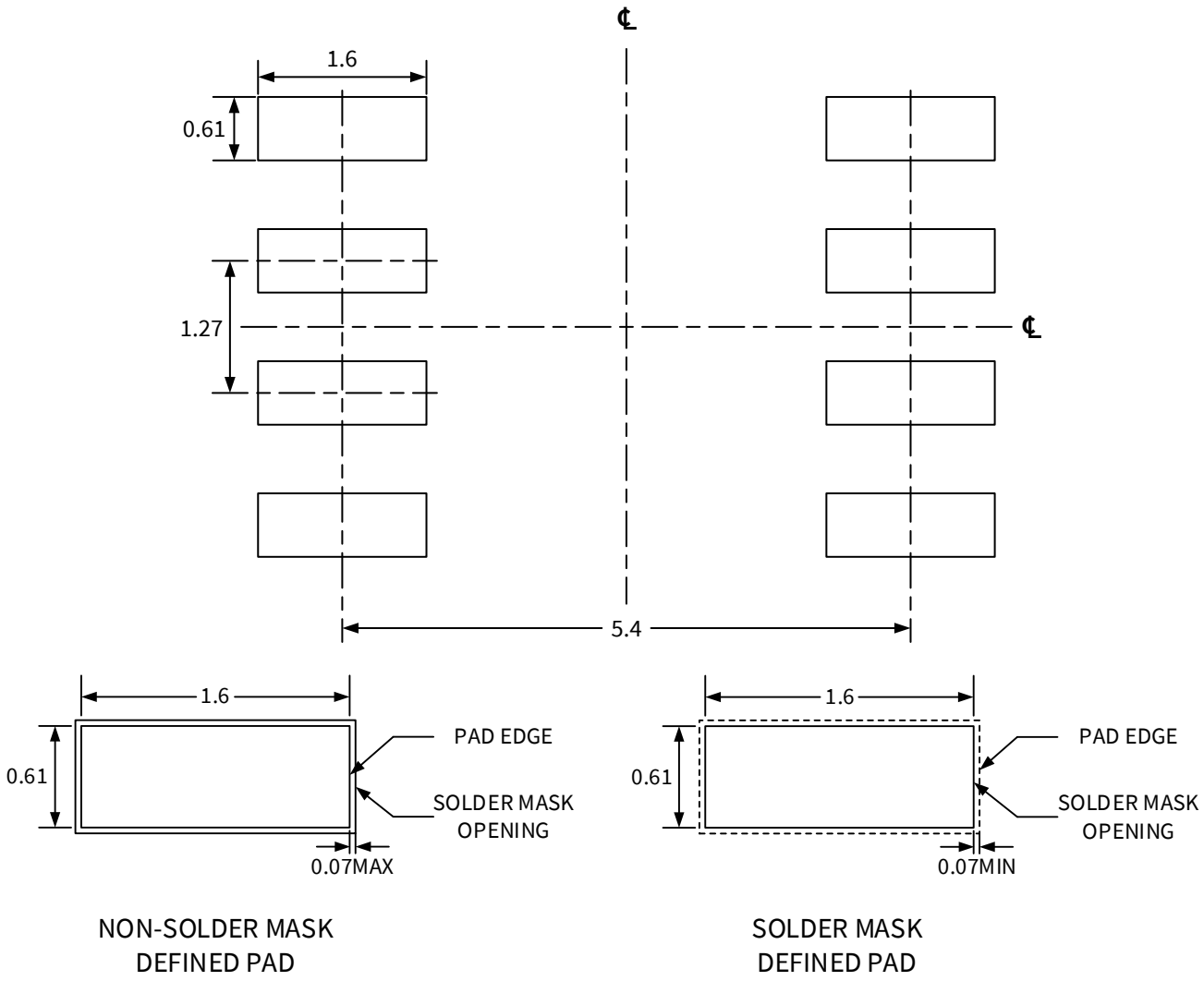
9.1.2. Mechanical Data



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	–	0.25
A2	1.30	1.40	1.50
A3	0.50	0.60	0.70
b	0.38	–	0.47
b1	0.37	0.40	0.43
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.17	1.27	1.37
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
θ	0°	–	8°
θ1	15°	17°	19°
θ2	11°	13°	15°

9.1.3. Recommended Land Pattern



10. Order Information

Orderable Part Number	MSL	Package	SPQ	Marking
NSR28C42-DSPR	1	SOP8	2500	C2842
NSR28C43-DSPR	1	SOP8	2500	C2843
NSR28C44-DSPR	1	SOP8	2500	C2844
NSR28C45-DSPR	1	SOP8	2500	C2845

11. Revision history

Revision	Description	Date
1.0	Initial	2025/06

IMPORTANT NOTICE

The information given in this document (the “Document”) shall in no event be regarded as any warranty or authorization of, express or implied, including but not limited to accuracy, completeness, merchantability, fitness for a particular purpose or infringement of any third party’s intellectual property rights.

Users of this Document shall be solely responsible for the use of NOVOSENSE’s products and applications, and for the safety thereof. Users shall comply with all laws, regulations and requirements related to NOVOSENSE’s products and applications, although information or support related to any application may still be provided by NOVOSENSE.

This Document is provided on an “AS IS” basis, and is intended only for skilled developers designing with NOVOSENSE’s products. NOVOSENSE reserves the rights to make corrections, modifications, enhancements, improvements or other changes to the products and services provided without notice. NOVOSENSE authorizes users to use this Document exclusively for the development of relevant applications or systems designed to integrate NOVOSENSE’s products. No license to any intellectual property rights of NOVOSENSE is granted by implication or otherwise. Using this Document for any other purpose, or any unauthorized reproduction or display of this Document is strictly prohibited. In no event shall NOVOSENSE be liable for any claims, damages, costs, losses or liabilities arising out of or in connection with this Document or the use of this Document.

For further information on applications, products and technologies, please contact NOVOSENSE (www.novosns.com).

Suzhou NOVOSENSE Microelectronics Co., Ltd