NSL23716x

16-CH Low Side LED Driver with Differential or UART Interface

Datasheet (EN) 1.0

NOVOSENSE

Product Overview

The NSL23716 is a 16-channel, 20-V low side LED driver with 100mA maximum current of each channel, and the integration with a differential interface, which is compatible with CAN transceivers, making it a suitable selection for the automotive exterior dynamic rear lighting application with differential interface. Furthermore, devices with UART interface are also available. In this case, an external CAN physical layer can be used for off-board communication with good EMC performance.

As a constant current regulator, a 12-bit PWM dimming register for each LED channel is employed in NSL23716, which can be utilized for brightness control.

To optimize the EMC performance, spread spectrum is designed in this IC, and phase shift between channels can be programmed to reduce the pulse power stress as well.

NSL23716 provides full diagnostics including LED open/short and over temperature protection with FAULT indicator. And the retry behavior which can be programed will release FAULT bus when channel fault is removed. In addition, two FS (fail safe) modes are integrated for the application without MCU or communication loss.

The OTP (one time programmable) for FS is provided to extend the flexibility in application.

QFN32 (5*6/4*4) packages are available, and both the devices are AEC-Q100 qualified.

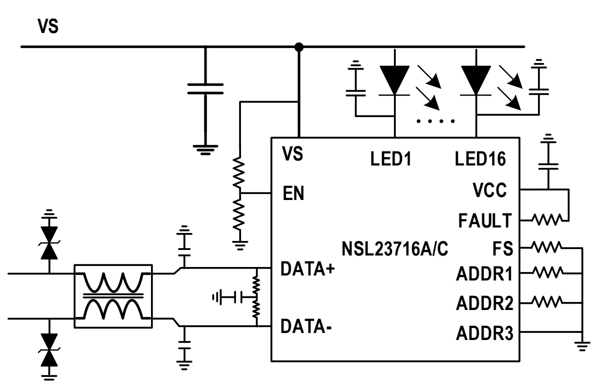
Key Features

- AEC-Q100 Qualified for Automotive Grade 1: T_A from −40 °C to 125 °C
- RoHS Compliant
- 3.7 V to 20 V wide supply voltage range
- 16-Channel, 100mA/ch max (channels can be paralleled)
- Cascade up to 16 ICs to support up to 256 channels
- Pin-programmable device address
- Maximum dropout: 800 mV at 100 mA
- 2Mbps differential/UART interface
- 12-bit PWM dimming for each channel
- Programmable phase shift
- Frequency spread spectrum (internal clock)
- EN control pin to enable/disable device for low power operation
- Full protection and diagnostics:
  1. LED open-load detection
  2. LED short-to-GND/Battery detection
  3. ISET pin open/short
  4. Thermal warning and derating
  5. Thermal shutdown
- One-time Programmable Memory (OTP)
- QFN-32 (5mm x 6mm) /(4mm x 4mm) Wettable Flank

Applications

- Automotive exterior dynamic rear lighting: position light, fog light, stop light, taillight.
- Automotive miscellaneous exterior lighting: center high mounted stop lamp, daytime-running lamp, turn indicator, door handle, blind spot detection indicator.
- Automotive interior lighting: reading lamp, overhead console.
- Matrix Headlamps
- General-purpose LED driver applications

Typical Application Diagram



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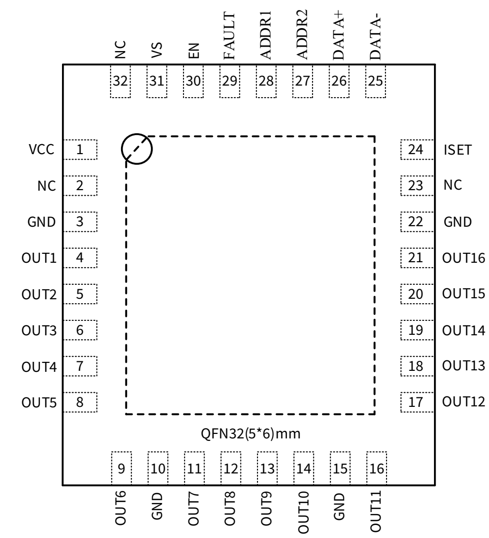
1. Device Comparison Table

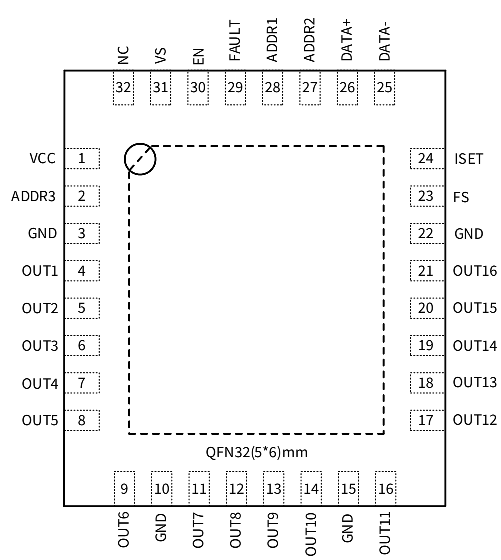
PN	Interface	Fail safe	ADDR Configuration	ADDR_OTP Bit	Package
NSL23716A-Q1QAMR	Differential interface	NO	ADDR_OTPbit+ADDR1/2	0	QFN32(5mm*6mm)
NSL237161A-Q1QAMR				1	
NSL23716C-Q1QAMR	Differential interface	YES	ADDR1/2/3 pin	/	
NSL23716D-Q1QAMR	UART interface				
NSL23716C-Q1QALR	Differential interface				QFN32(4mm*4mm)
NSL23716D-Q1QALR	UART interface				

2. Pin Configuration and Function

NSL23716(1)A-Q1QAMR



NSL23716C-Q1QAMR



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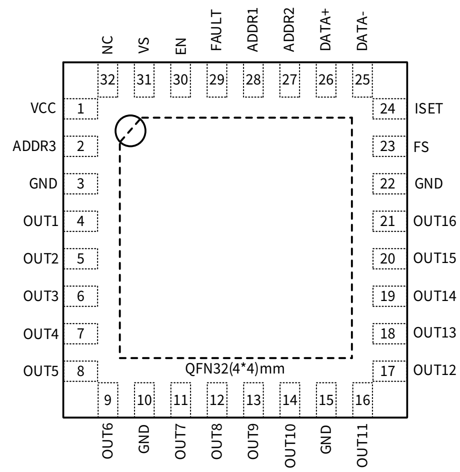
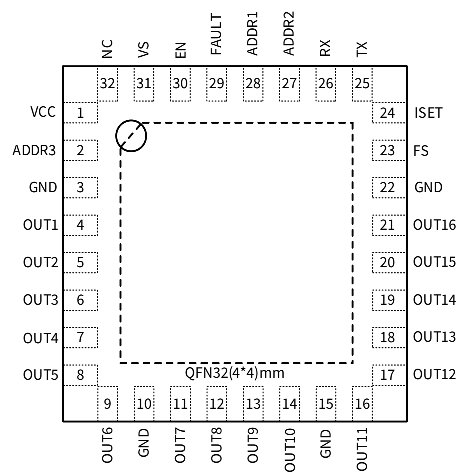
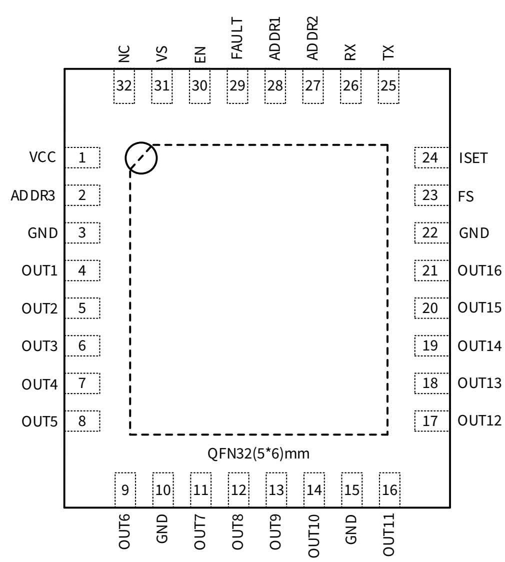


NSL23716D-Q1QALR



NSL23716D-Q1QAMR



NSL23716x Pin Configuration and Description

PIN NO.	NSL23716A	NSL23716C	NSL23716D	FUNCTION
1	VCC			Internal LDO output from VS. Place a ≥10μF decoupling capacitor to ground is required close to VCC.
2	NC	ADDR3		Address setting. Program part address with connecting to VCC/GND. Detail see Chip Address section. Not connected for NSL23716(1)A.
3，10，15，22	GND			GND is the reference ground of the power device and requires careful consideration during PCB layout.
4-9，11-14，16-21	OUT1-OUT16			LED current sink pins. Connect the LED channel 1-16 cathode to these pins. Connect to GND if LEDx is not used and disable it through the CHx_EN (0x03).
23	NC	FS		Fail safe input. Not connected for NSL23716(1)A.
24	ISET			LED current set pin. Connect an external resistor from ISET to ground to set the LED current, the ILED/Channel (mA) = 600/RISET(kΩ).
25	DATA-		TX	Differential interface negative for NSL23716A/C. UART Transmit for NSL23716D.
26	DATA+		RX	Differential interface positive for NSL23716A/C. UART Receive for NSL23716D.
27	ADDR2			Address setting. Program part address with connecting to VCC/ GND or a 35kΩ resistor to GND. Detail see Chip Address section.
28	ADDR1			Address setting. Program part address with connecting to VCC/ GND or a 35kΩ resistor to GND. Detail see Chip Address section.
29	FAULT			Fault output. OFAL (one fails all fail)/OFOO (one fails others on) can be achieved though connecting FAULT pin together (in FS mode).
30	EN			Enable input. Pull pin EN high to enable the part and pull EN pin low to shut down the part. EN pin can be pulled to VBIAS directly.
31	VS			Power supply. Requires capacitor to decouple the input rail.
32	NC			Not connected.
Thermal Pad	Thermal pad			Suggest to connect to GND.

3. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
Supply voltage	VS	−0.3	24	V
High voltage input	DATA+, DATA-, EN, FAULT	−0.3	24	V
High voltage output	OUTx	−0.3	24	V
All other pins	VCC, FS, ADDRx, ISET, RX, TX	−0.3	5.5	V
Ambient temperature	T_A	−40	125	°C
Junction temperature	T_J	−40	150	°C

Storage temperature	T_{stg}	−40	150	°C

4. ESD Ratings

Parameters	*Symbol*		*Valus*	*Unit*
Electrostatic discharge, Human-body model	Human body model (HBM), per AEC-Q100-002-RevD		±2000	V
Electrostatic discharge, Charged-device model	Charged device model (CDM), per AEC-Q100-011-RevB	All pins	±500	V
		Corner pins (1,8,9,16,17,24,25,32)	±750	V

5. Recommended Operating Conditions

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Supply voltage	VS	3.7		20	V
High voltage input	DATA+, DATA-, EN, FAULT	0		20	V
High voltage output	OUTx	0		20	V
All other pins	VCC, FS, ADDRx, ISET, RX, TX	0		5	V

6. Thermal Information

QFN32-5*6

Parameters	*Symbol*	*QFN32-5*6*	*Unit*
IC Junction-to-Air Thermal Resistance	θ_{JA}	27.8	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC(TOP)}$	15.5	°C/W
Junction-to-case (bottom) thermal resistance	$\theta_{JC(BOT)}$	4	°C/W
Junction-to-board thermal resistance	θ_{JB}	10.5	°C/W
Junction-to-top characterization parameter	ψ_{JT}	1.7	°C/W
Junction-to-board characterization parameter	ψ_{JB}	10.8	°C/W

QFN32-4*4

Parameters	*Symbol*	*QFN32-4*4*	*Unit*
IC Junction-to-Air Thermal Resistance	θ_{JA}	36.6	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC(TOP)}$	22.1	°C/W
Junction-to-case (bottom) thermal resistance	$\theta_{JC(BOT)}$	6.1	°C/W
Junction-to-board thermal resistance	θ_{JB}	14	°C/W

Parameters	*Symbol*	*QFN32-4*4*	*Unit*
Junction-to-top characterization parameter	ψ_{JT}	2.7	°C/W
Junction-to-board characterization parameter	ψ_{JB}	14.7	°C/W

7. Specifications

7.1. Electrical Characteristics

(V_{VS} = 6.5V, T_J = -40°C to +125°C, unless otherwise noted, typical values are at T_J = +25°C.)

Parameters	*Symbol*	*Condition*	*Min*	*Typ*	*Max*	*Unit*
Power Supply						
Supply voltage	VS	VCC=3.3V(NSL23716(1)A)	3.7		20	V
Supply voltage	VS	VCC=5V(NSL23716C/D)	5.5		20	V
VS Supply Current	I_{VS}	Disabled mode, EN pin is low (Shutdown)		0.5	2.5	µA
		Enabled, channel off (EN pin is high, EN_ANA bit=0) (Quiescent), VS = 6.5V		2.5	3.5	mA
		Enabled, No LED Load， channel on(EN pin is high, EN_ANA bit=1) (Quiescent), VS = 6.5V		11	13	mA
Internal VCC Regulator Voltage	VCC	I_{VCC}=0mA, NSL23716A/NSL237161A	3.1	3.3	3.5	V
Internal VCC Regulator Voltage	VCC	I_{VCC}=0mA, NSL23716C/NSL23716D	4.65	5	5.35	V
VCC Current Limit	I_{VCC_MAX}		70			mA
VS UVLO Threshold	VS_UVLO	VS rising edge		3.5	3.7	V
		VS falling edge	3.2	3.4		V
EN Input Threshold	V_{EN_H}	EN high level logic input	2.2			V
	V_{EN_L}	EN low level logic input			0.8	V
LED Stage						
Dropout Voltage		When the current drop to 95% of set current(100mA)			800	mV
ISET Voltage	V_{ISET}	Floating	585	600	615	mV
Channel Output Leakage Current	I_{LKG}	PWM = 0% (a single channel) -40°C ~125°C			2	µA
		PWM = 0% (all 16 channels) -40°C ~125°C			32	µA
Channel to Channel Current Error	I_{EER_CC}	ERR_CC = (I_{OUTx}-I_{AVE})/I_{AVE}×100% @Iout>20mA	-5%		+5%	

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Device to Device Accuracy	I_{EER_DD}	ERR_DD = (I_{OUTx}-I_{SET})/I_{SET}×100% @Iout>20mA	-5%		+5%	
PWM						
PWM Frequency	F_{PWM}	Default setting	212	250	286	Hz
PWM Frequency Range		Program range	250		1000	Hz
PWM Duty Step(1)	t_{PWM}	12-bit resolution, F_{PWM} = 250Hz	0.8	1	1.2	µs
Phase Shift Delay(1)	t_{Delay}	PHASE_SHIFT[1:0] = 11	16	20	24	µs
Diagnosis and Protection						
Short LED String Protection Threshold	V_{LED_S}	LED_SHORT_THR [1:0] = 00	1.8	2	2.2	V
Open LED String Protection Threshold	V_{LED_O}	LED fully on, real-time monitoring (cover pin short-to-GND)	250	300	350	mV
Short/open LED String Deglitch Time	$T_{LED\_S/O}$	@250Hz V_{LEDx} > V_{LED_S}/V_{LEDx}<V_{LED_O}	90	120	150	µs
ISET Current Threshold for Pin Short	I_{ISET_sth}		126	180	232	µA
ISET Current Threshold for Pin Open	I_{ISET_oth}	Corresponding to RISET = 120kΩ	2	5	7	µA
FAULT & FS PIN						
FAULT Logic Input High Threshold	V_{FAULT_IH}		2			V
FAULT Logic Input Low Threshold	V_{FAULT_IL}				0.7	V
FAULT Low Output Level	V_{Fault_OL}	I_{Fault_OL}=2mA active	0.15		0.5	V
FAULT Input Current Leakage	I_{F_LKG}				1	µA
FS Logic Input High Threshold	V_{FS_IH}		2			V
FS Logic Input Low Threshold	V_{FS_IL}				0.7	V
Driver(VCC=3.3V)						
Bus Output Voltage (recessive)	V_O(R)	RL = 180Ω, VCC=3.3V	1.5	1.65	1.8	V
Bus Output Voltage (DATA+) (dominant)	V_O(D+)	RL = 180Ω, VCC=3.3V	2.35	2.7	3.05	V
Bus Output Voltage (DATA-) (dominant)	V_O(D-)	RL = 180Ω, VCC=3.3V	0.5	0.6	0.7	V
Differential Output Voltage (dominant)	V_{OD}(D)	RL = 180Ω VCC=3.3V	1.8	2.1	2.4	V
Output Symmetry (dominant or recessive)	V_{SYM}	VCC=3.3V, VO(DATA+) + VO(DATA-)	3	3.3	3.6	V

Parameters	Symbol	Condition		Min	Typ	Max	Unit
Differential Output Rising Time[1]	t_r	RL=180Ω, CL=50pF, VCC=3.3V.		13	17	26	ns
Differential Output Falling Time[1]	t_f	RL=180Ω, CL=50pF, VCC=3.3V.		13	16	26	ns
Propagation Delay Time, low-to high level[1]	$t_{p(L2H)D}$	RL=180Ω, CL=50pF, VCC=3.3V. Refer to figure 1.2		22	28	38	ns
Propagation Delay Time, high-to low level[1]	$t_{p(H2L)D}$	RL=180Ω, CL=50pF, VCC=3.3V. Refer to figure 1.2		26	32	43	ns
Driver(VCC=5V)							
Bus Output Voltage (recessive)	$V_O(R)$	RL = 180Ω, VCC=5V		2.3	2.5	2.7	V
Bus Output Voltage (dominant)	$V_O(D+)$	RL = 180Ω, VCC=5V		3	4.1	4.8	V
	$V_O(D-)$	RL = 180Ω, VCC=5V		0.5	0.7	0.9	V
Differential Output Voltage (dominant)	$V_{OD}(D)$	RL = 180Ω	VCC=5V	2.4	3.4	4	V
Output Symmetry (dominant or recessive)	V_{SYM}	VCC=5V, VO(DATA+) + VO(DATA-)		3.8	4.8	5.5	V
TX Voltage for Recessive Mode	V_{OH_TX}	VCC=5V, NSL23716D only		4.5			V
TX Voltage for Dominant Mode	V_{OL_TX}	VCC=5V, NSL23716D only				0.5	V
Differential Output Rising Time[1]	t_r	RL=180Ω, CL=50pF, VCC=5V.		16	17	27	ns
Differential Output Falling Time[1]	t_f	RL=180Ω, CL=50pF, VCC=5V.		15	17	26	ns
Propagation Delay Time, low-to high level[1]	$t_{p(L2H)D}$	RL=180Ω, CL=50pF, VCC=5V. Refer to figure 1.2		15	18	23	ns
Propagation Delay Time, high-to low level[1]	$t_{p(H2L)D}$	RL=180Ω, CL=50pF, VCC=5V. Refer to figure 1.2		27	30	38	ns
Receiver							
Input Resistance (DATA+/-)	R_{IN}	VCC=3.3/5V, RIN=△V(DATA+)/△I(DATA+)		14	30	46	kΩ
Differential Threshold Voltage for RX Negative Going	V_{RXTH-}	VCC=3.3/5V		0.7	1.1	1.5	V
Differential Threshold Voltage for RX Positive Going	V_{RXTH+}	VCC=3.3/5V		0.3	0.7	1.1	V
Threshold Voltage for RX Negative Going	V_{IL_RX}	VCC=5V, NSL23716D only				0.7	V
Threshold Voltage for RX Positive Going	V_{IH_RX}	VCC=5V, NSL23716D only		2.2			V

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Threshold Voltage for TX Negative Going	V_{OL_TX}	VCC=5V, NSL23716D only			0.7	V
Threshold Voltage for TX Positive Going	V_{OH_TX}	VCC=5V, NSL23716D only	2.2			V
Propagation Delay Time, low-to high level[(1)]	$t_{p(L2H)R}$	RL=180Ω, CL=50pF, VCC=3.3/5V. Refer to figure 1.3	18	23	30	ns
Propagation Delay Time, high-to low level[(1)]	$t_{p(H2L)R}$	RL=180Ω, CL=50pF, VCC=3.3/5V. Refer to figure 1.3	12	16	23	ns
Thermal						
Thermal Warning Flag Threshold[(1)]	T_{WARN}			150		°C
Thermal Warning Flag Hysteresis[(1)]	T_{WARN_HYS}			20		°C
Device thermal shutdown temperature[(1)]	T_{SD}			170		°C
Thermal Shutdown Hysteresis[(1)]	T_{SD_HYS}			20		°C

[(1)] *Not test covered, guaranteed by design.*

7.2. Communication Interface Timing Diagrams

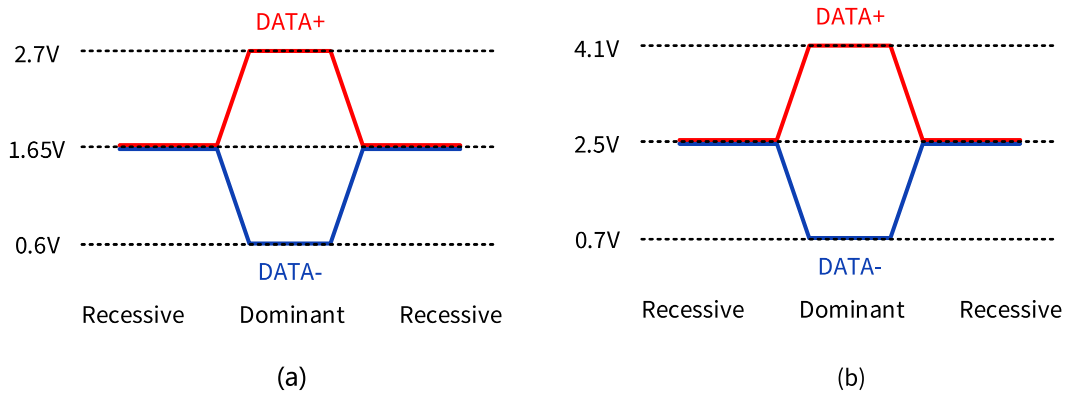


Figure1.1 Differential Interface Timing: (a)NSL23716(1)A (b)NSL23716C

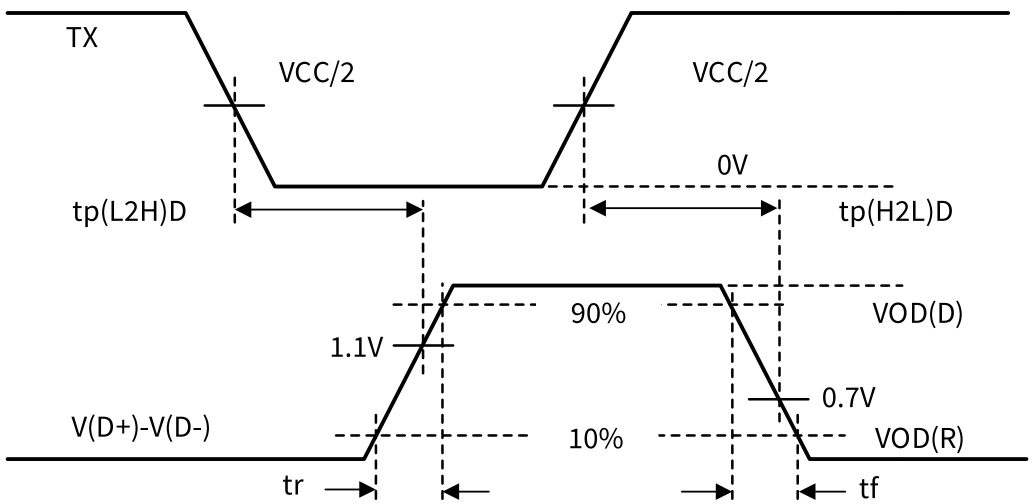


Figure1.2 Differential Interface Driver Timing

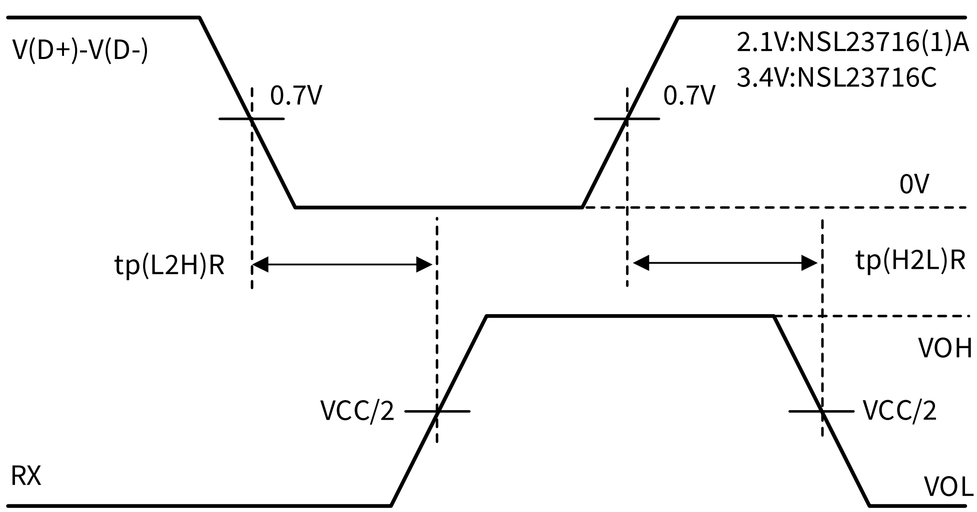


Figure1.3 Differential Interface Receiver Timing

7.3. Typical Performance

3 LEDs in series (VLED = 6V), ILED/channel = 100mA, TA = 25°C, unless otherwise noted.

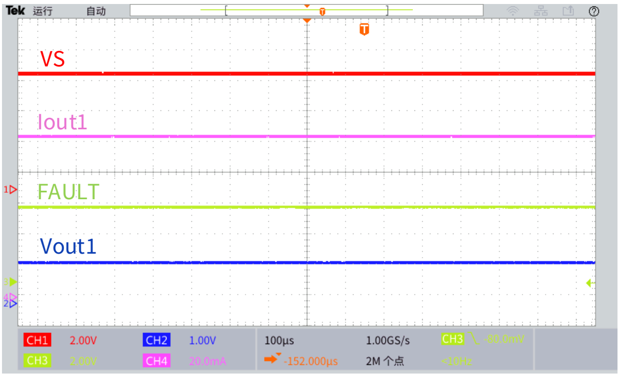


Figure7.1 Steady State(Vout=1.3V,Iout=100mA,no fault)

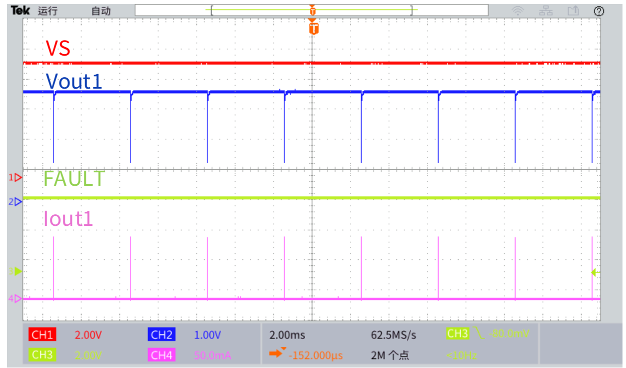


Figure7.2 PWM dimming(duty=1/4095,Fpwm=250Hz)

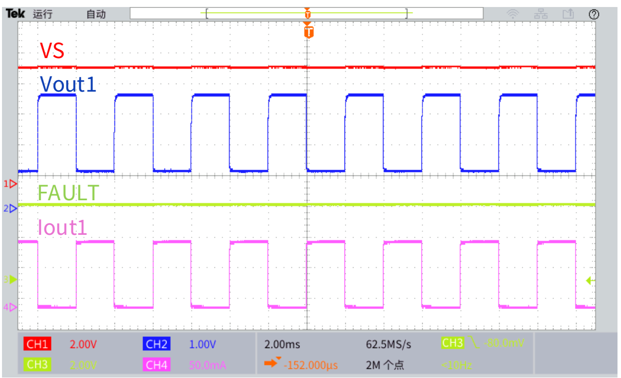


Figure7.3 PWM dimming(duty=50%,Fpwm=250Hz)

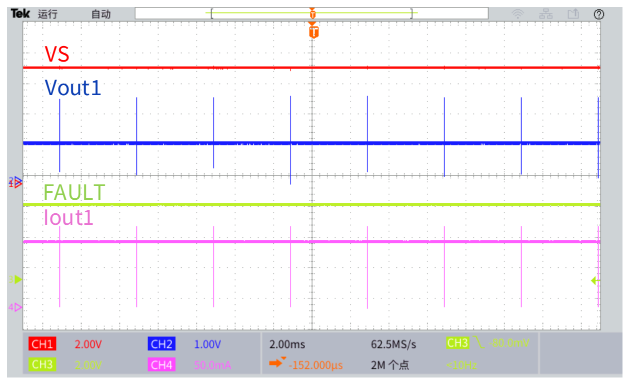


Figure7.4 PWM dimming(duty=4094/4095,Fpwm=250Hz)

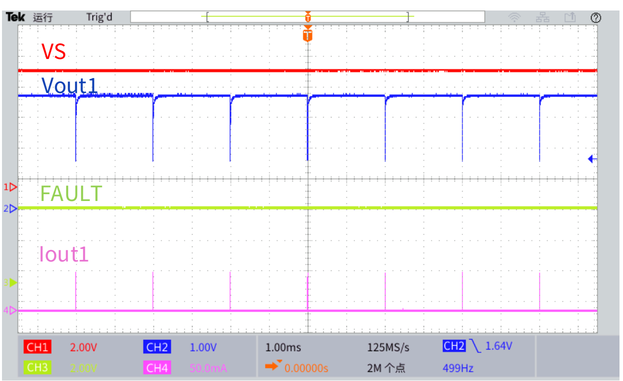


Figure7.5 PWM dimming(duty=1/4095,Fpwm=500Hz)

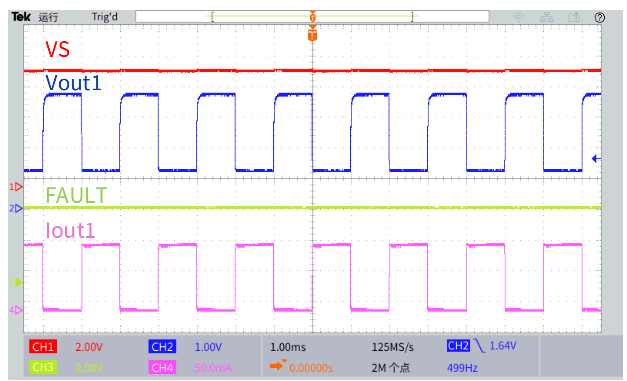
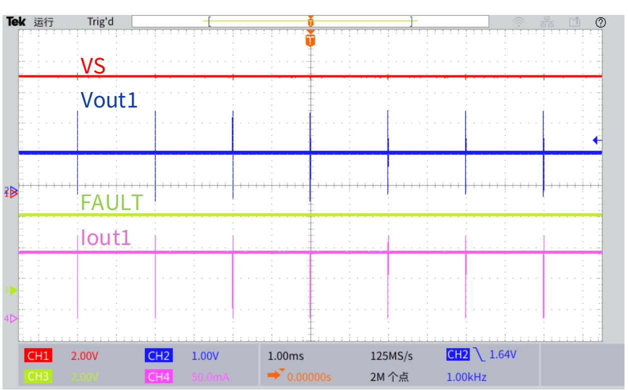


Figure7.6 PWM dimming(duty=50%,Fpwm=500Hz)



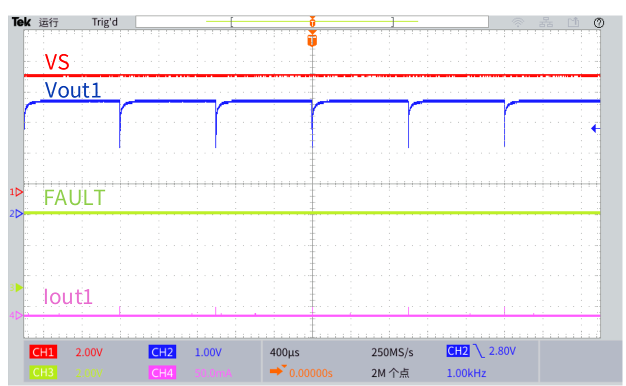
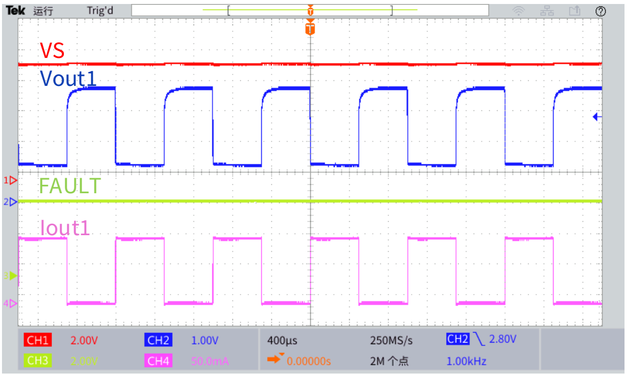


Figure7.7 PWM dimming(duty=4094/4095,Fpwm=500Hz)

Figure7.8 PWM dimming(duty=1/4095,Fpwm=1000Hz)



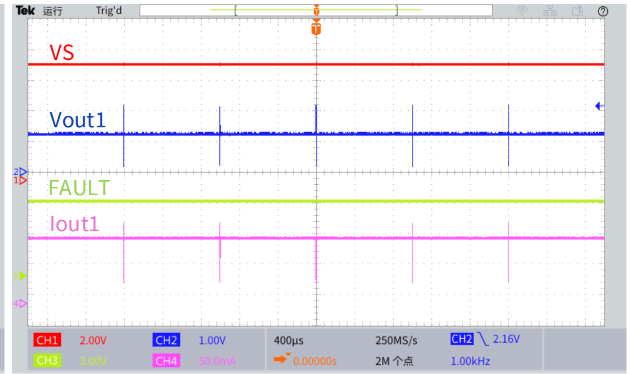
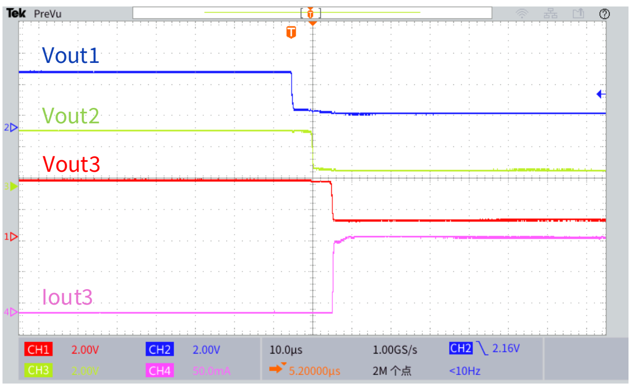


Figure7.9 PWM dimming(duty=50%,Fpwm=1000Hz)

Figure7.10 PWM dimming(duty=4094/4095,Fpwm=1000Hz)



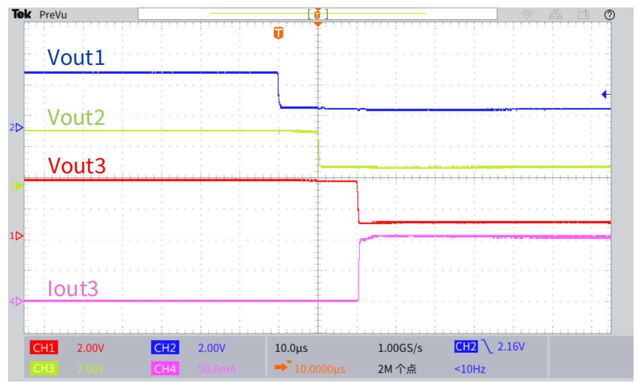
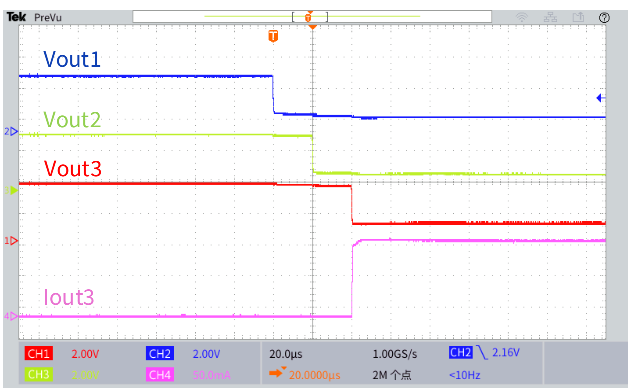


Figure7.11 Phase shift(5μs)

Figure7.12 Phase shift(10μs)



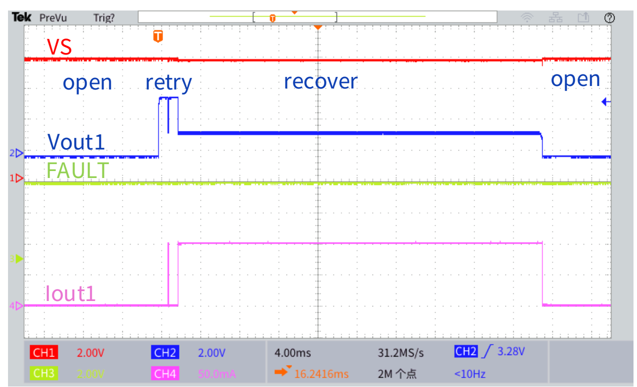


Figure7.13 Phase shift(20μs)

Figure7.14 LED open->retry->recover->open waveform(CH_FAULT_MASK=1)

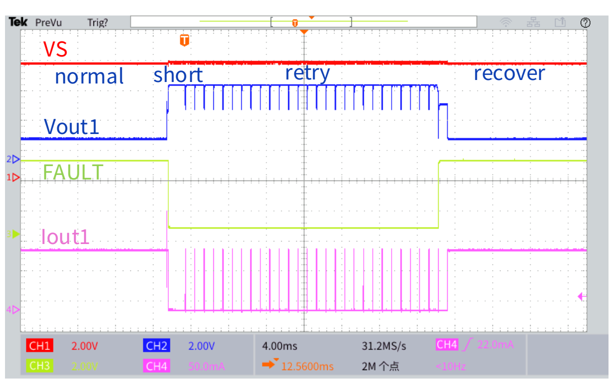


Figure7.15 LED normal->short->retry->recover waveform (CH_FAULT_MASK=0)

7.4. Typical Characteristics

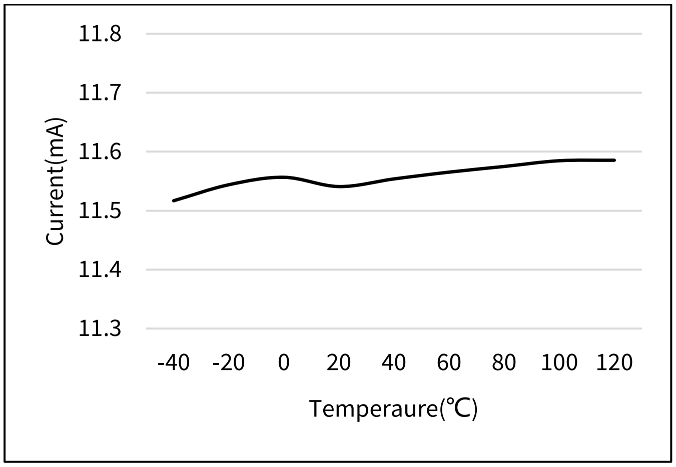


Figure7.16 Quiescent current VS. temperature

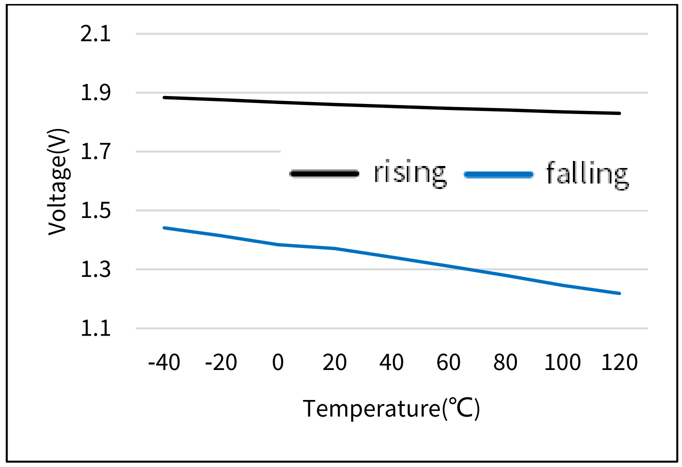


Figure7.17 EN threshold VS. temperature

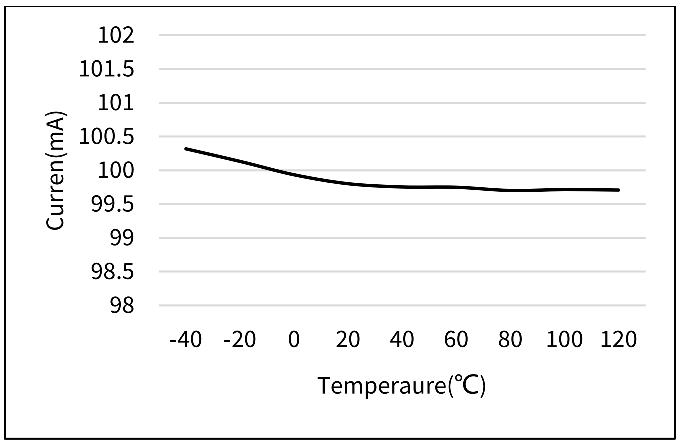


Figure7.18 Output current VS. temperature(100mA)

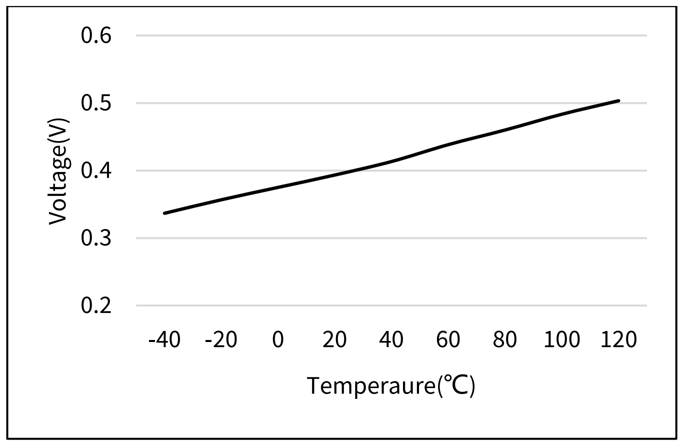


Figure7.19 Dropout voltage VS. temperature(100mA)

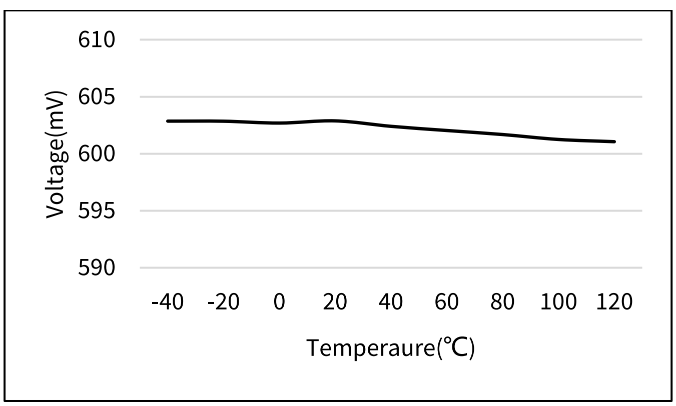


Figure7.20 ISET voltage VS. temperature

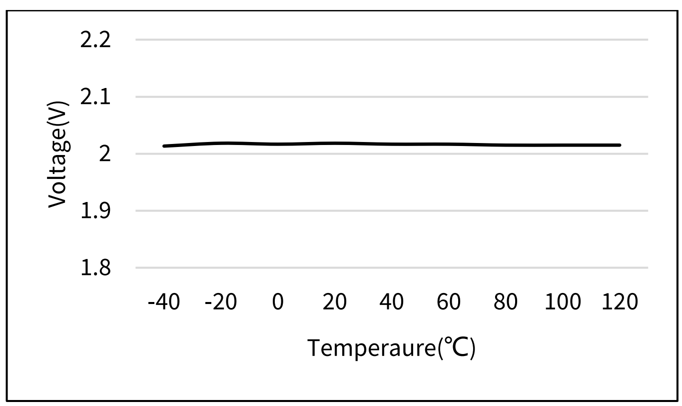


Figure7.21 OUT short threshold VS. temperature

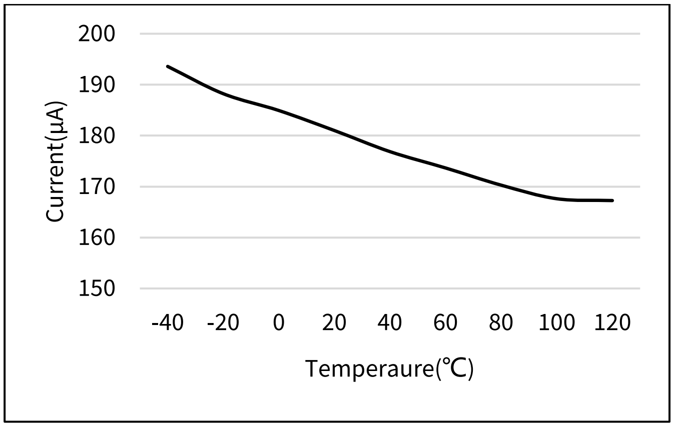


Figure7.22 ISET short threshold VS. temperature

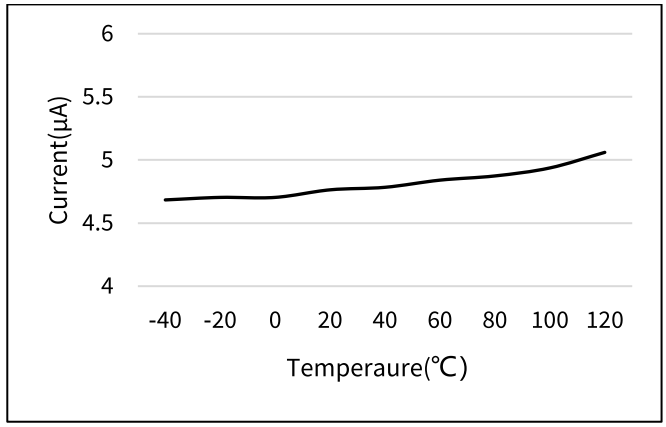


Figure7.23 ISET open threshold VS. temperature

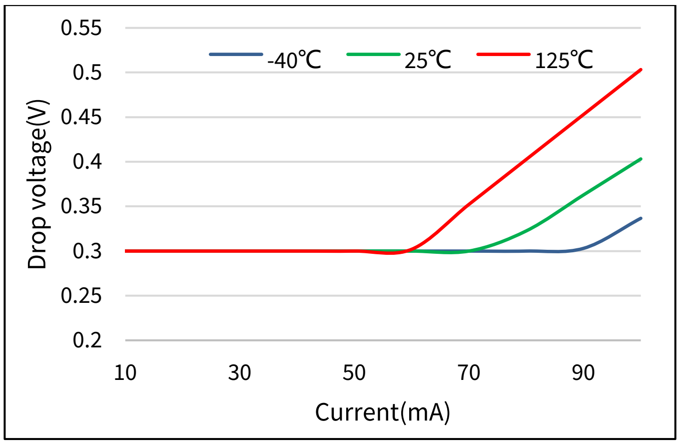


Figure7.24 Drop voltage VS. current

8. Function Description

8.1. System Diagram

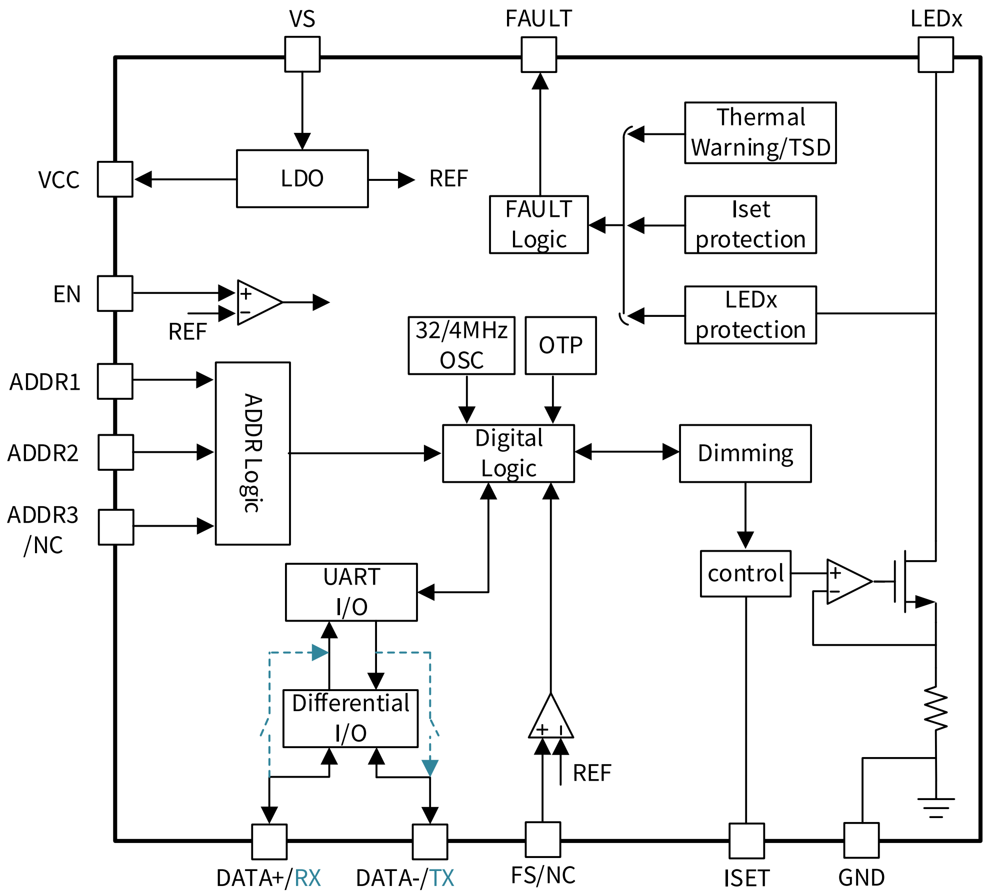


Figure8.1 System block diagram

8.2. Feature Description

8.2.1. Chip Address

There are 16 different addresses totally can be programmed through ADDR1, ADDR2 and ADDR3/ADDR_OTP, which is shown in table8.1. It means totally 256 channels can be utilized in a communication bus, where a series of dynamic performances and more pixels can be achieved.

Note that, the IC checks address first as power up, once the address is checked, the address keeps during operation unless EN toggle or IC POR (power on reset). To distinguish the address accurately of ICs, the resistance utilized in this part should be within the accuracy of +-10%.

There are 2 part numbers named NSL23716A and NSL237161A for custom to distinguish the ADDR_OTP bit 0 or 1. The default value of ADDR_OTP is 0 for NSL23716A, and the default value of ADDR_OTP is 1 for NSL237161A

For NSL23716C/D, custom can configure the ADDR3 pin directly to obtain the device address needed.

Table8.1 Device address

ADDR2	*ADDR1*	*ADDR3/ADDR_OTP*	*ADDR_bit<3:0>*
VCC	VCC	GND/0	0000
VCC	35k to GND	GND/0	0001
VCC	GND	GND/0	0010
35k to GND	VCC	GND/0	0011
35k to GND	35k to GND	GND/0	0100
35k to GND	GND	GND/0	0101
GND	VCC	GND/0	0110
GND	35k to GND	GND/0	0111
GND	GND	GND/0	1000
GND	GND	VCC/1	1000
VCC	VCC	VCC/1	1000
VCC	35k to GND	VCC/1	1001
VCC	GND	VCC/1	1010
35k to GND	VCC	VCC/1	1011
35k to GND	35k to GND	VCC/1	1100
35k to GND	GND	VCC/1	1101
GND	VCC	VCC/1	1110
GND	35k to GND	VCC/1	1111

8.2.2. Power Supply

The supply voltage input to the device through VS pin can be low to 3.7 V and up to 20 V, and EN pin can be connected to VS pin through the divider resistor or supplied by external signal such as GPIO of MCU. Once VS voltage and EN voltage is higher than the rising threshold, IC enter POR mode.

8.2.3. VCC and Startup

The NSL23716 has an integrated low-drop-out linear regulator to provide power (3.3/5V) supply to external devices. The internal LDO powered by input voltage $V_{(VS)}$ provides a stable 3.3/5V output with up to 80-mA constant current capability. Recommends a ceramic capacitor of 10 µF on the VCC pin. The LDO has an internal current limit $I_{(LDO\_LIMIT)}$ for protection and soft start. The capacitor charging time must be considered to total start-up period, because the device will work unnormal if the capacitor voltage is not charged to VCC voltage.

When VS is high, after the EN is high, the VCC is built up, then the internal logic circuits including differential interface are active. The startup sequence is as follows: VS and EN is high→ VCC →internal logic circuits are active and provide the output to LEDs.

The delay time between INT state to normal state can be programed by OTP register INIT_TIMER, and customers can select a suitable initialization time according to the system delay.

8.2.4. Output Current Setting

The NSL23716 uses an external resistor R_{ISET} to set the output current.

The 16 channels current sink regulators embedded in the NSL23716 can be configured to provide up to a maximum current of 100mA each channel. These 16 specialized current sinks are accurate to within ±5% for currents at 100mA over the full temperature range, with a string-to-string difference of ±5%. The $I_{(outx)}$ can be calculated with the equation below.

$$I_{(outx)} = \frac{V_{ISET}}{R_{ISET}(k\Omega)} \quad (1)$$

The nominal voltage of VISET pin is 0.6V. When ISET current higher than short threshold, it will be detected as pin short to ground. The ISET current threshold for short detection is 180µA (corresponding to 3.33kΩ resistor or 180mA ILED). When ISET current lower than 5µA (corresponding to 120kΩ resistor or 5mA ILED), pin open will be detected. Note that, if an ISET open or short fault is detected, the related flag will be set without FAULT pin pull down.

8.2.5. Spread Spectrum & Phase Shift

To improve EMI performance, the NSL23716 features two EMI reduction schemes.

The first scheme, programming the LED current phase shift function. This function is enabled by setting PHASE_SHIFT [1:0] bits 1 in the register. When the phase shift function is enabled, channel x+1(x = 1, 2...15) LED current phase shift is 5µs/10µs/20µs after channel x LED current rising edge. This function also can be utilized to reduce power stage current surge.

Spread spectrum is the second EMI reduction scheme of NSL23716. The spread spectrum function reduces EMI noise around the internal clock (only for output) frequency and its harmonic frequencies. This scheme deliberately spreads the frequency of the switching waveform and makes the bandwidth of the switching waveform wider, which ultimately reduces its EMI spectral density. The spread spectrum function modulates the internal clock frequency ±18% from the central frequency with a 15.6kHz modulation frequency Fm. The spread-spectrum function can be enabled or disabled by SPREAD_SPEC_EN bit.

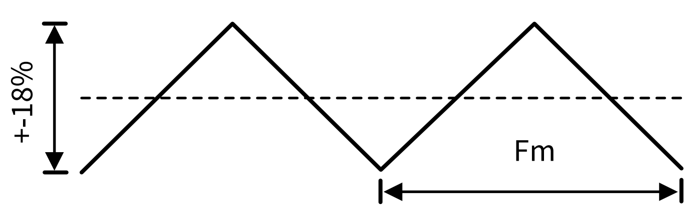


Figure8.2 Frequency spread spectrum

8.2.6. LED Brightness Dimming

8.2.6.1. PWM Dimming

NSL23716 integrates independent 12-bit PWM generators for each OUTx channel. The current output for each OUTx channel is turned on and off controlled by the integrated PWM generator. The average current of each OUTx can be adjusted by PWM duty cycle independently, therefore, to control the brightness for LEDs in each channel.

The 12-bit PWM generator constructs the cyclical PWM output based on a 12-bit digital binary input to control the output current

ON and OFF. Basically, the PWM generator counts 4095 pulses at base high frequency for PWM output cycle period and counts number of pulses determined by 12-bit binary input at the same frequency for PWM ON period. The base high frequency is generated by internal oscillator, which is 4095 times of the frequency programmed by PWM_FREQ. The PWM dimming duty is set by the register PWM_DIM_X [11:0] (x=1,2...16), and the duty is:

$$D = \frac{\text{PWMx}}{2^{12}-1} = \frac{\text{PWMx}}{4095} \quad (2)$$

Where, PWMx [11:0] is the PWM dimming duty code for channel x (x=1,2...16). When set the PWMx [11:0] =0x000, the corresponding LED channel current is 0.

8.2.6.2. Logarithmic Dimming

The NSL23716 can also generate PWM duty-cycle output following logarithmic curve. The integrated lookup table provides a one-to-one conversion from 8-bit register to 12-bit binary code following logarithmic increment when register PWM_EXPEN is set to 1. By using logarithmic brightness control, LED brightness change by one LSB is invisible to human eyes especially at low brightness range.

PWM_EXPEN bit selects the dimming method between linear or exponential. Setting the bit PWM_EXPEN to 1 enables the look-up table for logarithmic dimming curve. In logarithmic PWM dimming mode, 12-bit register is converted to 8-bit PWM duty cycle by look-up table automatically. Clear the bit PWM_EXPEN to 0 disables the look-up table. In this case, users must provide relevant 12-bit PWM duty cycle code for the same brightness to avoid flicker.

To avoid visible brightness flicker for logarithmic dimming, choose PWM frequency as higher as possible (1k Hz). Higher PWM frequency can also avoid the visible LED flash in video display due to the low beat frequency between digital camera shutter frequency and PWM frequency for LED dimming.

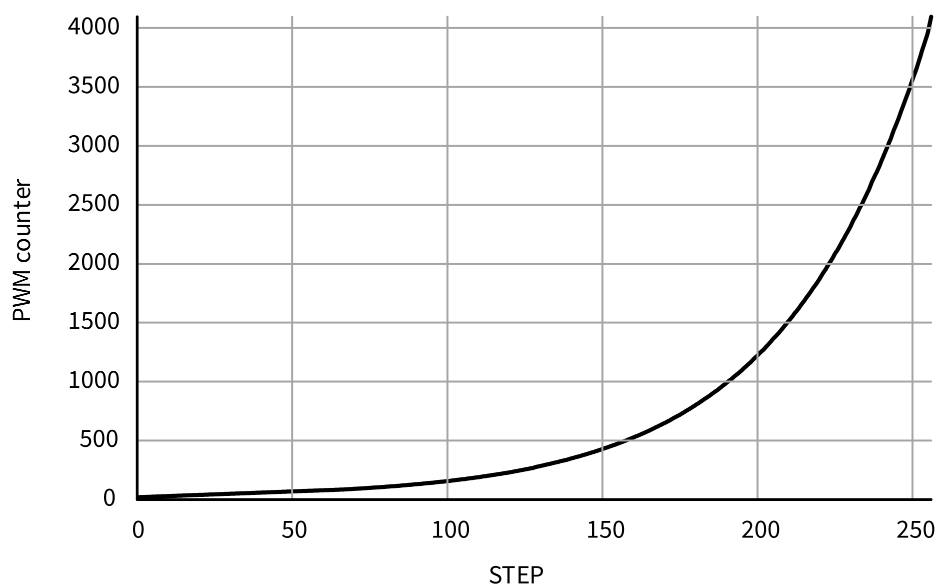


Figure8.3 Logarithmic dimming curve

8.2.7. Diagnostic and Fault Indications

The NSL23716 has full diagnostic coverage for supply voltage, LED output, LED current set and junction temperature, such as:

VS UVLO

LED short protection

LED open protection

ISET pin open/short

Thermal warning and shutdown

The FAULT pin is active low, open drain structure, and no internal pull up circuit is integrated. So, a pull up resistance is needed during real application. When protection is triggered, the corresponding fault bit in the register is set, and the fault pin state depends on the faut mask register (OT_WARN_FT_MASK, CH_FAULT_MASK). If the mask register is set, the fault pin will not pull down, otherwise it will pull down to indicator fault state.

The behavior of the output channel in fault condition depends on the register LATCH_EN. Fault channel should latch off or hiccup under LED open or short protection (not including VS UVLO, ISET pin open/short protection, thermal warning and shutdown).

If LATCH_EN = 1 (latch/interrupt mode), once the fault is triggered, the fault channel keeps off until POR (Power On Reset) or EN off to reset. While other healthy channels in the IC still work.

If LATCH_EN = 0 (hiccup/standard fault mode), the fault channel tries to conduct 32μs in every 1ms to detect if the fault is cleared or not. Channel will open again and FAULT pin release if fault condition is removed.

8.2.7.1. VS UVLO

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. When VS voltage drops below respective UVLO threshold, the device enters POR state. Upon voltage recovery, the device automatically switches to INIT state. VS UVLO will not trigger FAULT pin. When VS UVLO is triggered, IC stops work, and all the registers are reset.

8.2.7.2. LED Open

The NSL23716 device integrates LED open-circuit diagnostics to allow users to monitor LED status. If the voltage drops over the current sink channel is below the threshold $V_{LEDx} < V_{LED\_O}$(300mV) and a filter time of 120μs (250Hz) is passed, open load condition will be detected. If there is an open load on one of the outputs, the output is turned off and the corresponding open fault bit CHx_OPEN (x=1,2...16) is set, and FAULT pulls low if CH_FAULT_MASK is set to 0. If LATCH_EN= 1 (latch/interrupt mode), the fault channel keeps off until POR or EN off to reset. Other healthy channels in the IC still work. FAULT is released high when fault bit is read cleared by MCU. If LATCH_EN= 0 (hiccup/standard fault mode), the LED open is not latched, fault channel tries to conduct 32μs in every 1ms to detect if the fault is recovered or not. As soon as the open load condition is no longer present, the channel will be turned on again. FAULT(CH_FAULT_MASK=0) pin release high if fault condition is removed. The fault bit is still there until read cleared by MCU, not affected by LATCH_EN.

8.2.7.3. LED Short

The NSL23716 device integrates LED short-circuit diagnostics to allow users to monitor LED status. In LED short condition, the V_{LEDX} pull up to high, when the V_{LEDx} (x=1,2...16) is higher than V_{LED_S} for 120μs (250Hz), the LED short protection is triggered, the short channel is off, the corresponding fault bit CHx_SHORT (x=1,2...16) is set, and FAULT pull low if CH_FAULT_MAK is set to 0.

If LATCH_EN = 1 (latch/ interrupt mode), the fault channel keeps off until POR or EN off to reset. Other healthy channels in the IC still works. FAULT is released high when fault bit is reset by MCU, if LATCH_EN = 0 (hiccup/standard fault mode), in this case, the LED short is not latched, fault channel tries to conduct 32μs in every 1ms to detect if the fault is recovered or not. As soon as the short condition is no longer present, the channel will be turned on again. FAULT(CH_FAULT_MASK=0) pin release high if fault condition is removed.

The LED short protection threshold is programmed by LED_SHORT_THR [1:0] as follows:

LED_SHORT_THR =00, short protection threshold is 2V;

LED_SHORT_THR =01, short protection threshold is 3V;

LED_SHORT_THR =10, short protection threshold is 4V;

LED_SHORT_THR =11, short protection threshold is 5V.

8.2.7.4. ISET Pin Open/Short

NSL23716 implements a current monitor for ISET resistor open-and-short diagnostic and protection. The device monitors the current flowing out of the ISET pin. If the current is smaller than I_{ISET_oth}(5μA), a reference open condition is asserted. If the resistance of I_{ISET} is higher than I_{ISET_sth}(180μA), a short condition is asserted.

ISET resistor open or short protection is a no latch protection, when the fault situation of ISET is removed, the IC will enter normal state. Furthermore, this fault only effect response flag, and the FAULT pin will not be pulled down.

The fault flag can be cleared by either MCU or POR or EN reset.

8.2.7.5. Thermal Derating

To prevent LEDs from flickering because of rapid thermal changes, the device includes a programmable thermal deration feature to reduce power dissipation at high junction temperatures.

The NSL23716 device reduces the LED current as the silicon junction temperature over the configured thermal threshold of the NSL23716 device. By mounting the device on the same thermal substrate as the LEDs, this feature can also limit the dissipation of the LEDs. As the junction temperature of the NSL23716 device increases, the device reduces the regulated current, reducing the dissipated power in the IC and in the LEDs. The current reduction is from the 100% level at typically 2% of I(setting) per °C until the point at which the current drops to 50% of the full value.

Changing the register THERMAL_DERATING adjusts the temperature at which the current reduction begins.

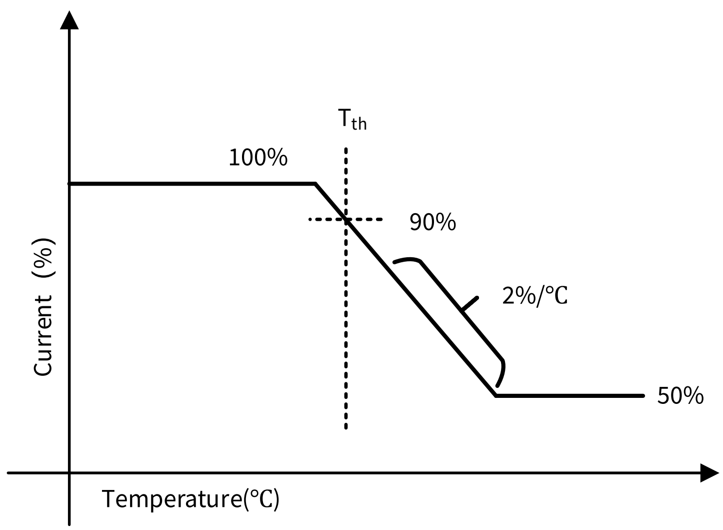


Figure8.4 Thermal derating curve

8.2.7.6. Thermal Pre-waring

The NSL23716 continuously monitors the junction temperature voltage and compares the results with internal threshold for pre-thermal warning.

When the junction temperature of NSL23716 rises above pre-thermal warning threshold, the device reports pre-thermal warning, sets the flag register OT_WARN to 1. The FAULT pin will pull down when OT_WARN_FT_MASK register is set to 0 and keeps when OT_WARN_FT_MASK register is set to 1.

The fault is latched in flag registers. When the junction temperature falls below pre-thermal warning threshold, MCU can clear this flag.

8.2.7.7. Thermal Shutdown

When the device junction temperature rises above TSD, all output channels are turned off for protection, the OT_TSD bit is set, and the FAULT pin is pulled down by continuous current to report the fault. FAULT releases high when IC recovers from thermal shutdown. Fault bit will be there until it is cleared by MCU or POR or EN reset.

The thermal protection is non-latch protection. When the junction temperature falls below $T_{SD} - T_{SD\_HYS}$, IC recovers and channels turn on using the previous settings without re-initializing.

8.2.8. Fail Safe State

NSL23716 supports independent channel brightness control through the interface (CAN or UART). The brightness of each channel is adjustable according to its PWM duty cycle register PWM_DIM_x, and channel enable register CHx_EN setting. The brightness of each channel reflects to its register setting value in next cycle after register successfully updated through the interface by master unit. However, the master unit loses the control for all current channels if communication fails between master unit and the NSL23716. For example, the interface cable is broken by accident. Consequently, the brightness for all output channels of the NSL23716 is stuck and the ON/OFF control for all output channels is missing too. To keep the basic ON/OFF control for each output channels, the NSL23716 provides a fail-safe state when the communication to master is lost.

When the NSL23716 is entering fail-safe states from normal state, all the registers are reloaded from OTP (FS register). NSL23716 provides two sets of channels enable configuration in fail-safe states, CHX_EN_FS0 and CHX_EN_FS1. In fail-safe state 0, the channel-enable register CHx_EN automatically loads code from CHx_EN_FS0; and in fail-safe state 1, the channel-enable register CHx_EN automatically loads code from CHx_EN_FS1. The fail-safe state is selected by FS pin voltage. The fail-safe state 1 is selected by pulling the FS pin to high, otherwise the fail-safe state 0 is selected. The flag register FS_Pin_State shows the FS input level at real-time. If FS pin input voltage is logic high, the FS_Pin_State is set to 1. The device does not reset diagnostics status or FLAG registers when switching between two fail-safe states.

Setting FORCE_FS to 1 forces the device into fail-safe state from normal state. The NSL23716 can quit from fail-safe state to normal state by setting CLEAR_FS to 1 with FLAG registers cleared. The CLR_LOCK register is automatically set to 1 when the NSL23716 goes into the fail-safe state to prevent the modification of configuration register by mistake. To get out of fail-safe states to normal state, CLR_LOCK register must be cleared to 0 before setting CLEAR_FS to 1.

Note that, THERMAL_DERATING and OFAF_EN registers will be set to 01 and 1 when enter fail safe state if the OTP register is not written. When quit this state, MCU must configure these registers to the value custom wanted. The global dim function and channel latch function is disabled in FS mode as well, it means LATCH_EN bit is always set to 0.

The fail-safe states also allow the NSL23716 operating as a standalone device without master controlling in the system. The FAULT pin is used as fault indicator to achieve one-fails-all-fail or one-fails-others-on diagnostics requirement.

8.2.9. Fault Table

Table8.2 FAULT Table in Normal State

Fault Type	Detection Mechanism	Action	Flag	Fault Pin	Recovery	
VS UVLO	VS<VS_UVLO	Device switch to POR state	/	/	Device switch to INIT state when voltage rails are good	
Thermal warning	T_J>Twarn	No action	OT_WARN	Pull down (OT_WARN_FT_MASK=0) no action (OT_WARN_FT_MASK=1)	Flag cleared by MCU or POR or EN rest	
Over-temperature protection	T_J>TSD	Turn off all channels	OT_TSD	Pull down	Automatically recover upon junction temperature falling below threshold with hysteresis. Flag cleared by MCU or POR or EN rest	
Communication loss fault	T(WDTIMER) overflows (Default disable this function)	Enter fail-safe states	FS_Flag	/	Set CLEAR_FS to 1 to set the device to quit Fail safe state	
LED open-circuit fault	VLEDx < VLED_O	Turn off failed channels	CHx_OPEN	Pull down (CH_FAULT_MASK=0) no action (CH_FAULT_MASK=1)	LATCH_EN = 0	Automatically recover, release FAULT upon fault removal. Cleared fault flags by MCU.
					LATCH_EN = 1	POR or EN reset
LED short-circuit fault	VLEDx >VLED_S	Turn off failed channels	CHx_SHORT	Pull down (CH_FAULT_MASK=0) no action (CH_FAULT_MASK=1)	LATCH_EN = 0	Automatically recover, release FAULT upon fault removal. Cleared fault flags by MCU.
					LATCH_EN = 1	POR or EN reset
ISET Pin Open	IISET<IISET_oth	No action	ISET_PIN_OPEN	No action	Automatically recover	
ISET Pin Short	IISET>IISET_sth	No action	ISET_PIN_SHORT	No action	Automatically recover	

Table8.3 FAULT Table in Fail-Safe State

Fault Type	Detection Mechanism	Action		Flag	Fault Pin	Recovery
VS UVLO	VS<VS_UVLO	Device switch to POR state		/	/	Device switch to INIT state when voltage rails are good
Thermal warning	T_J>Twarn	No action		OT_WARN	/	Automatically recover, cleared fault flags by MCU upon fault removal.
Over-temperature protection	T_J>TSD	Turn off all channels		OT_TSD	Pull down	Automatically recover, release FAULT and cleared fault flags by MCU upon fault removal.
LED open-circuit fault	VLEDx < VLED_O	OFAF_EN=1 (default)	Turn off all channels and fault channel retries (conducts 32µs in every 1ms)	CHx_OPEN	Pull down	Automatically recover, release FAULT and cleared fault flags by MCU upon fault removal.
		OFAF_EN=0	Turn off failed channels and fault channel retries (conducts 32µs in every 1ms)			
LED short-circuit fault	VLEDx >VLED_S	OFAF_EN=1 (default)	Turn off all channels and fault channel retries (conducts 32µs in every 1ms)	CHx_SHORT	Pull down	Automatically recover, release FAULT and cleared fault flags by MCU upon fault removal.
		OFAF_EN=0	Turn off failed channels and fault channel retries (conducts 32µs in every 1ms)			
ISET Pin Open	IISET<IISET_oth	No action		ISET_PIN_OPEN	No action	Automatically recover
ISET Pin Short	IISET>IISET_sth	No action		ISET_PIN_SHORT	No action	Automatically recover
External fault (OFAF_EN=1)	Fault occurs	Turn off all channels		Depend on fault type	External pull down	Automatically recover, failed channels retry when FAULT pin is external release high.
	No fault			/		Automatically recover, turn on channels when FAULT pin is release high.

8.2.10. Communication Interface

There are 2 type interfaces in NSL23716 device, which can provide more flexible selection for customers. The one is differential interface, and the other one is UART interface. The protocol of these 2 interfaces is the same (UART protocol).

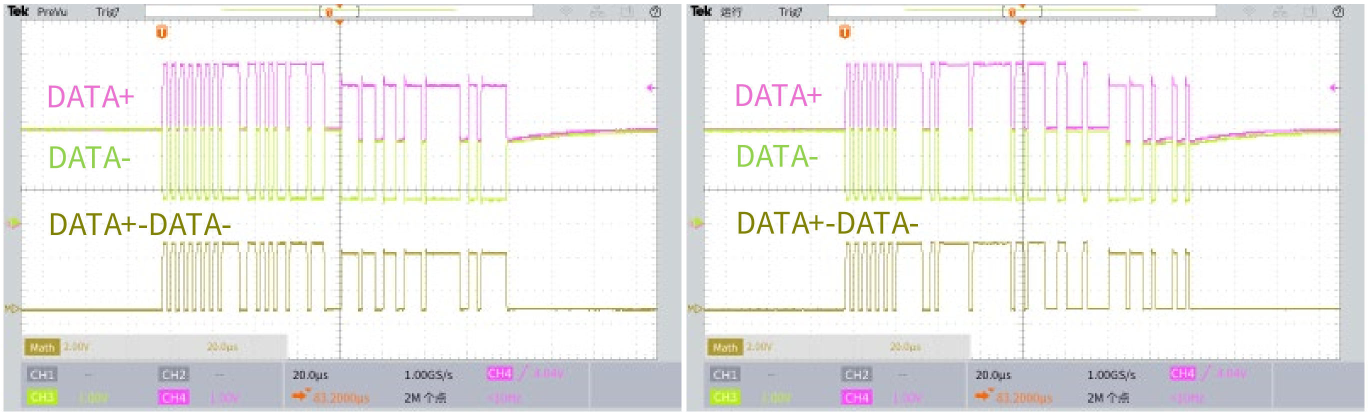
Differential interface:

Differential interface for automotive lighting applications is designed in NSL23716. The settings and timings are controlled by the on board MCU via differential interface through a CAN transceiver. The differential interface is compatible with most of the CAN transceiver. It can communicate with other CAN transceivers by connecting the DATA+ and DATA- to the CAN bus. It features a high-speed receiver and transmitter capable of operating up to 2 Mbps and longer communication distance.

The differential interface is supplied from the VCC pin which is transferred from internal LDO (3.3/5V), to maintain driver symmetry; the typical output common mode voltage is 1.65/2.5V in the dominant state. The internal common mode reference is set to VCC/2 = 1.65/2.5V to match the dominant state output common mode voltage.

The internal transmitter converts a single-ended input (TXD) from the external CAN transceiver to differential outputs for the bus lines (DATA+, DATA-).

The receiver reads differential inputs from the bus lines (DATA+, DATA-) and transfers this data as a single-ended output (RXD) to internal digital block. It consists of a comparator that senses the difference VDIFF = (DATA+, DATA-) with respect to an internal threshold of +1.1V. If this VDIFF is greater than 1.1V, a logic-low is present at RXD. If VDIFF is less than 0.7V, a logic-high is present.



(1) (2)

Figure8.5 Differential interface communication waveform: (1)Read CMD (2)Write CMD

UART interface:

The NSL23716 device also has UART-based interface supported by most microcontroller units (MCU). The protocol supports master-slave with star-connected topology. The communication baud rate is the same as differential interface.

Interface reset:

Both Differential and UART interface can be reset by master to avoid slavers loss control or logical error. The reset method is to set the communication bus as logical 0 last 13 bits, then all the slavers reset their interface and wait for the next valid messages.

Note that, a last 11bits data in the frame is also as an invalid data and this frame will be discarded.

8.2.10.1. Communication Protocol

The NSL23716 device configuration and status can be accessed through the communication bus interface. It uses a CAN/UART-based protocol supported by most microcontroller units (MCU). The protocol supports master-slave with star-connected topology. The structure of the frame is shown in Figure 8.6. The communication baud rate can range from 150kbps to 2Mbps.

The device integrates a watchdog timer to monitor communication. Once the slave device receives a communication frame, it firstly verifies its CRC byte. Only when CRC is verified, the slave device sends out the response frame and clears the watchdog timer. In addition, if one communication frame is interrupted in the middle without any bus toggling for a period longer than timeout timer, the device resets the communication and waits for next communication starting from synchronization byte.

If communication CRC check fails, the NSL23716 ignores the message without sending the feedback. The master does not receive any feedback if the communication is unsuccessful. In this case, communication can be reset by keeping communication bus idle, which forces the NSL23716 to clear its cache and be ready for new communication.

The interface supports both writing and readback. Both write and readback communication supports single-byte mode and burst mode. Figure 8.6 describes the frame structure of a typical write action. The master frame consists of SYNC, DEVID, REGADDR, DATA[0], DATA[n] and CRC bytes. Once CRC is verified, the slave immediately feeds back STATUS and CRC bytes. Figure 8.7 describes the frame structure of a typical readback action. The master frame consists of SYNC, DEVID, REGADDR and CRC bytes. Once CRC is verified, the slave immediately feeds back STATUS, DATA[0], DATA[n] and CRC bytes.

ST+8bit+SP	ST+8bit+SP	ST+8bit+SP	ST+8bit+SP	ST+8bit+SP	ST+8bit+SP	ST+8bit+SP	ST+8bit+SP
SYNC byte	DEVICE byte	REGADDR byte	DATA[0]	DFATA[n]	CRC byte	STATUS byte	CRC byte

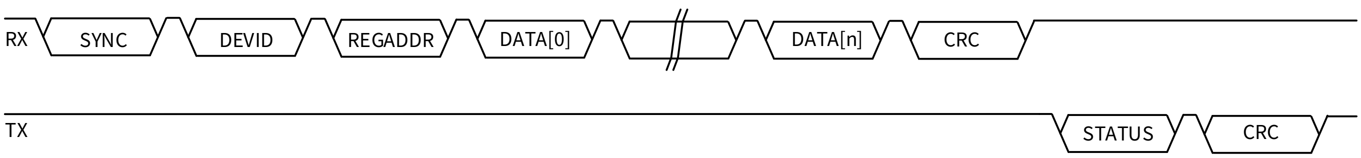


Figure8.6 Write command with feedback

ST+8bit+SP	ST+8bit+SP	ST+8bit+SP	ST+8bit+SP	ST+8bit+SP	ST+8bit+SP	ST+8bit+SP	ST+8bit+SP
SYNC byte	DEVICE byte	REGADDR byte	CRC byte	STATUS byte	DATA[0]	DATA[n]	CRC byte

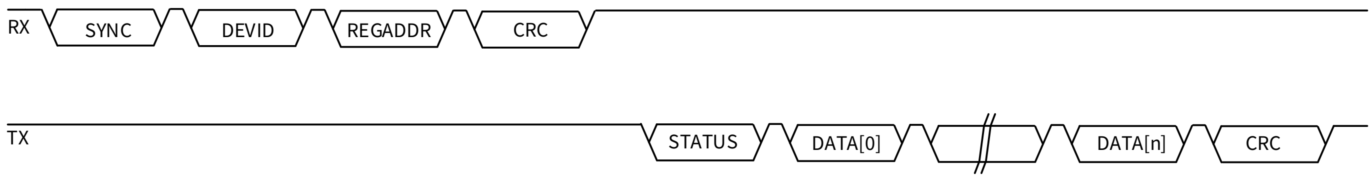


Figure8.7 Read command

8.2.10.2. Frame Structure

The frame starts with the sync field and followed by a few byte fields. Each byte field is transmitted as the byte structure shown in Figure 8.8. Each byte has 1 start bit, 8 data bits, 1 stop bit, and no parity check. The LSB of the data is sent first and the MSB last.

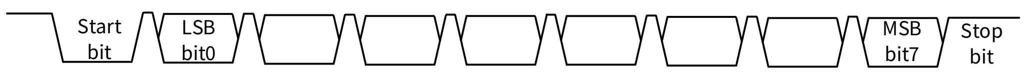


Figure 8.8 one data byte structure

8.2.10.3. Synchronization Byte

The SYNC byte is the first byte sent from the master. It is with the data value 0x55. The device detects the sync byte to communicate with the master at the same baud rate adaptively. Figure 8.9 shows the timing diagram for the sync byte.

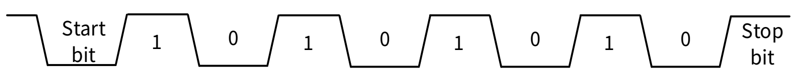


Figure 8.9 SYNC byte

8.2.10.4. Device Address Byte

The device address byte, DEVID, follows the SYNC byte. The definition for each bit in the DEVID byte is described in Table 8.1.

Table8.1 DEVID byte

BIT	Field	Description
7-4	DEVICE_ADDR	Target device address.
3	BROADCAST	Communication mode. 1: Broadcast; 0: Single device only
2	READ/WRITE	Select read/write mode. 0: write mode; 1: read mode
1-0	LENGTH	00b: Single-byte mode with 1 byte of data; 01b: Bust mode with 2 bytes of data; 10b: Burst mode with 4 bytes of data; 11b: Burst mode with 8 bytes of data

8.2.10.5. REGISTER Address Byte

The register address byte, REGADDR, follows the device address bye. The 8-bit register address value can be from 0x01 to 0x32 with a 16-bit width.

8.2.10.6. DATA Byte

The NSL23716 supports single data byte or multiple data bytes writing or reading in one frame. The number of bytes is defined in DEVID byte. There is total four options including 1, 2, 4, or 8 data bytes.

8.2.10.7. STATUS Byte

When NSL23716 as a slave device receives a non-broadcast frame, it first verifies the CRC byte. Once CRC check is succeeded, the device sends out the device status of fault flag and FAULT PIN status. In broadcast mode, the devices do not send out responses.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	CH_short	CH_open	FAULT_pin	0	0	0

8.2.10.8. CRC Byte

The CRC byte follows the data bytes as the final byte in the end of one data transaction to ensure the NSL23716 device correctly receiving all the data bytes from master controller. The master controller must calculate the CRC value for all byte's binary code including DEVID, REGADDR and data bytes and send it to NSL23716 to end the one-time communication. NSL23716 receives all byte's data, calculates the CRC and compares the calculated CRC code with the received CRC code. If two CRC codes do not match each other, the device ignores the data transaction and waits for the next data transaction without reset the watchdog timer. The CRC code algorithm for multiple bytes of binary data is based on the polynomial, X^8 + X^5 + X^4 + 1. The initial code for CRC is FFh as well.

8.2.11. OTP program

NSL23716 provides OTP bits for customers to configure many functions in FS mode, where the register address is from 0x2E to 0x32. The default value of these registers can be obtained in the next section, and the default configuration is suitable for most applications in general. If customs have special requests, these registers also support programing, but only one time. Figure 8.10 shows the program flowchart of program process.

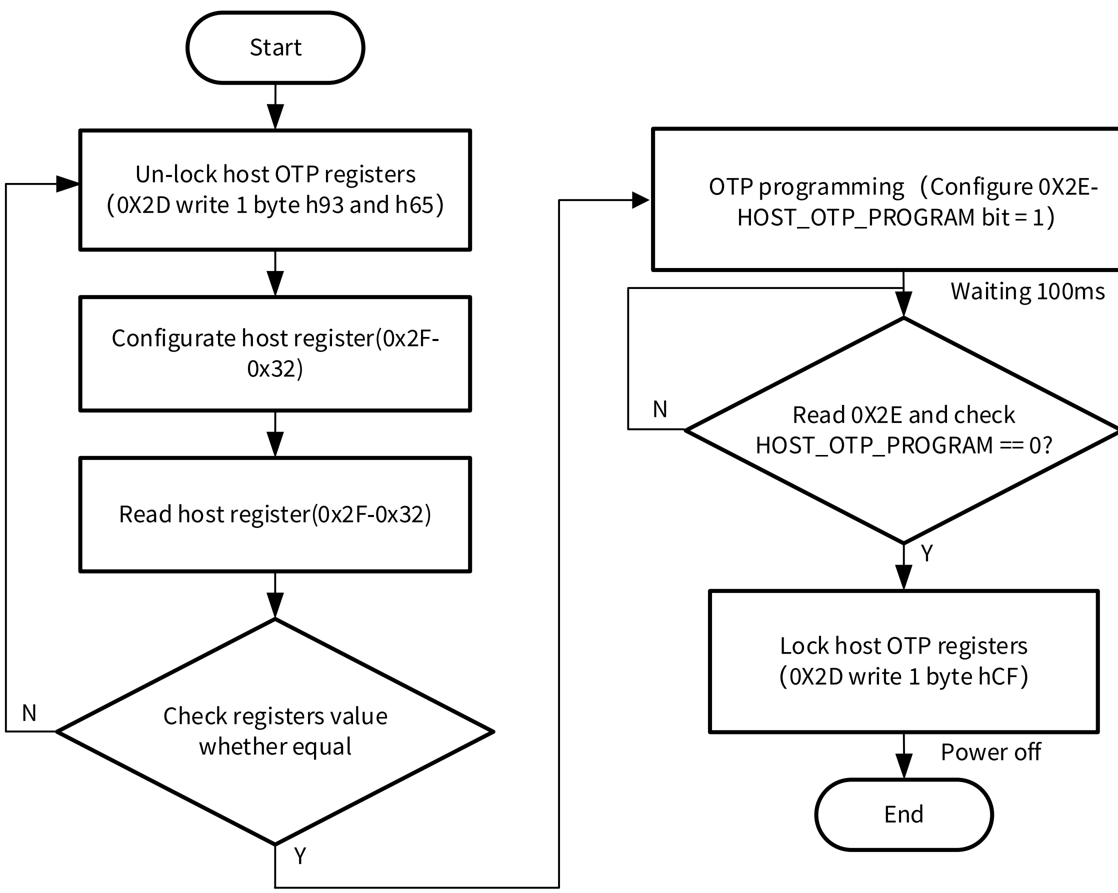


Figure8.10 OTP program flowchart

8.2.12. Register Map

Register Name	R/W	ADDR	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DEVICE CONFIG																			
DEV_REV	R	0X00	0x0000	RSV												SILICON_INFO			
DEV_CFG_1	R/W	0X01	0x0200	LED_SHORT_THR		RSV		PHASE_SHIFT		PWM_FREQ		RSV						GLOBAL_DIM	SPREAD_SPEC_EN
DEV_CFG_2	R/W	0X02	0xA081	CH_FAULT_MASK	LATCH_EN	RSV						OT_WARN_FT_MASK	RSV						EN_ANA
CH_EN	R/W	0X03	0x0000	CH16_EN	CH15_EN	CH14_EN	CH13_EN	CH12_EN	CH11_EN	CH10_EN	CH9_EN	CH8_EN	CH7_EN	CH6_EN	CH5_EN	CH4_EN	CH3_EN	CH2_EN	CH1_EN
DIAGNOSTIC AND DEVEICE STATUS																			
DIAG_STAT_1	W/R1C	0X04	0x0000	CH16_OPEN	CH15_OPEN	CH14_OPEN	CH13_OPEN	CH12_OPEN	CH11_OPEN	CH10_OPEN	CH9_OPEN	CH8_OPEN	CH7_OPEN	CH6_OPEN	CH5_OPEN	CH4_OPEN	CH3_OPEN	CH2_OPEN	CH1_OPEN
DIAG_STAT_2	W/R1C	0X05	0x0000	CH16_SHORT	CH15_SHORT	CH14_SHORT	CH13_SHORT	CH12_SHORT	CH11_SHORT	CH10_SHORT	CH9_SHORT	CH8_SHORT	CH7_SHORT	CH6_SHORT	CH5_SHORT	CH4_SHORT	CH3_SHORT	CH2_SHORT	CH1_SHORT
DIAG_STAT_3	W/R1C	0X06	0x0000	RSV	OT_WARN	ISET_PIN_SHORT	ISET_PIN_OPEN	RSV	OT_SD	RSV									
BRIGHTNESS CONTROL																			
CH1_PWM	R/W	0X07	0x0FFF	RSV				PWM_DIM _1											
CH2_PWM	R/W	0X08	0x0FFF	RSV				PWM_DIM _2											
CH3_PWM	R/W	0X09	0x0FFF	RSV				PWM_DIM _3											
CH4_PWM	R/W	0X0A	0x0FFF	RSV				PWM_DIM _4											
CH5_PWM	R/W	0X0B	0x0FFF	RSV				PWM_DIM _5											
CH6_PWM	R/W	0X0C	0x0FFF	RSV				PWM_DIM _6											
CH7_PWM	R/W	0X0D	0x0FFF	RSV				PWM_DIM _7											
CH8_PWM	R/W	0X0E	0x0FFF	RSV				PWM_DIM _8											
CH9_PWM	R/W	0X0F	0x0FFF	RSV				PWM_DIM _9											
CH10_PWM	R/W	0X10	0x0FFF	RSV				PWM_DIM _10											
CH11_PWM	R/W	0X11	0x0FFF	RSV				PWM_DIM _11											
CH12_PWM	R/W	0X12	0x0FFF	RSV				PWM_DIM _12											
CH13_PWM	R/W	0X13	0x0FFF	RSV				PWM_DIM _13											
CH14_PWM	R/W	0X14	0x0FFF	RSV				PWM_DIM _14											
CH15_PWM	R/W	0X15	0x0FFF	RSV				PWM_DIM _15											
CH16_PWM	R/W	0X16	0x0FFF	RSV				PWM_DIM _16											
DEV_CFG_3	R/W	0X2A	0x800C	HOST_EXT_LOCK	RSV								PWM_EXPEN	THERMAL_DERATING		STATUS_W1C	CLR_LOCK	CLEAR_FS	FORCE_FS
FS/Test Mode State	RO	0X2B	0x0000	RSV														FS_Flag	FS_Pin_State
FAIL SAFE CONFIG																			
	W	0X2D	0x0000	RSV								Host OTP registers password, enter: h93/h65; exit: hcf							

Register Name	R/W	ADDR	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	R/W	0X2E	0x0000	HOST_OTP_PROGRAM	RSV														
CH_FS0_EN	R/W	0X2F	OTP (0x0000)	CH16_EN_FS0	CH15_EN_FS0	CH14_EN_FS0	CH13_EN_FS0	CH12_EN_FS0	CH11_EN_FS0	CH10_EN_FS0	CH9_EN_FS0	CH8_EN_FS0	CH7_EN_FS0	CH6_EN_FS0	CH5_EN_FS0	CH4_EN_FS0	CH3_EN_FS0	CH2_EN_FS0	CH1_EN_FS0
CH_FS1_EN	R/W	0X30	OTP (0xFFFF)	CH16_EN_FS1	CH15_EN_FS1	CH14_EN_FS1	CH13_EN_FS1	CH12_EN_FS1	CH11_EN_FS1	CH10_EN_FS1	CH9_EN_FS1	CH8_EN_FS1	CH7_EN_FS1	CH6_EN_FS1	CH5_EN_FS1	CH4_EN_FS1	CH3_EN_FS1	CH2_EN_FS1	CH1_EN_FS1
PWM in FS	R/W	0X31	OTP (0x0FFF)	RSV				PWM_DIM _FS											
	R/W	0X32	OTP (0x0140)	RSV						THERMAL_DERATING_FS		CH_EN_INIT	OFAF_EN	INIT_TIMER			FS_TIMER		

8.2.13. Register Map Description

Address:0X00, Default Value: 0x0000			
Bit Name	Access	Default	Description
D[15:4]	RSV	8bit 0	RSV (Reserved)
D[3:0]	R	4bit 0	Device silicon information.
Address: 0x01, Default Value: 0x0200			
Bit Name	Access	Default	Description
D[15:14]	R/W	2bit 0	LED short threshold: 00: 2V; 01: 3V; 10: 4V; 11: 5V.
D[13:12]	RSV	2bit 0	RSV
D[11:10]	R/W	2bit 0	PWM dimming phase shift control: 00: No phase shift between channel; 01: 5µs, the rising edge of channel x+1 is 5µs after channel x; 10: 10µs, the rising edge of channel x+1 is 10µs after channel x; 11: 20µs, the rising edge of channel x+1 is 20µs after channel x.
D[9:8]	R/W	2bit 10	LED channel PWM dimming frequency setting (PWM frequency can be changed on the fly): 00: 1kHz; 01: 500Hz; 10: 250Hz; 11: 1kHz.
D[7:2]	RSV	6bit 0	RSV
D[1]	R/W	1bit 0	When global dimming bit is enabled, all channel dimming setting share the same setting with channel 1, this can use to adjust all the channels LED current at the same time: 0: Global dimming function is disabled;

			1: Global dimming function is enabled.
D[0]	R/W	1bit 0	Frequency spread spectrum function enable: 0: Frequency spread spectrum function is disabled; 1: Frequency spread spectrum function is enabled.
Address: 0x02, Default Value: 0xA081			
Bit Name	Access	Default	Description
D[15]	R/W	1bit 1	LED channel diagnostic enable: 0: if Any channel LED open/short happens, false error flags and FAULT pin is pulled down; 1: if Any channel LED open/short happens, false error flags but FAULT pin is not pulled down.
D[14]	R/W	1bit 0	LED fault action setting: Once a channel fault is detected, the related channel will be latched or hiccup mode while the other channels work normally. 0: Hiccup at fault condition; 1: Latch at fault condition.
D[13]	RSV	1bit 1	RSV
D[12:8]	RSV	5bit 0	RSV
D[7]	R/W	1bit 1	OT(over temperature) warning diagnostic: 0: OT warning signal pulls down the FAULT pin; 1: OT warning signal doesn't pull down the FAULT pin.
D[6:1]	RSV	6bit 0	RSV
D[0]	R/W	1bit 1	Based analog circuit enable: 0: Analog circuit is disable, when disable, part will shut down; 1: Analog circuit is enabled, when enable, part will turn ON.
Address: 0x03, Default Value: 0x0000			
Bit Name	Access	Default	Description
D[15:0]	R/W	16bit 0 (load OTP CH_EN_INIT)	Channel x enable bit: 0: Channel is disabled; 1: Channel is enabled.
Address: 0x04, Default Value: 0x0000			
Bit Name	Access	Default	Description
D[15:0]	R1C/ W1C(default)	16bit 0	Channel x open protection false flag: 0: if read 0, no open fault is detected; 1: if read 1, open fault is detected.
Address: 0x05, Default Value: 0x0000			
Bit Name	Access	Default	Description

D[15:0]	R1C/ W1C(default)	16bit 0	Channel x short protection fault flag: 0: if read 0, no short fault is detected; 1: if read 1, short fault is detected.
Address: 0x06, Default Value: 0x0000			
Bit Name	Access	Default	Description
D[15]	RSV	1bit 0	RSV
D[14]	R1C/ W1C	1bit 0	Over temperature warning status: 0: if read 0, no over temperature warning; 1: if read 1, over temperature warning.
D[13]	R1C/ W1C	1bit 0	ISET pin short flag: 0: if read 0, no short detected at ISET pin; 1: if read 1, short detected at ISET pin.
D[12]	R1C/ W1C	1bit 0	ISET pin open flag: 0: if read 0, no open detected at ISET pin; 1: if read 1, open detected at ISET pin.
D[11]	RSV	1bit 0	RSV
D[10]	R1C/ W1C	1bit 0	Over temperature shut-down status: 0: if read 0, no over temperature shut-down; 1: if read 1, over temperature shut-down.
D[9:0]	RSV	10bit 0	RSV
Address: 0x07-0x16, Default Value: 0x0FFF			
Bit Name	Access	Default	Description
D[15:12]	RSV	4bit 0	RSV
D[11:0]	W/R	12bit 1	Channel x PWM dimming setting
Address: 0x2A, Default Value: 0x800C			
Bit Name	Access	Default	Description
D[15]	W/R	1bit 1	Host extend region write protection: 0: disable write protection for "h2A[6:0]" register; 1: enable write protection for "h2A[6:0]" register.
D[14:7]	RSV	8bit 0	RSV
D[6]	W/R	1bit 0	Exponential PWM DIM setting value enable. 0: disable exponential pwm dim; 1: enable exponential pwm dim.
D[5:4]	W/R	2bit 0	Thermal derating start temperature: 00: disable; 01: 110C; 10: 130C; 11: 150C.
D[3]	W/R	1bit 1	0: status 0x04-0x06 registers defined as R1C read 1 clear attribute; 1: status 0x04-0x06 registers defined as W1C(write 1 clear) attribute.

D[2]	W/R	1bit 1	0: disable write protection for "CLEAR_FS" register; 1: enable write protection for "CLEAR_FS" register; when enter FS mode, will automatically set "CLR_LOCK" to 1'b1.
D[1]	W/R	1bit 0	Write 1 to force device out of Fail-Safe mode to Normal mode; automatically reset to 0.
D[0]	W/R	1bit 0	Write 1 to force the device into Fail-Safe mode from Normal mode; automatically reset to 0.
Address: 0x2B, Default Value: 0x0000			
Bit Name	Access	Default	Description
D[15:2]	RSV	14bit 0	RSV
D[1]	RO	1bit 0	0: device works in Normal mode; 1: device works in Fail-Safe mode.
D[0]	RO	1bit 0	Fs Pin state report
Address: 0x2D, Default Value: 0x0000			
Bit Name	Access	Default	Description
D[15:8]	RSV	8bit 0	RSV
D[7:0]	W	8bit 0	Host OTP registers R/W protection password: 1: un-lock: continue execute one byte write command, firstly configurate 8'h93, secondly configurate 8'h65, can un-lock Host OTP registers Region. 2: lock: execute one byte write command, configurate 8'hcf, lock Host OTP registers Region again with invalid password, can't access R/W in Host OTP registers.
Address: 0x2E, Default Value: 0x0000			
Bit Name	Access	Default	Description
D[15]	W/R	1bit 0	1: Host Region registers execute OTP programming; automatically reset to 0 after OTP programming finish.
Address: 0x2F, Default Value: 0x0000			
Bit Name	Access	Default	Description
D[15:0]	OTP	16bit 0	Channel enable/disable bit in FS0 mode. when enter FS0 mode, will automatically update "CHx_EN_FS0" to host register "CHx_EN"(0x03)
Address: 0x30, Default Value: 0xFFFF			
Bit Name	Access	Default	Description
D[15:0]	OTP	16bit 1	Channel enable/disable bit in FS1 mode. when enter FS1 mode, will automatically update "CHx_EN_FS1" to host register "CHx_EN"(0x03)
Address: 0x31, Default Value: 0x0FFF			
Bit Name	Access	Default	Description
D[15:12]	RSV	4bit 0	RSV

D[11:0]	OTP	12bit 1	Channel PWM_DIM set in FS0/FS1 mode. when enter FS0/FS1 mode, will automatically update "PWM_DIM _FS" to host register "PWM_DIM_x "(0x07-0x16)
Address: 0x32, Default Value: 0x0140			
Bit Name	Access	Default	Description
D[15:10]	RSV	6bit 0	RSV
D[9:8]	OTP	2bit 01	Thermal derating start point in FS mode. 00: disable; 01: 110°C; 10: 130°C; 11: 150°C.
D[7]	OTP	1bit 0	Channel initial station(on/off) after POR
D[6]	OTP	1bit 1	One-fail-all-fail enable/disable in FS mode. 0: disable OFAF function, FS pin set to OUTPUT ONLY type; 1: enable OFAF function, FS pin set to I/O type. in normal mode, automatically disable OFAF function, ignore this bit.
D[5:3]	OTP	3bit 0	Initialization Timer set delay after POR. 000: 0ms. 001: 20ms. 010: 10ms. 011: 5ms. 100: 2ms. 101: 1ms. 110: 500µs. 111: 200µs.
D[2:0]	OTP	3bit 0	Watchdog Timer overflow set enter Fail-Safe mode. 000: disable Watchdog Timer, don't automatically enter FS mode. 001: 2ms. 010: 20ms. 011: 100ms. 100: 200ms. 101: 500ms. 110: 1s. 111: enter FS mode immediately.

8.3. Typical Application Circuit

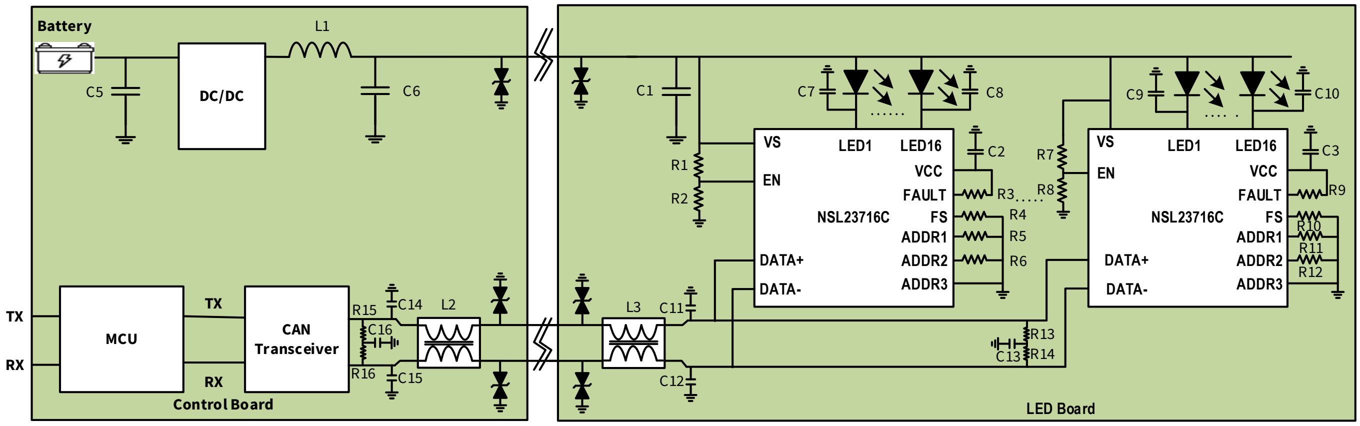


Figure8.11 Typical application diagram with differential interface (NSL23716C)

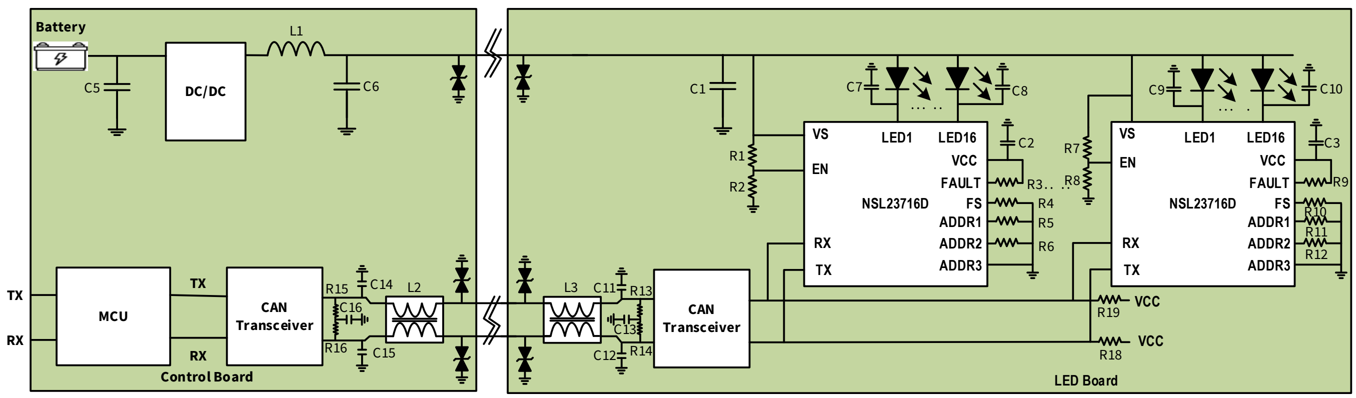


Figure8.12 Typical application diagram with UART interface (NSL23716D)

8.3.1. VS/VCC/OUTx Capacitor Selection

VS pin is the power supply for the total IC. Place 10µF and 0.1µF capacitors as close as possible to stable the VS pin voltage.

The VCC pin is an internal LDO output, and it supplies power to the internal control circuit and gate drivers. Place a ≥10µF decoupling capacitor to ground is required close to VCC. The capacitor's location of VCC should be as close as possible.

If the LED channels and LED driver IC are not on the same PCB board, which means the application is off board, the OUTx must connect a capacitor (10nF recommend) to GND to improve the ESD level. Furthermore, the capacitors connected between OUTx and GND are necessary for the EMI optimization even though LEDs and driver IC are on the same board application.

8.3.2. Design Consideration for BCI/EMC Test

To pass the BCI and EMC testing, please follow below suggestions:

1. Please place the capacitors as close to power pin including VS, VCC of IC.

2. The GND polygon is necessary since it provides good anti-interference ability, and it can improve the heat dissipation performance as well. The GND polygon is as large as good.

3. Please place the capacitors as close to OUTx pin of IC.

8.3.3. Typical Application Schematic and Layout

Figure8.13 and Figure8.14 show the typical application schematic and layout.

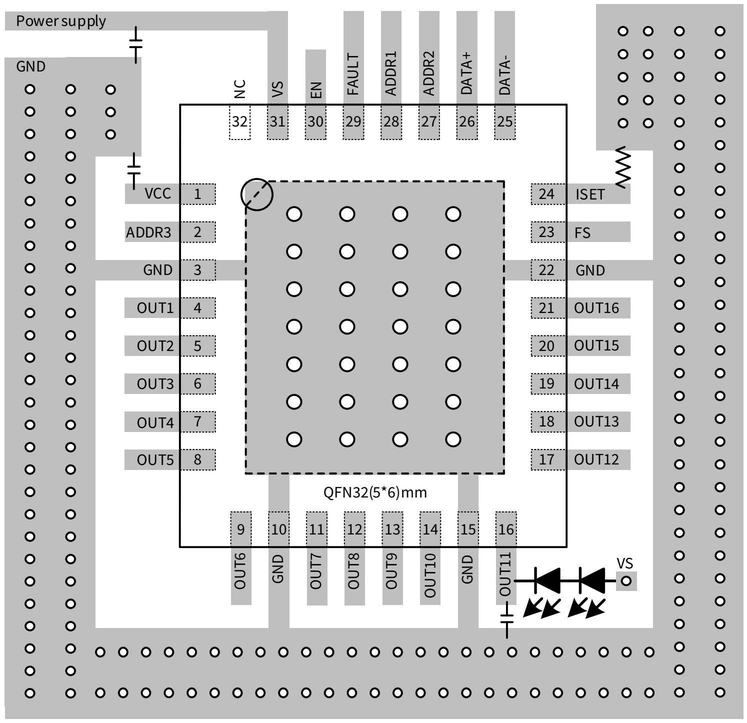


Figure8.13 NSL23716C layout

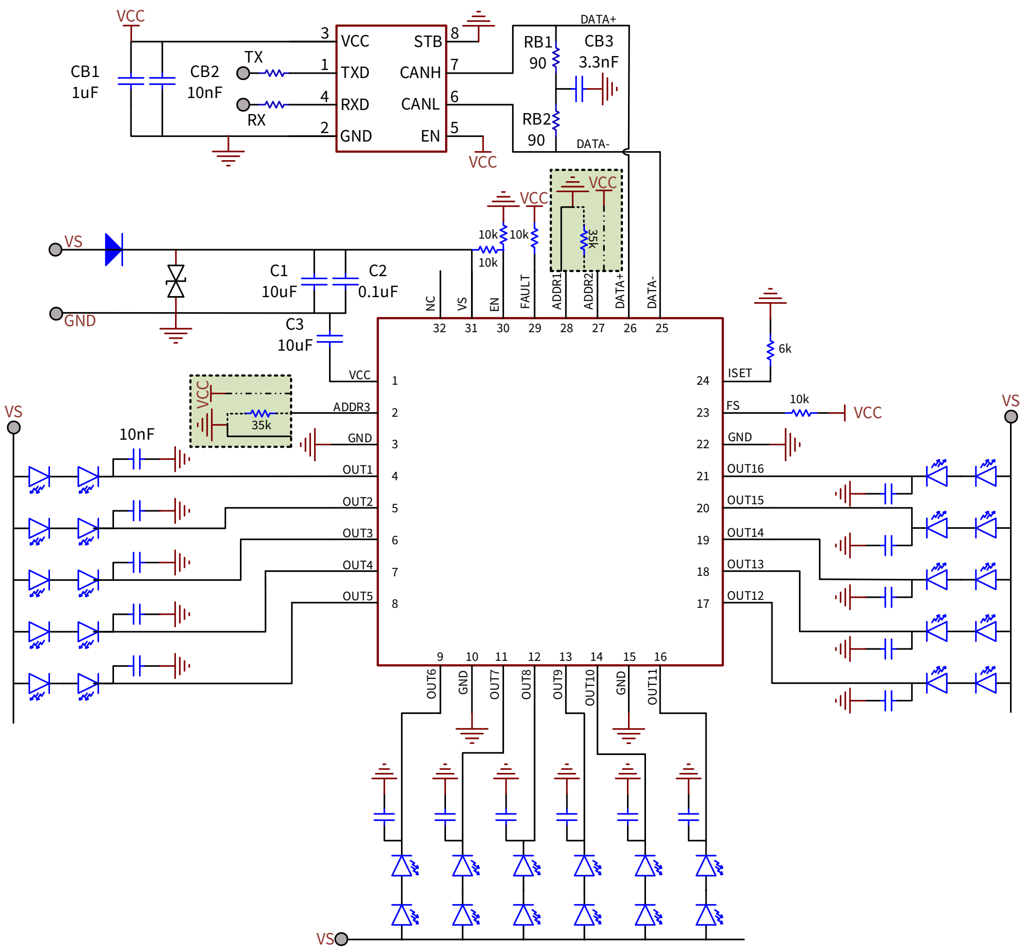
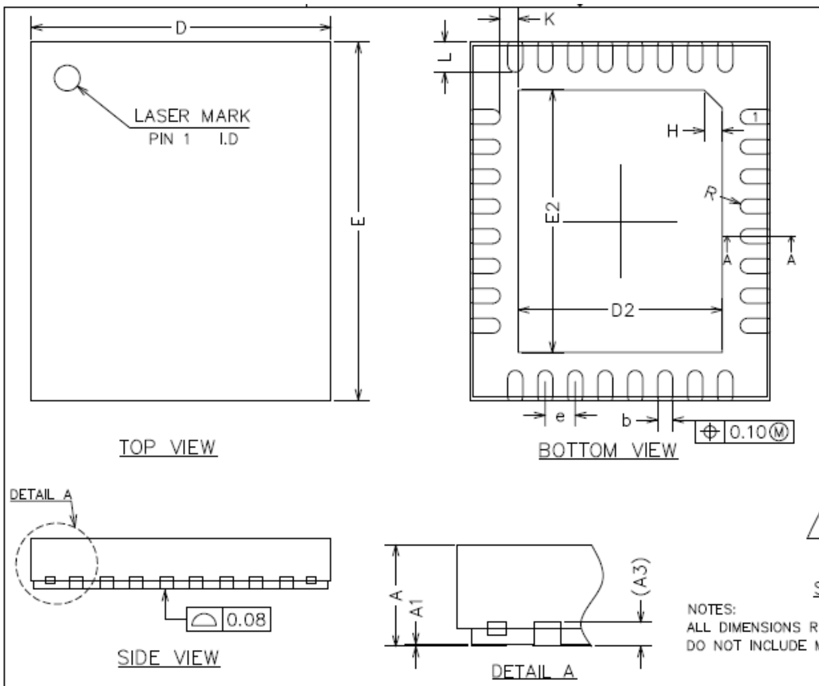


Figure8.14 Typical application schematic (NSL23716C)

9. Package Information

9.1. QFN32-5*6mm

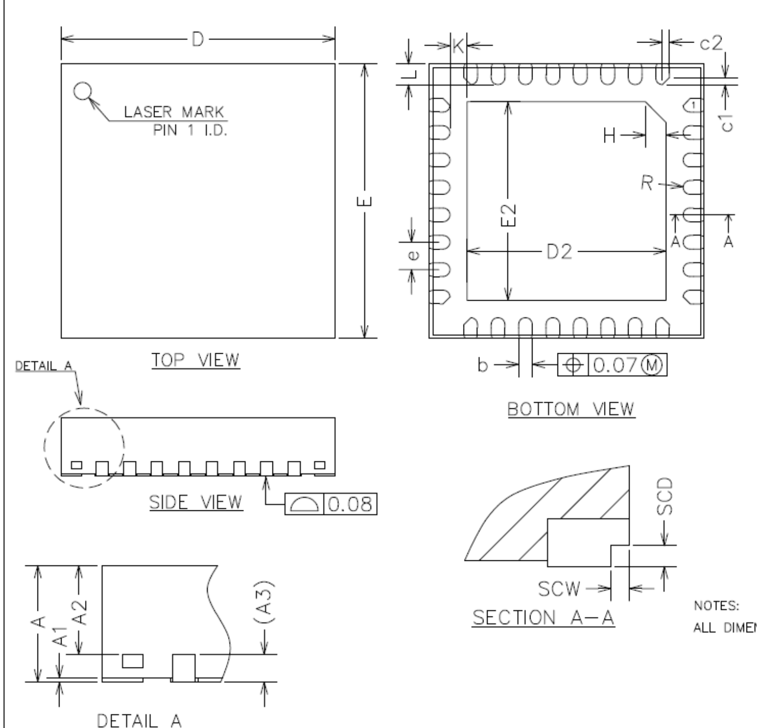


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
A3		0.20REF	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	5.90	6.00	6.10
D2	3.35	3.40	3.45
E2	4.35	4.40	4.45
e		0.50BSC	
H		0.30REF	
K	0.20	–	–
L	0.45	0.50	0.55
R	0.09	–	–
SCW	0.01	–	0.09
SCD	0.08	–	0.18

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO–220
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

9.2. QFN32-4*4mm



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	0.60	0.65	0.70
A3		0.20REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.80	2.90	3.00
E2	2.80	2.90	3.00
e	0.30	0.40	0.50
H		0.30REF	
K		0.25REF	
L	0.25	0.30	0.35
R	0.09	–	–
c1	–	0.10	–
c2	–	0.10	–
SCW	0.01	–	0.09
SCD	0.08	–	0.18

NOTES:
ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

10. Order Information

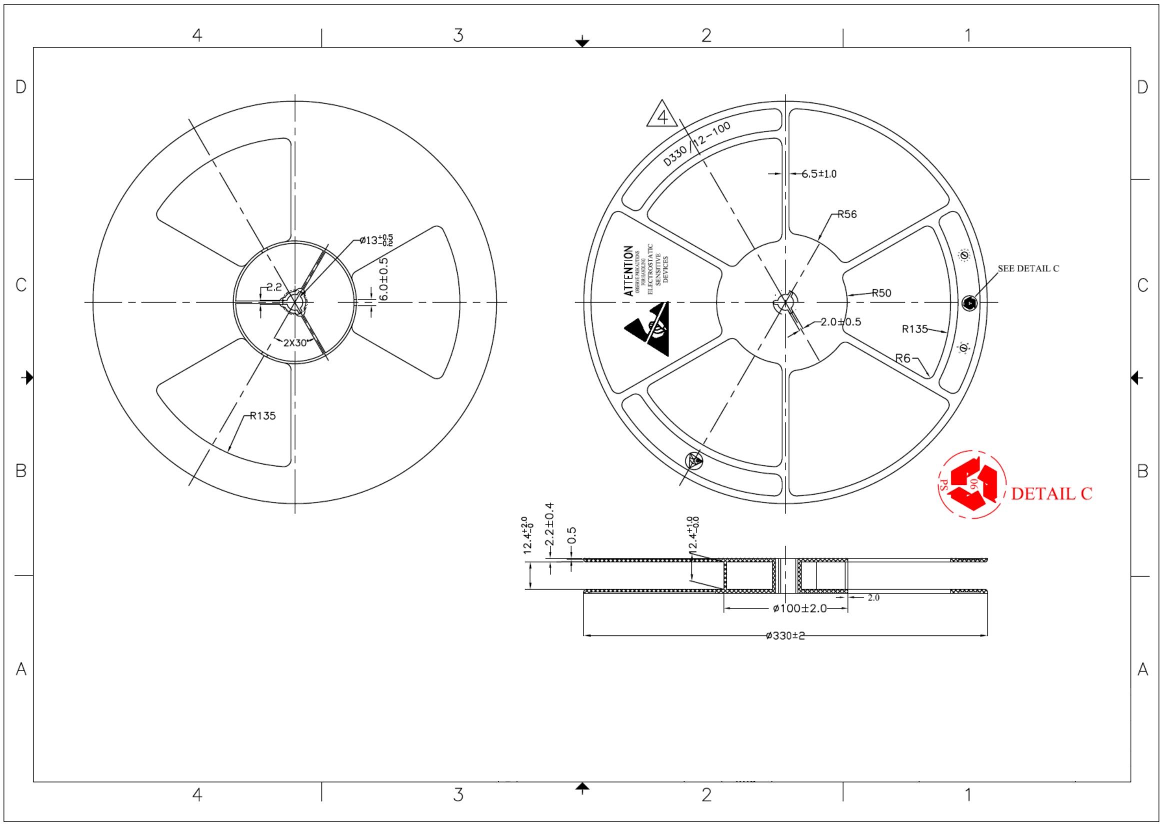
PN	Interface	Fail safe	MSL	ADDR Configuration	ADDR_OTP Bit	Package
NSL23716A-Q1QAMR	Differential interface	NO	3	ADDR_OTP bit+ADDR1/2	0	QFN32(5mm*6mm)
NSL237161A-Q1QAMR			3		1	
NSL23716C-Q1QAMR	Differential interface	YES	3	ADDR1/2/3 pin	/	
NSL23716D-Q1QAMR	UART interface		3			
NSL23716C-Q1QALR	Differential interface		3			QFN32(4mm*4mm)
NSL23716D-Q1QALR	UART interface		3			

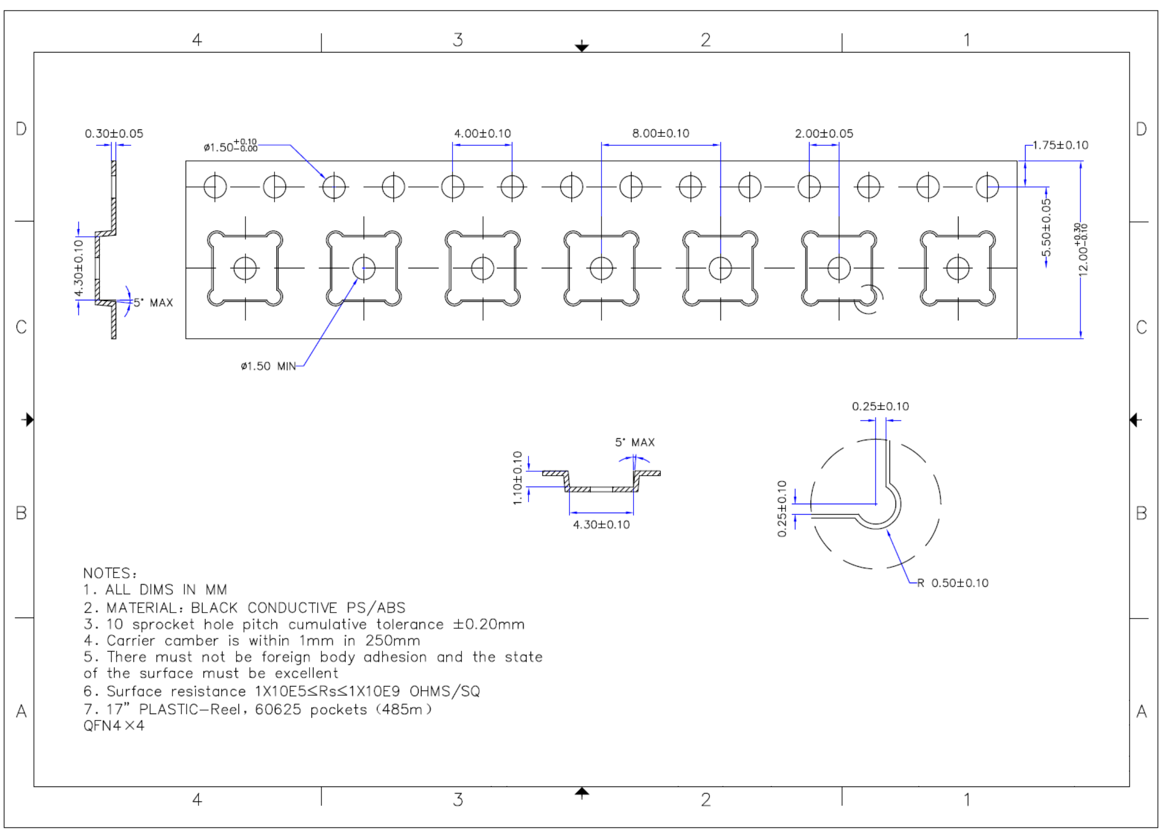
11. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	LED driver Selection Guide

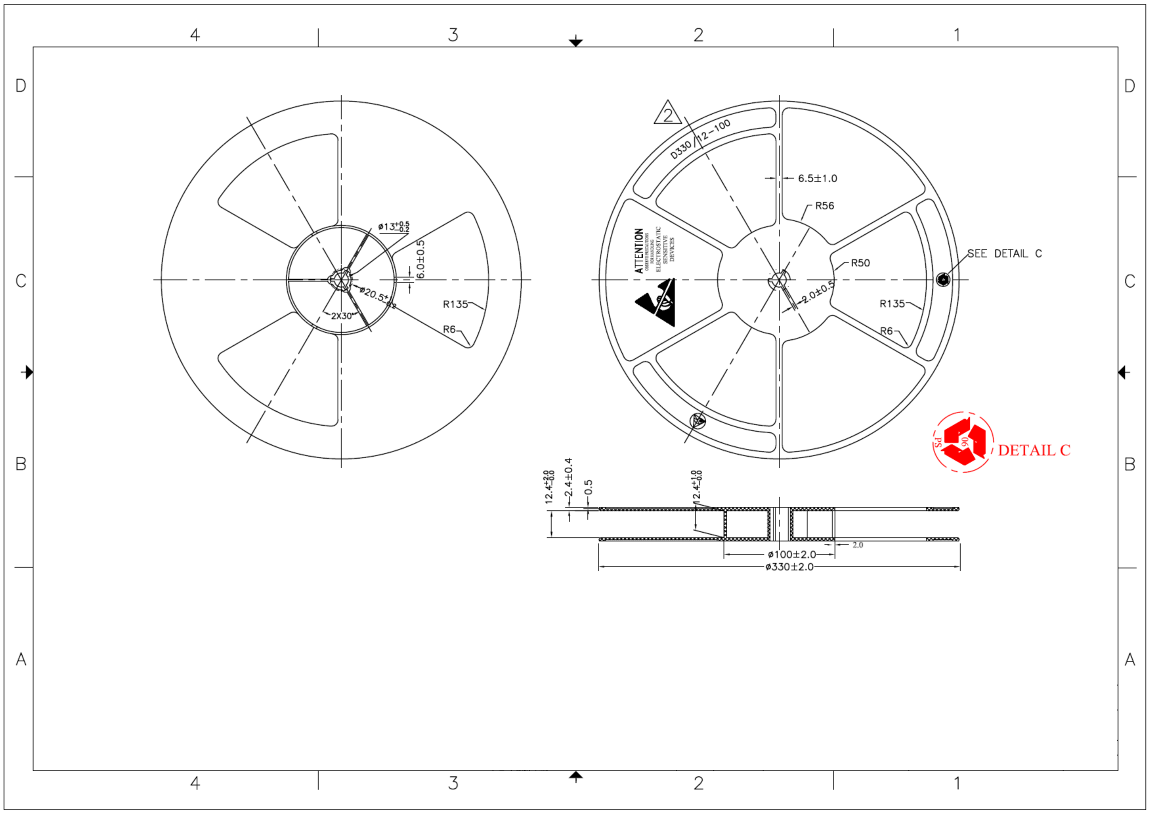
12. Tape and Reel Information

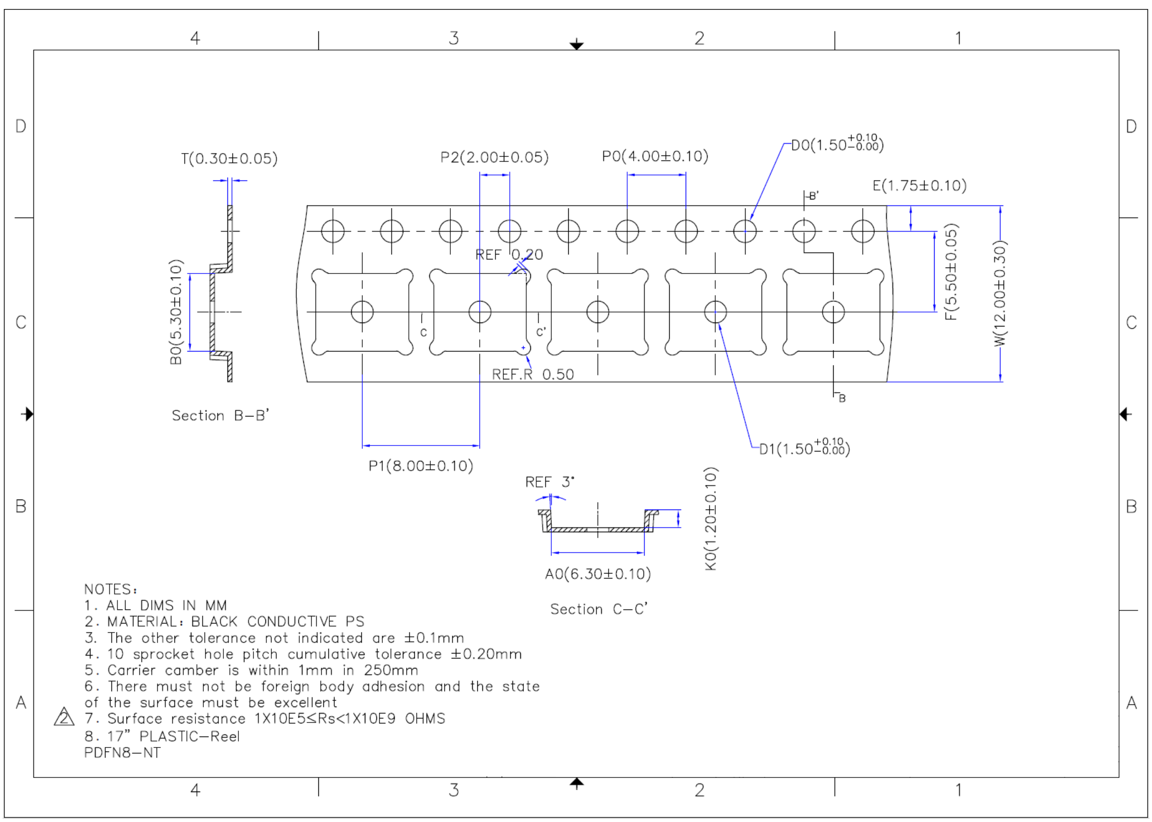
QFN32(4*4):5000/reel.





QFN32(5*6):4000/reel.





13. Revision History

Revision	Description	Date
1.0	Initial release	2025/03

IMPORTANT NOTICE