

## Product Overview

The NSIP984x devices are quad-channel digital isolators with integrated isolated DC-DC converter. The isolated DC-DC converter provides up to 500mW output power using on-chip transformer. The feedback PWM signal is sent to primary side by a digital isolator based on Novosense capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The NSIP984x devices are safety certified by UL1577, supporting 5.0kVrms withstand voltage while providing high electromagnetic immunity and low emissions. The data rate of the NSIP984x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 100kV/μs. The NSIP984x devices provide 5V to 5V, 5V to 3.3V, 3.3V to 3.3V conversion mode, the output voltage can be set by SEL pin.

## Key Features

- AEC-Q100 Qualified for Grade 1: TA from -40 °C to 125 °C
- Up to 5000Vrms insulation voltage
- Power supply voltage:  
 $V_{DD}$ : 3V to 5.25V  $V_{DDL}$ : 1.8V to 5.5V
- 5V to 5V, 5V to 3.3V, support 100mA load current
- 3.3V to 3.3V, support 60mA load current
- Over current and over temperature protection
- Data rate: DC to 150Mbps
- High CMTI: 100kV/μs
- High system level EMC performance:  
 Enhanced system level ESD, EFT, Surge immunity
- Operation temperature: -40°C~125°C
- RoHS-compliant packages: SOW16

## Safety Regulatory Approvals

- UL recognition: up to 5000V<sub>rms</sub> for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN VDE V 0884-17

## Applications

- Solar inverter & Energy storage
- EV charging piles
- Grid infrastructure & smart meter
- Heat pump
- Medical & Measurement

## Device Information

| Part Number    | Package | Body Size        |
|----------------|---------|------------------|
| NSIP984x-Q1SWR | SOW16   | 10.30mm × 7.50mm |

## Functional Block Diagrams

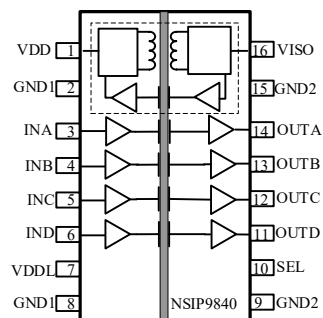


Figure 1. NSIP984x Block Diagram<sup>1</sup>

<sup>1</sup> The isolation channel direction can be either depend on different part number.

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# 1. Pin Configuration And Functions

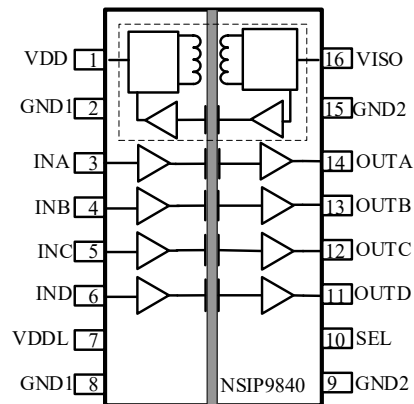


Figure 1.1 NSIP9840 Package

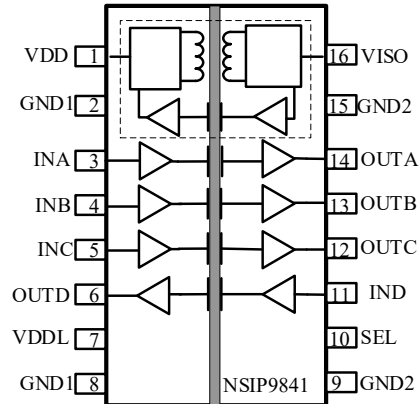


Figure 1.2 NSIP9841 Package

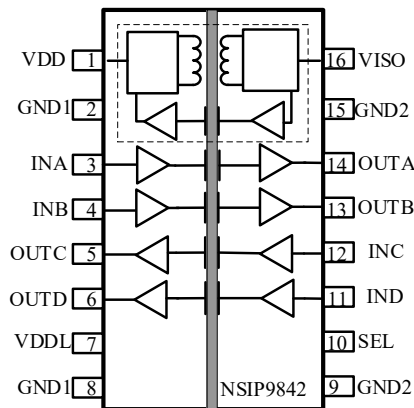


Figure 1.3 NSIP9842 Package

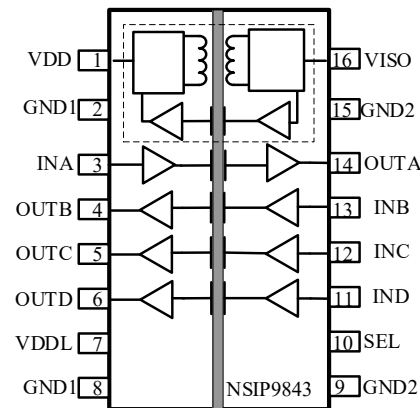


Figure 1.4 NSIP9843 Package

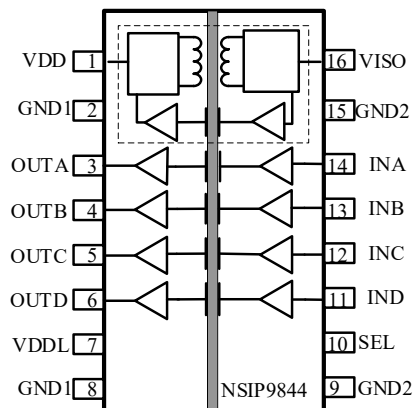


Figure 1.5 NSIP9844 Package

Table1.1 NSIP9840/ NSIP9841/ NSIP9842/ NSIP9843/NSIP9844 Pin Configuration and Description

| <b>NSIP9840<br/>PIN NO.</b> | <b>NSIP9841<br/>PIN NO.</b> | <b>NSIP9842<br/>PIN NO.</b> | <b>NSIP9843<br/>PIN NO.</b> | <b>NSIP9844<br/>PIN NO.</b> | <b>SYMBOL</b> | <b>FUNCTION</b>  |
|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|---------------|--|
| 1                           | 1                           | 1                           | 1                           | 1                           | VDD           | Primary Supply Voltage.  |
| 2                           | 2                           | 2                           | 2                           | 2                           | GND1          | Ground 1. Ground reference for Isolator Side primary. Pin 2 and Pin 8 are not internally connected. It is required that pin2 and pin8 be connected to a common ground. |
| 3                           | 3                           | 3                           | 3                           | 14                          | INA           | Logic Input A.   |
| 4                           | 4                           | 4                           | 13                          | 13                          | INB           | Logic Input B.   |
| 5                           | 5                           | 12                          | 12                          | 12                          | INC           | Logic Input C.   |
| 6                           | 11                          | 11                          | 11                          | 11                          | IND           | Logic Input D.   |
| 7                           | 7                           | 7                           | 7                           | 7                           | VDDL          | Side1 I/O logic level. When VDDL is not powered, the chip will shut down   |
| 8                           | 8                           | 8                           | 8                           | 8                           | GND1          | Ground 1. Ground reference for Isolator Side primary. Pin 2 and Pin 8 are not internally connected. It is required that pin2 and pin8 be connected to a common ground. |
| 9                           | 9                           | 9                           | 9                           | 9                           | GND2          | Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected. It is recommended that pin9 and pin16 be connected to a common ground.      |
| 10                          | 10                          | 10                          | 10                          | 10                          | SEL           | VISO output voltage selection. VISO=5V when SEL short to VISO, VISO=3.3V when SEL short to GND2 or floating.   |
| 11                          | 6                           | 6                           | 6                           | 6                           | OUTD          | Logic Output D.  |
| 12                          | 12                          | 5                           | 5                           | 5                           | OUTC          | Logic Output C.  |
| 13                          | 13                          | 13                          | 4                           | 4                           | OUTB          | Logic Output B.  |
| 14                          | 14                          | 14                          | 14                          | 3                           | OUTA          | Logic Output A.  |
| 15                          | 15                          | 15                          | 15                          | 15                          | GND2          | Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected. It is recommended that pin9 and pin16 be connected to a common ground.      |
| 16                          | 16                          | 16                          | 16                          | 16                          | VISO          | Secondary Supply Voltage Output for External Loads.  |

## 2. Absolute Maximum Ratings<sup>1</sup>

| Parameter                                   | Symbol   | Min  | Typ | Max                              | Unit | Comments |
|---|--|------|-----|----------------------------------|------|----------|
| Power Supply Voltage <sup>2</sup>           | $V_{DD}, V_{ISO}$  | -0.5 |     | 6                                | V    |          |
| Side1 I/O logic level <sup>2</sup>          | $V_{DDL}$  | -0.5 |     | 6                                | V    |          |
| Voltage at INx, OUTx, SEL pins <sup>2</sup> | $V_{INA}, V_{INB}$<br>$V_{INC}, V_{IND},$<br>$V_{OUTA}, V_{OUTB}$<br>$V_{OUTC}, V_{OUTD}$<br>$V_{SEL}$ | -0.5 |     | $V_{DDL}+0.5$<br>$V_{ISO}+0.5^3$ | V    |          |
| Logic output current                        | $I_o$  | -15  |     | 15                               | mA   |          |
| Junction Temperature                        | $T_J$  | -40  |     | 150                              | °C   |          |
| Storage Temperature                         | $T_{stg}$  | -40  |     | 150                              | °C   |          |

<sup>1</sup>Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>2</sup>All voltage values are with respect to the local ground pin (GND1 or GND2) and are peak voltage values.

<sup>3</sup>This value depends on whether the pin is located on the VDDL or VISO side. The maximum voltage at the I/O pins should not exceed 6 V.

## 3. ESD Ratings

|  | Ratings   | Value   | Unit |
|--|---|---|------|
|  | Electrostatic discharge                           | Human body model (HBM), per AEC-Q100-002-RevD | ±8.0 |
|  | Charged device model (CDM), per AEC-Q100-011-RevB | ±2.0  | kV   |

## 4. Recommended Operating Conditions

| Parameters                | Symbol                                  | min | typ | max  | unit |
|---------------------------|---|-----|-----|------|------|
| Power Supply Voltage      | $V_{DD} @ V_{SEL} = 0V/\text{Floating}$ | 3   |     | 5.25 | V    |
|                           | $V_{DD} @ V_{SEL} = V_{ISO}$            | 4.5 |     | 5.25 | V    |
| Side1 I/O logic level     | $V_{DDL}$                               | 1.8 |     | 5.5  | V    |
| High level output current | $I_{OH} @ V_{DO}^1 = 5V$                | -4  |     |      | mA   |
|                           | $I_{OH} @ V_{DO}^1 = 3.3V$              | -2  |     |      | mA   |
| Low level output current  | $I_{OL} @ V_{DO}^1 = 5V$                |     |     | 4    | mA   |

| Parameters               | Symbol                     | min              | typ | max              | unit |
|--------------------------|----------------------------|------------------|-----|------------------|------|
|                          | $I_{OL} @ V_{DO}^1 = 3.3V$ |                  |     | 2                | mA   |
| High Level Input Voltage | $V_{IH}$                   | $0.7 * V_{DI}^1$ |     | $V_{DI}^1$       | V    |
| Low Level Input Voltage  | $V_{IL}$                   | 0                |     | $0.3 * V_{DI}^1$ | V    |
| Data rate                | DR                         |                  |     | 150              | Mbps |
| Ambient temperature      | $T_a$                      | -40              |     | 125              | °C   |

<sup>1</sup> $V_{DI}$  is the input side supply,  $V_{DO}$  is the output side supply. This value depends on whether the pin is located on the VDDL or VISO side.

## 5. Thermal Characteristics

| Parameters                                | Symbol        | SOW16 | Unit |
|---|---------------|-------|------|
| IC Junction-to-Air Thermal Resistance     | $\theta_{JA}$ | 59.2  | °C/W |
| Junction-to-case (top) thermal resistance | $\psi_{JT}$   | 8.7   | °C/W |
| Junction-to-board thermal resistance      | $\psi_{JB}$   | 23    | °C/W |

## 6. Specifications

### 6.1. Isolated DC/DC Converter Static Specifications

( $V_{DD}=4.5V\sim 5.25V$ ,  $V_{DDL}=1.8V\sim 5.5V$ ,  $SEL=V_{ISO}$ ,  $T_a=-40^{\circ}C$  to  $125^{\circ}C$ . Unless otherwise noted, Typical values are at  $V_{DD} = V_{DDL} = 5V$ ,  $T_a = 25^{\circ}C$ )

| Parameters                                | Symbol          | Min | Typ | Max  | Unit | Comments   |
|---|-----------------|-----|-----|------|------|--|
| Isolated Supply Voltage                   | $V_{ISO}$       | 4.6 | 5   | 5.25 | V    | $I_{ISO} = 0$ to 100mA   |
| Positive-going UVLO threshold on $V_{DD}$ | $V_{DD+(UVLO)}$ |     | 2.7 | 3    | V    |  |
| Negative-going UVLO threshold on $V_{DD}$ | $V_{DD-(UVLO)}$ | 2.1 | 2.5 |      | V    |  |
| UVLO threshold hysteresis on $V_{DD}$     | $V_{HYS(UVLO)}$ |     | 0.2 |      | V    |  |
| Line Regulation                           | $V_{ISO(LINE)}$ |     | 2   |      | mV/V | $I_{ISO} = 50mA$ , $V_{DD} = 4.5V$ to $5.25V$                            |
| Load Regulation                           | $V_{ISO(LOAD)}$ |     | 0.5 |      | %    | $I_{ISO} = 10$ to 90mA   |
| Output Ripple                             | $V_{ISO(RIP)}$  |     | 70  |      | mVpp | 20MHz bandwidth, $C_{LOAD} = 0.1 \mu F    10 \mu F$ , $I_{ISO} = 100 mA$ |
| Efficiency at maximum load current        | EFF             |     | 49  |      | %    | $I_{ISO} = 100mA$ , $C_{LOAD} = 0.1 \mu F    10 \mu F$                   |
| Current available to isolated supply      | $I_{ISO}$       | 100 |     |      | mA   |  |

| Parameters                                  | Symbol                 | Min | Typ | Max | Unit | Comments                |
|---|------------------------|-----|-----|-----|------|-------------------------|
| VDD supply current without digital isolator | I <sub>VDD_POWER</sub> |     | 36  | 60  | mA   | No VISO Load            |
|   |                        |     | 200 | 265 | mA   | I <sub>ISO</sub> =100mA |

(V<sub>DD</sub>=4.5V~5.25V, V<sub>DDL</sub>=1.8V~ 5.5V, SEL=0V, T<sub>a</sub>=-40°C to 125°C. Unless otherwise noted, Typical values are at V<sub>DD</sub> = V<sub>DDL</sub> = 5V, T<sub>a</sub> = 25°C)

| Parameters                                       | Symbol                 | Min | Typ | Max | Unit | Comments  |
|--|------------------------|-----|-----|-----|------|---|
| Isolated Supply Voltage                          | V <sub>ISO</sub>       | 3   | 3.3 | 3.5 | V    | I <sub>ISO</sub> = 0 to 100mA   |
| Positive-going UVLO threshold on V <sub>DD</sub> | V <sub>DD+(UVLO)</sub> |     | 2.7 | 3   | V    |   |
| Negative-going UVLO threshold on V <sub>DD</sub> | V <sub>DD-(UVLO)</sub> | 2.1 | 2.5 |     | V    |   |
| UVLO threshold hysteresis on V <sub>DD</sub>     | V <sub>HYS(UVLO)</sub> |     | 0.2 |     | V    |   |
| Line Regulation                                  | V <sub>ISO(LINE)</sub> |     | 2   |     | mV/V | I <sub>ISO</sub> = 50mA, V <sub>DD</sub> = 4.5V to 5.25V                        |
| Load Regulation                                  | V <sub>ISO(LOAD)</sub> |     | 0.5 |     | %    | I <sub>ISO</sub> = 10 to 90mA   |
| Output Ripple                                    | V <sub>ISO(RIP)</sub>  |     | 70  |     | mVpp | 20MHz bandwidth, C <sub>LOAD</sub> = 0.1 μF    10 μF, I <sub>ISO</sub> = 100 mA |
| Efficiency at maximum load current               | EFF                    |     | 40  |     | %    | I <sub>ISO</sub> = 100mA, C <sub>LOAD</sub> = 0.1μF   10μF                      |
| Current available to isolated supply             | I <sub>ISO</sub>       | 100 |     |     | mA   |   |
| VDD supply current without digital isolator      | I <sub>VDD_POWER</sub> |     | 32  | 55  | mA   | No VISO Load  |
|  |                        |     | 165 | 230 | mA   | I <sub>ISO</sub> =100mA   |

(V<sub>DD</sub>=3V~3.6V, V<sub>DDL</sub>=1.8V~ 5.5V, SEL=0V, T<sub>a</sub>=-40°C to 125°C. Unless otherwise noted, Typical values are at V<sub>DD</sub> = V<sub>DDL</sub> = 3.3V, T<sub>a</sub> = 25°C)

| Parameters                                       | Symbol                 | Min | Typ | Max | Unit | Comments  |
|--|------------------------|-----|-----|-----|------|---|
| Isolated Supply Voltage                          | V <sub>ISO</sub>       | 3   | 3.3 | 3.5 | V    | I <sub>ISO</sub> = 0 to 60mA                          |
| Positive-going UVLO threshold on V <sub>DD</sub> | V <sub>DD+(UVLO)</sub> |     | 2.7 | 3   | V    |   |
| Negative-going UVLO threshold on V <sub>DD</sub> | V <sub>DD-(UVLO)</sub> | 2.1 | 2.5 |     | V    |   |
| UVLO threshold hysteresis on V <sub>DD</sub>     | V <sub>HYS(UVLO)</sub> |     | 0.2 |     | V    |   |
| Line Regulation                                  | V <sub>ISO(LINE)</sub> |     | 3   |     | mV/V | I <sub>ISO</sub> = 30mA, V <sub>DD</sub> = 3V to 3.6V |
| Load Regulation                                  | V <sub>ISO(LOAD)</sub> |     | 1   |     | %    | I <sub>ISO</sub> = 10 to 54mA                         |

| Parameters                                  | Symbol           | Min | Typ | Max | Unit | Comments   |
|---|------------------|-----|-----|-----|------|--|
| Output Ripple                               | $V_{ISO(RIP)}$   |     | 45  |     | mVpp | 20MHz bandwidth, $C_{LOAD} = 0.1 \mu F \parallel 10 \mu F$ , $I_{ISO} = 60 \text{ mA}$ |
| Efficiency at maximum load current          | EFF              |     | 48  |     | %    | $I_{ISO} = 60 \text{ mA}$ , $C_{LOAD} = 0.1 \mu F \parallel 10 \mu F$                  |
| Current available to isolated supply        | $I_{ISO}$        | 60  |     |     | mA   |  |
| VDD supply current without digital isolator | $I_{VDD\_POWER}$ |     | 35  | 60  | mA   | No VISO Load   |
|   |                  |     | 131 | 170 | mA   | $I_{ISO} = 60 \text{ mA}$  |

## 6.2. Digital Isolator Electrical Characteristics

| Parameters                     | Symbol        | Min                  | Typ | Max                  | Unit        | Comments  |
|--------------------------------|---------------|----------------------|-----|----------------------|-------------|---|
| Input pin rising threshold     | $V_{ITH}$     | $0.7 \cdot V_{DI}^1$ |     |                      | V           |   |
| Input pin falling threshold    | $V_{ITL}$     |                      |     | $0.3 \cdot V_{DI}^1$ | V           |   |
| Input pin threshold hysteresis | $V_{I(UVLO)}$ | $0.1 \cdot V_{DI}^1$ |     |                      | V           |   |
| High level input current       | $I_{IH}$      |                      | 8   | 15                   | $\mu A$     | $V_I = V_{DI}^1$ at INx or SEL                  |
| Low level input current        | $I_{IL}$      | -15                  | -8  |                      | $\mu A$     | $V_I = 0$ at INx or SEL                         |
| High Level Output Voltage      | $V_{OH}$      | $V_{DO}^1 - 0.4$     |     |                      | V           | $V_{DO}^1 = 5V$ , $I_{OH} \geq -4 \text{ mA}$   |
|                                |               | $V_{DO}^1 - 0.3$     |     |                      | V           | $V_{DO}^1 = 3.3V$ , $I_{OH} \geq -2 \text{ mA}$ |
| Low Level Output Voltage       | $V_{OL}$      |                      |     | 0.4                  | V           | $V_{DO}^1 = 5V$ , $I_{OL} \leq 4 \text{ mA}$    |
|                                |               |                      |     | 0.3                  | V           | $V_{DO}^1 = 3.3V$ , $I_{OL} \leq 2 \text{ mA}$  |
| Output Impedance               | $R_{out}$     |                      | 50  |                      | ohm         |   |
| Common Mode Transient Immunity | CMTI          | 100                  | 150 |                      | kV/ $\mu s$ | $V_I = V_{DI}^1$ or 0 V                         |
| Thermal Shutdown Temperature   |               |                      | 165 |                      | $^{\circ}C$ |   |

<sup>1</sup> $V_{DI}$  is the input side supply,  $V_{DO}$  is the output side supply. This value depends on whether the pin is located on the VDDL or VISO side.

( $V_{DD}=4.5V\sim 5.25V$ ,  $V_{DDL}=1.8V\sim 5.5V$ ,  $SEL=V_{ISO}$ ,  $T_a=-40^{\circ}C$  to  $125^{\circ}C$ . Unless otherwise noted, Typical values are at  $V_{DD} = V_{DDL} = 5V$ ,  $T_a = 25^{\circ}C$ )

| Parameters     | Symbol         | Min | Typ | Max | Unit | Comments  |
|----------------|----------------|-----|-----|-----|------|---|
| Supply Current | NSIP9840       |     |     |     |      |   |
|                | $I_{DD(Q0)}$   |     | 35  |     | mA   | All Input 0V for NSIP9840W0 or All Input at supply for NSIP9840W1 |
|                | $I_{DD(Q1)}$   |     | 38  |     | mA   | All Input at supply for NSIP9840W0 or All Input 0V for NSIP9840W1 |
|                | $I_{DD(1M)}$   |     | 35  |     | mA   | All Input with 1Mbps square wave, $C_L=15pF$                      |
|                | $I_{DD(10M)}$  |     | 39  |     | mA   | All Input with 10Mbps square wave, $C_L=15pF$                     |
|                | $I_{DD(100M)}$ |     | 70  |     | mA   | All Input with 100Mbps square wave, $C_L=15pF$                    |
|                | NSIP9841       |     |     |     |      |   |
|                | $I_{DD(Q0)}$   |     | 36  |     | mA   | All Input 0V for NSIP9841W0 or All Input at supply for NSIP9841W1 |
|                | $I_{DD(Q1)}$   |     | 40  |     | mA   | All Input at supply for NSIP9841W0 or All Input 0V for NSIP9841W1 |
|                | $I_{DD(1M)}$   |     | 38  |     | mA   | All Input with 1Mbps square wave, $C_L=15pF$                      |
|                | $I_{DD(10M)}$  |     | 42  |     | mA   | All Input with 10Mbps square wave, $C_L=15pF$                     |
|                | $I_{DD(100M)}$ |     | 74  |     | mA   | All Input with 100Mbps square wave, $C_L=15pF$                    |
|                | NSIP9842       |     |     |     |      |   |
|                | $I_{DD(Q0)}$   |     | 37  |     | mA   | All Input 0V for NSIP9842W0 or All Input at supply for NSIP9842W1 |
|                | $I_{DD(Q1)}$   |     | 42  |     | mA   | All Input at supply for NSIP9842W0 or All Input 0V for NSIP9842W1 |
|                | $I_{DD(1M)}$   |     | 41  |     | mA   | All Input with 1Mbps square wave, $C_L=15pF$                      |
|                | $I_{DD(10M)}$  |     | 45  |     | mA   | All Input with 10Mbps square wave, $C_L=15pF$                     |
|                | $I_{DD(100M)}$ |     | 78  |     | mA   | All Input with 100Mbps square wave, $C_L=15pF$                    |
|                | NSIP9843       |     |     |     |      |   |
|                | $I_{DD(Q0)}$   |     | 38  |     | mA   | All Input 0V for NSIP9843W0 or All Input at supply for NSIP9843W1 |

| Parameters                    | Symbol                | Min | Typ | Max | Unit   | Comments  |  |
|-------------------------------|-----------------------|-----|-----|-----|--|---|--|
| Supply Current                | I <sub>DD(Q1)</sub>   |     | 44  |     | mA   | All Input at supply for NSIP9843W0 or All Input 0V for NSIP9843W1 |  |
|                               | I <sub>DD(1M)</sub>   |     | 44  |     | mA   | All Input with 1Mbps square wave, C <sub>L</sub> =15pF            |  |
|                               | I <sub>DD(10M)</sub>  |     | 48  |     | mA   | All Input with 10Mbps square wave, C <sub>L</sub> =15pF           |  |
|                               | I <sub>DD(100M)</sub> |     | 82  |     | mA   | All Input with 100Mbps square wave, C <sub>L</sub> =15pF          |  |
|                               | NSIP9844              |     |     |     |  |   |  |
|                               | I <sub>DD(Q0)</sub>   |     | 39  |     | mA   | All Input 0V for NSIP9844W0 or All Input at supply for NSIP9844W1 |  |
|                               | I <sub>DD(Q1)</sub>   |     | 46  |     | mA   | All Input at supply for NSIP9844W0 or All Input 0V for NSIP9844W1 |  |
|                               | I <sub>DD(1M)</sub>   |     | 47  |     | mA   | All Input with 1Mbps square wave, C <sub>L</sub> =15pF            |  |
| I <sub>DD(10M)</sub>          |                       | 51  |     | mA  | All Input with 10Mbps square wave, C <sub>L</sub> =15pF  |   |  |
| I <sub>DD(100M)</sub>         |                       | 86  |     | mA  | All Input with 100Mbps square wave, C <sub>L</sub> =15pF |   |  |
| Data Rate                     | DR                    | 0   |     | 150 | Mbps   |   |  |
| Minimum Pulse Width           | PW                    |     |     | 5   | ns   |   |  |
| Propagation Delay             | t <sub>PLH</sub>      |     | 10  | 25  | ns   |   |  |
|                               | t <sub>PHL</sub>      |     | 10  | 25  | ns   |   |  |
| Pulse Width Distortion        | PWD                   |     |     | 5   | ns   | t <sub>PHL</sub> - t <sub>PLH</sub>                               |  |
| Rising Time                   | t <sub>r</sub>        |     |     | 5   | ns   | C <sub>L</sub> = 15pF   |  |
| Falling Time                  | t <sub>f</sub>        |     |     | 5   | ns   | C <sub>L</sub> = 15pF   |  |
| Channel-to-Channel Delay Skew | t <sub>SK(c2c)</sub>  |     |     | 2.5 | ns   |   |  |
| Part-to-Part Delay Skew       | t <sub>SK(p2p)</sub>  |     |     | 5   | ns   |   |  |

( $V_{DD}=4.5V\sim 5.25V$ ,  $V_{DDL}=1.8V\sim 5.5V$ ,  $SEL=0V$ ,  $T_a=-40^{\circ}C$  to  $125^{\circ}C$ . Unless otherwise noted, Typical values are at  $V_{DD} = V_{DDL} = 5V$ ,  $T_a = 25^{\circ}C$ )

| Parameters     | Symbol         | Min | Typ | Max | Unit | Comments  |
|----------------|----------------|-----|-----|-----|------|---|
| Supply Current | NSIP9840       |     |     |     |      |   |
|                | $I_{DD(Q0)}$   |     | 32  |     | mA   | All Input 0V for NSIP9840W0 or All Input at supply for NSIP9840W1 |
|                | $I_{DD(Q1)}$   |     | 36  |     | mA   | All Input at supply for NSIP9840W0 or All Input 0V for NSIP9840W1 |
|                | $I_{DD(1M)}$   |     | 35  |     | mA   | All Input with 1Mbps square wave, $C_L=15pF$                      |
|                | $I_{DD(10M)}$  |     | 34  |     | mA   | All Input with 10Mbps square wave, $C_L=15pF$                     |
|                | $I_{DD(100M)}$ |     | 50  |     | mA   | All Input with 100Mbps square wave, $C_L=15pF$                    |
|                | NSIP9841       |     |     |     |      |   |
|                | $I_{DD(Q0)}$   |     | 32  |     | mA   | All Input 0V for NSIP9841W0 or All Input at supply for NSIP9841W1 |
|                | $I_{DD(Q1)}$   |     | 36  |     | mA   | All Input at supply for NSIP9841W0 or All Input 0V for NSIP9841W1 |
|                | $I_{DD(1M)}$   |     | 35  |     | mA   | All Input with 1Mbps square wave, $C_L=15pF$                      |
|                | $I_{DD(10M)}$  |     | 36  |     | mA   | All Input with 10Mbps square wave, $C_L=15pF$                     |
|                | $I_{DD(100M)}$ |     | 53  |     | mA   | All Input with 100Mbps square wave, $C_L=15pF$                    |
|                | NSIP9842       |     |     |     |      |   |
|                | $I_{DD(Q0)}$   |     | 32  |     | mA   | All Input 0V for NSIP9842W0 or All Input at supply for NSIP9842W1 |
|                | $I_{DD(Q1)}$   |     | 36  |     | mA   | All Input at supply for NSIP9842W0 or All Input 0V for NSIP9842W1 |
|                | $I_{DD(1M)}$   |     | 35  |     | mA   | All Input with 1Mbps square wave, $C_L=15pF$                      |
|                | $I_{DD(10M)}$  |     | 38  |     | mA   | All Input with 10Mbps square wave, $C_L=15pF$                     |
|                | $I_{DD(100M)}$ |     | 56  |     | mA   | All Input with 100Mbps square wave, $C_L=15pF$                    |
|                | NSIP9843       |     |     |     |      |   |
|                | $I_{DD(Q0)}$   |     | 32  |     | mA   | All Input 0V for NSIP9843W0 or All Input at supply for NSIP9843W1 |

| Parameters                    | Symbol         | Min | Typ | Max | Unit | Comments  |  |
|-------------------------------|----------------|-----|-----|-----|------|---|--|
| Supply Current                | $I_{DD(Q1)}$   |     | 36  |     | mA   | All Input at supply for NSIP9843W0 or All Input 0V for NSIP9843W1 |  |
|                               | $I_{DD(1M)}$   |     | 35  |     | mA   | All Input with 1Mbps square wave, $C_L=15pF$                      |  |
|                               | $I_{DD(10M)}$  |     | 40  |     | mA   | All Input with 10Mbps square wave, $C_L=15pF$                     |  |
|                               | $I_{DD(100M)}$ |     | 59  |     | mA   | All Input with 100Mbps square wave, $C_L=15pF$                    |  |
|                               | NSIP9844       |     |     |     |      |   |  |
|                               | $I_{DD(Q0)}$   |     | 32  |     | mA   | All Input 0V for NSIP9844W0 or All Input at supply for NSIP9844W1 |  |
|                               | $I_{DD(Q1)}$   |     | 36  |     | mA   | All Input at supply for NSIP9844W0 or All Input 0V for NSIP9844W1 |  |
|                               | $I_{DD(1M)}$   |     | 35  |     | mA   | All Input with 1Mbps square wave, $C_L=15pF$                      |  |
|                               | $I_{DD(10M)}$  |     | 42  |     | mA   | All Input with 10Mbps square wave, $C_L=15pF$                     |  |
|                               | $I_{DD(100M)}$ |     | 62  |     | mA   | All Input with 100Mbps square wave, $C_L=15pF$                    |  |
| Data Rate                     | DR             | 0   |     | 150 | Mbps |   |  |
| Minimum Pulse Width           | PW             |     |     | 5   | ns   |   |  |
| Propagation Delay             | $t_{PLH}$      |     | 10  | 25  | ns   |   |  |
|                               | $t_{PHL}$      |     | 10  | 25  | ns   |   |  |
| Pulse Width Distortion        | PWD            |     |     | 5   | ns   | $ t_{PHL} - t_{PLH} $   |  |
| Rising Time                   | $t_r$          |     |     | 5   | ns   | $C_L = 15pF$  |  |
| Falling Time                  | $t_f$          |     |     | 5   | ns   | $C_L = 15pF$  |  |
| Channel-to-Channel Delay Skew | $t_{SK(c2c)}$  |     |     | 2.5 | ns   |   |  |
| Part-to-Part Delay Skew       | $t_{SK(p2p)}$  |     |     | 5   | ns   |   |  |

( $V_{DD}=3V\sim 3.6V$ ,  $V_{DDL}=1.8V\sim 5.5V$ ,  $SEL=0V$ ,  $T_a=-40^{\circ}C$  to  $125^{\circ}C$ . Unless otherwise noted, Typical values are at  $V_{DD} = V_{DDL} = 3.3V$ ,  $T_a = 25^{\circ}C$ )

| Parameters     | Symbol         | Min | Typ | Max | Unit | Comments  |
|----------------|----------------|-----|-----|-----|------|---|
| Supply current | NSIP9840       |     |     |     |      |   |
|                | $I_{DD(Q0)}$   |     | 35  |     | mA   | All Input 0V for NSIP9840W0 or All Input at supply for NSIP9840W1 |
|                | $I_{DD(Q1)}$   |     | 40  |     | mA   | All Input at supply for NSIP9840W0 or All Input 0V for NSIP9840W1 |
|                | $I_{DD(1M)}$   |     | 38  |     | mA   | All Input with 1Mbps square wave, $C_L=15pF$                      |
|                | $I_{DD(10M)}$  |     | 40  |     | mA   | All Input with 10Mbps square wave, $C_L=15pF$                     |
|                | $I_{DD(100M)}$ |     | 55  |     | mA   | All Input with 100Mbps square wave, $C_L=15pF$                    |
|                | NSIP9841       |     |     |     |      |   |
|                | $I_{DD(Q0)}$   |     | 36  |     | mA   | All Input 0V for NSIP9841W0 or All Input at supply for NSIP9841W1 |
|                | $I_{DD(Q1)}$   |     | 41  |     | mA   | All Input at supply for NSIP9841W0 or All Input 0V for NSIP9841W1 |
|                | $I_{DD(1M)}$   |     | 39  |     | mA   | All Input with 1Mbps square wave, $C_L=15pF$                      |
|                | $I_{DD(10M)}$  |     | 41  |     | mA   | All Input with 10Mbps square wave, $C_L=15pF$                     |
|                | $I_{DD(100M)}$ |     | 59  |     | mA   | All Input with 100Mbps square wave, $C_L=15pF$                    |
|                | NSIP9842       |     |     |     |      |   |
|                | $I_{DD(Q0)}$   |     | 37  |     | mA   | All Input 0V for NSIP9842W0 or All Input at supply for NSIP9842W1 |
|                | $I_{DD(Q1)}$   |     | 42  |     | mA   | All Input at supply for NSIP9842W0 or All Input 0V for NSIP9842W1 |
|                | $I_{DD(1M)}$   |     | 40  |     | mA   | All Input with 1Mbps square wave, $C_L=15pF$                      |
|                | $I_{DD(10M)}$  |     | 42  |     | mA   | All Input with 10Mbps square wave, $C_L=15pF$                     |
|                | $I_{DD(100M)}$ |     | 63  |     | mA   | All Input with 100Mbps square wave, $C_L=15pF$                    |
|                | NSIP9843       |     |     |     |      |   |
|                | $I_{DD(Q0)}$   |     | 38  |     | mA   | All Input 0V for NSIP9843W0 or All Input at supply for NSIP9843W1 |

| Parameters                    | Symbol         | Min | Typ | Max | Unit | Comments  |  |
|-------------------------------|----------------|-----|-----|-----|------|---|--|
| Supply Current                | $I_{DD(Q1)}$   |     | 43  |     | mA   | All Input at supply for NSIP9843W0 or All Input 0V for NSIP9843W1 |  |
|                               | $I_{DD(1M)}$   |     | 41  |     | mA   | All Input with 1Mbps square wave, $C_L=15pF$                      |  |
|                               | $I_{DD(10M)}$  |     | 43  |     | mA   | All Input with 10Mbps square wave, $C_L=15pF$                     |  |
|                               | $I_{DD(100M)}$ |     | 67  |     | mA   | All Input with 100Mbps square wave, $C_L=15pF$                    |  |
|                               | NSIP9844       |     |     |     |      |   |  |
|                               | $I_{DD(Q0)}$   |     | 39  |     | mA   | All Input 0V for NSIP9844W0 or All Input at supply for NSIP9844W1 |  |
|                               | $I_{DD(Q1)}$   |     | 44  |     | mA   | All Input at supply for NSIP9844W0 or All Input 0V for NSIP9844W1 |  |
|                               | $I_{DD(1M)}$   |     | 42  |     | mA   | All Input with 1Mbps square wave, $C_L=15pF$                      |  |
|                               | $I_{DD(10M)}$  |     | 44  |     | mA   | All Input with 10Mbps square wave, $C_L=15pF$                     |  |
|                               | $I_{DD(100M)}$ |     | 71  |     | mA   | All Input with 100Mbps square wave, $C_L=15pF$                    |  |
| Data Rate                     | DR             | 0   |     | 150 | Mbps |   |  |
| Minimum Pulse Width           | PW             |     |     | 5   | ns   |   |  |
| Propagation Delay             | $t_{PLH}$      |     | 10  | 25  | ns   |   |  |
|                               | $t_{PHL}$      |     | 10  | 25  | ns   |   |  |
| Pulse Width Distortion        | PWD            |     |     | 5   | ns   | $ t_{PHL} - t_{PLH} $   |  |
| Rising Time                   | $t_r$          |     |     | 5   | ns   | $C_L = 15pF$  |  |
| Falling Time                  | $t_f$          |     |     | 5   | ns   | $C_L = 15pF$  |  |
| Channel-to-Channel Delay Skew | $t_{SK(c2c)}$  |     |     | 2.5 | ns   |   |  |
| Part-to-Part Delay Skew       | $t_{SK(p2p)}$  |     |     | 5   | ns   |   |  |

### 6.3. Typical Performance Characteristics

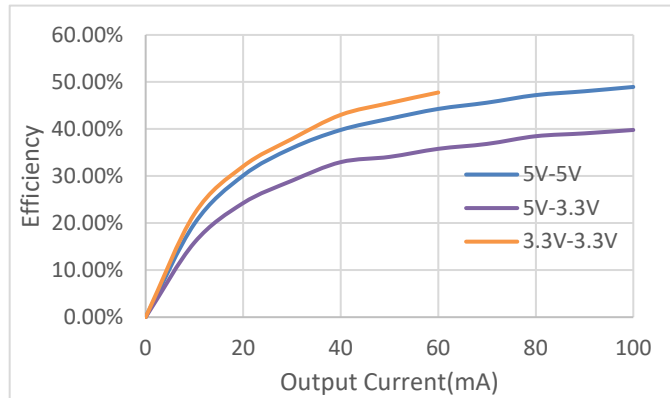


Figure 6.1 Output Current vs Efficiency

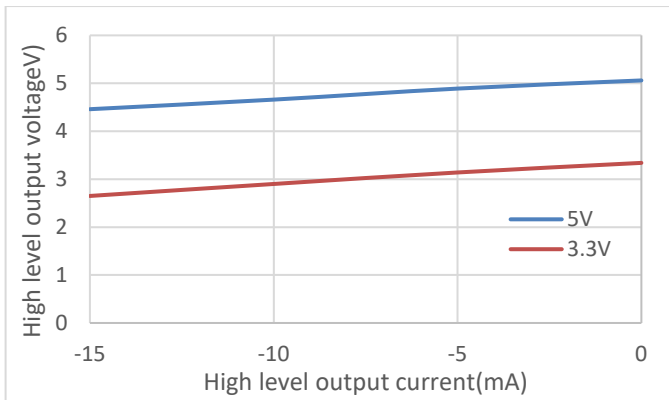


Figure 6.2 High-level Output Voltage vs Output Current

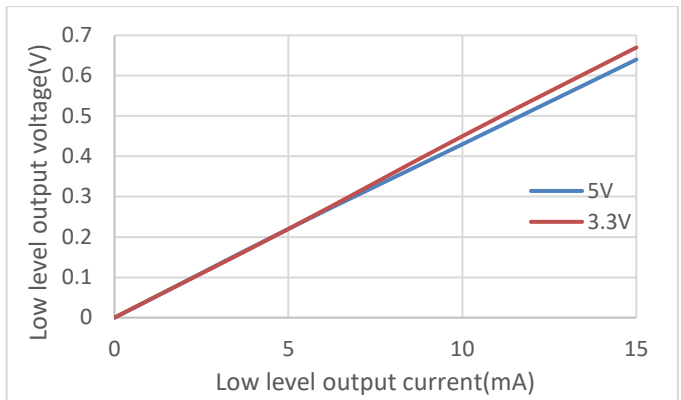


Figure 6.3 Low-level Output Voltage vs Output Current

### 6.4. Parameter Measurement Information

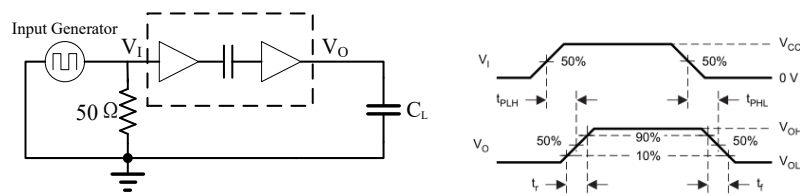


Figure 6.4 Switching Characteristics Test Circuit and Waveform

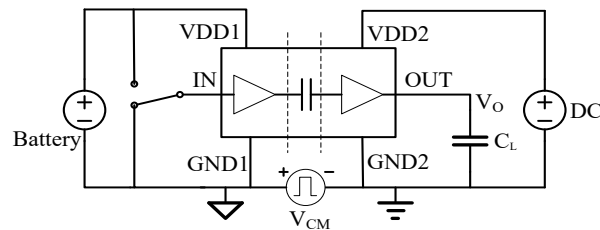


Figure 6.5 Common-Mode Transient Immunity Test Circuit

## 7. High Voltage Feature Description

### 7.1. Insulation and Safety Related Specifications

| <i>Parameters</i>                                | <i>Symbol</i> | <i>Value</i> | <i>Unit</i> | <i>Comments</i>   |
|--|---------------|--------------|-------------|---|
| Minimum External Air Gap (Clearance)             | CLR           | 8.15         | mm          | Shortest terminal-to-terminal distance through air                |
| Minimum External Tracking (Creepage)             | CPG           | 8.15         | mm          | Shortest terminal-to-terminal distance across the package surface |
| Distance Through Insulation                      | DTI           | 26           | µm          | Distance through insulation                                       |
| Tracking Resistance (Comparative Tracking Index) | CTI           | >600         | V           | DIN EN 60112 (VDE 0303-11); IEC 60112                             |
| Material Group                                   |               | I            |             | IEC 60664-1   |

| <i>Description</i>                  | <i>Test Condition</i>                  | <i>Value</i> |
|-------------------------------------|--|--------------|
| Overvoltage Category per IEC60664-1 | For Rated Mains Voltage $\leq$ 150Vrms | I to IV      |
|                                     | For Rated Mains Voltage $\leq$ 300Vrms | I to IV      |
|                                     | For Rated Mains Voltage $\leq$ 600Vrms | I to III     |
| Climatic Classification             |  | 40/125/21    |
| Pollution Degree per DIN VDE 0110,  |  | 2            |

## 7.2. Insulation Characteristics

| Description                             | Test Condition  | Symbo<br>l | Value      | Unit       |
|---|---|------------|------------|------------|
| Maximum repetitive isolation voltage    |   | $V_{IORM}$ | 1500       | $V_{PEAK}$ |
| Maximum working isolation voltage       | AC Voltage  | $V_{IOWM}$ | 1061       | $V_{RMS}$  |
|   | DC Voltage  |            | 1500       | $V_{DC}$   |
| Apparent Charge                         | Method a, after Input/output safety test subgroup 2/3,<br>$V_{ini}=V_{IOTM}$ , $t_{ini} = 60s$ ,<br>$V_{pd(m)}=1.2*V_{IORM}$ , $t_m=10s$ .  | $q_{pd}$   | <5         | pC         |
|   | Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$ ,<br>$t_{ini}=60s$ , $V_{pd(m)}=1.6*V_{IORM}$ ,<br>$t_m=10s$   |            |            | pC         |
|   | Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}$ , $t_{ini}=1s$<br>$V_{pd(m)}=1.875*V_{IORM}$ , $t_m=1s$<br>(method b1) or<br>$V_{pd(m)}=V_{ini}$ , $t_m=t_{ini}$ (method b2) |            |            | pC         |
| Maximum transient isolation voltage     | $t = 60s$   | $V_{IOTM}$ | 7070       | $V_{PEAK}$ |
| Maximum impulse voltage                 | Tested in air, 1.2/50- $\mu s$ waveform per IEC62368-1  | $V_{IMP}$  | 7600       | $V_{PEAK}$ |
| Maximum Surge Isolation Voltage         | Test method per IEC62368-1, 1.2/50 $\mu s$ waveform,<br>$V_{IOSM} \geq V_{IMP} \times 1.3$  | $V_{IOSM}$ | 10000      | $V_{PEAK}$ |
| Isolation resistance                    | $V_{IO} = 500V$ , $T_{amb}=25^{\circ}C$   | $R_{IO}$   | $>10^{12}$ | $\Omega$   |
|   | $V_{IO} = 500V$ , $100^{\circ}C \leq T_{amb} \leq 125^{\circ}C$   | $R_{IO}$   | $>10^{11}$ | $\Omega$   |
|   | $V_{IO} = 500V$ , $T_{amb}=T_s$   | $R_{IO}$   | $>10^9$    | $\Omega$   |
| Isolation capacitance                   | $f = 1MHz$  | $C_{IO}$   | $\sim 4$   | pF         |
| Safety total power dissipation          | $\theta_{JA} = 59.2^{\circ}C/W$ , $V_I = 5.25V$ , $T_J = 150^{\circ}C$ , $T_A = 25^{\circ}C$  | $P_s$      | 2111       | mW         |
| Safety input, output, or supply current | $\theta_{JA} = 59.2^{\circ}C/W$ , $V_I = 5.25V$ ,<br>$T_J = 150^{\circ}C$ , $T_A = 25^{\circ}C$   | $I_s$      | 402        | mA         |

| Description                | Test Condition  | Symbo<br>/       | Value | Unit             |
|----------------------------|---|------------------|-------|------------------|
| Maximum safety temperature |   | Ts               | 150   | °C               |
| <b>UL1577</b>              |   |                  |       |                  |
| Insulation voltage per UL  | V <sub>TEST</sub> = V <sub>ISO</sub> , t = 60s<br>(qualification),<br>V <sub>TEST</sub> = 1.2 × V <sub>ISO</sub> , t = 1s<br>(100% production test) | V <sub>ISO</sub> | 5000  | V <sub>RMS</sub> |

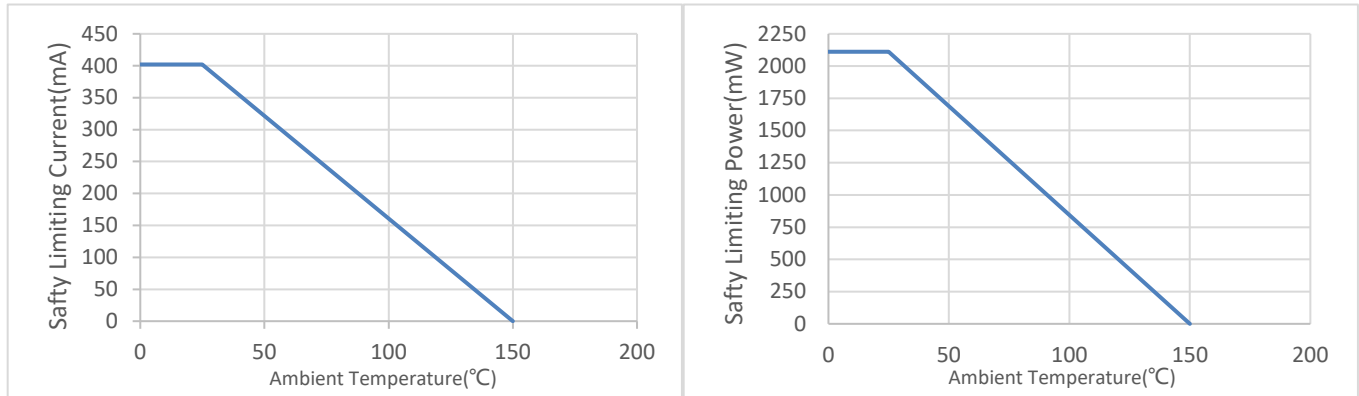


Figure 7.1 NSIP984x Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17

### 7.3. Regulatory Information

The NSIP984xWx-Q1SWR are certified with UL1577, VDE0884-17, GB4943.1, EN IEC 62368-1.

| UL1577 & CSA Component Acceptance<br>Notice 5A                  |   | DIN EN IEC 60747-17<br>(VDE 0884-17)  | EN IEC62368-1     | GB4943.1                              |
|---|---|---|-------------------|---------------------------------------|
| Single Protection,<br>5000V <sub>rms</sub> Isolation<br>voltage | Single Protection,<br>5000V <sub>rms</sub> Isolation<br>voltage | Reinforced Insulation<br>V <sub>IORM</sub> =1500Vpeak<br>V <sub>IOTM</sub> =7070Vpeak | 5000Vrms for 1min | Certified according<br>to<br>GB4943.1 |
| Certified by UL   |   | Certified by TUV  |                   | Certified by CQC                      |
| File (Pending)  | File (Pending)  | File (Pending)  | File (Pending)    | File (Pending)                        |

## 8. Function Description

### 8.1. Overview

The NSIP984x devices are quad-channel digital isolators with integrated isolated DC-DC converter. The digital isolators are based on Novosense capacity isolation barrier technique. The isolated DC-DC converter provides up to 500mW output power using on chip transformer. The feedback PWM signal is sent to primary side by a digital isolator based on capacity isolation technology. The NSIP984x devices are safety certified by UL1577, supporting 5kVrms insulation withstand voltage, while providing high electromagnetic immunity and low emissions. The data rate of the NSIP984x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 100kV/μs.

The high integrated solution can help to simplify system design and improve reliability. The NSIP984x devices are suitable for the limited PCB space applications. The devices are also suitable for wide temperature application which the most the power module can not support.

### 8.2. Device Functional Modes

The NSIP984x devices provide 5V to 5V, 5V to 3.3V, 3.3V to 3.3V conversion mode, the output voltage can be set by SEL pin. Supply configuration table showed below.

| <i>SEL PIN</i>              | <i>VDD</i> | <i>VISO</i> |
|-----------------------------|------------|-------------|
| Shorted to VISO             | 5V         | 5V          |
| Shorted to GND2 or floating | 5V         | 3.3V        |
| Shorted to GND2 or floating | 3.3V       | 3.3V        |

The NSIP984x devices provide four channel digital isolators. The digital isolators have default weak pull up or pull down input status when input is floating as shown in below table.

| <i>Input</i> | <i>VDD1 status</i> | <i>VDDOUT status</i> | <i>Output</i>                  | <i>Comment</i>        |
|--------------|--------------------|----------------------|--------------------------------|-----------------------|
| H            | Ready              | Ready                | H                              | Normal operation.     |
| L            | Ready              | Ready                | L                              |                       |
| floating     | Ready              | Ready                | L(NSIP984xW0)<br>H(NSIP984xW1) | Floating input status |

### 8.3. Output Short and Over Temperature Protection

The NSIP984x devices are protected against output short. When the devices detect the output is short, the device will be in Hiccup mode and the transfer power will be limited. So, the temperature of the device will be low, and the device is protected.

The NSIP984x devices are also protected against over temperature. When the devices detect the chip is over 165°C, the device will be shut down until the temperature of the device is below 145°C.

## 9. Application Note

### 9.1. Typical Application

The NSIP984x requires 0.1  $\mu\text{F}$  and 10 $\mu\text{F}$  bypass capacitors between VDD and GND1, VISO and GND2. The capacitors should be placed as close as possible to the package. This is very important for the performance of the device.

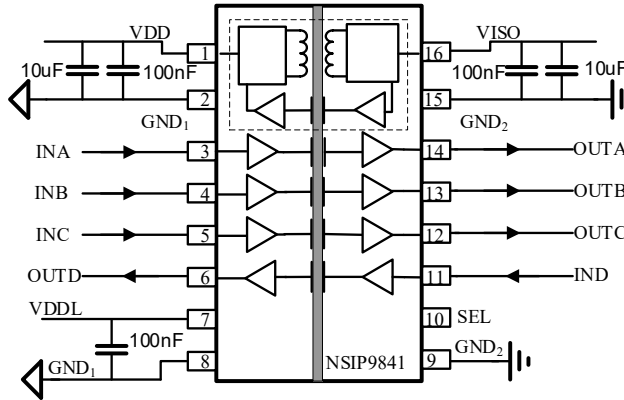


Figure 9.1 Basic schematic of NSIP984x

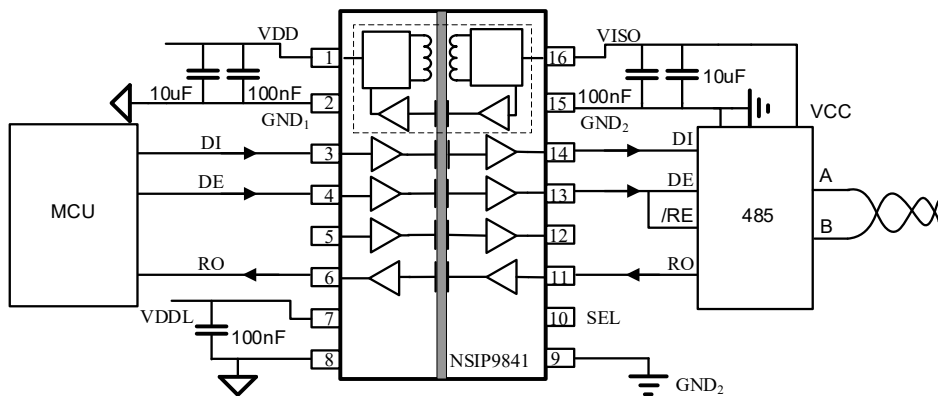


Figure 9.2 Half-Duplex RS-485 schematic using NSIP984x

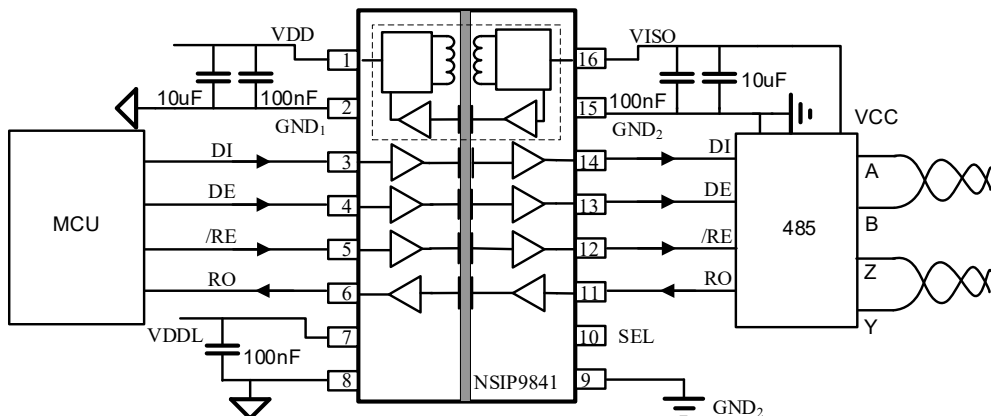


Figure 9.3 full-Duplex RS-485 schematic using NSIP984x

### 9.2. PCB Layout

The recommended PCB layout shown below. The low ESR capacitor C1 should be closed to PIN1 and PIN2, the distance should be less than 1mm. The low ESR capacitor C3 should be closed to PIN15 and PIN16, the distance should be less than 1mm. It is recommended that C1=C3=100nF and C2=C4=10μF.

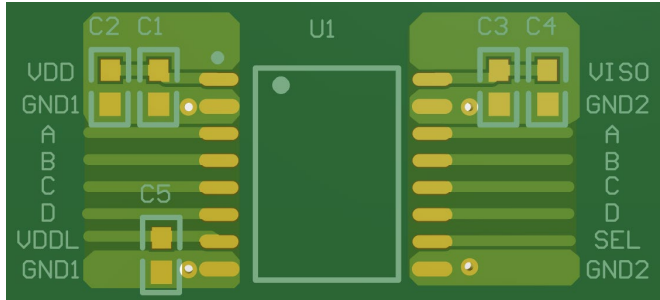


Figure 9.4 SOW16 Recommended PCB Layout — Top Layer

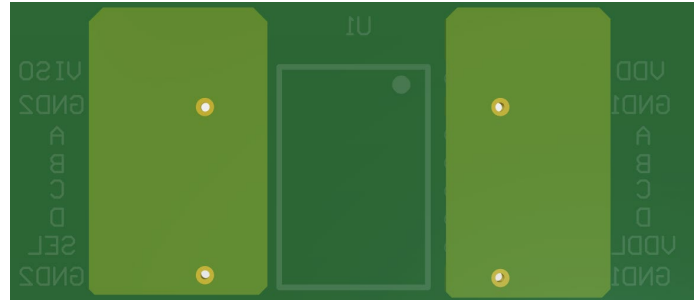


Figure 9.5 SOW16 Recommended PCB Layout — Bottom Layer

### 10. Package Information

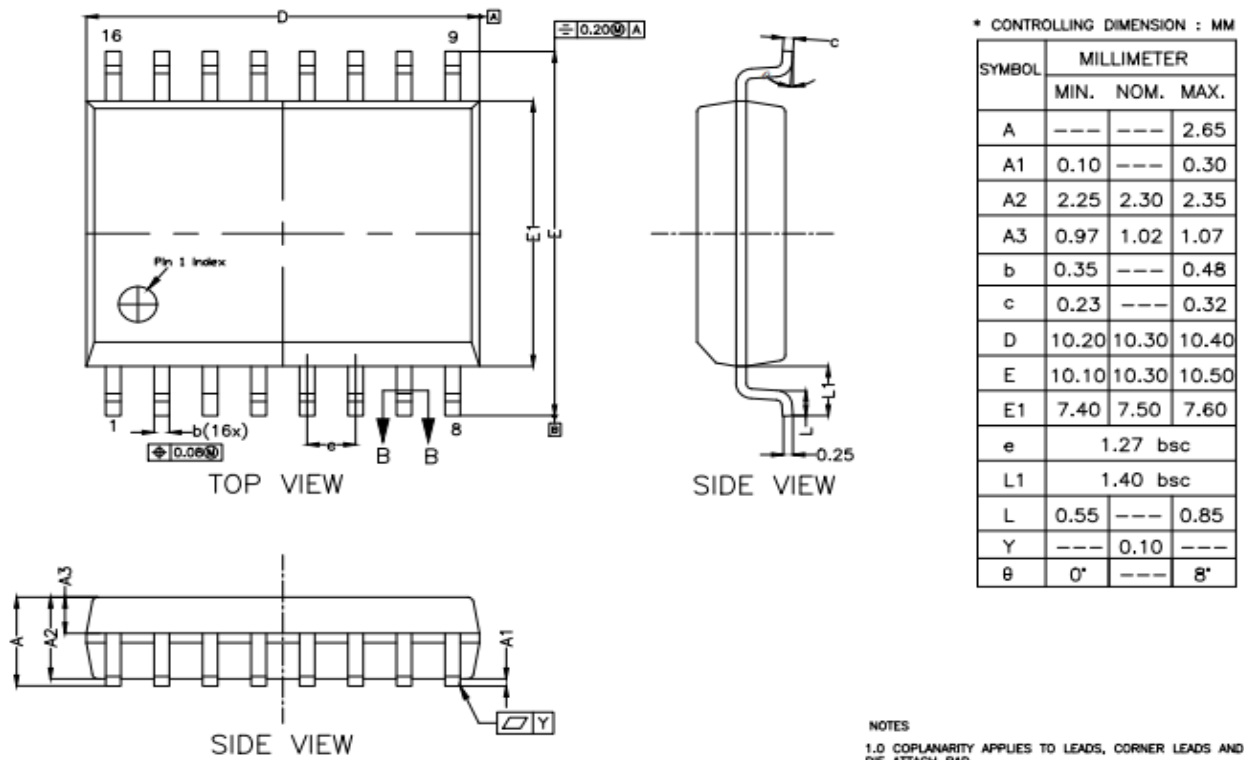
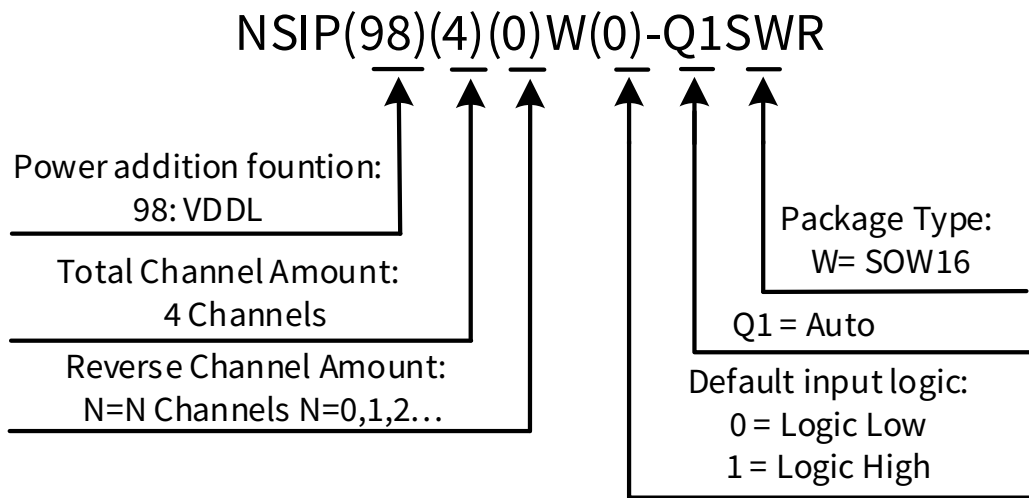


Figure 10.1 SOW16 Package Shape and Dimension in millimeters

## 11. Order Information

| Part Number      | Isolation Rating (kV) | Number of side 1 inputs | Number of side 2 inputs | Max Data Rate (Mbps) | Default input logic | Temperature  | MSL | Package Type   | Package Drawing | SPQ  |
|------------------|-----------------------|-------------------------|-------------------------|----------------------|---------------------|--------------|-----|----------------|-----------------|------|
| NSIP9840W0-Q1SWR | 5                     | 4                       | 0                       | 150                  | Low                 | -40 to 125°C | 3   | SOP16 (300mil) | SOW16           | 1500 |
| NSIP9840W1-Q1SWR | 5                     | 4                       | 0                       | 150                  | High                | -40 to 125°C | 3   | SOP16 (300mil) | SOW16           | 1500 |
| NSIP9841W0-Q1SWR | 5                     | 3                       | 1                       | 150                  | Low                 | -40 to 125°C | 3   | SOP16 (300mil) | SOW16           | 1500 |
| NSIP9841W1-Q1SWR | 5                     | 3                       | 1                       | 150                  | High                | -40 to 125°C | 3   | SOP16 (300mil) | SOW16           | 1500 |
| NSIP9842W0-Q1SWR | 5                     | 2                       | 2                       | 150                  | Low                 | -40 to 125°C | 3   | SOP16 (300mil) | SOW16           | 1500 |
| NSIP9842W1-Q1SWR | 5                     | 2                       | 2                       | 150                  | High                | -40 to 125°C | 3   | SOP16 (300mil) | SOW16           | 1500 |
| NSIP9843W0-Q1SWR | 5                     | 1                       | 3                       | 150                  | Low                 | -40 to 125°C | 3   | SOP16 (300mil) | SOW16           | 1500 |
| NSIP9843W1-Q1SWR | 5                     | 1                       | 3                       | 150                  | High                | -40 to 125°C | 3   | SOP16 (300mil) | SOW16           | 1500 |
| NSIP9844W0-Q1SWR | 5                     | 0                       | 4                       | 150                  | Low                 | -40 to 125°C | 3   | SOP16 (300mil) | SOW16           | 1500 |
| NSIP9844W1-Q1SWR | 5                     | 0                       | 4                       | 150                  | High                | -40 to 125°C | 3   | SOP16 (300mil) | SOW16           | 1500 |

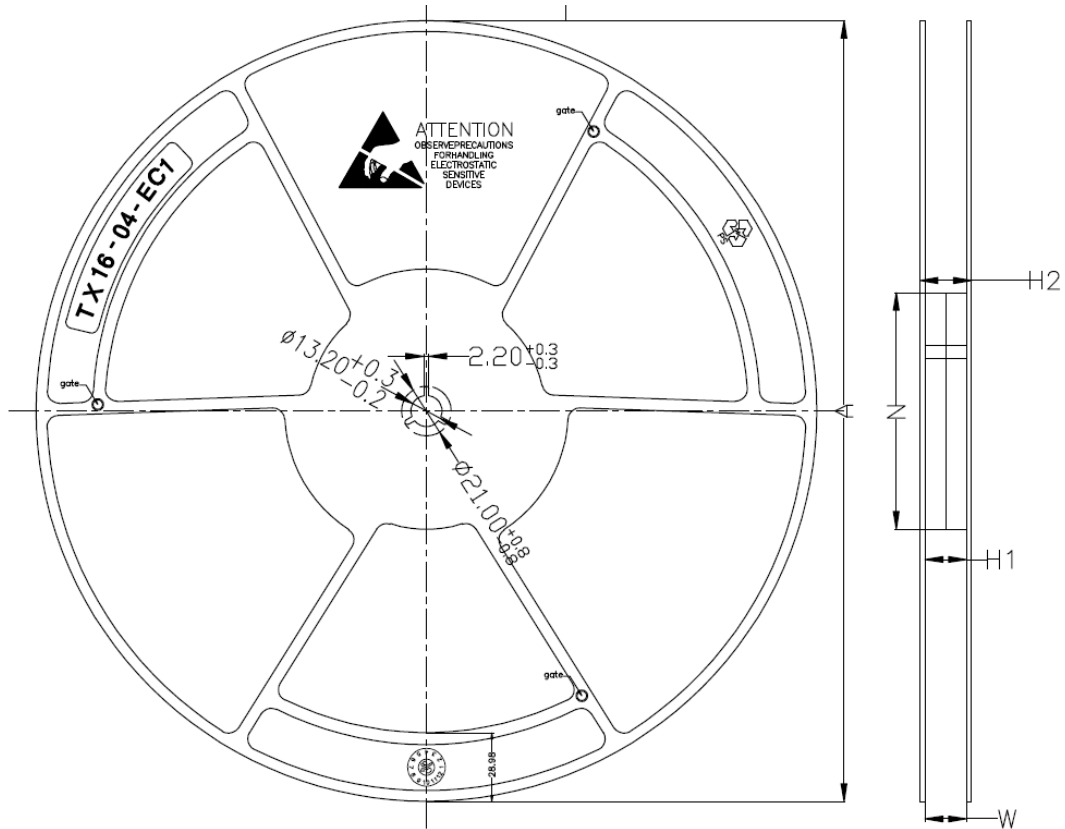
**Part Number Rule:**



## 12. Documentation Support

| Part Number | Product Folder             | Datasheet                  | Technical Documents        | Isolator selection guide   |
|-------------|----------------------------|----------------------------|----------------------------|----------------------------|
| NSIP984x    | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

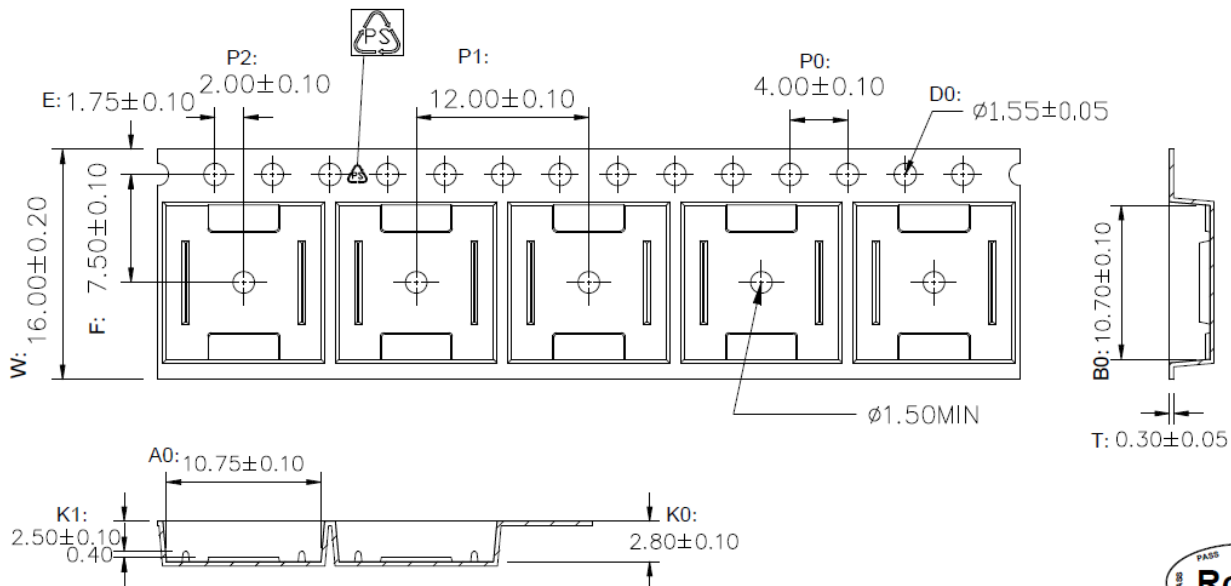
### 13. Tape And Reel Information



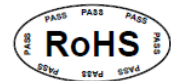
| PRODUCT SPECIFICATIONS |   |   |   |   |  |
|------------------------|---|---|---|---|--|
| TAPE WIDTH             | $\phi A \begin{smallmatrix} +2 \\ -2 \end{smallmatrix}$ | $\phi N \begin{smallmatrix} +2 \\ -2 \end{smallmatrix}$ | $H1 \begin{smallmatrix} +2 \\ -0 \end{smallmatrix}$ | $H2 \begin{smallmatrix} +1 \\ -1 \end{smallmatrix}$ | $W \begin{smallmatrix} +3.5 \\ -0.2 \end{smallmatrix}$ |
| 16MM                   | 330   | 100   | 16.4  | 20.6  | 16.4   |

- NOTES:**
1. MATERIAL: DISSIPATIVE (BLACK)
  2. FLANGE WARPAGE: 3 MM MAXIMUM
  3. ALL DIMENSIONS ARE IN MM
  4. ESD - SURFACE RESISTIVITY: 10 TO 10<sup>10</sup> OHMS/SQ
  5. GENERAL TOLERANCE: ±0.25 MM

Figure 13.1 Tape Information of SOW16



1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.20$  .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy .
4. All dimensions meet EIA-481 requirements.
5. Thickness :  $0.30 \pm 0.05$ mm.
6. Packing length per 22" reel : 378 Meters.(復巻 N=122)
7. Component load per 13" reel : 1000 pcs.
8. Surface resistivity :  $10^5 \sim 10^{10} \Omega/\square$



|    |            |
|----|------------|
| W  | 16.00±0.20 |
| A0 | 10.75±0.10 |
| B0 | 10.70±0.10 |
| K0 | 2.80±0.10  |
| K1 | 2.50±0.10  |

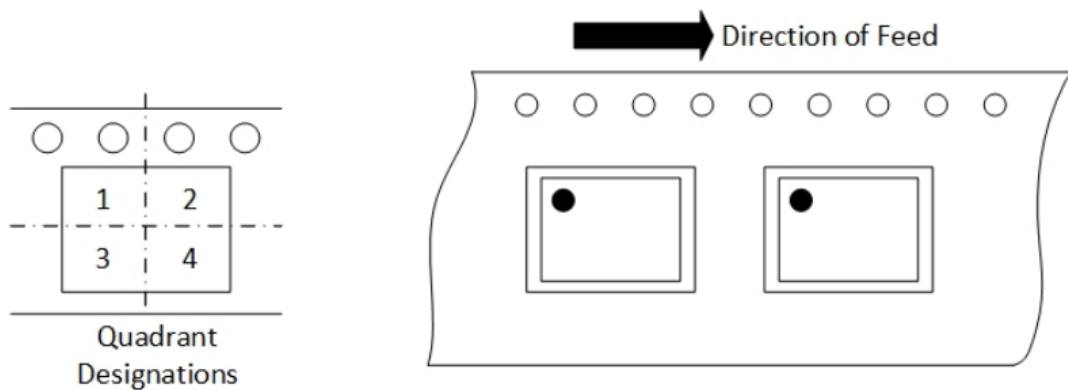


Figure 13.2 Reel Information of SOW16

## 14. Revision History

| Revision | Description     | Date       |
|----------|-----------------|------------|
| 1.0      | Initial version | 2025/10/21 |

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