NSIP9042

Signal Isolated CAN Transceiver With Integrated DC to DC Converter

Datasheet (EN) 1.0

Product Overview

NSIP9042 is a high reliability isolated controller area network (CAN) physical layer transceiver with integrated DC to DC converter. The isolated DC-DC converter provides output power using on-chip transformer. The feedback PWM signal is sent to primary side by a digital isolator based on Novosense capacitive isolation technology. Both devices are safety certified by UL1577, supporting 5kVrms insulation withstand voltage, while the high integrated solution can help to simplify system design and improve reliability.

The Bus pins of NSIP9042 are protected from ±8kV system level ESD to GND2 on Bus side. The data rate of the NSIP9042 is up to 5Mbps. The NSIP9042 provides thermal protection and transmit data dominant time out function.

Key Features

- Up to 5000Vrms Insulation voltage
- ISO power: integrated isolated DC-DC converter
- Power supply voltage:
  - VDD:4.5V to 5.25V
  - VDDL:1.8V to 5.5V
- Over current and over temperature protection
- High CMTI: ±150kV/µs
- Data rate: 5Mbps
- High system level EMC performance
- Operation temperature: -40℃~125℃
- RoHS-compliant packages: SOW20 SOW16

Safety Regulatory Approvals

- UL recognition: up to 5000V_{RMS} for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN VDE V 0884-17

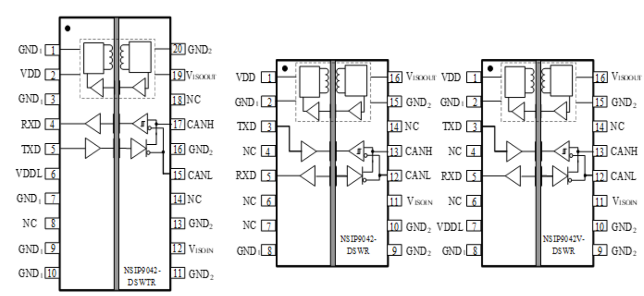
Applications

- Industrial automation system
- Smart electric meter and water meter
- Security and protection monitoring

Device Information

Part Number	Package	Body Size
NSIP9042-DSWTR	SOW20	12.80mm × 7.50mm
NSIP9042-DSWR	SOW16	10.30mm × 7.50mm
NSIP9042V-DSWR	SOW16	10.30mm × 7.50mm

Functional Block Diagrams



NSIP9042-DSWTR NSIP9042-DSWR NSIP9042V-DSWR

Figure 1. NSIP9042 Block Diagrams

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1. Pin Configuration and Functions

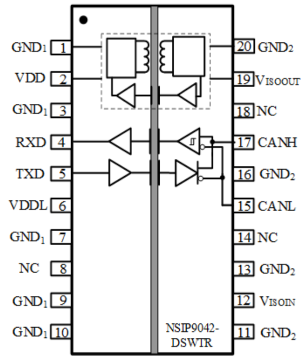


Figure 1.1 NSIP9042-DSWTR Package

Table1.1 NSIP9042-DSWTR Pin Configuration and Description

NSIP9042 PIN NO.	SYMBOL	FUNCTION
1	GND_1	Ground 1, the ground reference for Isolator Side 1
2	V_{DD}	Power Supply for Isolator Side 1
3	GND_1	Ground 1, the ground reference for Isolator Side 1
4	RXD	Receiver output
5	TXD	Driver transmit data input
6	V_{DDL}	Side1 I/O logic level.
7	GND_1	Ground 1, the ground reference for Isolator Side 1
8	NC	Not connected
9	GND_1	Ground 1, the ground reference for Isolator Side 1
10	GND_1	Ground 1, the ground reference for Isolator Side 1
11	GND_2	Ground 2, the ground reference for Isolator Side 2
12	V_{ISOIN}	Isolated power supply input. This pin must be connected externally to V_{ISOOUT}. It is recommended this pin have a 0.1μF capacitor to GND_2. Connect this pin through a ferrite bead and short trace length to V_{ISOOUT} for operation.
13	GND_2	Ground 2, the ground reference for Isolator Side 2
14	NC	Not connected
15	CANL	Low-level CAN bus line, when VDD is powered down, Pin CANL is put into a high impedance state to avoid overloading the bus
16	GND_2	Ground 2, the ground reference for Isolator Side 2
17	CANH	High-level CAN bus line, when VDD is powered down, Pin CANH is put into a high impedance state to avoid overloading the bus
18	NC	Not connected

19	V_{ISOOUT}	Isolated Power Supply Output. This pin must be connected externally to V_{ISOIN}. It is recommended this pin have a 0.1μF and 10uF capacitor to GND_2. Connect this pin through a ferrite bead and short trace length to V_{ISOIN} for operation.
20	GND_2	Ground 2, the ground reference for Isolator Side 2

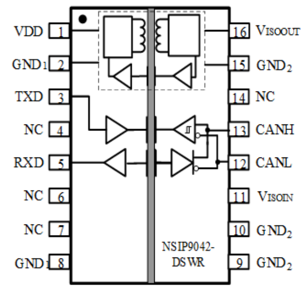


Figure 1.2 NSIP9042-DSWR Package

Table1.2 NSIP9042-DSWR Pin Configuration and Description

NSIP9042 PIN NO.	***SYMBOL***	***FUNCTION***
1	V_{DD}	Power Supply for Isolator Side 1
2	GND_1	Ground 1, the ground reference for Isolator Side 1
3	TXD	Driver transmit data input
4	NC	Not connected
5	RXD	Receiver output
6	NC	Not connected
7	NC	Not connected
8	GND_1	Ground 1, the ground reference for Isolator Side 1
9	GND_2	Ground 2, the ground reference for Isolator Side 2
10	GND_2	Ground 2, the ground reference for Isolator Side 2
11	V_{ISOIN}	Isolated power supply input. This pin must be connected externally to V_{ISOOUT}. It is recommended this pin have a 0.1μF capacitor to GND_2. Connect this pin through a ferrite bead and short trace length to V_{ISOOUT} for operation.
12	CANL	Low-level CAN bus line, when VDD is powered down, Pin CANL is put into a high impedance state to avoid overloading the bus
13	CANH	High-level CAN bus line, when VDD is powered down, Pin CANH is put into a high impedance state to avoid overloading the bus
14	NC	Not connected
15	GND_2	Ground 2, the ground reference for Isolator Side 2
16	V_{ISOOUT}	Isolated Power Supply Output. This pin must be connected externally to V_{ISOIN}. It is recommended this pin have a 0.1μF and 10uF capacitor to GND_2. Connect this pin through a ferrite bead and short trace length to V_{ISOIN} for operation.

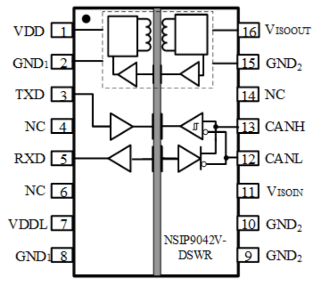


Figure 1.3 NSIP9042V-DSWR Package

Table1.3 NSIP9042V-DSWR Pin Configuration and Description

NSIP9042 PIN NO.	SYMBOL	FUNCTION
1	V_{DD}	Power Supply for Isolator Side 1
2	GND_1	Ground 1, the ground reference for Isolator Side 1
3	TXD	Driver transmit data input
4	NC	Not connected
5	RXD	Receiver output
6	NC	Not connected
7	V_{DDL}	Side1 I/O logic level.
8	GND_1	Ground 1, the ground reference for Isolator Side 1
9	GND_2	Ground 2, the ground reference for Isolator Side 2
10	GND_2	Ground 2, the ground reference for Isolator Side 2
11	V_{ISOIN}	Isolated power supply input. This pin must be connected externally to V_{ISOOUT}. It is recommended this pin have a 0.1μF capacitor to GND_2. Connect this pin through a ferrite bead and short trace length to V_{ISOOUT} for operation.
12	CANL	Low-level CAN bus line, when VDD is powered down, Pin CANL is put into a high impedance state to avoid overloading the bus
13	CANH	High-level CAN bus line, when VDD is powered down, Pin CANH is put into a high impedance state to avoid overloading the bus
14	NC	Not connected
15	GND_2	Ground 2, the ground reference for Isolator Side 2
16	V_{ISOOUT}	Isolated Power Supply Output. This pin must be connected externally to V_{ISOIN}. It is recommended this pin have a 0.1μF and 10uF capacitor to GND_2. Connect this pin through a ferrite bead and short trace length to V_{ISOIN} for operation.

2. Absolute Maximum Ratings[1]

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage[2]	V_{DD}	-0.5		6	V	
Side1 I/O logic level[2]	V_{DDL}	-0.5		6	V	
Maximum Input Voltage[2]	TXD	-0.5		V_{DDL}[3]+0.5	V	
Driver Output/Receiver Input Voltage	CANH, CANL	-58		58	V	
R output current	I_O	-15		15	mA	
Junction Temperature	T_J	-40		150	°C	
Storage Temperature	T_{stg}	-40		150	°C	

[1]Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2]All voltage values are with respect to the local ground pin (GND_1 or GND_2) and are peak voltage values.

[3]The maximum voltage at the I/O pins should not exceed 6 V. For NSIP9042-DSWR, V_{DD} replaces V_{DDL}.

3. ESD Ratings

Ratings		Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD ● CANH and CANL ● Other pins	 ±6.0 ±8.0	kV
	Charged device model (CDM), per AEC-Q100-011-RevB	±2.0	kV

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	4.5		5.25	V
	V_{DDL}	1.8		5.5	V
High level output current	I_{OH} @ V_{DDL}[1] = 5V	-4			mA
	I_{OH} @ V_{DDL}[1] = 3.3V	-2			mA
Low level output current	I_{OL} @ V_{DDL}[1] = 5V			4	mA
	I_{OL} @ V_{DDL}[1] = 3.3V			2	mA
High Level Input Voltage	V_{IH}	0.7*V_{DDL}[1]		V_{DDL}[1]	V
Low Level Input Voltage	V_{IL}	0		0.3*V_{DDL}[1]	V
Data rate	DR			5	Mbps
Ambient Temperature	T_a	-40		125	℃

[1]For NSIP9042-DSWR, V_{DD} replaces V_{DDL}.

5. Thermal Information

Parameters	Symbol	SOW16	SOW20	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	59.2	55.7	°C/W
Junction-to-top characterization parameter	ψ_{JT}	8.7	8.2	°C/W
Junction-to-board characterization parameter	ψ_{JB}	23	24.5	°C/W

6. Specifications

6.1. DC Electrical Characteristics

(V_{DD}=4.5V~5.25V, V_{DDL}=1.8~5.5V, T_a=-40℃ to 125℃. Unless otherwise noted, Typical values are at V_{DD} =5V, V_{DDL} = 3.3V, T_a = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	V_{DD}	4.5		5.25	V	
	V_{DDL}	1.8		5.5	V	
V_{DD} supply current	I_{DD}		123	150	mA	V_{DD}=5V, TXD=0,R_{load}=60Ω
			46	63	mA	V_{DD}=5V, TXD=V_{DD}
V_{DDL} supply current	I_{DDL}			1	mA	
Thermal-Shutdown Threshold	T_{TS}		165		℃	
Isolated supply voltage	V_{ISOOUT}		5		V	
Common Mode Transient Immunity	CMTI	±100	±150		kV/μs	See Figure 6.3.9
Logic Side						
High level input voltage	V_{IH}	0.7*V_{DDL}[1]			V	TXD pin
Low level input voltage	V_{IL}			0.3*V_{DDL}[1]	V	TXD pin
Input Current	I_I	-20		20	μA	TXD pin
High Level Output Voltage	V_{OH}	V_{DDL}[1]-0.4			V	V_{DDL}[1] = 5V, I_{OH} ≥- 4mA
		V_{DDL}[1]-0.3			V	V_{DDL}[1] = 3.3V, I_{OH} ≥- 2mA
Low Level Output Voltage	V_{OL}			0.4	V	V_{DDL}[1] = 5V, I_{OL} ≤ 4mA
				0.3	V	V_{DDL}[1] = 3.3V, I_{OL} ≤ 2mA
Driver						
CANH output voltage (Dominant)	$V_{OH(D)}$	2.75	3.4	4.5	V	V_I=0V, R_{Load} = 50Ω to 65Ω,see Figure 6.3.1 and Figure 6.3.2
CANL output voltage (Dominant)	$V_{OL(D)}$	0.5	1.2	2.25	V	V_I=0V, R_{Load} = 50Ω to 65Ω,see Figure 6.3.1 and Figure 6.3.2
CAN bus output voltage (Recessive)	$V_{O(R)}$	2	2.5	3	V	TXD=V_{DDL}, no load,see Figure 6.3.1 and Figure 6.3.2
Differential output voltage (Dominant)	$V_{OD(D)}$	1.5		3	V	TXD=0, R_{Load} =50Ω to 65Ω, see Figure 6.3.1 and Figure 6.3.2

Parameters	Symbol	Min	Typ	Max	Unit	Comments
		1.4		3.3	V	TXD=0, R_{Load} =45Ω to 70Ω, see Figure 6.3.1 and Figure 6.3.2
Differential output voltage (Recessive)	$V_{OD(R)}$	-0.05		0.05	V	TXD=V_{DDL}, no Load, see Figure 6.3.1 and Figure 6.3.2
Common-mode output voltage	V_{OC}	1.5	2.5	3	V	see Figure 6.3.1 and Figure 6.3.2
Short- circuit output current	I_{OS}	-115	-70	115	mA	CANH=-30V to 30V, CANL open, see Figure 6.3.8
		-115	70	115	mA	CANL=-30V to 30V, CANH open, see Figure 6.3.8
Receiver						
Differential input threshold voltage, dominant to recessive	$V_{ID(R)}$	500	700	900	mV	-12V≤CANH≤12V -12V≤CANL≤12V see Figure 6.3.4
Differential input threshold voltage, recessive to dominant	$V_{ID(D)}$	500	800	900	mV	-12V≤CANH≤12V -12V≤CANL≤12V see Figure 6.3.4
Bus Differential input threshold Hysteresis	V_{HYS}		50	100	mV	-12V≤CANH≤12V -12V≤CANL≤12V $\mid V_{ID(R)} - V_{ID(D)} \mid$
Input capacitance to ground	C_I			30	pF	CANH or CANL
Differential input capacitance	C_{ID}			15	pF	
Differential input resistance	R_{ID}	50	80	100	kΩ	-2V≤CANH≤7V -2V≤CANL≤7V $R_{ID}=R_{CANH}+R_{CANL}$
Input resistance	R_{IN}	25	40	50	kΩ	-2V≤CANH≤7V -2V≤CANL≤7V
Input resistance matching	R_{Imatch}	-3		+3	%	V_{CANH} = 5V, V_{CANL} = 5V $R_{I(match)}=2*(R_{CANH}-R_{CANL})/(R_{CANH}+R_{CANL})$

[1]For NSIP9042-DSWR, V_{DD} replaces V_{DDL}.

6.2. Switching Electrical Characteristics

(V_{DD}=4.5V~5.25V, V_{DDL}=1.8~5.5V, T_a=-40℃ to 125℃. Unless otherwise noted, Typical values are at V_{DD} =5V, V_{DDL} = 3.3V, T_a = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Loop delay1	T_{Loop1}		150	255	ns	Driver input TXD to receiver output RXD, Recessive to Dominant， see Figure 6.3.6
Loop delay2	T_{Loop2}		170	255	ns	Driver input TXD to receiver output RXD, Dominant to Recessive， see Figure 6.3.6
Driver						
Propagation delay time, recessive -to- dominant output	$t_{d(TXD\text{-}bus, dom)}$		45	140	ns	See Figure 6.3.3
Propagation delay time, dominant -to- recessive output	$t_{d(TXD\text{-}bus, rec)}$		70	140	ns	See Figure 6.3.3
Differential output signal rise time	t_{rD}		26		ns	See Figure 6.3.3
Differential output signal fall time	t_{fD}		40		ns	See Figure 6.3.3
Bus dominant time-out time	t_{TXD_DTO}	800	2200	5000	μs	See Figure 6.3.7
Receiver						
Propagation delay time, high-to-low-level output	$t_{d(bus\text{-}RXD, dom)}$		95	140	ns	See Figure 6.3.5
Propagation delay time, low-to-high-level output	$t_{d(bus\text{-}RXD, rec)}$		95	140	ns	See Figure 6.3.5
RXD signal rise time	t_{rR}		3		ns	See Figure 6.3.5
RXD signal fall time	t_{rF}		3		ns	See Figure 6.3.5

6.3. Parameter Measurement Information

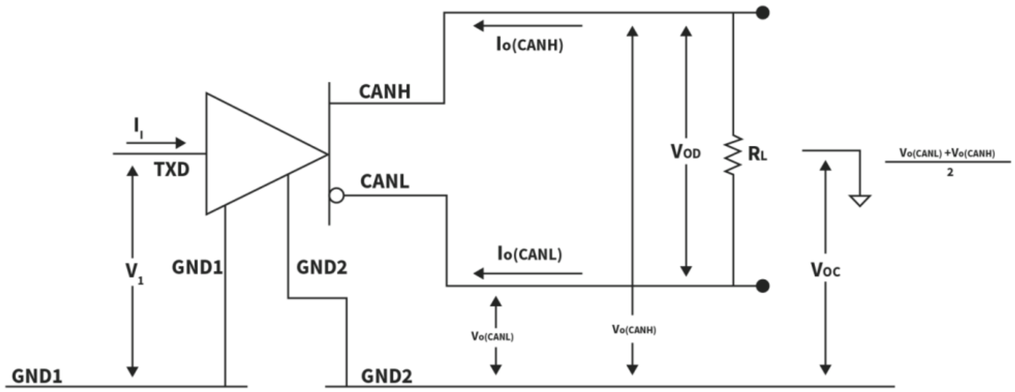


Figure 6.3.1. Driver Voltage, Current and Test Definitions

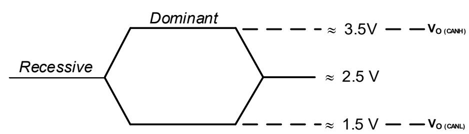


Figure 6.3.2. Bus Logic State Voltage Definitions

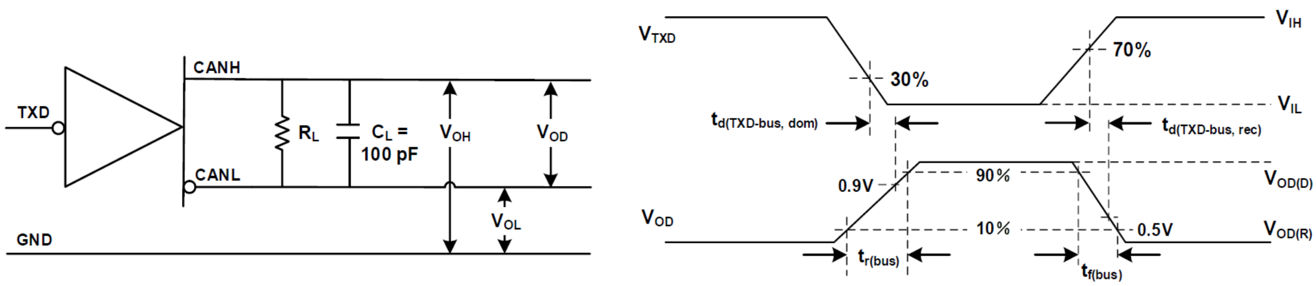


Figure 6.3.3. Driver Test Circuit and Voltage Waveform

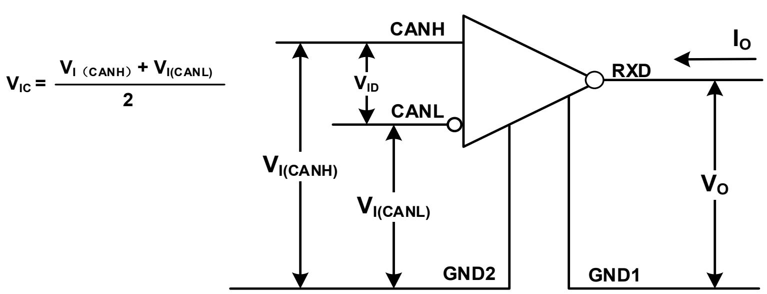


Figure 6.3.4. Receiver Voltage and Current Definitions

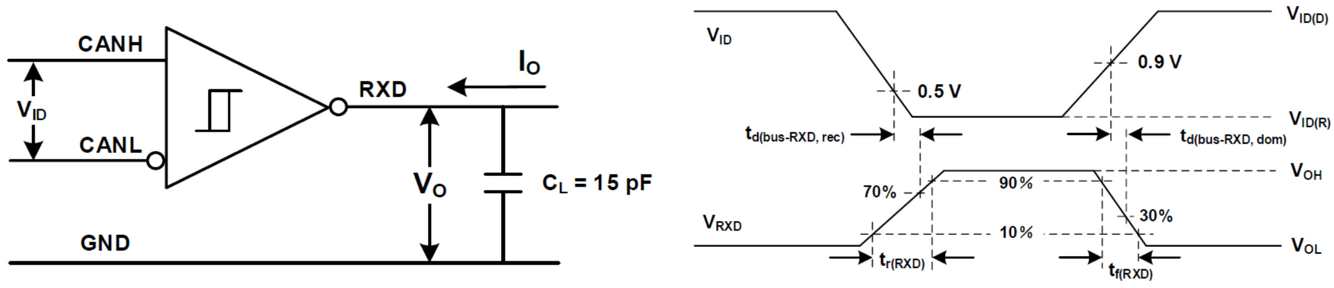


Figure 6.3.5. Receiver Test Circuit and Voltage Waveform

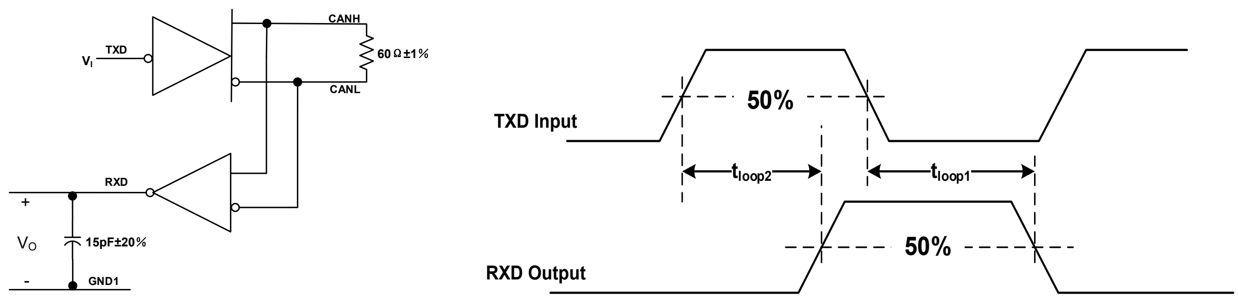


Figure 6.3.6. t_{LOOP} Test Circuit and Voltage Waveform

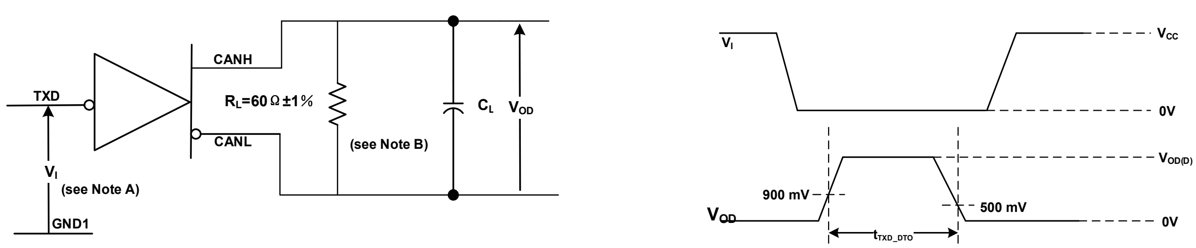


Figure 6.3.7. Dominant Time-out Test Circuit and Voltage Waveform

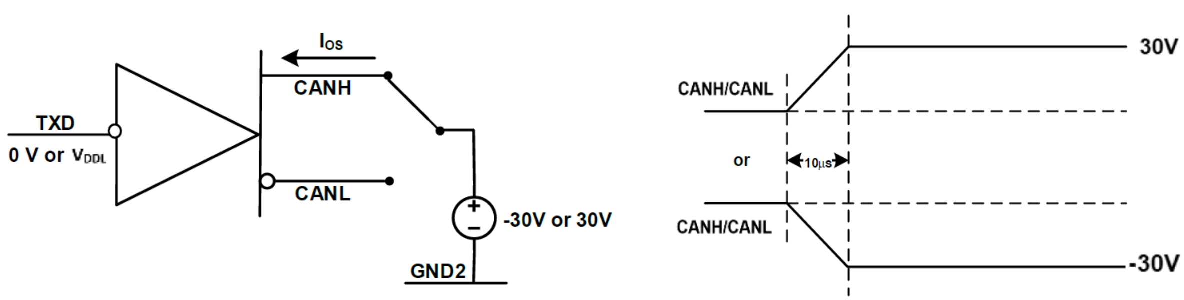


Figure 6.3.8. Driver Short-Circuit Current Test Circuit and Waveform

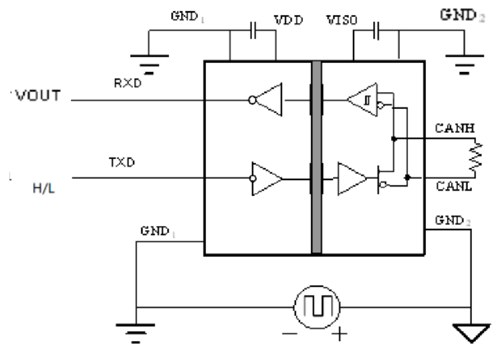


Figure 6.3.9 Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value	Unit	Comments
Minimum External Air Gap (Clearance)	CLR	8.15	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	CPG	8.15	mm	Shortest terminal-to-terminal distance across the package surface
Distance Through Insulation	DTI	26	μm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

Description	Test Condition	Value
Overvoltage Category per IEC60664-1	For Rated Mains Voltage 150Vrms	I to IV
	For Rated Mains Voltage 300Vrms	I to IV
	For Rated Mains Voltage 600Vrms	I to III
Climatic Classification		40/125/21
Pollution Degree per DIN VDE 0110,		2

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value	Unit
Maximum repetitive isolation voltage		V_{IORM}	1500	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	1061	V_{RMS}

	DC Voltage		1500	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, Vini=V_{IOTM}, t_{ini} = 60s , $V_{pd(m)}$=1.2*V_{IORM}, t_m=10s.	q_{pd}	<5	pC
	Method a, after environmental tests subgroup 1, Vini=V_{IOTM}, t_{ini}=60s ,$V_{pd(m)}$=1.6*V_{IORM}, t_m=10s			pC
	Method b, routine test (100% production) and preconditioning (type test);V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd (m)}$=1.875*V_{IORM}, t_m=1s （method b1） or $V_{pd(m)}$=Vini, t_m=t_{ini}(method b2)			pC
Maximum transient isolation voltage	t = 60s	V_{IOTM}	7070	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50μs waveform per IEC62368-1	V_{IMP}	7600	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50μs waveform, V_{IOSM}≥V_{IMP} × 1.3	V_{IOSM}	10000	V_{PEAK}
Isolation resistance	V_{IO} =500V, T_{amb}=25℃	R_{IO}	>10^{12}	Ω
	V_{IO} =500V, 100℃ ≤ T_{amb} ≤ 125℃	R_{IO}	>10^{11}	Ω
	V_{IO} =500V, T_{amb}=T_s	R_{IO}	>10^9	Ω
Isolation capacitance	f = 1MHz	C_{IO}	~4	pF
Safety total power dissipation	$θ_{JA}$ = 59.2 °C/W, V_I = 5.25 V, T_J = 150 °C, T_A = 25 °C, package SOW16	Ps	2111	mW
	$θ_{JA}$ = 55.7 °C/W, V_I = 5.25 V, T_J = 150 °C, T_A = 25 °C, package SOW20	Ps	2244	mW
Safety input, output, or supply current	$θ_{JA}$ = 59.2 °C/W, V_I = 5.25 V, T_J = 150 °C, T_A = 25 °C, package SOW16	Is	402	mA

	θ_{JA} = 55.7 °C/W, V_I = 5.25 V, T_J = 150 °C, T_A = 25 °C, package SOW20	Is	427	mA
Maximum safety temperature		Ts	150	℃
UL1577				
Insulation voltage per UL	V_{TEST} = V_{ISO}, t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO}, t = 1 s (100% production test)	V_{ISO}	5000	V_{RMS}

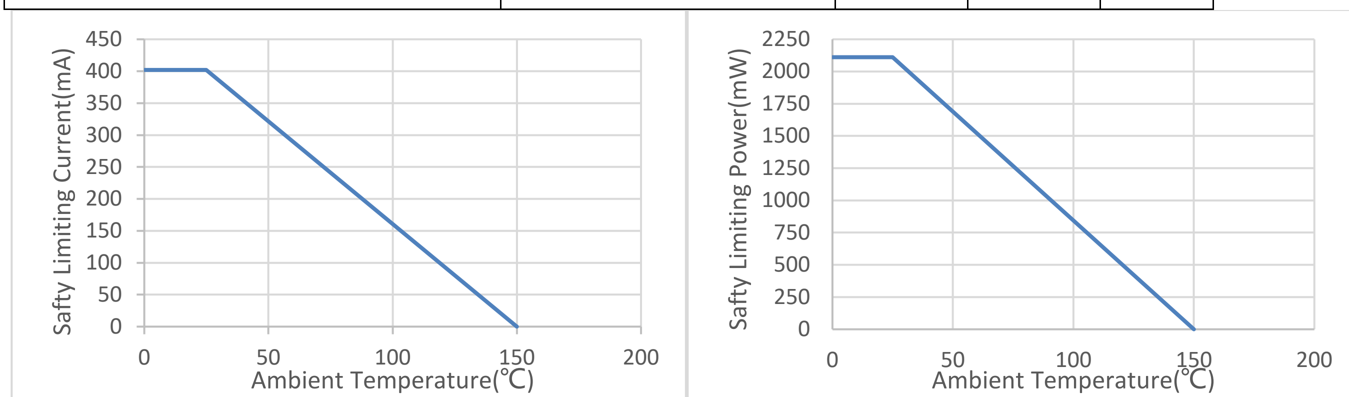


Figure 7.1 NSIP9042 SOW16 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17

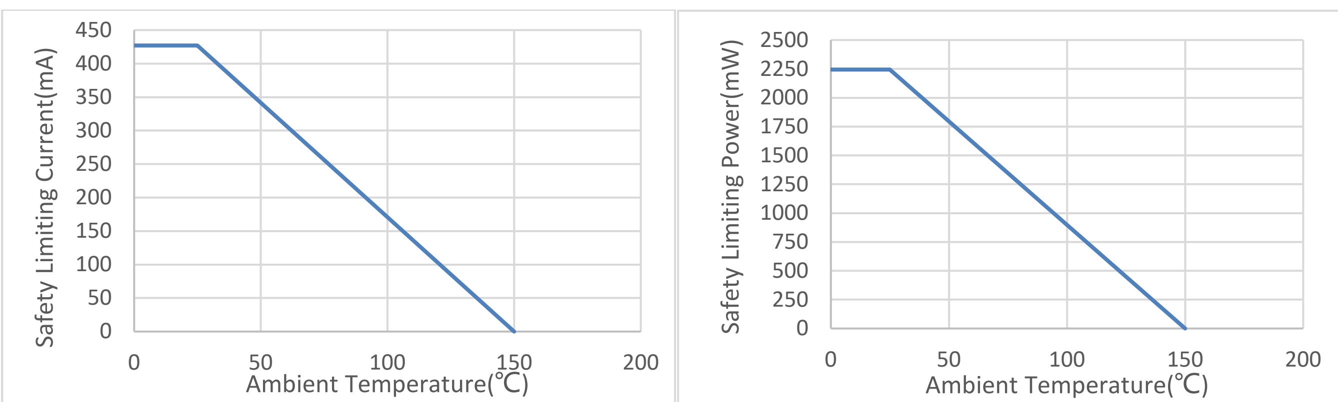


Figure 7.2 NSIP9042 SOW20 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17

7.3. Regulatory Information

The NSIP9042 are approved or pending approval by the organizations listed in table.

UL1577 & CSA Component Acceptance Notice 5A		***DIN EN IEC 60747-17 (VDE 0884-17)***	***EN IEC62368-1***	***GB4943.1***
Single Protection, 5000V_{rms} Isolation voltage	Single Protection, 5000V_{rms} Isolation voltage	Reinforced Insulation V_{IORM}=1500Vpeak V_{IOTM}=7070Vpeak	5000Vrms for 1min	Certified according to GB4943.1
Certified by UL		Certified by TUV		Certified by CQC
E500602	E500602	R50632560 0002	R50574061	CQC23001378663

8. Function Description

The NSIP9042 is an isolated CAN transceiver which is fully compatible with the ISO11898-2 standard. The NSIP9042 is a high reliability isolated controller area network(CAN) physical layer transceiver with integrated DC to DC converter. The digital isolator is SiO_2 isolation based on Novosense capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The NSIP9042 device is safety certified by UL1577, supporting 5kVrms insulation withstand voltages. The NSIP9042 provides high electromagnetic immunity and low emission. The data rate of the NSIP9042 is up to 5Mbps. The NSIP9042 provides thermal protection and transmit data dominant time out function.

8.1. Device Functional Modes

TXD	CANH	CANL	BUS STATE
L	H	L	Dominant
H	Z	Z	Recessive
Open	Z	Z	Recessive

[1] H= high level; L=low level; Z= common mode(recessive) bias to $V_{ISOIN}/2$

Table 8.1. Driver Function Table

V_{ID}=CANH-CANL	RXD	BUS STATE
$V_{ID} \geq 0.9V$	L	Dominant
$0.5 < V_{ID} < 0.9V$	X	Uncertain
$V_{ID} \leq 0.5V$	H	Recessive
Open	H	Recessive

[1] H= high level; L=low level; X= uncertain

Table 8.2. Receiver Function Table

8.2. TXD dominant time-out function

A ‘TXD dominant time-out’ timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD.

If the duration of the LOW level on pin TXD exceeds the internal timer value (t_{TXD_DTO}), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD.

8.3. Current Protection

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

8.4. Over Temperature Protection

The NSIP9042 is protected against over-temperature conditions. When the chip is over 165℃, it will be shut down until the temperature of below 145℃.

9. Application Note

9.1. Layout Considerations

The NSIP9042 require a 10 μF + 0.1 μF bypass capacitor between VDD_1 and GND_1, 10uF + 0.1 μF bypass capacitor between V_{ISOOUT} and GND_2. The capacitor should be placed as close as possible to the package. To eliminate line reflections, each cable end is terminated with a resistor, whose value matches the characteristic impedance of the cable. It's good practice to place the bus connectors and termination resistor as close as possible to the CANH and CANL pins.

9.2. Typical Application

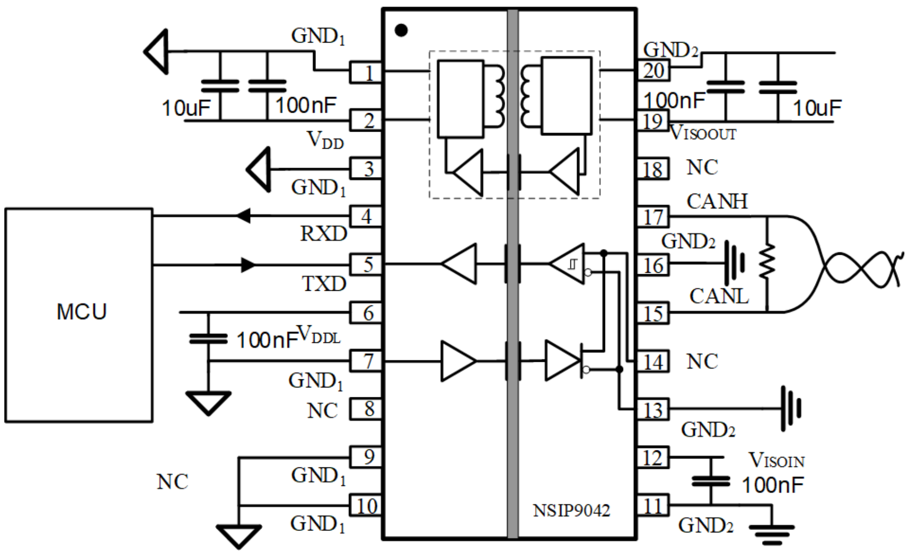
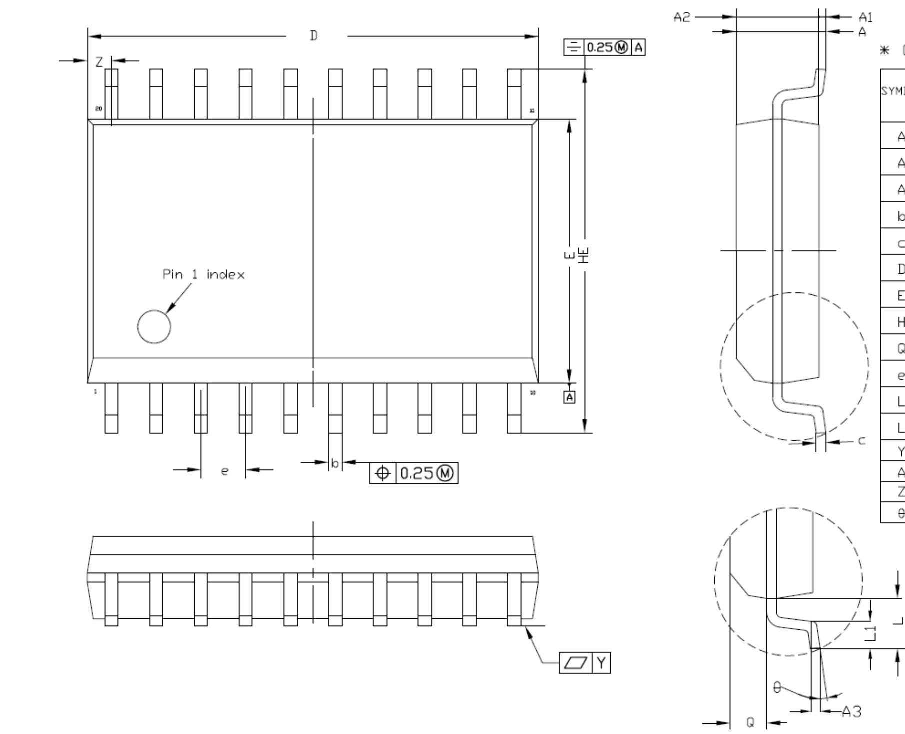


Figure 9.1 NSIP9042 typical application circuit

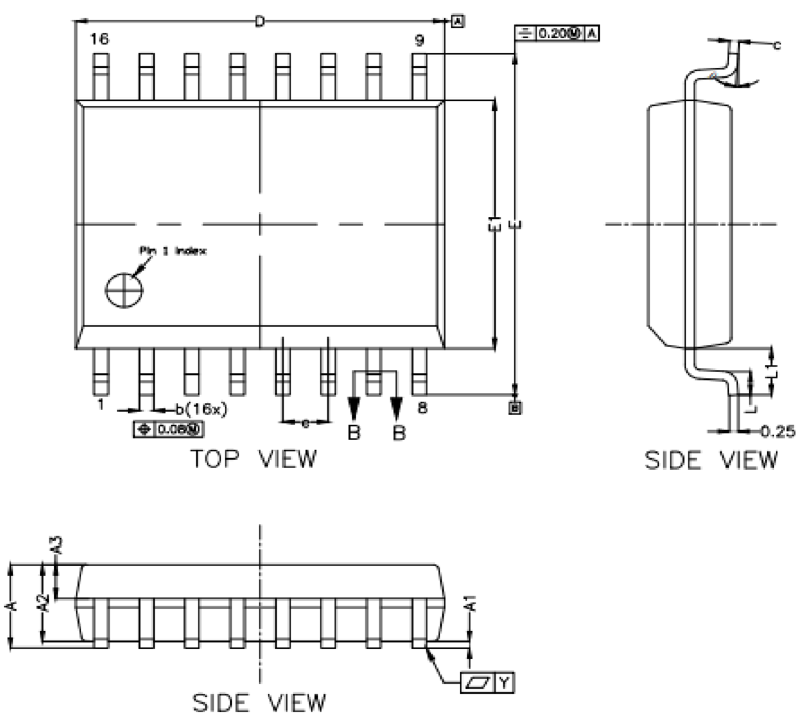
10. Package Information



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	2.65	---	---	0.100
A1	0.10	---	0.30	0.004	---	0.012
A2	2.25	---	2.45	0.089	---	0.096
b	0.36	---	0.49	0.014	---	0.019
c	0.23	---	0.32	0.009	---	0.013
D	12.6	---	13.0	0.49	---	0.51
E	7.4	---	7.6	0.29	---	0.30
HE	10.00	---	10.65	0.394	---	0.419
Q	1.0	---	1.1	0.039	---	0.043
e	1.27 bsc			0.050 bsc		
L	1.40 bsc			0.055 bsc		
L1	0.40	---	1.10	0.016	---	0.043
Y	---	0.10	---	---	0.004	---
A3	---	0.25	---	---	0.010	---
Z	0.40		0.90	0.016		0.035
θ	0°	---	8°	0°	---	8°

Figure 10.1 SOW20 Package Shape and Dimension in millimeters



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.48
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 10.2 SOW16 Package Shape and Dimension in millimeters

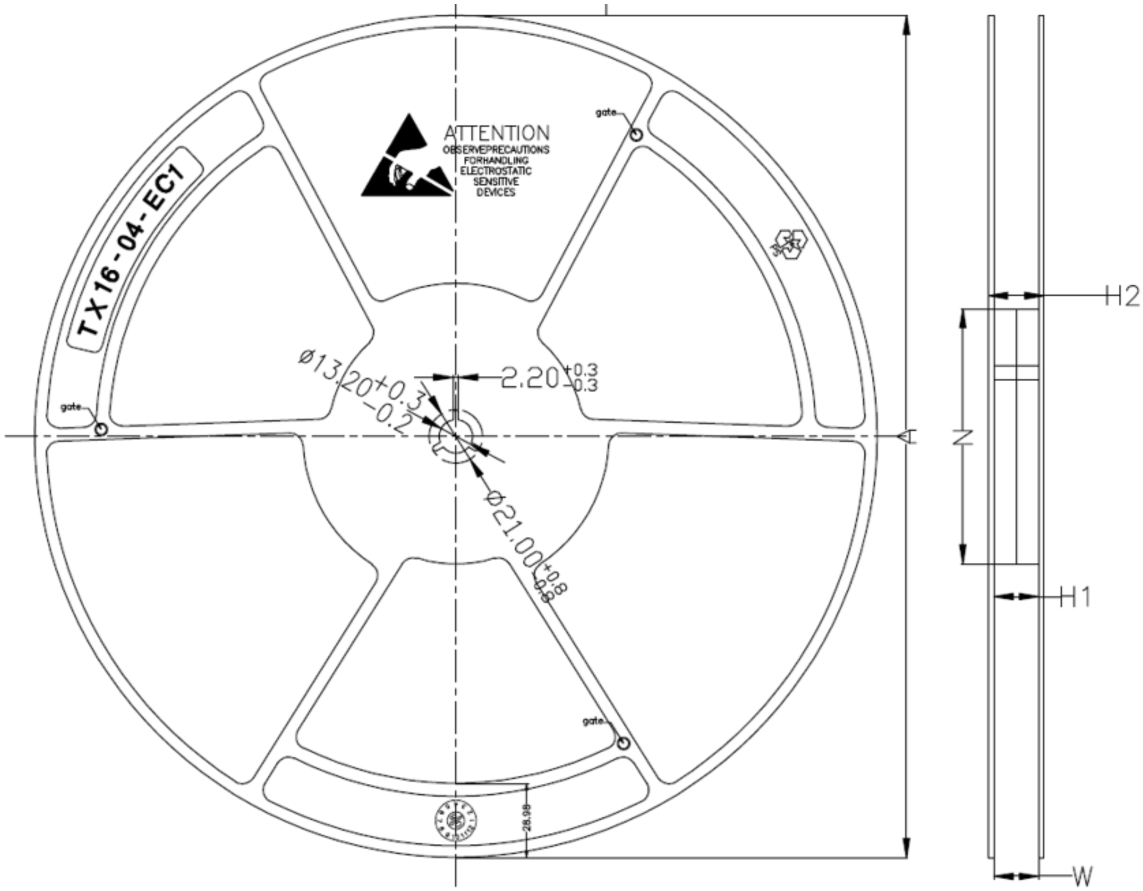
11. Order Information

Part Number	Isolation Rating (kVrms)	Max Data Rate (Mbps)	MSL	Temperature	Package	SPQ
NSIP9042-DSWTR	5	5 (CAN FD)	3	-40 to 125℃	SOW20	1000
NSIP9042-DSWR	5	5 (CAN FD)	3	-40 to 125℃	SOW16	1500
NSIP9042V-DSWR	5	5 (CAN FD)	3	-40 to 125℃	SOW16	1500

12. Documentation Support

Part Number	Product Folder	Datasheet	Application Note
NSIP9042	Tbd	Tbd	Tbd

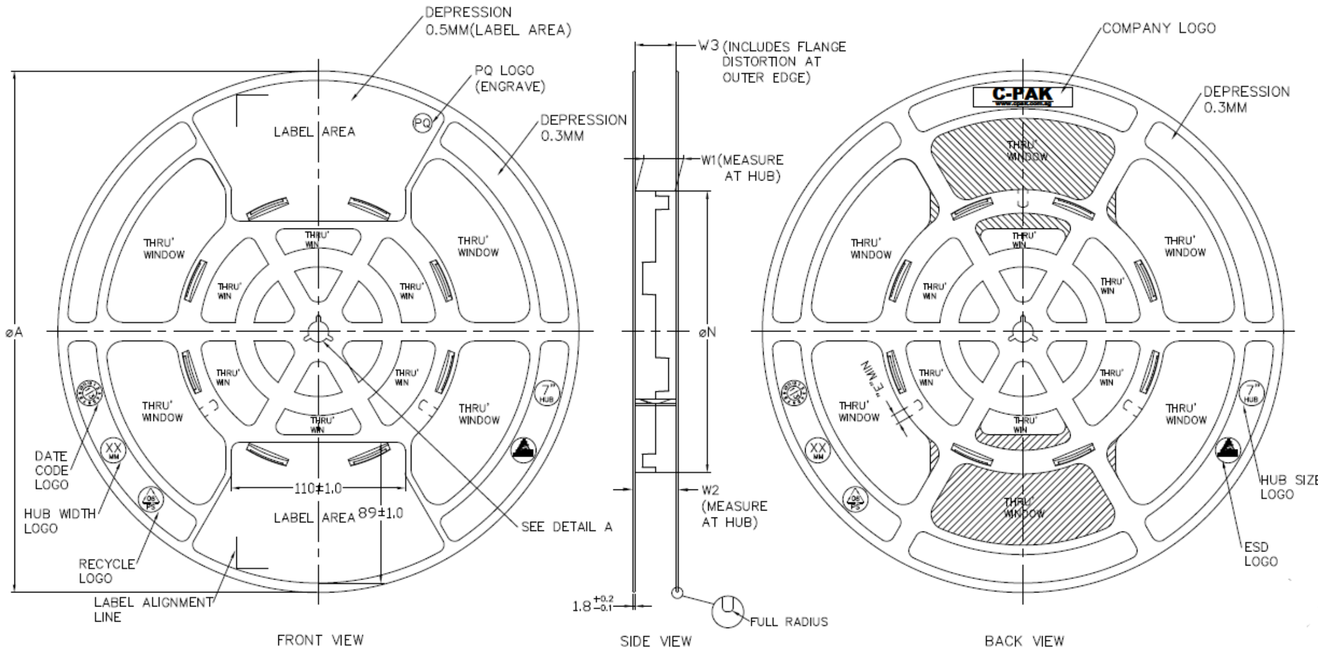
13. Tape And Reel Information

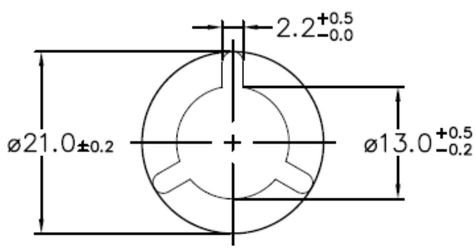


PRODUCT SPECIFICATIONS					
TAPE WIDTH	ØA $^{+2}_{-2}$	ØN $^{+2}_{-2}$	H1 $^{+2}_{-0}$	H2 $^{+1}_{-1}$	W $^{+3.5}_{-0.2}$
16MM	330	100	16.4	20.6	16.4

NOTES:
1.MATERIAL:DISSIPATIVE(BLACK)
2.FLANGE WARPAGE:3 MM MAXIMUM 5
3.ALL DIMENSIONS ARE IN MM
4.ESD - SURFACE RESISTIVITY-10 TO 10 OHMS/SQ
5.GENERAL TOLERANCE: ±0.25 MM

Figure 13.1 Tape Information of SOW16



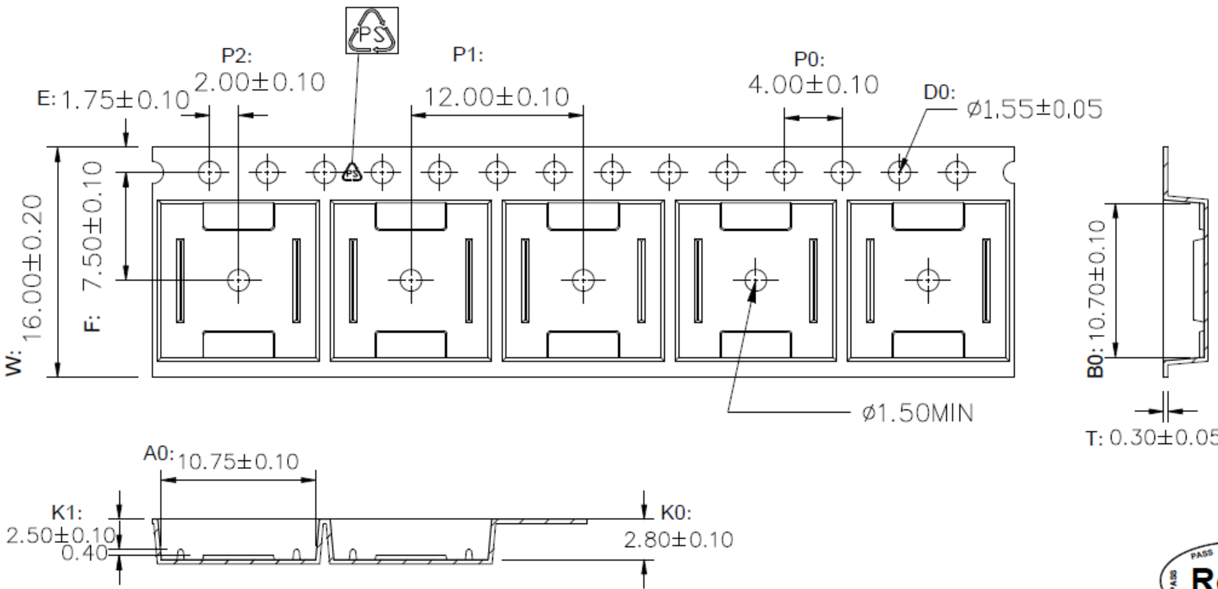


ARBOR HOLE
DETAIL A
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	ØA ±2.0	ØN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	$8.4^{+1.5}_{-0.0}$	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	$12.4^{+2.0}_{-0.0}$	18.4		5.5
16MM	330	178	$16.4^{+2.0}_{-0.0}$	22.4		5.5
24MM	330	178	$24.4^{+2.0}_{-0.0}$	30.4		5.5
32MM	330	178	$32.4^{+2.0}_{-0.0}$	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES

Figure 13.2 Tape Information of SOW20



1. 10 sprocket hole pitch cumulative tolerance ±0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy .
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 378 Meters.(復卷 N=122)
7. Component load per 13" reel : 1000 pcs.
8. Surface resistivity :$10^{5} \sim 10^{10}\Omega/\square$

W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

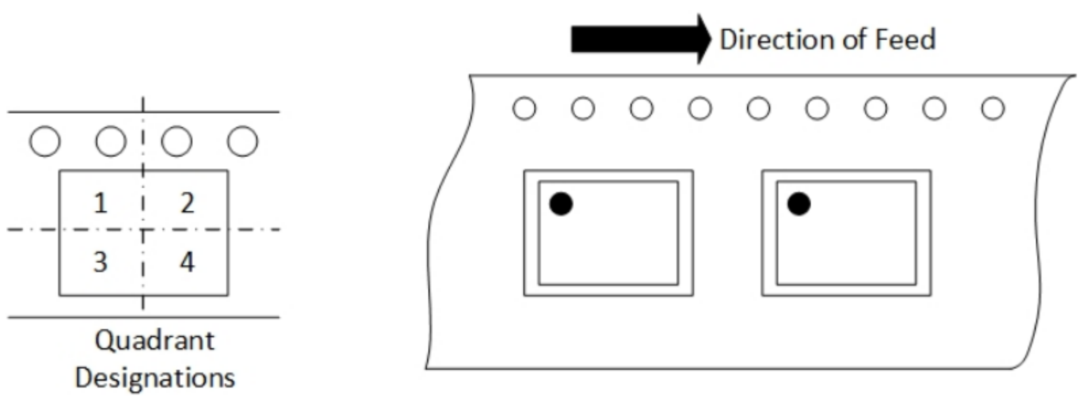
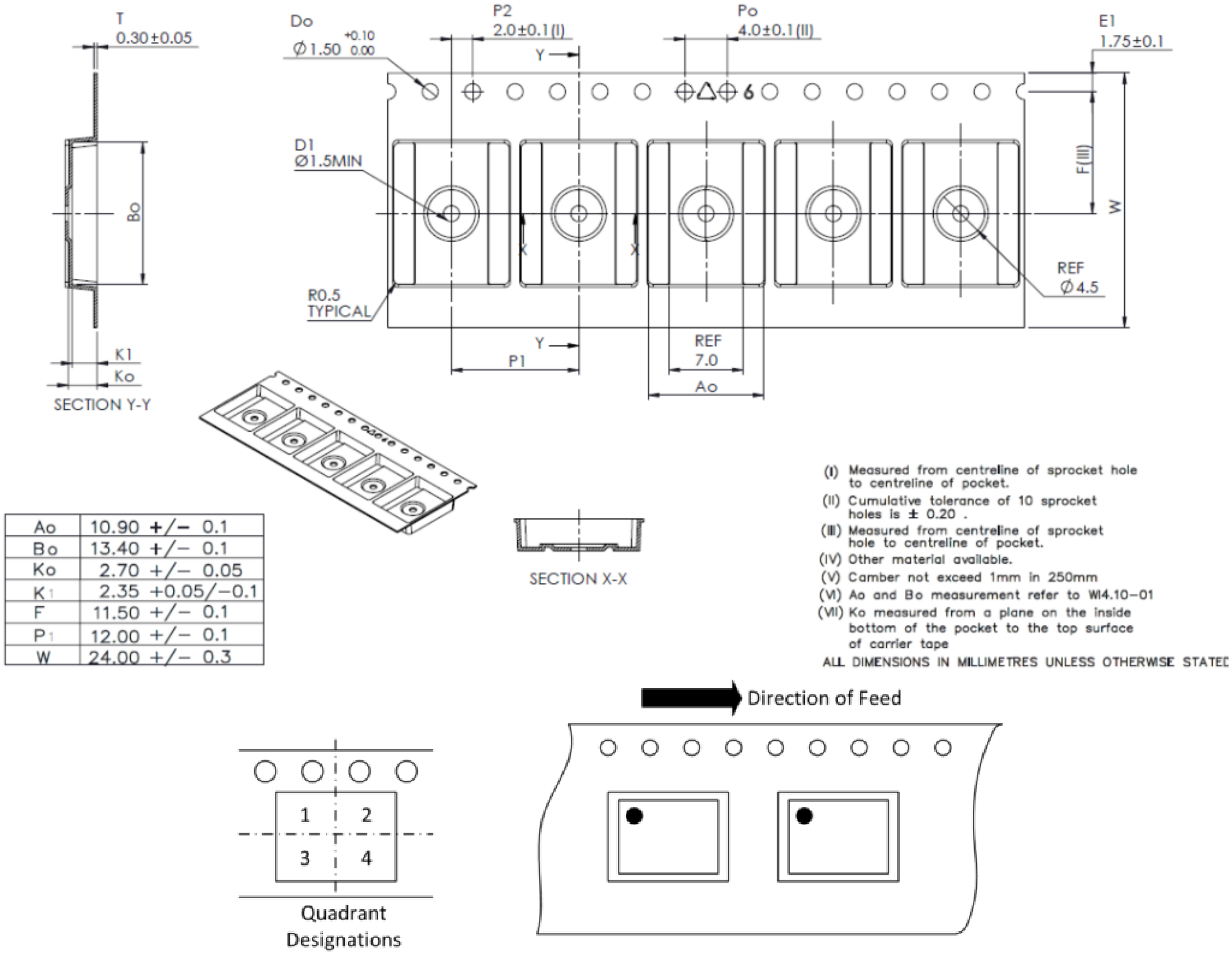


Figure 13.3 Reel Information of SOW16



Ao	10.90 +/− 0.1
Bo	13.40 +/− 0.1
Ko	2.70 +/− 0.05
K1	2.35 +0.05/−0.1
F	11.50 +/− 0.1
P1	12.00 +/− 0.1
W	24.00 +/− 0.3

Figure 13.4 Reel Information of SOW20

14. Revision History

Revision	Description	Date
1.0	Initial version	2025/12/15

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