

### Product Overview

NSI8266C0 is a high reliability six-channel digital isolator, The NSI8266C0 device is safety certified by UL1577 support several insulations withstand voltage(5kV), while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of NSI8266C0 is up to 30Mbps, and the common-mode transient immunity (CMTI) is up to 100kV/us. NSI8266C0's default output is low when input power is lost to prevent IPM switching during power on stage. Wide supply voltage of NSI8266C0 supports to connect with most digital interface directly. High system level EMC performance enhance reliability and stability of use. NSI8266C0 has the interlock function for adjacent channels to provide the shoot-through protection, to eliminate the short-circuit risk of IGBT inside the IPM, to enhance system robust.

### Key Features

- Up to 5000V<sub>rms</sub> Insulation voltage
- Date rate: DC to 30Mbps
- Power supply voltage: 2.5V to 5.5V
- High CMTI: 100V/us
- Chip level ESD: HBM: ±6kV
- Interlock function
- High system level EMC performance:
  - Enhanced system level ESD, EFT, Surge immunity
- Default output low level option
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <50ns
- Operation temperature: -40°C~125°C
- RoHS-compliant packages:
  - SOP16(300mil)

### Safety Regulatory Approvals

- UL recognition: up to 5000V<sub>rms</sub> for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A approval IEC60950-1 standard
- DIN VDE V 0884-11:2017-01

### Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor Control

### Device Information

Part Number	Package	Body Size
NSI8266C0-DSWR	SOP16 (300mil)	10.30mm × 7.50mm

### Functional Block Diagrams

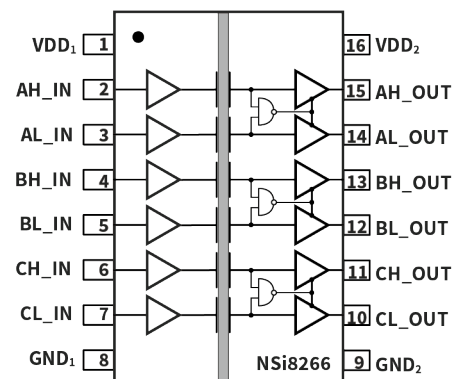


Figure 1. NSI8266C0 Block Diagram

**INDEX**

**1. PIN CONFIGURATION AND FUNCTIONS.....3**

**2. ABSOLUTE MAXIMUM RATINGS .....3**

**3. RECOMMENDED OPERATING CONDITIONS.....4**

**4. THERMAL INFORMATION .....5**

**5. SPECIFICATIONS ..... 5**

    5.1. ELECTRICAL CHARACTERISTICS ..... 5

    5.2. SUPPLY CURRENT CHARACTERISTICS – 5V SUPPLY ..... 5

    5.3. SUPPLY CURRENT CHARACTERISTICS –3.3V SUPPLY ..... 6

    5.4. SUPPLY CURRENT CHARACTERISTICS–2.5V SUPPLY ..... 6

    5.5. SWITCHING CHARACTERISTICS - 5V SUPPLY ..... 8

    5.6. SWITCHING CHARACTERISTICS - 3.3V SUPPLY ..... 8

    5.7. SWITCHING CHARACTERISTICS - 2.5V SUPPLY ..... 9

    5.8. TYPICAL PERFORMANCE CHARACTERISTICS ..... 10

    5.9. PARAMETER MEASUREMENT INFORMATION ..... 10

**6. HIGH VOLTAGE FEATURE DESCRIPTION ..... 11**

    6.1. INSULATION AND SAFETY RELATED SPECIFICATIONS..... 11

    6.2. SAFETY-LIMITING VALUES ..... 13

    6.3. REGULATORY INFORMATION..... 13

**7. FUNCTION DESCRIPTION ..... 14**

    7.1. OVERVIEW ..... 14

    7.2. OOK MODULATION ..... 14

    7.3. SHOOT THROUGH PROTECTION ..... 15

**8. APPLICATION NOTE..... 16**

    8.1. TYPICAL APPLICATION CIRCUIT..... 16

    8.2. PCB LAYOUT..... 16

    8.3. HIGH SPEED PERFORMANCE ..... 17

    8.4. TYPICAL SUPPLY CURRENT EQUATIONS ..... 17

**9. PACKAGE INFORMATION ..... 18**

**10. ORDERING INFORMATION ..... 19**

**11. DOCUMENTATION SUPPORT ..... 19**

**12. TAPE AND REEL INFORMATION ..... 20**

**13. REVISION HISTORY ..... 22**

## 1. Pin Configuration and Functions

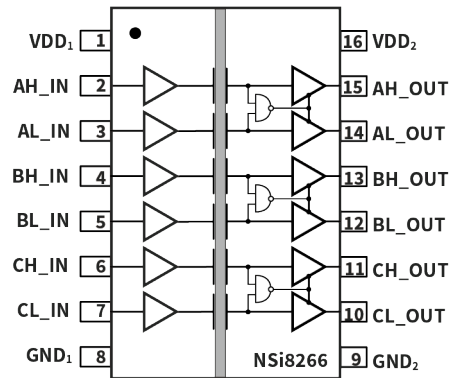


Figure 1.1 NSI8266C0 Package

Table 1.1 NSI8266C0 Pin Configuration and Description

<b>NSI8266C0 PIN NO.</b>	<b>SYMBOL</b>	<b>FUNCTION</b>
1	VDD <sub>1</sub>	Power Supply for Isolator Side 1
2	AH_IN	High side Logic Input AH
3	AL_IN	Low side Logic Input AL
4	BH_IN	High side Logic Input BH
5	BL_IN	Low side Logic Input BL
6	CH_IN	High side Logic Input CH
7	CL_IN	Low side Logic Input CL
8	GND <sub>1</sub>	Ground 1, the ground reference for Isolator Side 1
9	GND <sub>2</sub>	Ground 2, the ground reference for Isolator Side 2
10	CL_OUT	Low side Logic Output CL
11	CH_OUT	High side Logic Output CH
12	BL_OUT	Low side Logic Output BL
13	BH_OUT	High side Logic Output BH
14	AL_OUT	Low side Logic Output AL
15	AH_OUT	High side Logic Output AH
16	VDD <sub>2</sub>	Power Supply for Isolator Side 2

## 2. Absolute Maximum Ratings

<b>Parameters</b>	<b>Symbol</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Unit</b>	<b>Comments</b>
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	VINA, VINB, VINC, VIND, VINE, VINF	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Output Voltage	VOUTA, VOUTB, VOUTC, VOUTD, VOUTE, VOUTF	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Input/Output Pulse Voltage	ALL I/O Pin	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Output current	I <sub>o</sub>	-15		15	mA	
Maximum Surge Isolation Voltage	V <sub>IOSM</sub>			6.25	kV	
Operating Temperature	T <sub>opr</sub>	-40		125	°C	
Junction Temperature	T <sub>j</sub>			150	°C	
Storage Temperature	T <sub>stg</sub>	-65		150	°C	
Electrostatic discharge	HBM			±6000	V	
	CDM			±2000	V	

### 3. Recommended Operating Conditions

<b>Parameters</b>	<b>Symbol</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Unit</b>	<b>Comments</b>
Power Supply Voltage	VDD1, VDD2	2.5		5.5	V	
High-level Input Voltage	V <sub>IH</sub>	2			V	
Low-level Input Voltage	V <sub>IL</sub>			0.8	V	
Data Rate	DR	0		30	Mbps	
Ambient Temperature	T <sub>a</sub>	-40		125	°C	

## 4. Thermal Information

Parameters	Symbol	SOP16(300mil)	Unit
Junction-to-ambient thermal resistance	$\theta_{JA}$	60.3	°C/W
Junction-to-case(top) thermal resistance	$\theta_{JC (top)}$	24.0	°C/W
Junction-to-board thermal resistance	$\theta_{JB}$	29.3	°C/W

## 5. Specifications

### 5.1. Electrical Characteristics

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power on Reset	VDD <sub>POR</sub>		2.2		V	POR threshold as during power-up
	VDD <sub>HYS</sub>		0.1		V	POR threshold Hysteresis
Input Threshold	V <sub>IT</sub>		1.6		V	Input Threshold at rising edge
	V <sub>IT_HYS</sub>		0.4		V	Input Threshold Hysteresis
High Level Input Voltage	V <sub>IH</sub>	2			V	
Low Level Input Voltage	V <sub>IL</sub>			0.8	V	
High Level Output Voltage	V <sub>OH</sub>	VDD-0.4			V	I <sub>OH</sub> = -4mA
Low Level Output Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 4mA
Output Impedance	R <sub>out</sub>		50		ohm	
Input Pull high or low Current	I <sub>pull</sub>		8	15	µA	
Start Up Time after POR	tr <sub>bs</sub>		10		µs	
Common Mode Transient Immunity	CMTI	±100	±150		kV/µs	

### 5.2. Supply Current Characteristics – 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSI8266C0					

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I <sub>DD1</sub> (Q0)		1.39	3.09	mA	All Input 0V
	I <sub>DD2</sub> (Q0)		3.41	5.63	mA	
	I <sub>DD1</sub> (Q1)		7.37	12.16	mA	All Input at supply
	I <sub>DD2</sub> (Q1)		3.49	5.76	mA	
	I <sub>DD1</sub> (16k)		4.39	7.24	mA	All Input with 16kbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (16k)		3.67	6.06	mA	
	I <sub>DD1</sub> (1M)		1.39	3.09	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		3.41	5.63	mA	

### 5.3. Supply Current Characteristics –3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	<b>NSI8266C0</b>					
	I <sub>DD1</sub> (Q0)		1.33	3.00	mA	All Input 0V
	I <sub>DD2</sub> (Q0)		3.36	5.54	mA	
	I <sub>DD1</sub> (Q1)		7.26	11.98	mA	All Input at supply
	I <sub>DD2</sub> (Q1)		3.43	5.66	mA	
	I <sub>DD1</sub> (16k)		4.31	7.11	mA	All Input with 16kbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (16k)		3.55	5.86	mA	
	I <sub>DD1</sub> (1M)		1.33	3.00	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		3.36	5.54	mA	

### 5.4. Supply Current Characteristics–2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	<b>NSI8266C0</b>					
	I <sub>DD1</sub> (Q0)		1.29	2.94	mA	All Input 0V
	I <sub>DD2</sub> (Q0)		3.33	5.49	mA	
	I <sub>DD1</sub> (Q1)		7	11.55	mA	All Input at supply
	I <sub>DD2</sub> (Q1)		3.39	5.59	mA	
	I <sub>DD1</sub> (16k)		4.17	6.88	mA	All Input with 16kbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (16k)		3.47	5.73	mA	
	I <sub>DD1</sub> (1M)		1.29	2.94	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
I <sub>DD2</sub> (1M)		3.33	5.49	mA		

### 5.5. Switching Characteristics - 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		30	Mbps	
Minimum Pulse Width	PW			30	ns	
Propagation Delay	t <sub>PLH</sub>	2.5		50	ns	See <a href="#">Figure 5.5</a> , C <sub>L</sub> = 15pF
	t <sub>PHL</sub>	2.5		50	ns	See <a href="#">Figure 5.5</a> , C <sub>L</sub> = 15pF
Pulse Width Distortion  t <sub>PHL</sub> - t <sub>PLH</sub>	PWD			5.0	ns	See <a href="#">Figure 5.5</a> , C <sub>L</sub> = 15pF
Rising Time	t <sub>r</sub>			5.0	ns	See <a href="#">Figure 5.5</a> , C <sub>L</sub> = 15pF
Falling Time	t <sub>f</sub>			5.0	ns	See <a href="#">Figure 5.5</a> , C <sub>L</sub> = 15pF
Peak Eye Diagram Jitter	t <sub>JIT(PK)</sub>		350		ps	
Channel-to-Channel Delay Skew	t <sub>SK(c2c)</sub>			2.5	ns	
Part-to-Part Delay Skew	t <sub>SK(p2p)</sub>			5.0	ns	

### 5.6. Switching Characteristics - 3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		30	Mbps	
Minimum Pulse Width	PW			30	ns	
Propagation Delay	t <sub>PLH</sub>	2.5		50	ns	See <a href="#">Figure 5.5</a> , C <sub>L</sub> = 15pF
	t <sub>PHL</sub>	2.5		50	ns	See <a href="#">Figure 5.5</a> , C <sub>L</sub> = 15pF
Pulse Width Distortion  t <sub>PHL</sub> - t <sub>PLH</sub>	PWD			5.0	ns	See <a href="#">Figure 5.5</a> , C <sub>L</sub> = 15pF
Rising Time	t <sub>r</sub>			5.0	ns	See <a href="#">Figure 5.5</a> , C <sub>L</sub> = 15pF
Falling Time	t <sub>f</sub>			5.0	ns	See <a href="#">Figure 5.5</a> , C <sub>L</sub> = 15pF
Peak Eye Diagram Jitter	t <sub>JIT(PK)</sub>		350		ps	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Channel-to-Channel Delay Skew	$t_{sk(c2c)}$			2.5	ns	
Part-to-Part Delay Skew	$t_{sk(p2p)}$			5.0	ns	

### 5.7. Switching Characteristics - 2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		30	Mbps	
Minimum Pulse Width	PW			30	ns	
Propagation Delay	$t_{PLH}$	2.5		50	ns	See <a href="#">Figure 5.5</a> , $C_L = 15pF$
	$t_{PHL}$	2.5		50	ns	See <a href="#">Figure 5.5</a> , $C_L = 15pF$
Pulse Width Distortion $ t_{PHL} - t_{PLH} $	PWD			5.0	ns	See <a href="#">Figure 5.5</a> , $C_L = 15pF$
Rising Time	$t_r$			5.0	ns	See <a href="#">Figure 5.5</a> , $C_L = 15pF$
Falling Time	$t_f$			5.0	ns	See <a href="#">Figure 5.5</a> , $C_L = 15pF$
Peak Eye Diagram Jitter	$t_{JIT(PK)}$		350		ps	
Channel-to-Channel Delay Skew	$t_{sk(c2c)}$			2.5	ns	
Part-to-Part Delay Skew	$t_{sk(p2p)}$			5.0	ns	

5.8. Typical Performance Characteristics

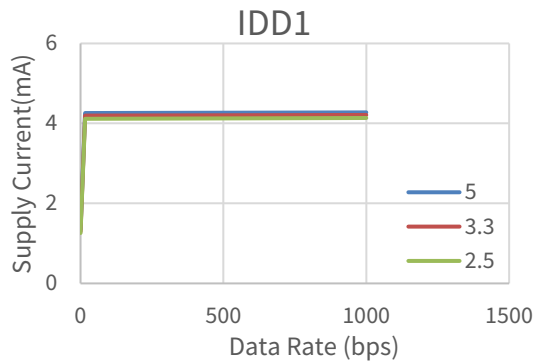


Figure 5.1 NSI8266 VDD1 Supply Current vs Data Rate



Figure 5.2 NSI8266 VDD2 Supply Current vs Data Rate

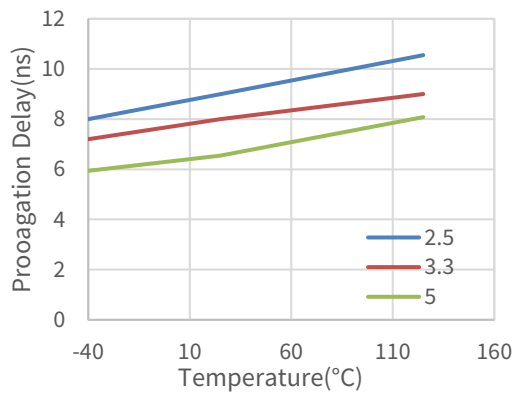


Figure 5.3 Rising Edge Propagation Delay Vs Temp

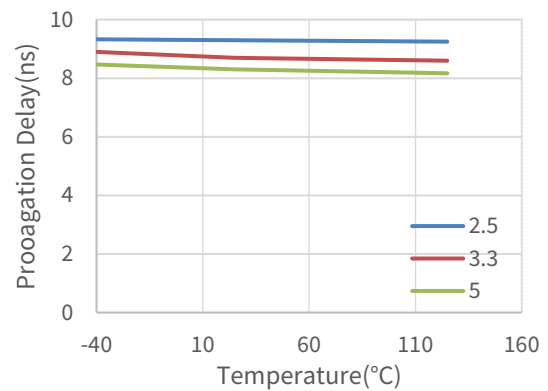


Figure 5.4 Falling Edge Propagation Delay Vs Temp

5.9. Parameter Measurement Information

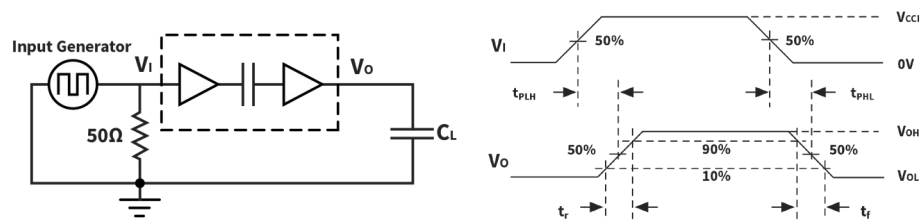


Figure 5.5 Switching Characteristics Test Circuit and Waveform

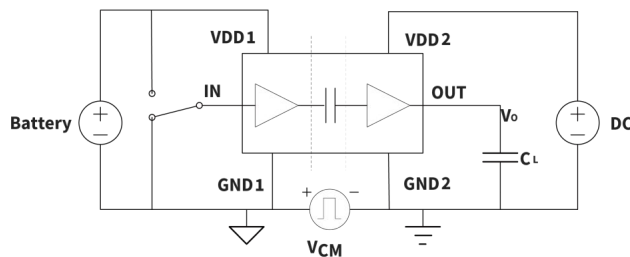


Figure 5.6 Common-Mode Transient Immunity Test Circuit

## 6. High Voltage Feature Description

### 6.1. Insulation and Safety Related Specifications

Description	Test Condition	Symbol	Value	Unit
			SOP16 (300mil)	
Min. External Air Gap (Clearance)		CLR	8	mm
Min. External Tracking (Creepage)		CPG	8	mm
Distance through the Insulation		DTI	28	um
Comparative Tracking Index	DIN EN 60112 (VDE 0303-11)	CTI	>600	V
Material Group	IEC 60112		I	
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150Vrms			I to IV	
For Rated Mains Voltage ≤ 300Vrms			I to IV	
For Rated Mains Voltage ≤ 600Vrms			I to IV	
For Rated Mains Voltage ≤ 1000Vrms			I to III	
Insulation Specification per DIN VDE V 0884-11:2017-01 <sup>1)</sup>				
Climatic Category			40/125/21	
Pollution Degree	per DIN VDE 0110, Table 1		2	
Maximum Working Isolation Voltage	AC voltage	V <sub>IOWM</sub>	1500	V <sub>RMS</sub>
	DC voltage		2121	V <sub>DC</sub>
Maximum Repetitive Isolation Voltage		V <sub>IORM</sub>	2121	V <sub>peak</sub>
Input to Output Test Voltage, Method B1	V <sub>ini. b</sub> = V <sub>IOTM</sub> , V <sub>pd(m)</sub> = V <sub>IORM</sub> × 1.875, t <sub>ini</sub> = t <sub>m</sub> = 1 sec, q <sub>pd</sub> ≤ 5 pC, 100% production test	V <sub>pd (m)</sub>	3977	V <sub>peak</sub>
Input to Output Test Voltage, Method A. After Environmental Tests Subgroup 1	V <sub>ini. a</sub> = V <sub>IOTM</sub> , V <sub>pd(m)</sub> = V <sub>IORM</sub> × 1.6, t <sub>ini</sub> = 60 sec, t <sub>m</sub> = 10 sec, q <sub>pd</sub> ≤ 5 pC	V <sub>pd (m)</sub>	3394	V <sub>peak</sub>

Description	Test Condition	Symbol	Value	Unit
Input to Output Test Voltage, Method A. After Input and Output Safety Test Subgroup 2 and Subgroup 3	$V_{ini.a} = V_{IOTM}$ , $V_{pd(m)} = V_{IORM} \times 1.2$ , $t_{ini} = 60 \text{ sec}$ , $t_m = 10 \text{ sec}$ , $q_{pd} \leq 5 \text{ pC}$	$V_{pd(m)}$	2545	$V_{peak}$
Maximum Transient Isolation Voltage	$t = 60 \text{ sec}$	$V_{IOTM}$	8000	$V_{peak}$
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{TEST} = 1.6 \times V_{IOSM}$	$V_{IOSM}$	6250	$V_{peak}$
Isolation Resistance	$V_{IO} = 500 \text{ V}$ , $T_{amb} = T_S$	$R_{IO}$	$>10^9$	$\Omega$
	$V_{IO} = 500 \text{ V}$ , $100 \text{ }^\circ\text{C} \leq T_{amb} \leq 125 \text{ }^\circ\text{C}$		$>10^{11}$	$\Omega$
Isolation Capacitance	$f = 1\text{MHz}$	$C_{IO}$	1.2	pF
Insulation Specification per UL1577				
Withstand Isolation Voltage	$V_{TEST} = 1.2 \times V_{ISO}$ , $t = 1 \text{ sec}$ , 100% production test	$V_{ISO}$	5000	$V_{rms}$

- 1) This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

### 6.2. Safety-Limiting Values

Reinforced isolation safety-limiting values as outlined in VDE-0884-11 of NSI8266C0-DSWR

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{\theta JA} = 60.3 \text{ }^\circ\text{C/W}$ , $T_J = 150 \text{ }^\circ\text{C}$ , $T_A = 25 \text{ }^\circ\text{C}$	2073	mW
Safety Supply Current	$R_{\theta JA} = 60.3 \text{ }^\circ\text{C/W}$ , $V_I = 5\text{V}$ , $T_J = 150 \text{ }^\circ\text{C}$ , $T_A = 25 \text{ }^\circ\text{C}$	414	mA
Safety Temperature <sup>2)</sup>		150	$^\circ\text{C}$

- 1) Calculate with the junction-to-air thermal resistance,  $R_{\theta JA}$ , of SOP16(300mil) package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature ( $T_J$ ) specified for the device.

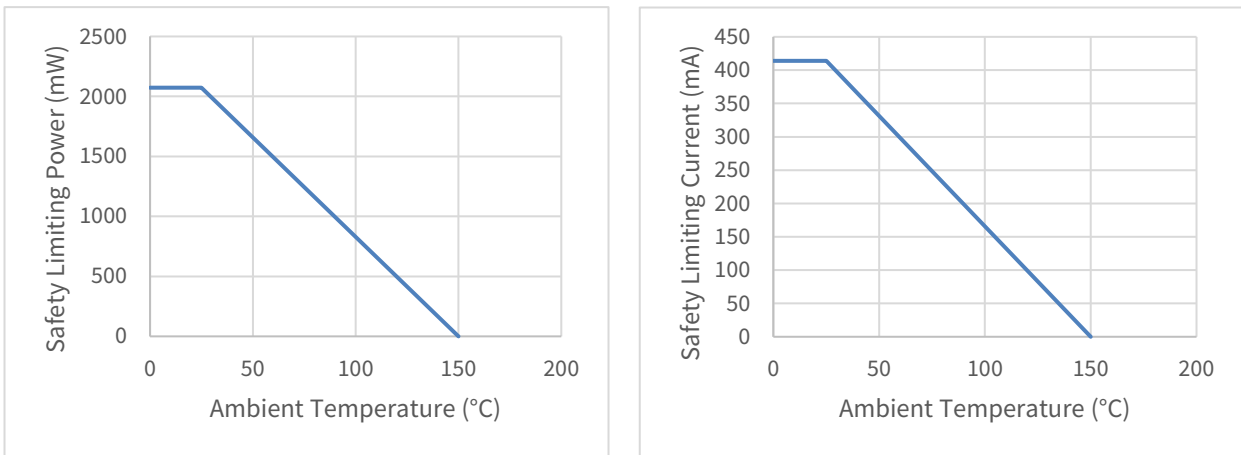


Figure 6.1 NSI8266C0-DSWR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

### 6.3. Regulatory Information

The NSI8266C0-DSWR are approved or pending approval by the organizations listed in table.

UL	VDE	CQC	TUV	
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1-2022	Certified According to EN IEC 62368-1
Single Protection, 5000V <sub>rms</sub> Isolation voltage	Single Protection, 5000V <sub>rms</sub> Isolation voltage	Reinforce Insulation 2121V <sub>peak</sub> , V <sub>IOSM</sub> =6250V <sub>peak</sub>	Reinforced insulation at 1500V <sub>RMS</sub> (2121V <sub>peak</sub> )	5000V <sub>rms</sub> for 1min
E500602	E500602	40052820	CQC20001264939	R 50574061

## 7. Function Description

### 7.1. Overview

NSI8266C0 is high reliability six-channel digital isolator. NSI8266C0 is safety certified by UL1577 support 5kV<sub>rms</sub> insulation withstand voltages, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate is up to 30Mbps, and the common-mode transient immunity (CMTI) is up to 100kV/us. NSI8266C0's default output is low when input power is lost to prevent IPM switching during power on stage. Wide supply voltage of NSI8266C0 support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

NSI8266C0 has a default output status when VDDIN is unready and VDDOUT is ready as shown in Table 7.1, which helps for diagnosis when power is missing at the transmitter side. The other outputs follow the same status with the input A after powering up respectively.

Table 7.1 Output status vs. power status

<i>XH_IN</i>	<i>XL_IN</i>	<i>VDD1 status</i>	<i>VDD2 status</i>	<i>XH_OUT</i>	<i>XL_OUT</i>	<i>Comment</i>
H	H	Ready	Ready	L	L	Normal operation.
L or NC	H	Ready	Ready	L	H	
H	L or NC	Ready	Ready	H	L	
L or NC	L or NC	Ready	Ready	L	L	
X	X	Unready	Ready	L	L	The output follows the Normal operation after input side VDD1 is powered on.
X	X	Ready	Unready	X	X	The output follows the Normal operation after output side VDD2 is powered on.

Note: H=Logic high; L=Logic low; X=Logic low or logic high  
VDD1 is input side power; VDD2 is outside power.

### 7.2. OOK Modulation

NSI8266C0 is based on a capacitive isolation barrier technique and the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, as shown in Fig7.1, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI.

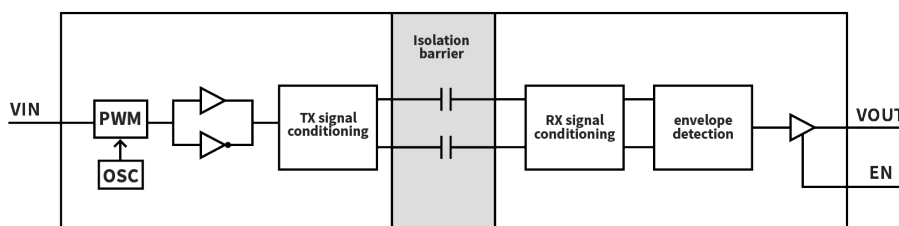


Figure 7.1 Single Channel Function Block Diagram

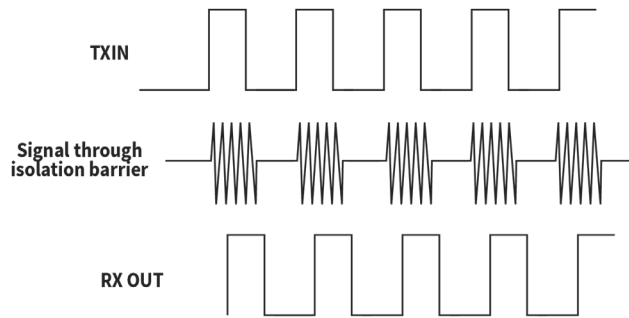


Figure 7.2 OOK Modulation

### 7.3. Shoot Through Protection

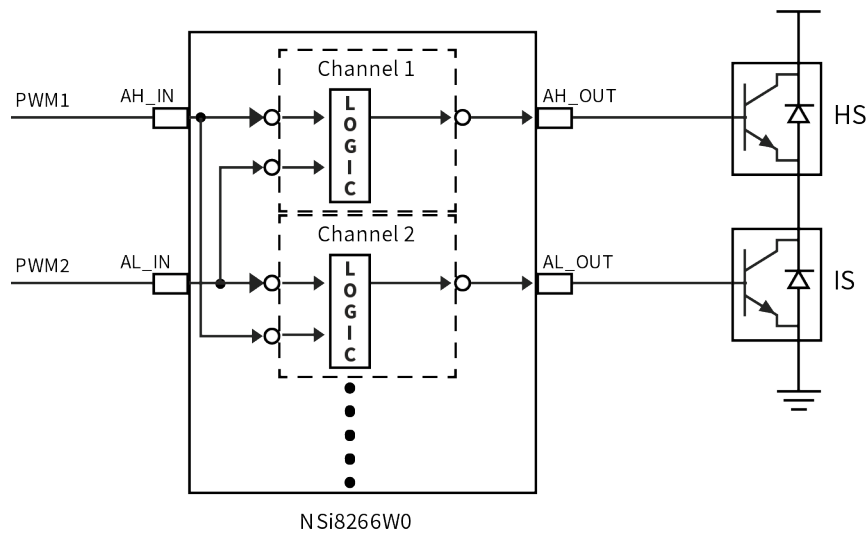


Figure 7.3 Typical IPM isolated driving Circuit

As shown in Fig. 7.3, NSI8266C0 has the interlock function to provide the shoot through protection to prevent both high-side and low-side switches to be activated simultaneously, if one of the adjacent channels is in ON state, the counterpart PWM signal is inhibited, preventing it to turn high. Fig. 7.4 & Fig.7.5 show the test waveform.

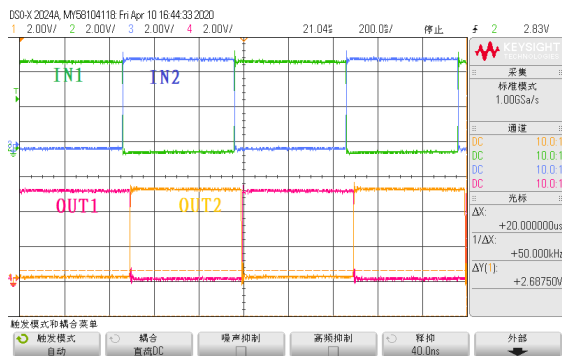


Figure 7.4 NSI8266C0 normal driving signal waveform

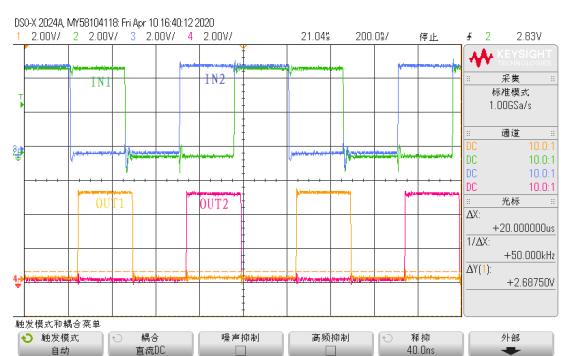


Figure 7.5 NSI8266C0 driving signal with interlock triggered

## 8. Application Note

### 8.1. Typical Application Circuit

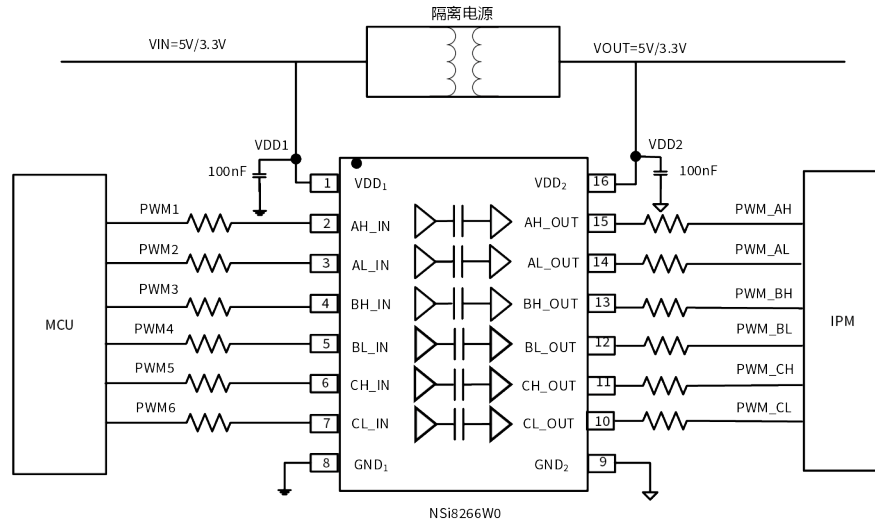


Figure 8.1 Typical IPM isolated driving Circuit

### 8.2. PCB Layout

NSI8266C0 requires a 0.1  $\mu\text{F}$  bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. Figure 5.1 to Figure 5.2 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300  $\Omega$ ) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50  $\Omega$ ,  $\pm 40\%$ . When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

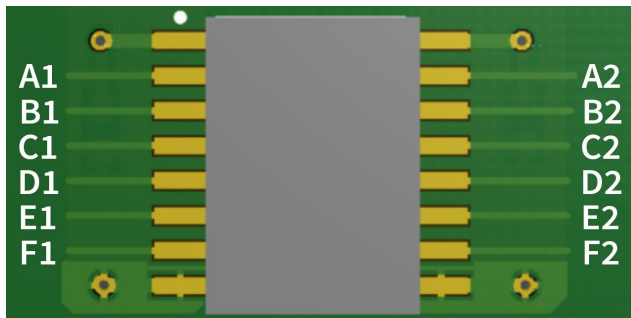
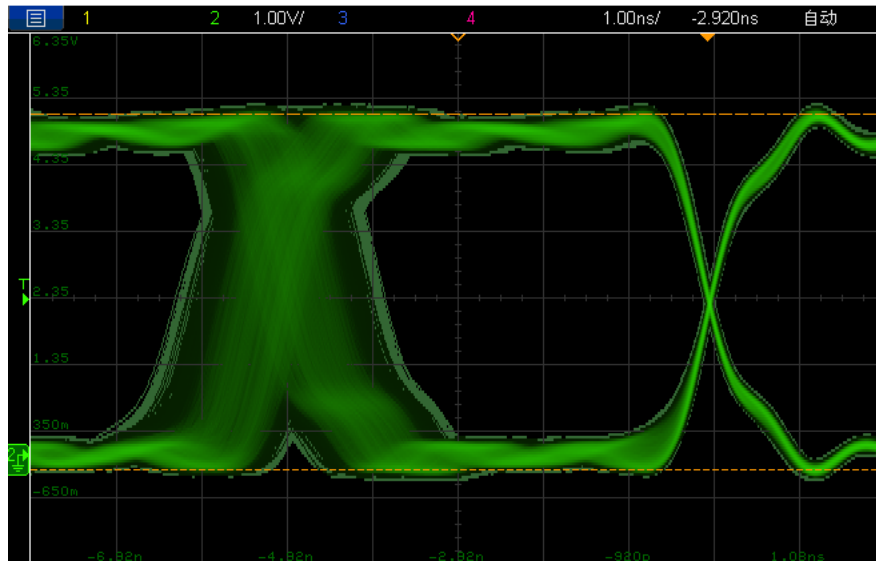


Figure 8.2 Recommended PCB Layout — Top Layer



Figure 8.3 Recommended PCB Layout — Bottom Layer

### 8.3. High Speed Performance



### 8.4. Typical Supply Current Equations

The typical supply current of NSI8266C0 can be calculated using below equations.  $I_{DD1}$  and  $I_{DD2}$  are typical supply currents measured in mA,  $f$  is data rate measured in Mbps,  $C_L$  is the capacitive load measured in pF

#### NSI8266:

$$I_{DD1} = 0.22 * a1 + 1.2 * b1 + 0.7 * c1.$$

$$I_{DD2} = 3.3 + VDD1 * f * C_L * c1 * 10^{-9}$$

Where  $a1$  is the channel number of low inputs at side 1,  $b1$  is the channel number of high inputs at side 1,  $c1$  is the channel number of switch signal inputs at side 1.

### 9. Package Information

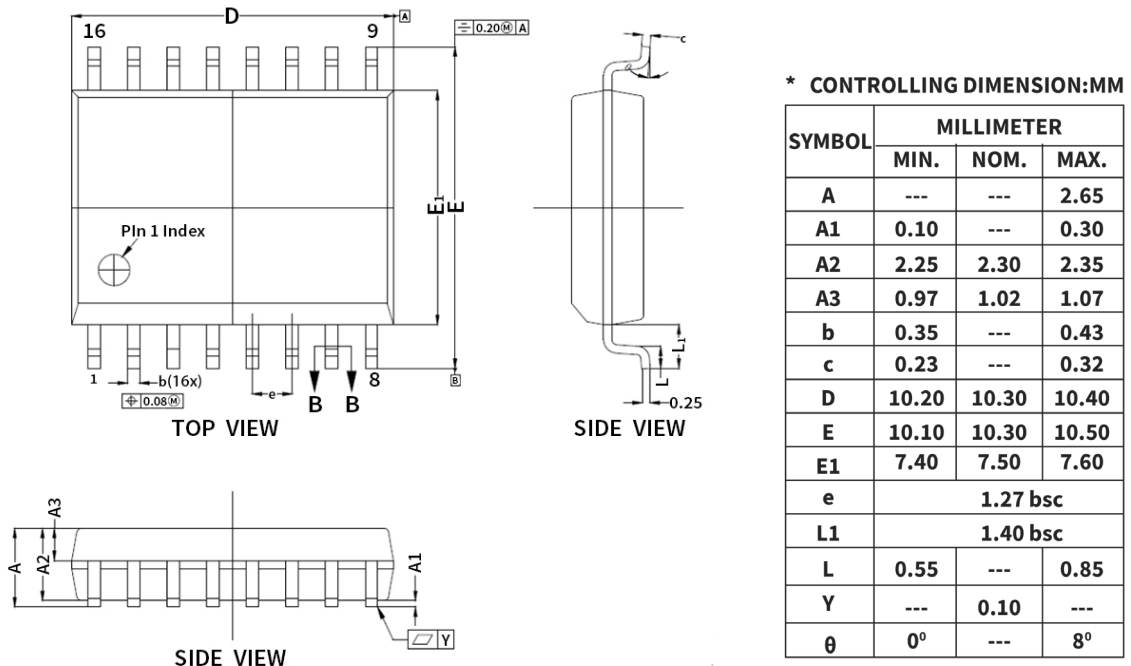


Figure 9.1 SOP16(300mil) Package Shape and Dimension in millimeters

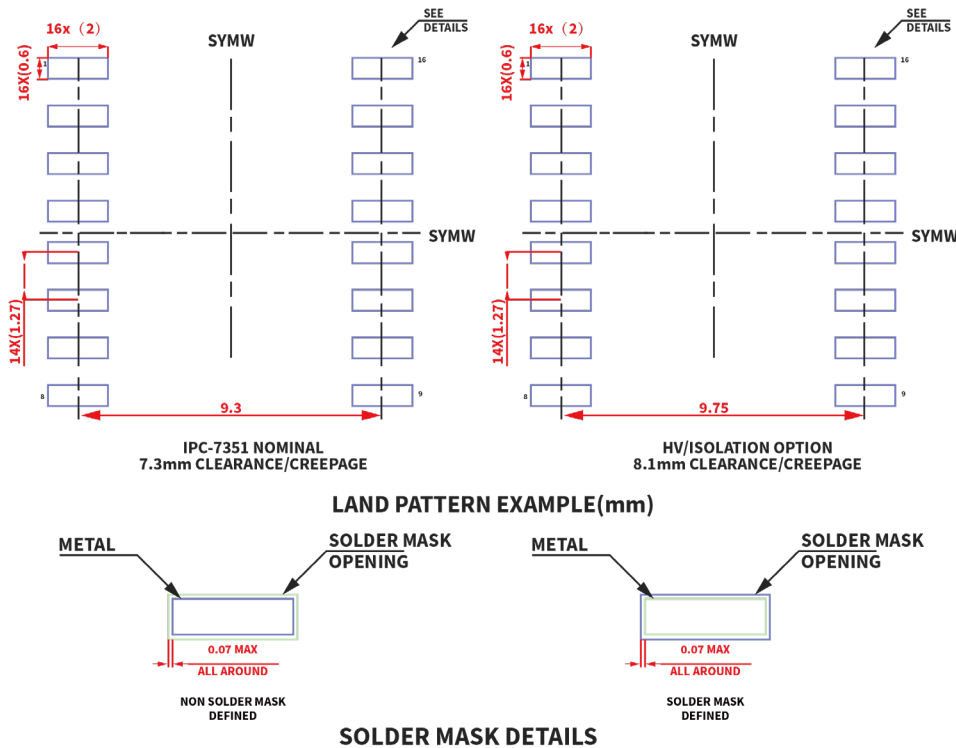
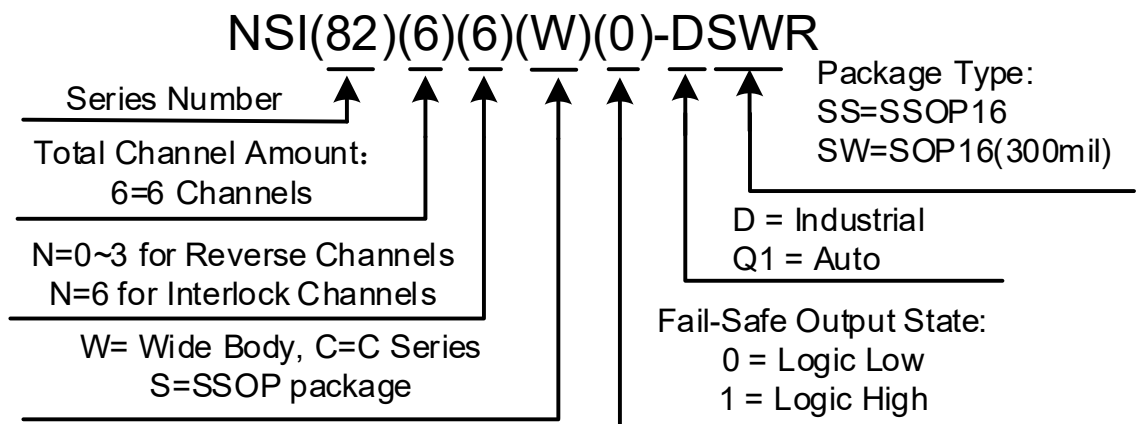


Figure 9.2 SOP16(300mil) Package Board Layout Example

### 10. Ordering Information

Part Number	Isolation Rating (kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	MSL	Package Type	Package Drawing	SPQ
NSI8266C0-DSWR	5	6	0	30	Low	-40 to 125°C	2	SOP16 (300mil)	SOW16	1000

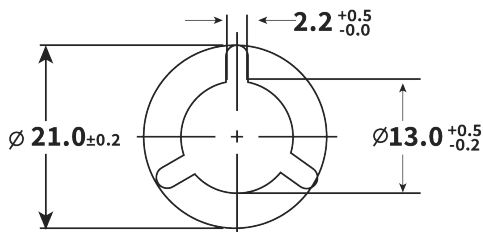
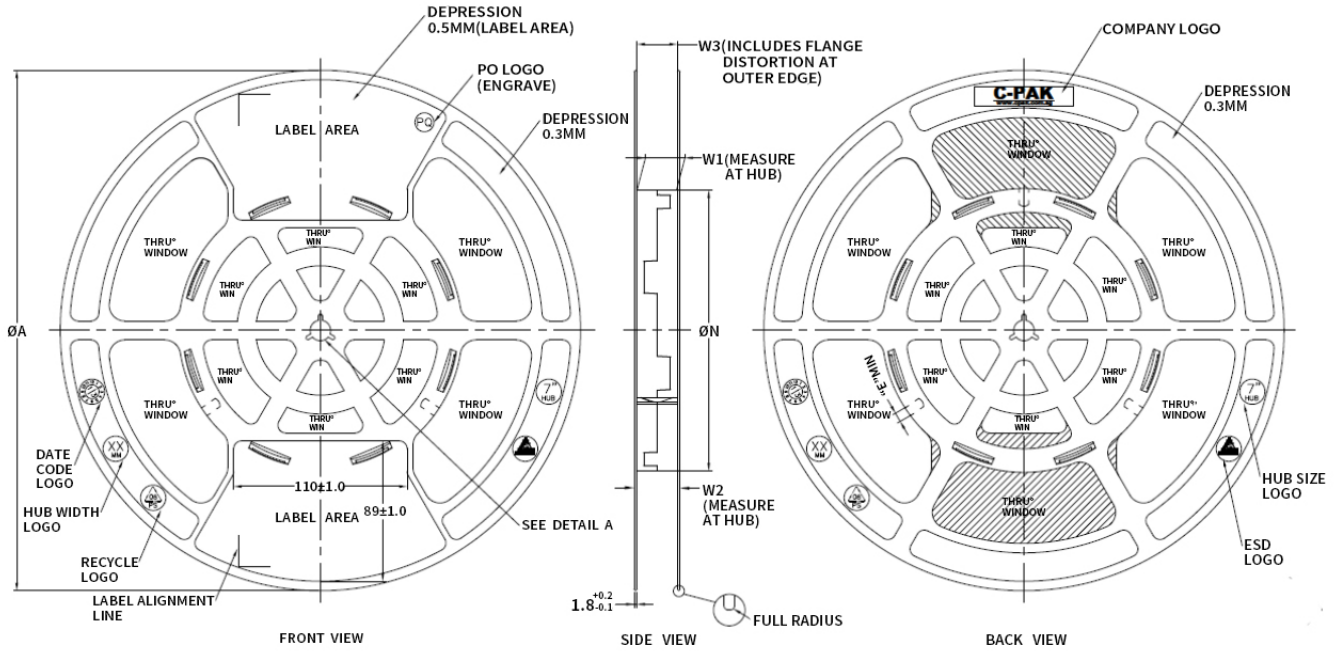
**Part Number Rule:**



### 11. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NSI8266C0	tbd	tbd	tbd	tbd

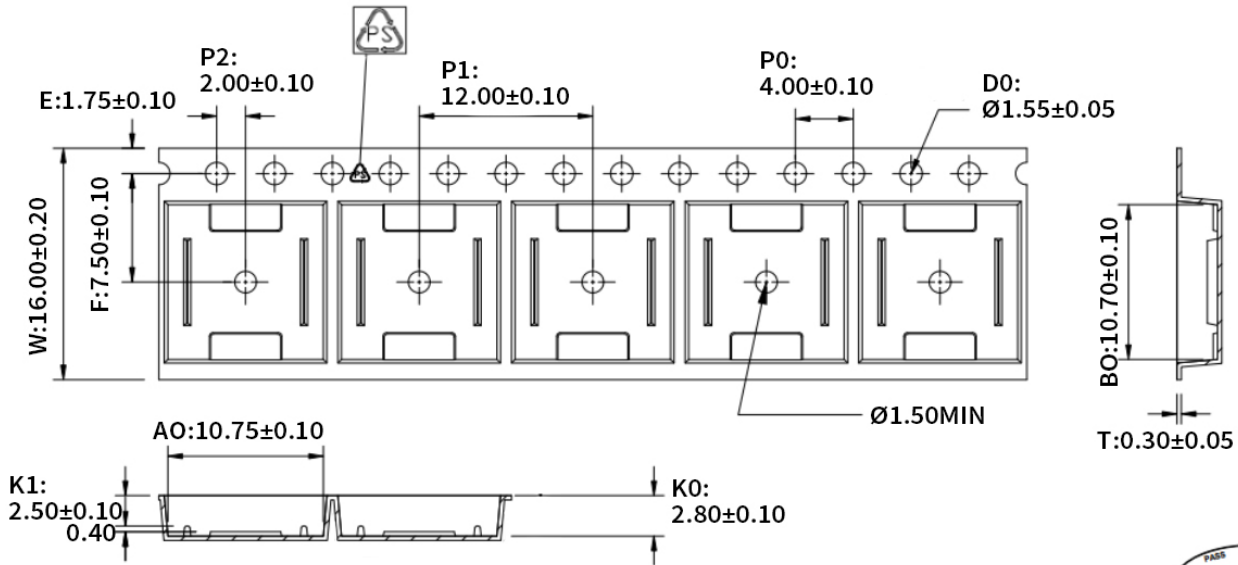
## 12. Tape and Reel Information



PRODUCT SPECIFICATION						
TAPE WIDTH	$\varnothing A \pm 2.0$	$\varnothing N \pm 2.0$	W1	W2 (Max)	W3	E (MIN)
08MM	330	178	$8.4^{+1.5}_{-0.0}$	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	$12.4^{+2.0}_{-0.0}$	18.4		5.5
16MM	330	178	$16.4^{+2.0}_{-0.0}$	22.4		5.5
24MM	330	178	$24.4^{+2.0}_{-0.0}$	30.4		5.5
32MM	330	178	$32.4^{+2.0}_{-0.0}$	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW $10^{12}$	ANTISTATIC	ALL TYPES
B	$10^6$ TO $10^{11}$	STATIC DISSIPATIVE	BLACK ONLY
C	$10^5$ & BELOW $10^5$	CONDUCTIVE(GENERIC)	BLACK ONLY
E	$10^9$ TO $10^{11}$	ANTISTATIC(COATED)	ALL TYPES

Figure 12.1 Reel Information (for all packages)



1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.20$ .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness:  $0.30 \pm 0.05$ mm.
6. Packing length per 22" reel: 378 Meters. (Rewind N=122 )
7. Component load per 13" reel: 1000 pcs.
8. Surface resistivity:  $10^5 \sim 10^{10} \Omega/\square$

W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

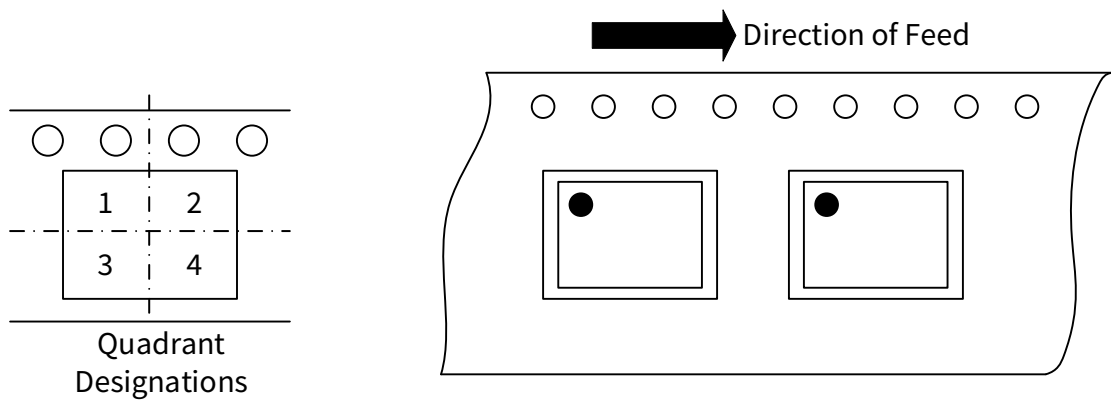


Figure 12.2 Tape Information of SOP16(300mil)

### 13. Revision History

Revision	Description	Date
1.0	Initial version	2022/5/16
1.1	Delete Isolation barrier life: >60 years, change DTI to 28, change High CMTI from 200 to 100, add Tj, change sop16 package information	2022/9/29
1.2	Update Part Number Rule	2024/1/16
1.3	Correct formatting; Update max data rate from 100Mbps to 30Mbps; Update max propagation delay from 15ns to 50ns; Update Safety certification info throughout the document. Update part number rule.	2026/1/28

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