NOVOSENSE
纳芯微电子

NSI823x-Q1

High Reliability Reinforced Triple-Channel Digital Isolators

Datasheet (EN) 1.2

Product Overview

The NSI823x devices are high reliability triple-channel digital isolators. The NSI823x device is safety certified by UL1577 support several insulation withstand voltages (3kVrms, 5kVrms), while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI823x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 250kV/us. The NSI823x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI823x device supports to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use. AEC-Q100 (Grade 1) option is provided for all devices.

Key Features

- Up to 5000V_{rms} Insulation voltage
- Data rate: DC to 150Mbps
- Power supply voltage: 2.5V to 5.5V
- AEC-Q100 Grade 1 available for all devices
- High CMTI: 250kV/us
- Chip level ESD: HBM: ±8kV
- Robust Electromagnetic Compatibility (EMC)
  - – System-Level ESD, EFT, and Surge Immunity
  - – Low Emissions
- Default output high level or low-level option
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <15ns
- Operation temperature: -40℃~125℃
- RoHS-compliant packages:
  - – SOP16(300mil)
  - – SSOP16

Safety Regulatory Approvals

- UL recognition: up to 5000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1-2022
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor control
- For automotive application

Device Information

Part Number	*Package*	*Body Size*
NSI823x-Q1SWR	SOP16(300mil)	10.30mm × 7.50mm
NSI823x-Q1SSR	SSOP16	4.90mm × 3.90mm

Functional Block Diagrams

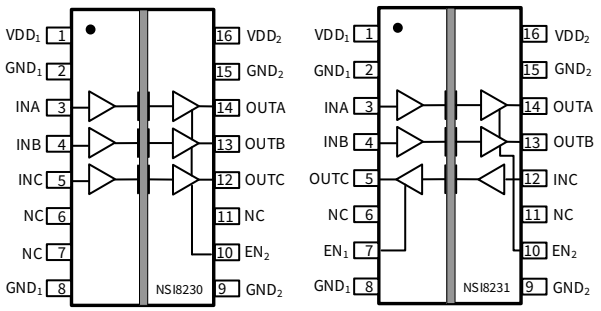

Figure 1. NSI823x Block Diagram

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1. Pin Configuration and Functions

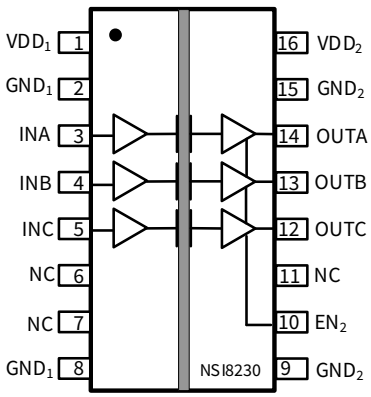


Figure 1.1 NSI8230 Package

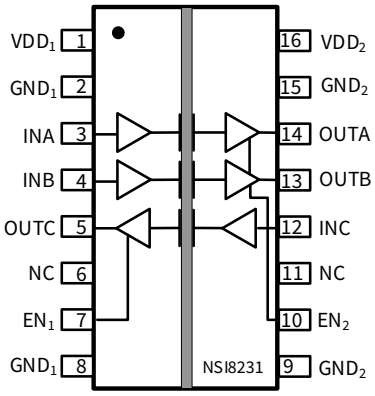


Figure 1.2 NSI8231 Package

Table 1.1 NSI8230/ NSI8231 Pin Configuration and Description

NSI8230 PIN NO.	*NSI8231 PIN NO.*	*SYMBOL*	*FUNCTION*
1	1	VDD_1	Power Supply for Isolator Side 1
2	2	GND_1	Ground 1, the ground reference for Isolator Side 1
3	3	INA	Logic Input A
4	4	INB	Logic Input B
5	12	INC	Logic Input C
6	6	NC	No Connection.
7	7	NC/ EN_1	No Connection. or Output Enable 1. Active high logic input. When EN_1 is high or NC, the output of Side 1 is enabled. When EN_1 is low, the output of Side 1 is disabled to high impedance state.
8	8	GND_1	Ground 1, the ground reference for Isolator Side 1
9	9	GND_2	Ground 2, the ground reference for Isolator Side 2
10	10	EN_2	Output Enable 2. Active high logic input. When EN_2 is high or NC, the output of Side 2 is enabled. When EN_2 is low, the output of Side 2 is disabled to high impedance state.
11	11	NC	No Connection.
12	5	OUTC	Logic Output C
13	13	OUTB	Logic Output B
14	14	OUTA	Logic Output A

NSI8230 PIN NO.	NSI8231 PIN NO.	SYMBOL	FUNCTION
15	15	GND2	Ground 2, the ground reference for Isolator Side 2
16	16	VDD2	Power Supply for Isolator Side 2

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	VINA, VINB, VINC	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Output Voltage	VOUTA, VOUTB, VOUTC	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Input/Output Pulse Voltage	VINA, VINB, VINC, VOUTA, VOUTB, VOUTC	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Output current	I_o	-15		15	mA	
Operating Temperature	T_{opr}	-40		125	℃	
Junction Temperature	T_J			150	℃	
Storage Temperature	T_{stg}	-65		150	℃	
Electrostatic discharge	HBM			±8000	V	
	CDM			±2000	V	

3. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit
Power Supply Voltage	VDD1, VDD2	2.5		5.5	V
Operating Temperature	T_{opr}	-40		125	℃
High Level Input Voltage	VIH	2			V
Low Level Input Voltage	VIL			0.8	V
Data rate	DR			150	Mbps

4. Thermal Information

Parameters	*Symbol*	*SOP16(300mil)*	*SSOP16*	*Unit*
IC Junction-to-Air Thermal Resistance	θ_{JA}	78.9	140	℃/W
Junction-to-case (top) thermal resistance	$\theta_{JC(top)}$	41.6	54.4	℃/W
Junction-to-board thermal resistance	θ_{JB}	43.6	51.9	℃/W

5. Specifications

5.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, T_A=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, T_A = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power on Reset	VDD_{POR}		2.2		V	POR threshold as during power-up
	VDD_{HYS}		0.1		V	POR threshold Hysteresis
High Level Input Voltage	V_{IH}	2			V	
Low Level Input Voltage	V_{IL}			0.8	V	
High Level Output Voltage	V_{OH}	VDD-0.4			V	I_{OH} = - 4mA
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 4mA
Output Impedance	R_{out}		50		ohm	
Input Pull high or low Current	I_{pull}		8	15	uA	
Start Up Time after POR	t_{rbs}		10		us	
Common Mode Transient Immunity	CMTI	±200	±250		kV/us	See Figure 5.11 , C_L = 15pF

5.2. Supply Current Characteristics – 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, T_A=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V,** T_A = 25℃)

Parameters	*Symbol*	*Min*	*Typ.*	*Max*	*Unit*	*Comments*
Supply current	**NSI8230**					
	I_{DD1}(Q0)		1.24	2.04	mA	All Input 0V for NSI8230x0 Or All Input at supply for NSI8230x1
	I_{DD2}(Q0)		2.94	4.84	mA	
	I_{DD1}(Q1)		4.25	7.02	mA	All Input at supply for NSI8230x0 Or All Input 0V for NSI8230x1
	I_{DD2}(Q1)		3.00	4.95	mA	
	I_{DD1}(1M)		2.43	4.00	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		2.45	4.27	mA	
	I_{DD1}(10M)		2.92	4.82	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		3.06	5.99	mA	
	I_{DD1}(100M)		3.97	7.93	mA	All Input with 100Mbps, C_L=15pF
	I_{DD2}(100M)		12.47	29.28	mA	
	NSI8231					
	I_{DD1}(Q0)		1.66	2.74	mA	All Input 0V for NSI8231x0 Or All Input at supply for NSI8231x1
	I_{DD2}(Q0)		2.51	4.14	mA	
	I_{DD1}(Q1)		3.69	6.09	mA	All Input at supply for NSI8231x0 Or All Input 0V for NSI8231x1
	I_{DD2}(Q1)		3.56	5.87	mA	
	I_{DD1}(1M)		2.31	3.81	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		2.40	4.17	mA	
	I_{DD1}(10M)		2.75	4.53	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		3.40	5.61	mA	
	I_{DD1}(100M)		6.69	13.38	mA	All Input with 100Mbps, C_L= 15pF
	I_{DD2}(100M)		12.47	24.94	mA	

5.3. Supply Current Characteristics –3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, T_A=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 3.3V, VDD2 = 3.3V, T_A = 25℃)

Parameters	*Symbol*	*Min*	*Typ.*	*Max*	*Unit*	*Comments*
Supply current	**NSI8230**					
	I_{DD1}(Q0)		1.19	1.96	mA	All Input 0V for NSI8230x0 Or All Input at supply for NSI8230x1
	I_{DD2}(Q0)		2.87	4.74	mA	
	I_{DD1}(Q1)		4.20	6.93	mA	All Input at supply for NSI8230x0 Or All Input 0V for NSI8230x1
	I_{DD2}(Q1)		2.93	4.83	mA	
	I_{DD1}(1M)		2.38	3.92	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		2.37	4.14	mA	
	I_{DD1}(10M)		2.81	4.64	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		2.66	5.27	mA	
	I_{DD1}(100M)		3.30	6.59	mA	All Input with 100Mbps, C_L=15pF
	I_{DD2}(100M)		10.01	20.01	mA	
	NSI8231					
	I_{DD1}(Q0)		1.61	2.66	mA	All Input 0V for NSI8231x0 Or All Input at supply for NSI8231x1
	I_{DD2}(Q0)		2.45	4.04	mA	
	I_{DD1}(Q1)		3.64	6.00	mA	All Input at supply for NSI8231x0 Or All Input 0V for NSI8231x1
	I_{DD2}(Q1)		3.49	5.76	mA	
	I_{DD1}(1M)		2.25	3.71	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		2.34	4.06	mA	
	I_{DD1}(10M)		2.53	4.18	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		3.00	4.94	mA	
	I_{DD1}(100M)		5.42	10.84	mA	All Input with 100Mbps, C_L= 15pF
	I_{DD2}(100M)		10.01	20.01	mA	

5.4. Supply Current Characteristics–2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, T_A=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 2.5V, VDD2 = 2.5V, T_A = 25℃)

Parameters	*Symbol*	*Min*	*Typ.*	*Max*	*Unit*	*Comments*
Supply current	**NSI8230**					
	I_{DD1}(Q0)		1.17	1.92	mA	All Input 0V for NSI8230x0 Or All Input at supply for NSI8230x1
	I_{DD2}(Q0)		2.83	4.66	mA	
	I_{DD1}(Q1)		4.14	6.83	mA	All Input at supply for NSI8230x0 Or All Input 0V for NSI8230x1
	I_{DD2}(Q1)		2.87	4.74	mA	
	I_{DD1}(1M)		2.30	3.80	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		2.31	4.05	mA	
	I_{DD1}(10M)		2.70	4.46	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		2.46	4.90	mA	
	I_{DD1}(100M)		2.85	5.70	mA	All Input with 100Mbps, C_L=15pF
	I_{DD2}(100M)		8.22	16.44	mA	
	NSI8231					
	I_{DD1}(Q0)		1.58	2.61	mA	All Input 0V for NSI8231x0 Or All Input at supply for NSI8231x1
	I_{DD2}(Q0)		2.41	3.98	mA	
	I_{DD1}(Q1)		3.58	5.90	mA	All Input at supply for NSI8231x0 Or All Input 0V for NSI8231x1
	I_{DD2}(Q1)		3.43	5.67	mA	
	I_{DD1}(1M)		2.18	3.60	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		2.29	3.95	mA	
	I_{DD1}(10M)		2.39	3.95	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		2.80	4.61	mA	
	I_{DD1}(100M)		4.53	9.05	mA	All Input with 100Mbps, C_L= 15pF
	I_{DD2}(100M)		8.22	16.44	mA	

5.5. Switching Characteristics - 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, T_A=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V,** T_A = 25℃)

Parameters	*Symbol*	*Min*	*Typ.*	*Max*	*Unit*	*Comments*
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	2.5	6.54	15	ns	See Figure 5.9 , C_L = 15pF
	t_{PHL}	2.5	8.30	15	ns	See Figure 5.9 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 5.9 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 5.9 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 5.9 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	
Disable high to Tri-State	t_{PHZ}		10.0	30	ns	See Figure 5.10 , C_L = 15pF, R_L=1k
Enable to Data high Valid	t_{PZH}		8.3	30	ns	See Figure 5.10 , C_L = 15pF, R_L=1k
Disable low to Tri-State	t_{PLZ}		10.2	30	ns	See Figure 5.10 , C_L = 15pF, R_L=1k
Enable to Data low Valid	t_{PZL}		8.6	30	ns	See Figure 5.10 , C_L = 15pF, R_L=1k

5.6. Switching Characteristics - 3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, T_A=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V,** T_A = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	2.5	7.5	15	ns	See Figure 5.9 , C_L = 15pF
	t_{PHL}	2.5	8.7	15	ns	See Figure 5.9 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 5.9 , C_L = 15pF

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Rising Time	t_r			5.0	ns	See Figure 5.9 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 5.9 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	
Disable high to Tri-State	t_{PHZ}		11.6	30	ns	See Figure 5.10 , C_L = 15pF, R_L=1k
Enable to Data high Valid	t_{PZH}		11.7	30	ns	See Figure 5.10 , C_L = 15pF, R_L=1k
Disable low to Tri-State	t_{PLZ}		14.5	30	ns	See Figure 5.10 , C_L = 15pF, R_L=1k
Enable to Data low Valid	t_{PZL}		11.8	30	ns	See Figure 5.10 , C_L = 15pF, R_L=1k

5.7. Switching Characteristics - 2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, T_A=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 2.5V, VDD2 = 2.5V,** T_A = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	2.5	9.0	15	ns	See Figure 5.9 , C_L = 15pF
	t_{PHL}	2.5	9.3	15	ns	See Figure 5.9 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 5.9 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 5.9 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 5.9 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	
Disable high to Tri-State	t_{PHZ}		12.2	30	ns	See Figure 5.10 , C_L = 15pF, R_L=1k
Enable to Data high Valid	t_{PZH}		17.0	30	ns	See Figure 5.10 , C_L = 15pF, R_L=1k
Disable low to Tri-State	t_{PLZ}		17.2	30	ns	See Figure 5.10 , C_L = 15pF, R_L=1k

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Enable to Data low Valid	t_{PZL}		17.8	30	ns	See Figure 5.10 , C_L = 15pF, R_L=1k

5.8. Typical Performance Characteristics

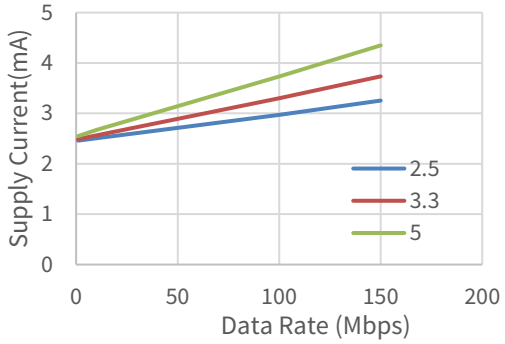


Figure 5.1 NSI8130 VDD1 Supply Current vs Data Rate

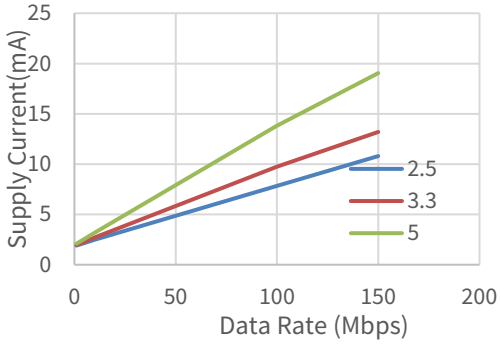


Figure 5.2 NSI8130 VDD2 Supply Current vs Data Rate

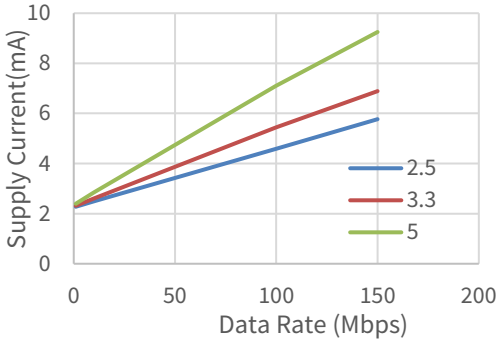


Figure 5.3 NSI8131 VDD1 Supply Current vs Data Rate

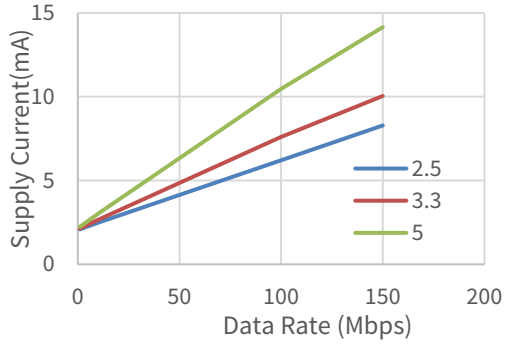


Figure 5.4 NSI8131 VDD2 Supply Current vs Data Rate

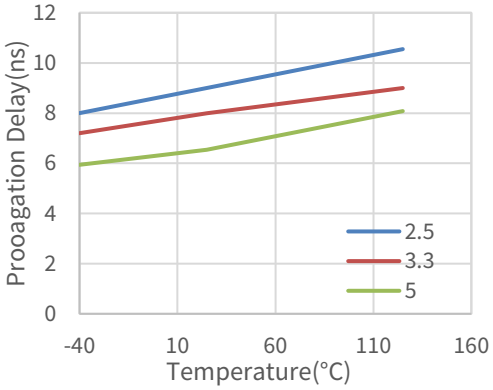


Figure 5.5 Rising Edge Propagation Delay Vs Temp

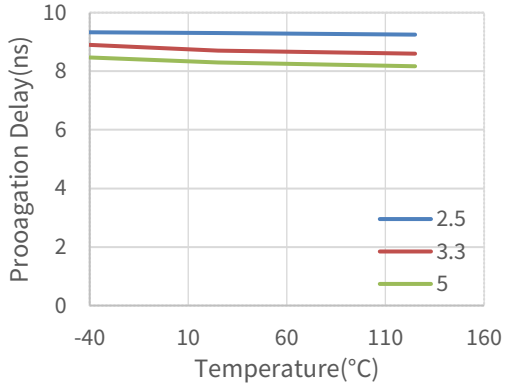


Figure 5.6 Falling Edge Propagation Delay Vs Temp

5.9. Parameter Measurement Information

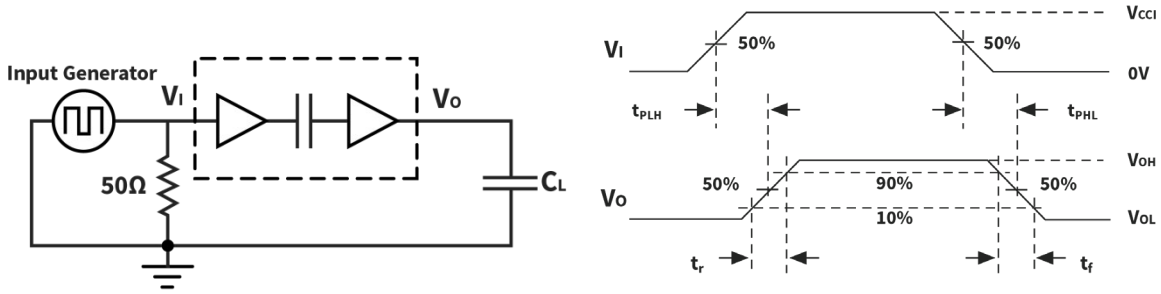


Figure 5.7 Switching Characteristics Test Circuit and Waveform

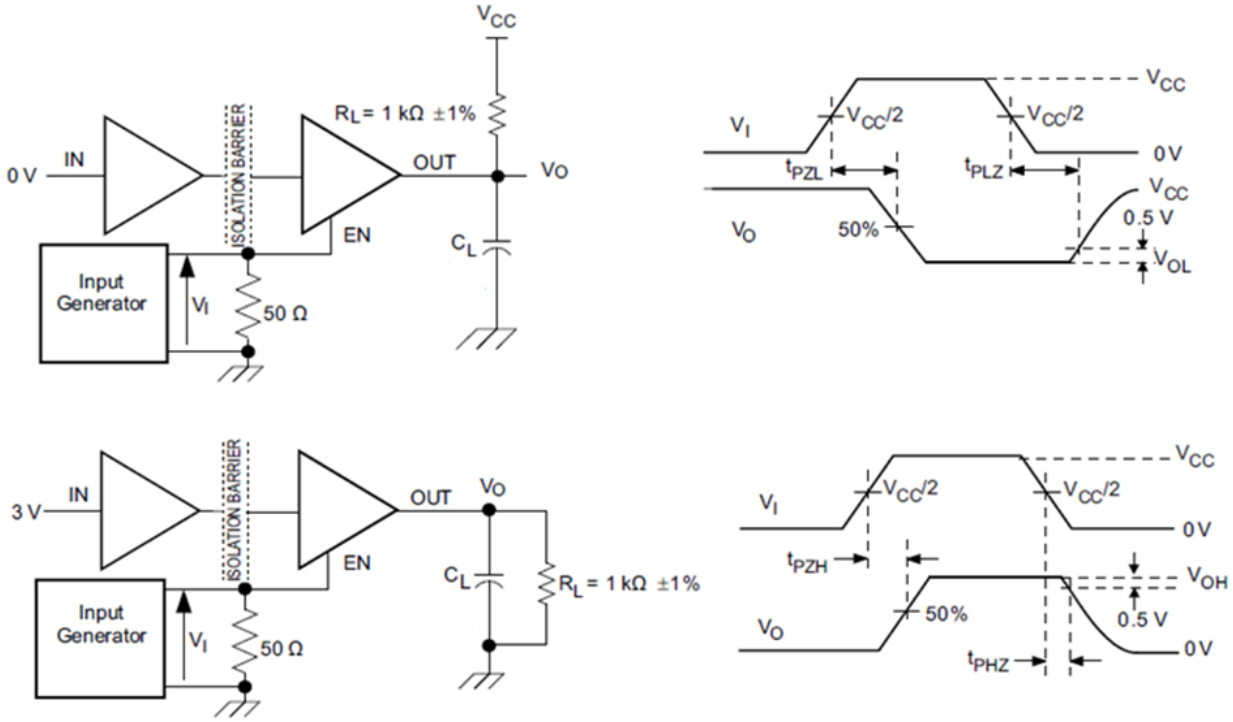


Figure 5.8 Enable/Disable Propagation Delay Time Test Circuit and Waveform

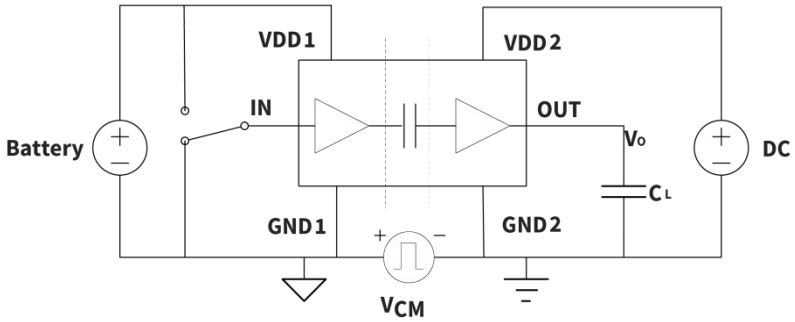


Figure 5.9 Common-Mode Transient Immunity Test Circuit

6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

Parameters	*Symbol*	*Value*		*Unit*	*Comments*
		SOP16 (300mil)	SSOP16		
Minimum External Clearance	CLR	8	3.9	mm	IEC 60664-1:2007
Minimum External Creepage	CPG	8	3.9	mm	IEC 60664-1:2007
Distance Through Insulation	DTI	28		μm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600		V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I			IEC 60664-1

Description	*Test Condition*	*Value*	
		SOP16 (300mil)	SSOP16
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	I to IV	I to IV
	For Rated Mains Voltage ≤ 300Vrms	I to IV	I to III
	For Rated Mains Voltage ≤ 600Vrms	I to IV	I to II
	For Rated Mains Voltage ≤ 1000Vrms	I to III	I
Climatic Classification		40/125/21	
Pollution Degree per DIN VDE 0110		2	

6.2. Insulation Characteristics

Description	*Test Condition*	*Symbol*	*Value*		*Unit*
			SOP16 (300mil)	SSOP16	
Maximum repetitive isolation voltage		V_{IORM}	2121	565	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	1500	400	V_{RMS}
	DC Voltage		2121	565	V_{DC}

Description	*Test Condition*	*Symbol*	*Value*		*Unit*
			SOP16 (300mil)	SSOP16	
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, Vini=V_{IOTM}, t_{ini} = 60 s , $V_{pd(m)}$=1.2*V_{IORM}, t_m=10s.	q_{pd}	<5	\	pC
	Method a, after environmental tests subgroup 1, Vini=V_{IOTM}, t_{ini}=60s ,$V_{pd(m)}$=1.6*V_{IORM}, t_m=10s				pC
	Method b, routine test (100% production) and preconditioning (type test);V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd\ (m)}$=1.875*V_{IORM}, t_m=1s （method b1） or $V_{pd(m)}$=Vini, t_m=t_{ini}(method b2)				pC
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, Vini=V_{IOTM}, t_{ini} = 60 s , $V_{pd(m)}$=1.2*V_{IORM}, t_m=10s.	q_{pd}	\	<5	pC
	Method a, after environmental tests subgroup 1, Vini=V_{IOTM}, t_{ini}=60s ,$V_{pd(m)}$=1.3*V_{IORM}, t_m=10s				pC
	Method b, routine test (100% production) and preconditioning (type test);V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd\ (m)}$=1.5*V_{IORM}, t_m=1s （method b1） or $V_{pd(m)}$=Vini, t_m=t_{ini}(method b2)				pC
Maximum transient isolation voltage	t = 60 sec	V_{IOTM}	8000	5000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50-us waveform per IEC62368-1	V_{IMP}	6250	5384	V_{PEAK}

Description	Test Condition	Symbol	Value		Unit
			SOP16 (300mil)	SSOP16	
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{IOSM} \geqslant V_{IMP} \times 1.3$	V_{IOSM}	10000	7000	V_{PEAK}
Isolation resistance	V_{IO} =500V, T_{amb}=25℃	R_{IO}	$>10^{12}$	$>10^{12}$	Ω
	V_{IO} =500V, 100℃ ≤ T_{amb} ≤ 125℃	R_{IO}	$>10^{11}$	$>10^{11}$	Ω
	V_{IO} =500V, T_{amb}=T_s	R_{IO}	$>10^{9}$	$>10^{9}$	Ω
Isolation capacitance	f = 1MHz	C_{IO}	0.8	0.8	pF
UL1577					
Insulation voltage per UL	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	V_{ISO}	5000	3000	V_{RMS}

6.3. Safety-Limiting Values

Reinforced isolation safety-limiting values as outlined in VDE 0884-17 of NSI823x-Q1SWR (SOP16(300mil))

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{\theta JA}$ = 78.9 °C/W[1)], T_J = 150 °C, T_A = 25 °C	1584	mW
Safety Supply Current	$R_{\theta JA}$ = 78.9 °C/W[1)], V_I = 5V, T_J = 150 °C, T_A = 25 °C	316.8	mA
Safety Temperature[2)]		150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP16(300mil) package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

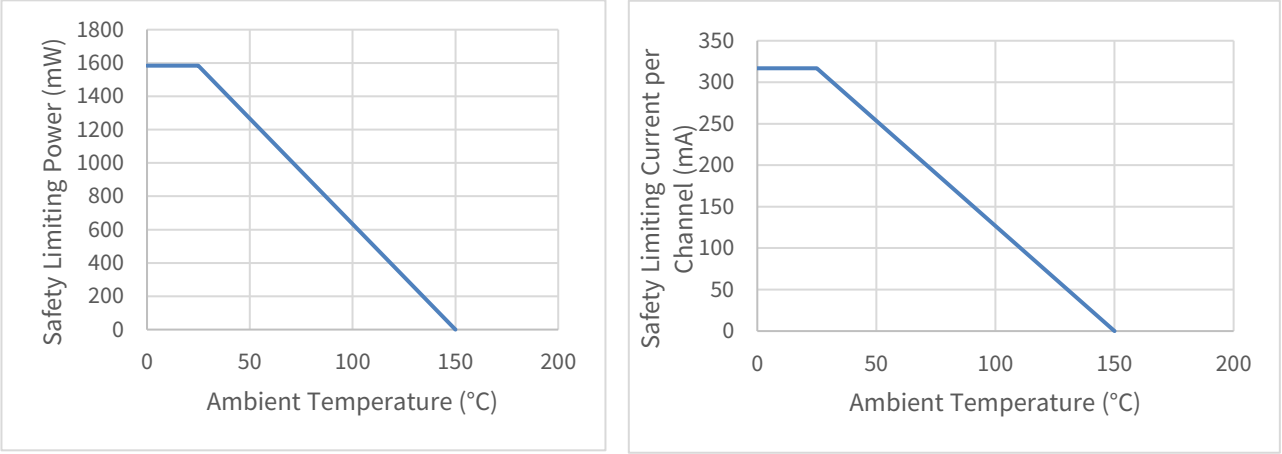


Figure 6.1 NSI823xW Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

Basic isolation safety-limiting values as outlined in VDE 0884-17 of NSI823x-DSSR (SSOP16)

Description	*Test Condition*	*Value*	*Unit*
Safety Supply Power	$R_{\theta JA}$ = 140°C/W[1)], T_J = 150 °C, T_A = 25 °C	880	mW
Safety Supply Current	$R_{\theta JA}$ = 140°C/W[1)], V_I = 5V, T_J = 150 °C, T_A = 25 °C	176	mA
Safety Temperature[2)]		150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SSOP16 package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

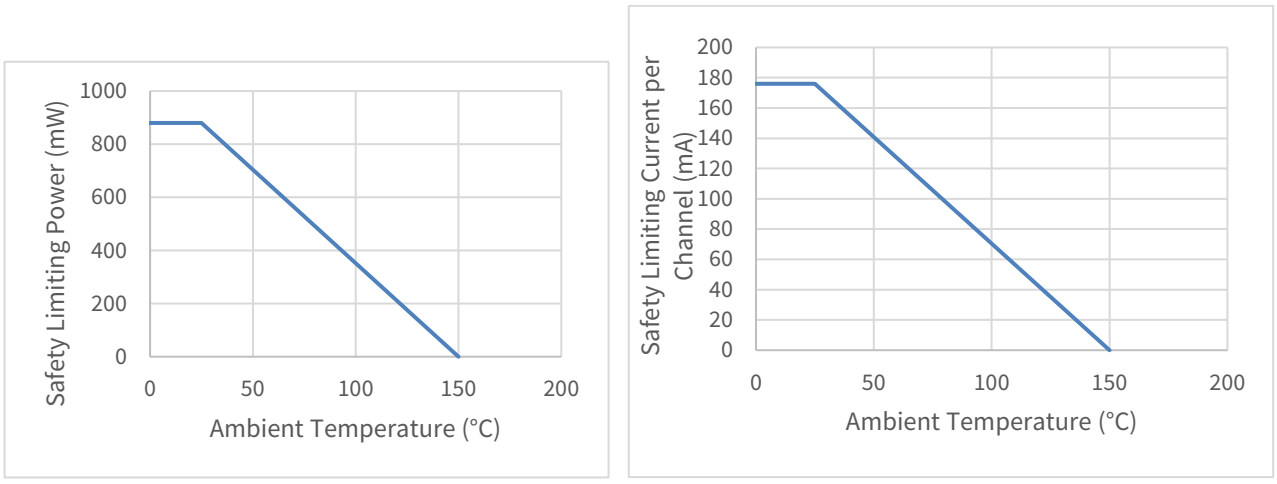


Figure 6.2 NSI823xS Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

6.4. Regulatory Information

The NSI823xW-Q1SWR are approved or pending approval by the organizations listed in table.

CUL		*VDE*	*CQC*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1-2022
Single Protection, 5000V_{rms} Isolation voltage	Single Protection, 5000V_{rms} Isolation voltage	Reinforce Insulation 2121Vpeak, V_{IOSM}=6250Vpeak	Reinforced insulation
File (E500602)	File (E500602)	File (40052820)	File (CQC20001264939)

The NSI823xS-Q1SSR are approved or pending approval by the organizations listed in table.

CUL		*VDE*	*CQC*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1-2022
Single Protection, 3000Vrms Isolation voltage	Single Protection, 3000Vrms Isolation voltage	Basic Insulation 565Vpeak, V_{IOSM}=5384Vpeak	Basic insulation
File (E500602)	File (E500602)	File (40057024)	File (pending)

7. Function Description

7.1. Overview

The NSI823x is a Triple-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NSI823x devices are high reliability Triple-channel digital isolator with AEC-Q100 qualified. The NSI823x device is safety certified by UL1577 support 5kV$_{rms}$ insulation withstand voltages, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI823x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 250kV/us. The NSI823x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI823x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

The NSI823x has a default output status when VDDIN is unready and VDDOUT is ready as shown in Table 7.1, which helps for diagnosis when power is missing at the transmitter side. The output B follows the same status with the input A after powering up.

Table 7.1 Output status vs. power status

Input	***EN$_x$***	***VDDIN status***	***VDDOUT status***	***Output***	***Comment***
H	H or NC	Ready	Ready	H	Normal operation.
L	H or NC	Ready	Ready	L	
X	L	Ready	Ready	Z	Output Disabled, the output is high impedance
X	H or NC	Unready	Ready	L(NSI823xW0) H(NSI823xW1)	The output follows the same status with the input after input side VDDIN is powered on.
X	L	Unready	Ready	Z	Output Disabled, the output is high impedance
X	X	Ready	Unready	X	The output follows the same status with the input after output side VDDOUT is powered on.
Note: H=Logic high; L=Logic low; X=Logic low or logic high VDDIN is input side power; VDDOUT is output side power.					

7.2. OOK Modulation

NSI823x is based on a capacitive isolation barrier technique and the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, as shown in Fig.1, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI.

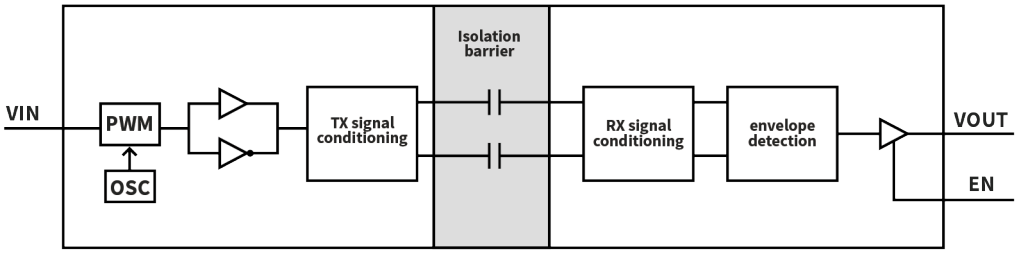


Figure 7.1 Single Channel Function Block Diagram

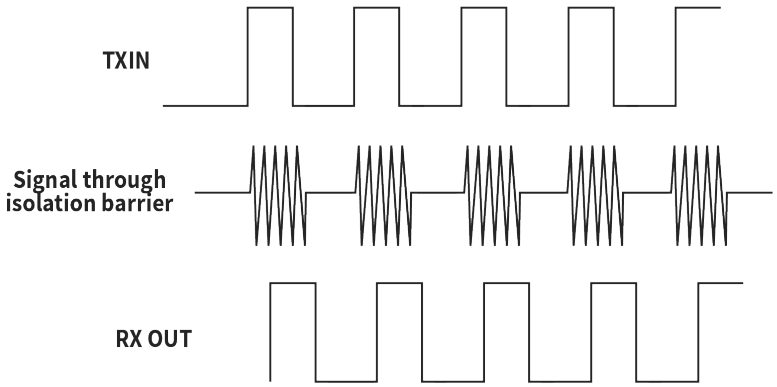


Figure 7.2 OOK Modulation

8. Application Note

8.1. Typical Application Circuit

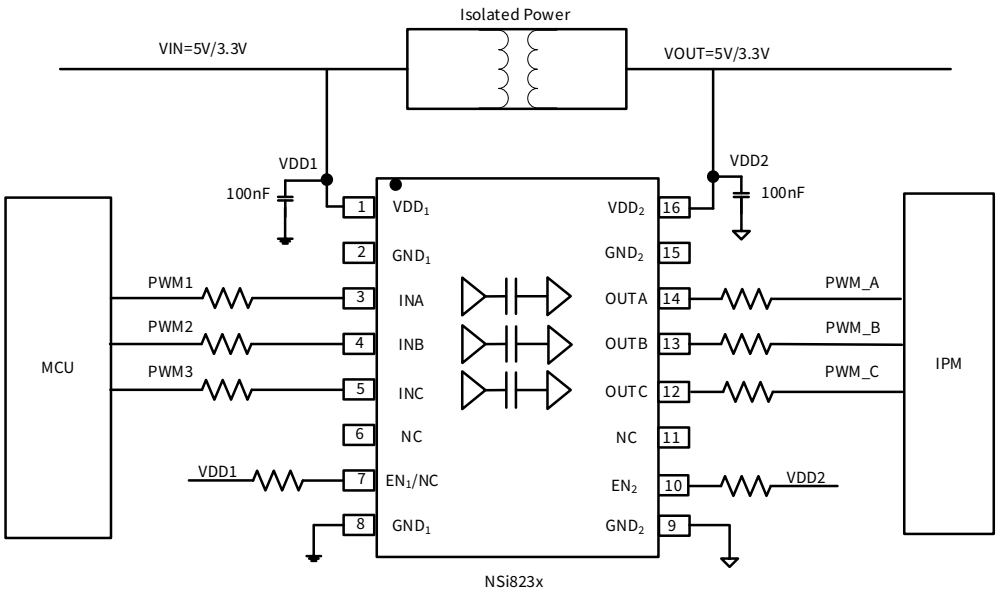


Figure 8.1 Typical PWM isolation circuit for IPM

8.2. PCB Layout

The NSI823x requires a 0.1 µF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. Figure 8.2 to Figure 8.3 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω, ±40%. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

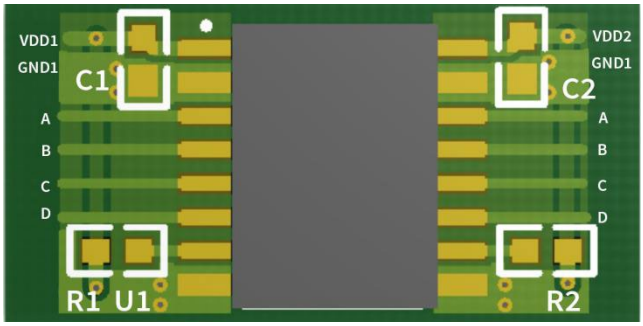


Figure8.2 Recommended PCB Layout — Top Layer

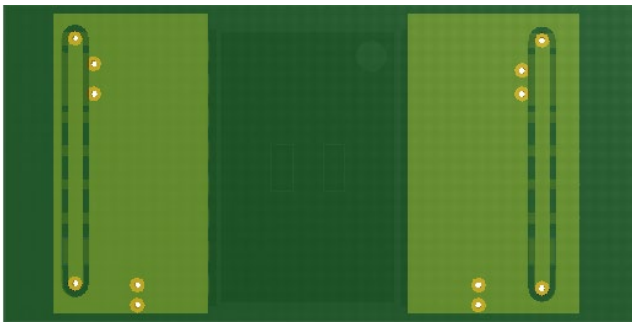


Figure8.3 Recommended PCB Layout — Bottom Layer

8.3. High Speed Performance

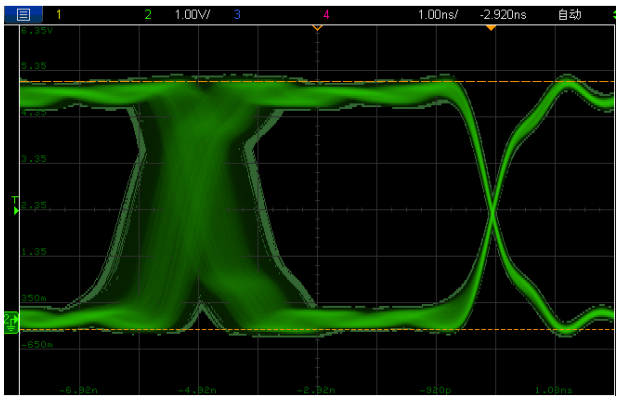


Figure8.4 Eye Diagram

8.4. Typical Supply Current Equations

The typical supply current of NSI823x can be calculated using below equations. I_{DD1} and I_{DD2} are typical supply currents measured in mA, f is data rate measured in Mbps, C_L is the capacitive load measured in pF

NSI8230:

I_{DD1} = 0.19 *a1+1.45*b1+0.82*c1.

I_{DD2} = 1.36+ VDD2*f* C_L *c1*10^{-9}

When a1 is the channel number of default state input at side 1, b1 is the channel number of non-default state input at side 1, c1 is the channel number of switch signal input at side 1.

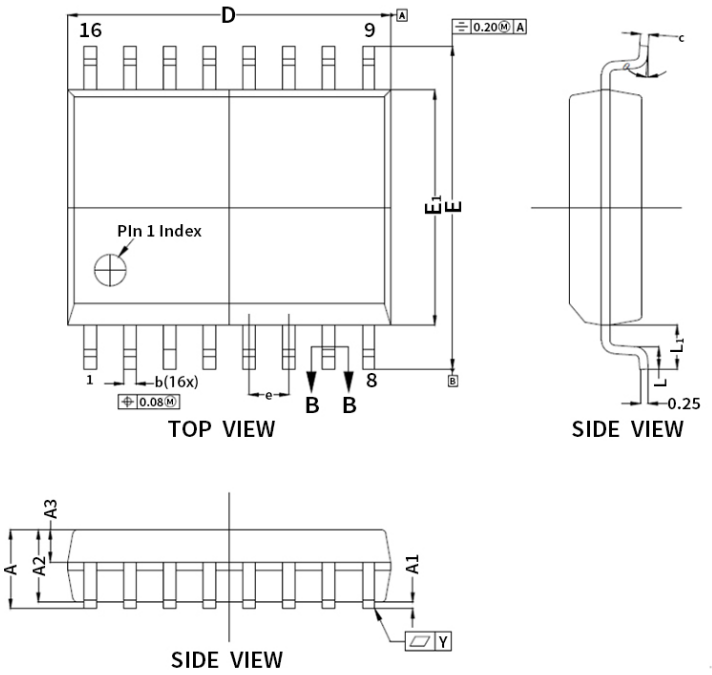
NSI8231:

I_{DD1} = 0.87 +1.26*b1+0.63*c1+ VDD1*f* C_L *c2*10^{-9}

I_{DD2} = 0.87 +1.26*b2+0.63*c2+ VDD2*f* C_L *c1*10^{-9}

When b1 is the channel number of non-default state input at side 1, c1 is the channel number of switch signal input at side 1, b2 is the channel number of non-default state input at side 2, c2 is the channel number of switch signal input at side 2.

9. Package Information



* CONTROLLING DIMENSION:MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 9.1 SOP16(300mil) Package Shape and Dimension in millimeters

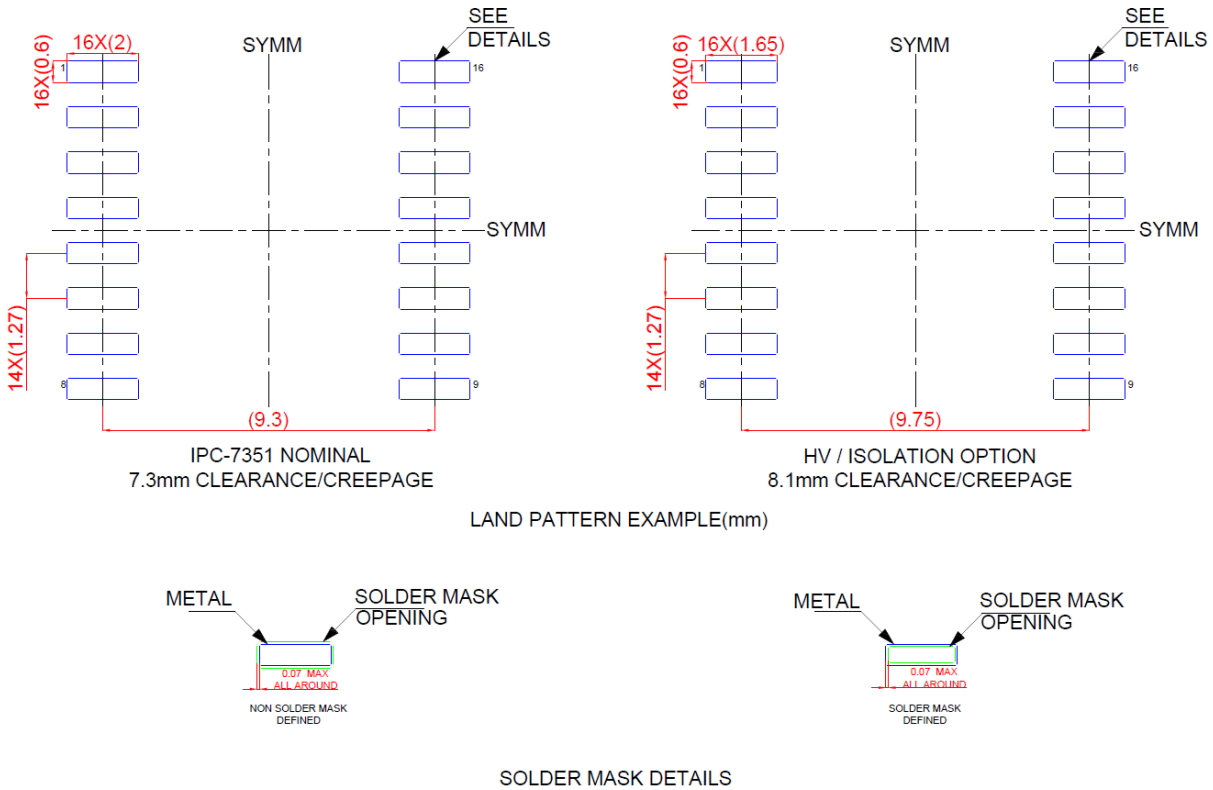
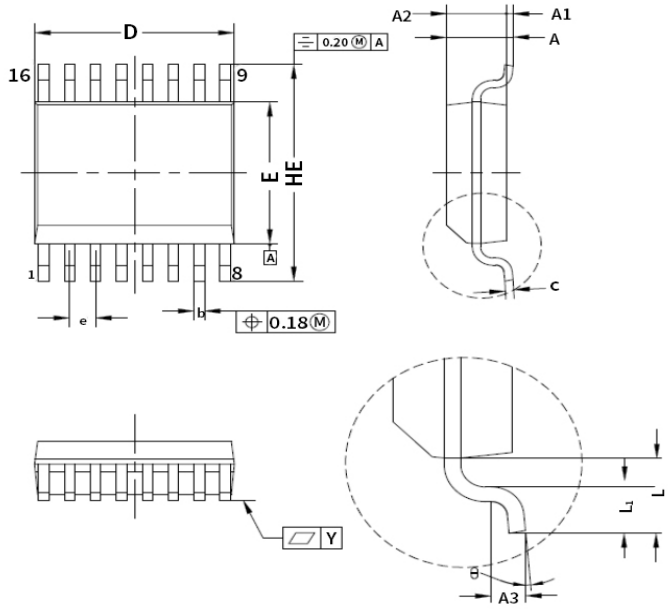


Figure 9.2 SOP16(300mil) Package Board Layout Example

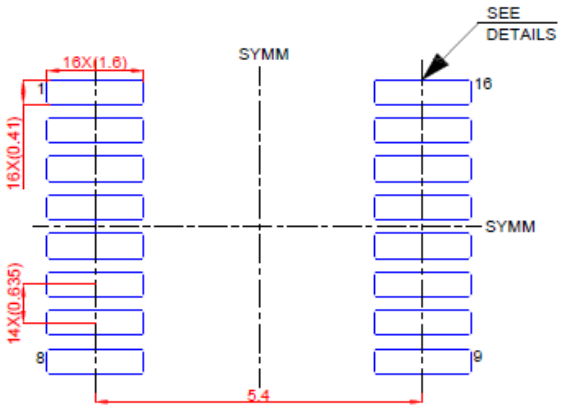


* CONTROLLING DIMENSION:MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.73	---	---	0.068
A1	0.10	---	0.25	0.004	---	0.010
A2	1.40	---	1.55	0.055	---	0.061
b	0.20	---	0.31	0.008	---	0.012
c	0.18	---	0.25	0.007	---	0.010
D	4.80	---	5.00	0.189	---	0.197
E	3.80	---	4.00	0.150	---	0.157
HE	5.80	---	6.20	0.228	---	0.244
e	0.635 bsc			0.025 bsc		
L	1.00 bsc			0.039 bsc		
L1	0.41	---	0.89	0.016	---	0.035
Y	---	0.09	---	---	0.004	---
A3	---	0.25	---	---	0.010	---
θ	0°	---	8°	0°	---	8°

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 9.3 SSOP16 Package Shape and Dimension in millimeters



LAND PATTERN EXAMPLE(mm)

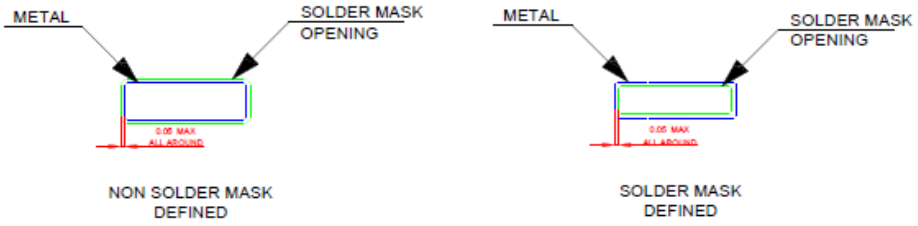


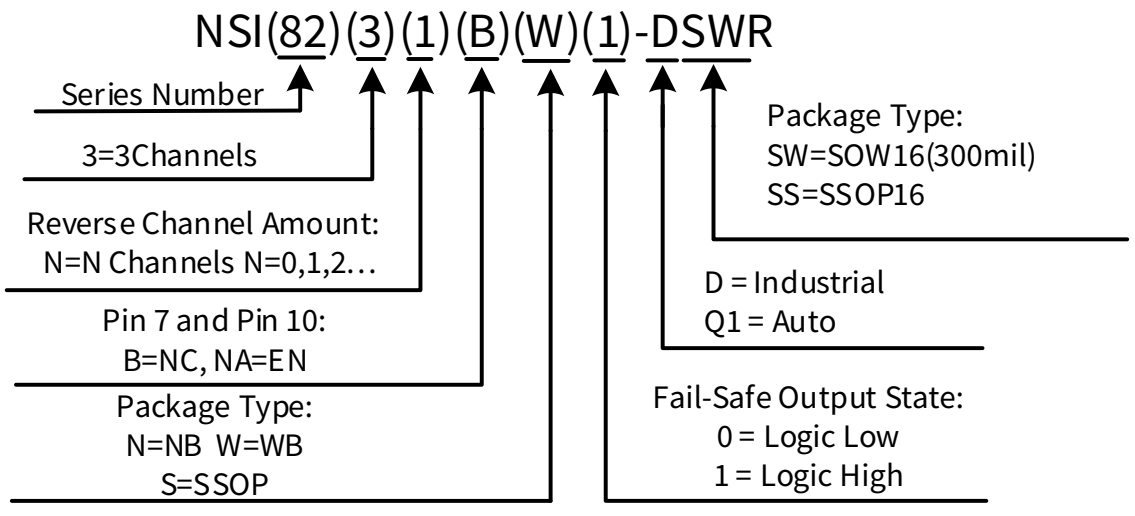
Figure 9.4 SSOP16 Package Board Layout Example

10. Order Information

Part Number	Isolation Rating (kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	MSL	Package Type	Package Drawing	SPQ
NSI8230W0-Q1SWR	5	3	0	150	Low	-40 to 125℃	2	SOP16 (300mil)	SOW16	1000
NSI8230W1-Q1SWR	5	3	0	150	High	-40 to 125℃	2	SOP16 (300mil)	SOW16	1000
NSI8231W0-Q1SWR	5	2	1	150	Low	-40 to 125℃	2	SOP16 (300mil)	SOW16	1000
NSI8231W1-Q1SWR	5	2	1	150	High	-40 to 125℃	2	SOP16 (300mil)	SOW16	1000
NSI8230S0-Q1SSR	3	3	0	150	Low	-40 to 125℃	1	SSOP16	SSOP16	2500
NSI8230S1-Q1SSR	3	3	0	150	High	-40 to 125℃	1	SSOP16	SSOP16	2500
NSI8231S0-Q1SSR	3	2	1	150	Low	-40 to 125℃	1	SSOP16	SSOP16	2500
NSI8231S1-Q1SSR	3	2	1	150	High	-40 to 125℃	1	SSOP16	SSOP16	2500

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
All devices are AEC-Q100 qualified.

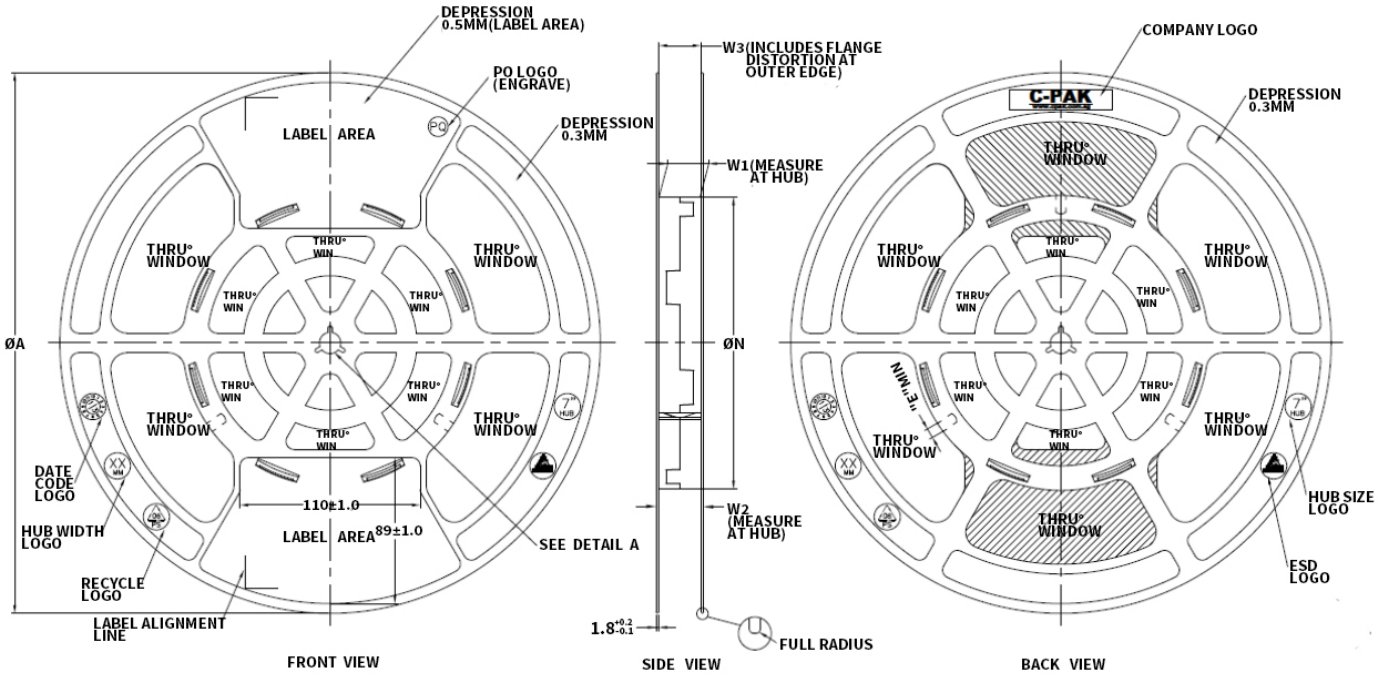
Part Number Rule:

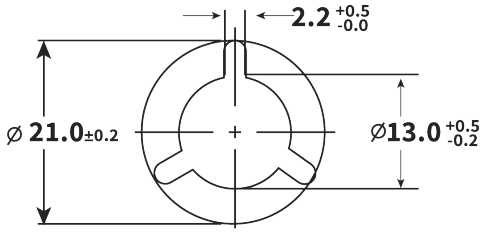


11. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
NSI823x	tbd	tbd	tbd	tbd

12. Tape and Reel Information



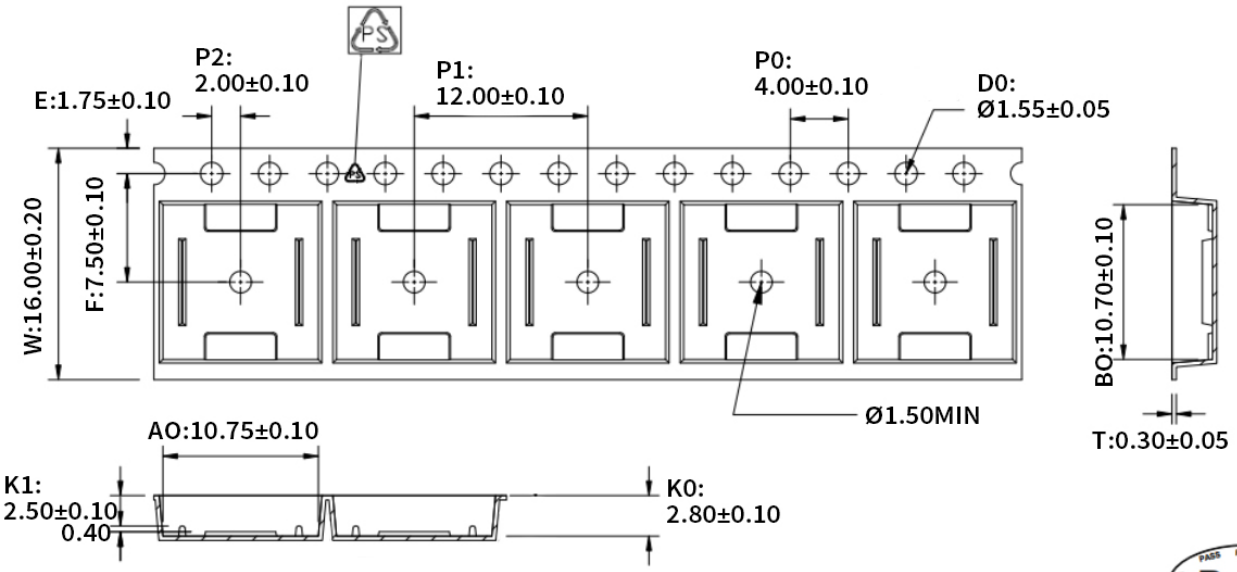


ARBOR HOLE
DETAIL A
SCALE: 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	Ø A ±2.0	Ø N ±2.0	W1	W2 (Max)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT NTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE(GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC(COATED)	ALL TYPES

Figure 12.1 Reel Information (for all packages)



1.10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness: 0.30±0.05mm.
6. Packing length per 22" reel: 378 Meters.(Rewind N=122)
7. Component load per 13" reel: 1000 pcs.
8. Surface resistivity:10^5~ 10^{10}Ω/口

W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

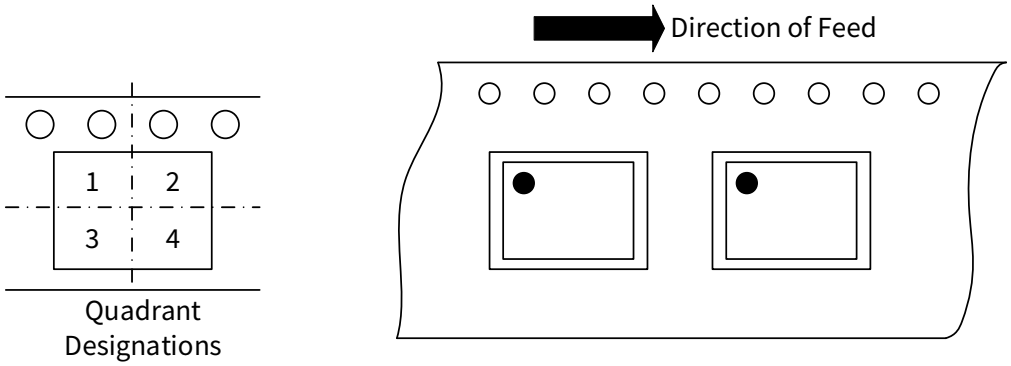
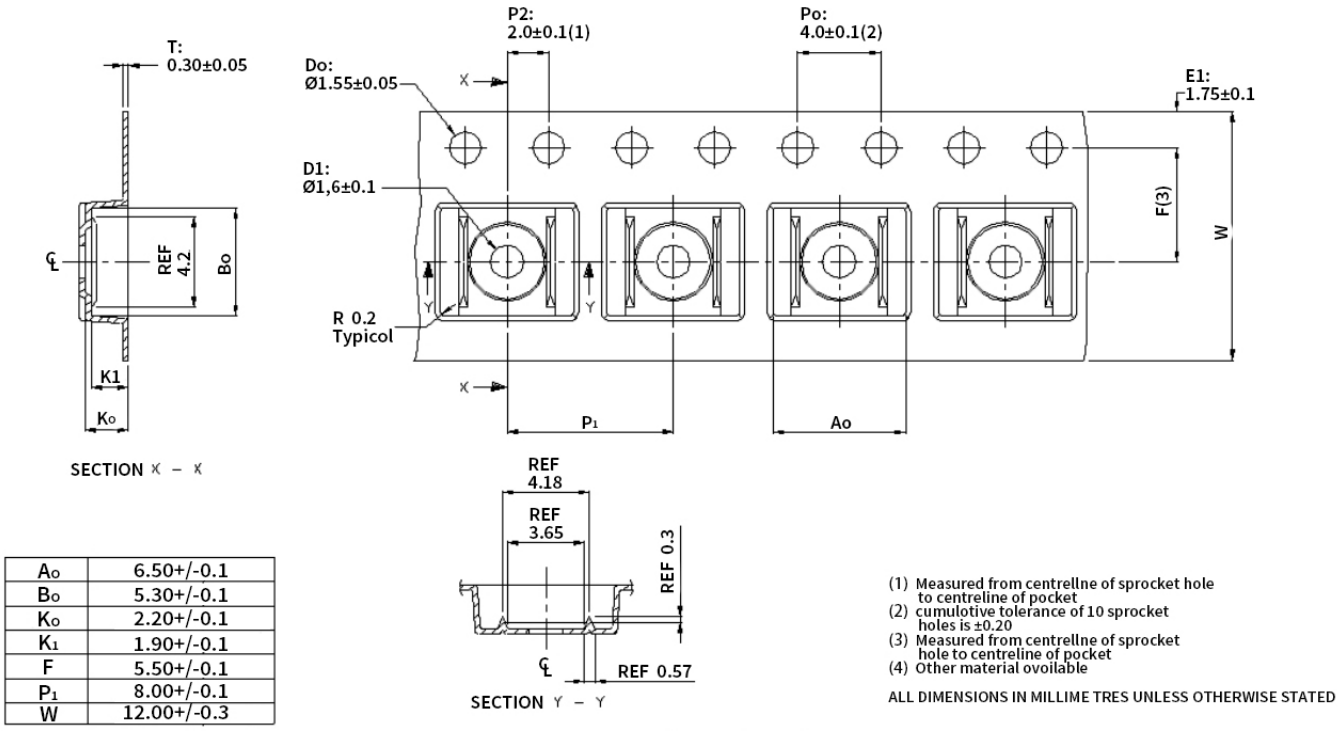


Figure 12.2 Tape Information of SOP16(300mil)



A_o	6.50+/-0.1
B_o	5.30+/-0.1
K_o	2.20+/-0.1
K_1	1.90+/-0.1
F	5.50+/-0.1
P_1	8.00+/-0.1
W	12.00+/-0.3

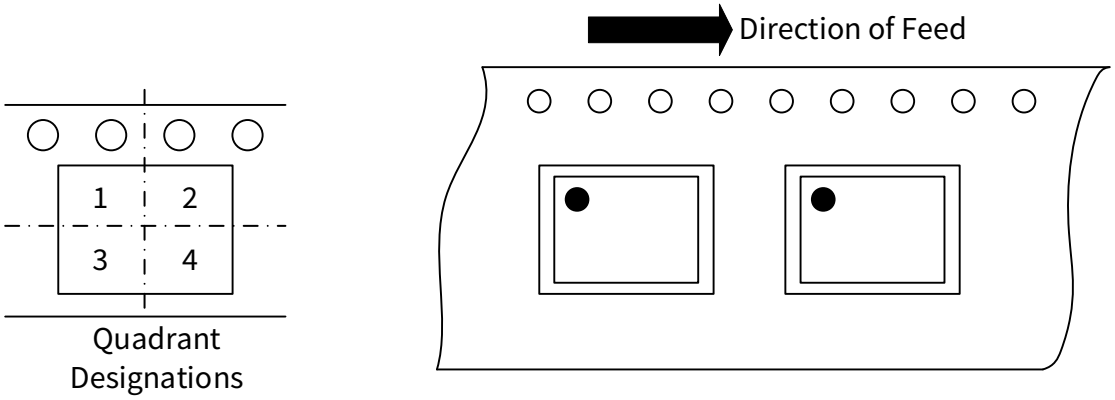


Figure 12.3 Tape Information of SSOP16

13. Revision History

Revision	Description	Date
1.0	Initial version	2021/7/16
1.1	add Junction Temperature, delete “Isolation barrier life: >60 years”, change DPI from 32 to 28, Change Min Storage Temperature to -65, add Junction Temperature, Update Regular Information VDE file	2022/8/31
1.2	Updata SSOP16 package, Typical Supply Current Equations, Figure 5.10. Update Regulatory Information and Safety Regulatory Approvals.	2024/5/17

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