

## Product Overview

NSI66x2x is a family of high reliability isolated dual-channel gate driver ICs which can be configured as two low-side drivers, two high-side drivers, or a half-bridge driver. Each output could source 6A and sink 8A peak current with fast 33ns propagation delay and 6ns maximum delay matching. It is designed to drive power MOSFET, SiC, GaN, and IGBT transistors.

The NSI66x2x provides 2500V<sub>rms</sub> isolation per UL1577 in 5-mm x 5-mm LGA13 package, 3000V<sub>rms</sub> isolation in SOP16 or SOP14 package, and 5700V<sub>rms</sub> isolation in SOW16 or SOW14 package. System robustness is supported by 150kV/us typical common-mode transient immunity (CMTI).

The driver operates with a maximum supply voltage of 25V, while the input-side accepts from 3V to 18V supply voltage. Under voltage lock-out (UVLO) protection is supported by all the power supply voltage pins.

## Key Features

- Isolated dual channel driver
- Input side supply voltage: 3V to 18V
- Driver side supply voltage: up to 25V with UVLO
- 6A peak source and 8A peak sink output
- High CMTI:  $\pm 150\text{kV/us}$  typical
- 33ns typical propagation delay
- 6ns maximum delay matching
- 9ns maximum pulse width distortion
- Programmable deadtime
- Accepts minimum input pulse width 20ns
- Operation temperature:  $-40^{\circ}\text{C}\sim 125^{\circ}\text{C}$
- RoHS & REACH Compliance

## Safety Regulatory Approvals

- UL recognition:
  - LGA13 (5x5mm): 2500V<sub>rms</sub> for 1 minute per UL1577
  - SOW16/SOW14: 5700V<sub>rms</sub> for 1 minute per UL1577
  - SOP16/SOP14: 3000V<sub>rms</sub> for 1 minute per UL1577
- DIN EN IEC 60747-17 (VDE 0884-17)
- CSA component notice 5A
- CQC certification per GB4943.

## Applications

- Isolated DC-DC and AC-to-DC power supplies in server, telecom, and industry
- DC-to-AC solar inverters
- Motor drives and EV battery chargers
- Uninterruptible power supply (UPS)

### Functional Block Diagram

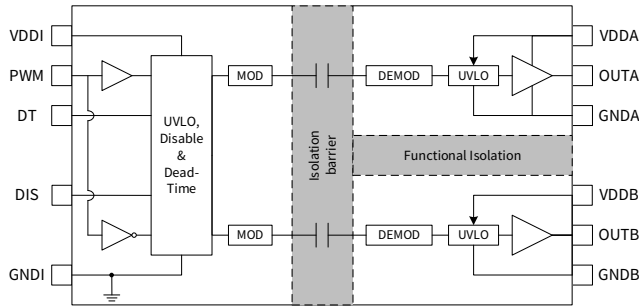


Figure 0.1 NSI6642 Block Diagram

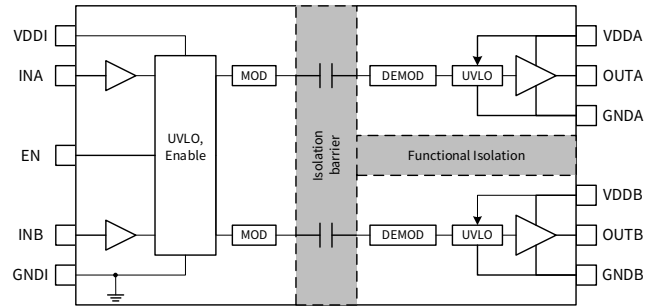


Figure 0.2 NSI6622N Block Diagram

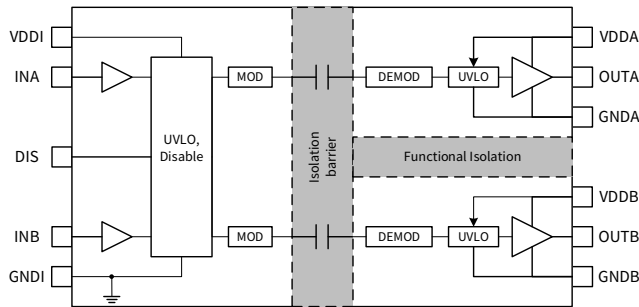


Figure 0.3 NSI6622V Block Diagram

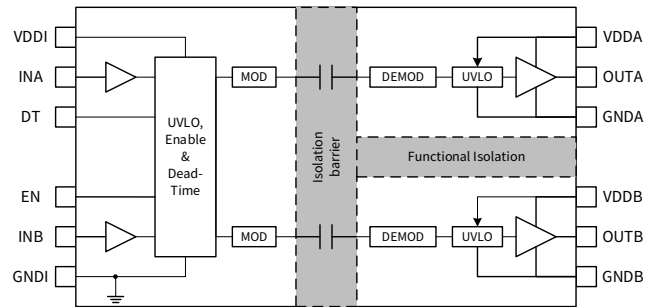


Figure 0.4 NSI6602N Block Diagram

### Products

The table below shows the configuration and functional overview for each product in this family.

Table 0.1 NSI66x2x Family Overview

| Part No.  | Driver-side UVLO TYP. | Inputs   | Programmable Dead Time | Enable pin | Peak current |
|-----------|-----------------------|----------|------------------------|------------|--------------|
| NSI6602NA | 6V                    | INA, INB | YES                    | EN         | 6A/8A        |
| NSI6602NB | 8V                    | INA, INB | YES                    | EN         | 6A/8A        |
| NSI6602NC | 12V                   | INA, INB | YES                    | EN         | 6A/8A        |
| NSI6602ND | 4V                    | INA, INB | YES                    | EN         | 6A/8A        |
| NSI6642A  | 6V                    | PWM      | YES                    | DIS        | 6A/8A        |
| NSI6642B  | 8V                    | PWM      | YES                    | DIS        | 6A/8A        |
| NSI6642C  | 12V                   | PWM      | YES                    | DIS        | 6A/8A        |
| NSI6642D  | 4V                    | PWM      | YES                    | DIS        | 6A/8A        |
| NSI6622NA | 6V                    | INA, INB | NO                     | EN         | 6A/8A        |
| NSI6622NB | 8V                    | INA, INB | NO                     | EN         | 6A/8A        |
| NSI6622NC | 12V                   | INA, INB | NO                     | EN         | 6A/8A        |
| NSI6622ND | 4V                    | INA, INB | NO                     | EN         | 6A/8A        |
| NSI6622VA | 6V                    | INA, INB | NO                     | DIS        | 6A/8A        |
| NSI6622VB | 8V                    | INA, INB | NO                     | DIS        | 6A/8A        |
| NSI6622VC | 12V                   | INA, INB | NO                     | DIS        | 6A/8A        |
| NSI6622VD | 4V                    | INA, INB | NO                     | DIS        | 6A/8A        |

## INDEX

|   |    |
|---|----|
| 1. PIN CONFIGURATION AND FUNCTIONS .....  | 4  |
| 2. ABSOLUTE MAXIMUM RATINGS .....   | 6  |
| 3. ESD RATINGS .....  | 6  |
| 4. RECOMMENDED OPERATING CONDITIONS .....   | 6  |
| 5. THERMAL INFORMATION .....  | 7  |
| 6. SPECIFICATIONS .....   | 8  |
| 6.1. ELECTRICAL CHARACTERISTICS .....   | 8  |
| 6.2. SWITCHING CHARACTERISTICS .....  | 9  |
| 6.3. TYPICAL PERFORMANCE CHARACTERISTICS .....  | 10 |
| 6.4. PARAMETER MEASUREMENT INFORMATION .....  | 13 |
| 7. HIGH VOLTAGE FEATURE DESCRIPTION .....   | 16 |
| 7.1. INSULATION CHARACTERISTICS .....   | 16 |
| 7.2. SAFETY-LIMITING VALUES .....   | 17 |
| 7.3. SAFETY-RELATED CERTIFICATIONS .....  | 21 |
| 8. FUNCTION DESCRIPTION .....   | 22 |
| 8.1. OVERVIEW .....   | 22 |
| 8.2. UNDERVOLTAGE LOCKOUT (UVLO) .....  | 23 |
| 8.3. INPUT AND OUTPUT LOGIC TABLE .....   | 24 |
| 8.4. PROGRAMMABLE DEADTIME (DT PIN) .....   | 25 |
| 8.4.1. PULLING THE DT PIN TO VDDI .....   | 25 |
| 8.4.2. DT PIN LEFT OPEN OR CONNECTED TO A PROGRAMMING RESISTOR BETWEEN DT AND GNDI PINS ..... | 25 |
| 8.5. ESD PROTECTION .....   | 27 |
| 9. APPLICATION NOTE .....   | 27 |
| 9.1. TYPICAL APPLICATION CIRCUIT .....  | 27 |
| 9.2. PCB LAYOUT .....   | 27 |
| 10. PACKAGE INFORMATION .....   | 28 |
| 11. ORDERING INFORMATION .....  | 34 |
| 12. TAPE AND REEL INFORMATION .....   | 37 |
| 13. REVISION HISTORY .....  | 40 |

# 1. Pin Configuration and Functions

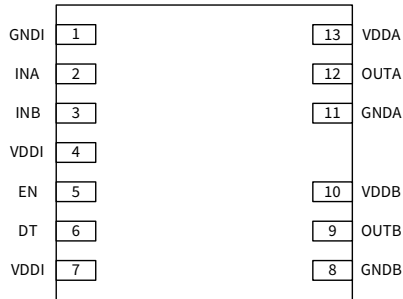


Figure 1.1 NSI6602N LGA13 Package

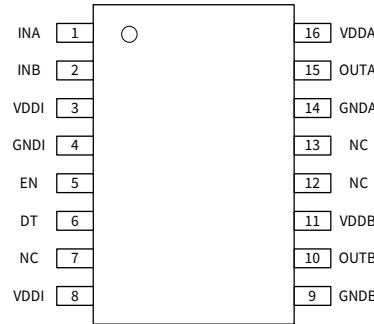


Figure 1.2 NSI6602N SOW16/SOP16 Package

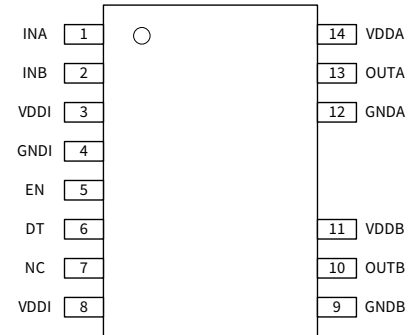


Figure 1.3 NSI6602N SOW14/SOP14 Package

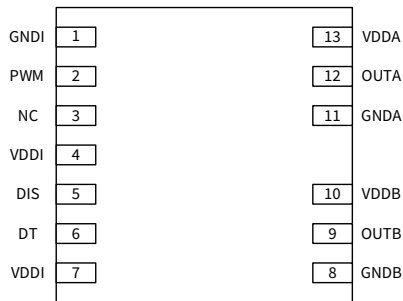


Figure 1.4 NSI6642 LGA13 Package

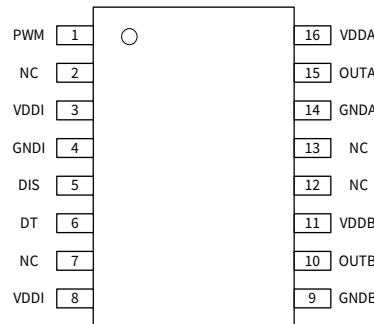


Figure 1.5 NSI6642 SOW16/SOP16 Package

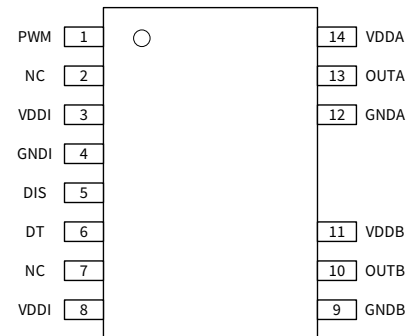


Figure 1.6 NSI6642 SOW14/SOP14 Package

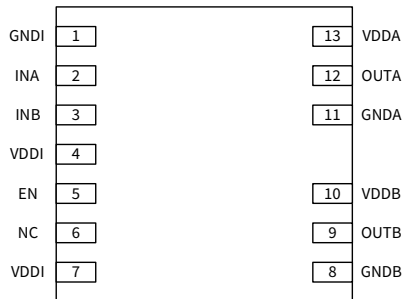


Figure 1.7 NSI6622N LGA13 Package

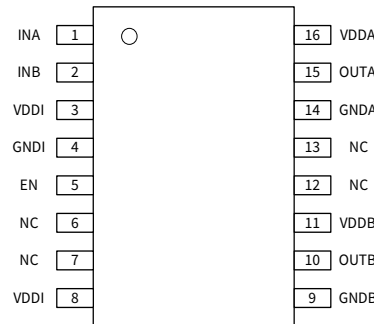


Figure 1.8 NSI6622N SOW16/SOP16 Package

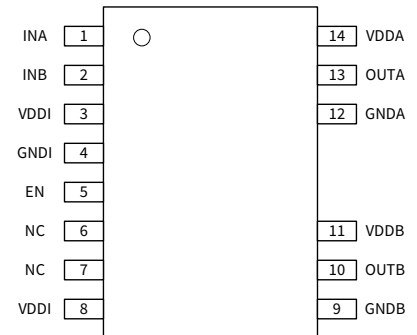


Figure 1.9 NSI6622N SOW14/SOP14 Package

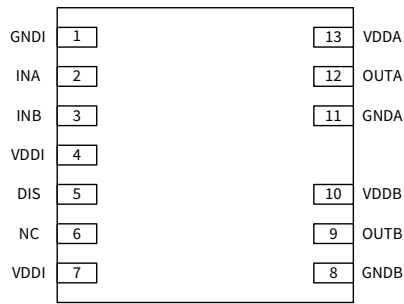


Figure 1.10 NSI6622V LGA13 Package

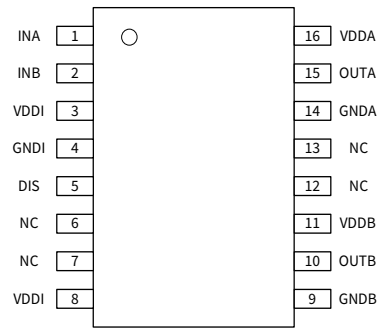


Figure 1.11 NSI6622V SOW16/SOP16 Package

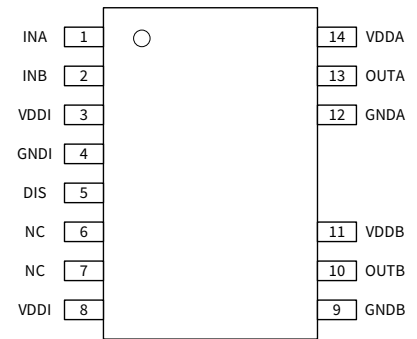


Figure 1.12 NSI6622V SOW14/SOP14 Package

Table 1.1 NSI66x2x Pin Description

| Symbol | Function  |
|--------|---|
| GNDI   | Input-side ground reference.  |
| INA    | TTL compatible input signal for channel A with internal pull down to GNDI. It is recommended to connect this pin to GNDI if not used.   |
| INB    | TTL compatible input signal for channel B with internal pull down to GNDI. It is recommended to connect this pin to GNDI if not used.   |
| PWM    | TTL compatible input signal for channel A and channel B with internal pull down to GNDI. OUTA is high and OUTB is low when the PWM input is high, and OUTA is low and OUTB is high when the PWM input is low. (for NSI6642)   |
| VDDI   | Input-side supply voltage. It is recommended to place a bypass capacitor from this pin to GNDI as close as possible.  |
| DIS    | Disables the isolator inputs and driver outputs if asserted high, enables if asserted low or left open. It is recommended to connect this pin to GNDI if not used.  |
| EN     | Enable the isolator inputs and driver outputs if asserted high, disable if asserted low or left open. It is recommended to connect this pin to VDDI if not used.  |
| DT     | <p>Programmable deadtime control.</p> <ul style="list-style-type: none"> <li>DT pin short to VCCI disables dead time interlock function to allow the outputs overlapping.</li> <li>DT pin open or floating enables interlock function, deadtime will be typically 8ns.</li> <li>Place a 1kΩ - 200kΩ resistor (<math>R_{DT}</math>) between DT and GND to adjust deadtime following: <math>t_{DT} (ns) = 10 \times R_{DT} (k\Omega)</math>.</li> </ul> <p>Connecting with a low ESR 2.2nF capacitor to GND is recommended to limit the noise interference.</p> |
| GNDB   | Ground for output channel B   |
| OUTB   | Output gate driver for channel B  |
| VDDB   | Supply voltage for channel B  |

|       |                                  |
|-------|----------------------------------|
| GND A | Ground for output channel A      |
| OUT A | Output gate driver for channel A |
| VDD A | Supply voltage for channel A     |
| NC    | Not connected                    |

## 2. Absolute Maximum Ratings

| Parameters                     | Symbol   | Min  | Max   | Unit |
|--------------------------------|--|------|---|------|
| Input Side Supply Voltage      | VDDI to GNDI                                     | -0.3 | 24  | V    |
| Output Side Supply Voltage     | VDDA to GNDA, VDD B to GNDB                      | -0.3 | 30  | V    |
| Input Signal Voltage           | INA, INB, DIS/EN, DT to GNDI                     | -0.3 | V <sub>VDDI</sub> +0.3                            | V    |
|                                | INA, INB, DIS/EN, DT to GNDI, Transient for 50ns | -5   | V <sub>VDDI</sub> +0.3                            | V    |
| Output Signal Voltage          | OUTA to GNDA, OUTB to GNDB                       | -0.3 | V <sub>VDDA</sub> +0.3<br>V <sub>VDD B</sub> +0.3 | V    |
|                                | OUTA to GNDA, OUTB to GNDB, Transient for 200ns  | -2   | V <sub>VDDA</sub> +0.3<br>V <sub>VDD B</sub> +0.3 | V    |
| Channel A to Channel B Voltage | GNDA to GNDB in LGA13 (5 x 5) package            |      | 700   | V    |
|                                | GNDA to GNDB in SOP16&SOW16 package              |      | 1500  | V    |
|                                | GNDA to GNDB in SOW14 & SOP14 package            |      | 1850  | V    |
| Junction Temperature           | T <sub>J</sub>                                   | -40  | 150   | °C   |
| Storage Temperature            | T <sub>stg</sub>                                 | -65  | 150   | °C   |

## 3. ESD Ratings

|                         | Ratings   | Value  | Unit |
|-------------------------|---|--------|------|
| Electrostatic discharge | Human body model (HBM), per AEC-Q100-002-RevD<br><ul style="list-style-type: none"> <li>All pins</li> </ul>     | ± 3000 | V    |
|                         | Charged device model (CDM), per AEC-Q100-011-RevB<br><ul style="list-style-type: none"> <li>All pins</li> </ul> | ± 1500 | V    |

## 4. Recommended Operating Conditions

| Parameters                | Symbol       | Min | Max | Unit |
|---------------------------|--------------|-----|-----|------|
| Input Side Supply Voltage | VDDI to GNDI | 3   | 18  | V    |

|                            |                            |  |                   |    |
|----------------------------|----------------------------|--|-------------------|----|
| Driver Side Supply Voltage | VDDA to GNDA, VDDB to GNDB | V <sub>VDDA_ON</sub> ,<br>V <sub>VDDB_ON</sub> | 25                | V  |
| Input Signal Voltage       | INA/PWM, INB, DIS/EN, DT   | 0  | V <sub>VDDI</sub> | V  |
| Ambient Temperature        | T <sub>a</sub>             | -40  | 125               | °C |

## 5. Thermal Information

| <i>Parameters</i>  | <i>Symbol</i>         | <i>LGA13</i> | <i>SOW16/<br/>SOW14</i> | <i>SOP16/<br/>SOP14</i> | <i>Unit</i> |
|--|-----------------------|--------------|-------------------------|-------------------------|-------------|
| Junction-to-ambient thermal resistance <sup>1)</sup>       | R <sub>JA</sub>       | 209.5        | 97.0                    | 150.5                   | °C/W        |
| Junction-to-case(top) thermal resistance <sup>2)</sup>     | R <sub>JC (top)</sub> | 48.4         | 23.3                    | 21.2                    | °C/W        |
| Junction-to-top characterization parameter <sup>3)</sup>   | Ψ <sub>JT</sub>       | 41.8         | 35.8                    | 52.3                    | °C/W        |
| Junction-to-board characterization parameter <sup>3)</sup> | Ψ <sub>JB</sub>       | 31.9         | 39.0                    | 55.6                    | °C/W        |

- 1) Standard JESD51-3 Low Effective Thermal Conductivity Test Board (1s) in an environment described in JESD51-2a.
- 2) Standard JESD51-3 Low Effective Thermal Conductivity Test Board (1s) by transient dual interface test method described in JESD51-14.
- 3) Obtained by Simulating in an environment described in JESD51-2a.

## 6. Specifications

### 6.1. Electrical Characteristics

VDDI=3.3V or 5V, VDDA=VDDDB=15V, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at Ta=25°C.

| Parameter                             | Symbol  | Min  | Typ  | Max  | Unit | Comments                |
|---------------------------------------|---|------|------|------|------|-------------------------|
| Input Side Supply                     |   |      |      |      |      |                         |
| VDDI Quiescent Current                | I <sub>VDDIQ</sub>                                |      | 1.0  | 2    | mA   | INA=0, INB=0            |
| VDDI Operating Current, per Channel   | I <sub>VDDI</sub>                                 |      | 1.6  |      | mA   | Input frequency 500kHz  |
| VDDI UVLO Rising Threshold            | V <sub>VDDI_ON</sub>                              | 2.5  | 2.7  | 2.9  | V    |                         |
| VDDI UVLO Falling Threshold           | V <sub>VDDI_OFF</sub>                             | 2.3  | 2.5  | 2.7  | V    |                         |
| VDDI UVLO Hysteresis                  | V <sub>VDDI_HYS</sub>                             |      | 0.2  |      | V    |                         |
| Output Side Supply                    |   |      |      |      |      |                         |
| VDDA/B Quiescent Current, per Channel | I <sub>VDDAQ</sub> , I <sub>VDDBQ</sub>           |      | 1.0  | 2    | mA   | INA=0, INB=0            |
| VDDA/B Operation Current, per Channel | I <sub>VDDA</sub> , I <sub>VDDDB</sub>            |      | 3.0  |      | mA   | 100pF, 500kHz, VDDx=15V |
| VDDA/B UVLO Rising Threshold          | V <sub>VDDA_ON</sub> ,<br>V <sub>VDDDB_ON</sub>   | 5.7  | 6.15 | 6.5  | V    | NSI66x2xA (6V)          |
| VDDA/B UVLO Falling Threshold         | V <sub>VDDA_OFF</sub> ,<br>V <sub>VDDDB_OFF</sub> | 5.4  | 5.85 | 6.2  | V    |                         |
| VDDA/B UVLO Hysteresis                | V <sub>VDDA_HYS</sub> ,<br>V <sub>VDDDB_HYS</sub> |      | 0.3  |      | V    |                         |
| VDDA/B UVLO Rising Threshold          | V <sub>VDDA_ON</sub> ,<br>V <sub>VDDDB_ON</sub>   | 8.1  | 8.5  | 8.9  | V    | NSI66x2xB (8V)          |
| VDDA/B UVLO Falling Threshold         | V <sub>VDDA_OFF</sub> ,<br>V <sub>VDDDB_OFF</sub> | 7.6  | 8.0  | 8.4  | V    |                         |
| VDDA/B UVLO Hysteresis                | V <sub>VDDA_HYS</sub> ,<br>V <sub>VDDDB_HYS</sub> |      | 0.5  |      | V    |                         |
| VDDA/B UVLO Rising Threshold          | V <sub>VDDA_ON</sub> ,<br>V <sub>VDDDB_ON</sub>   | 12.7 | 13.2 | 13.7 | V    | NSI66x2xC (12V)         |
| VDDA/B UVLO Falling Threshold         | V <sub>VDDA_OFF</sub> ,<br>V <sub>VDDDB_OFF</sub> | 11.7 | 12.2 | 12.7 | V    |                         |
| VDDA/B UVLO Hysteresis                | V <sub>VDDA_HYS</sub> ,<br>V <sub>VDDDB_HYS</sub> |      | 1    |      | V    |                         |
| VDDA/B UVLO Rising Threshold          | V <sub>VDDA_ON</sub> ,<br>V <sub>VDDDB_ON</sub>   | 3.9  | 4.2  | 4.4  | V    | NSI66x2xD (4V)          |
| VDDA/B UVLO Falling Threshold         | V <sub>VDDA_OFF</sub> ,<br>V <sub>VDDDB_OFF</sub> | 3.5  | 3.8  | 4.1  | V    |                         |
| VDDA/B UVLO Hysteresis                | V <sub>VDDA_HYS</sub> ,<br>V <sub>VDDDB_HYS</sub> |      | 0.4  |      | V    |                         |

| Parameter                                | Symbol  | Min | Typ  | Max | Unit       | Comments           |
|--|---|-----|------|-----|------------|--------------------|
| Input Side Characteristic                |   |     |      |     |            |                    |
| Input Pin Pull Down Resistance, INA, INB | $R_{INA\_PD}/R_{PWM\_PD}, R_{INB\_PD}$                                | 80  | 100  | 125 | k $\Omega$ |                    |
| Input Pin Pull Down Resistance, DIS /EN  | $R_{DIS\_PD} /R_{EN\_PD}$   | 80  | 100  | 125 | k $\Omega$ |                    |
| Logic High Input Threshold               | $V_{INA\_H} /V_{PWM\_H}, V_{INB\_H}, V_{DIS\_H} /V_{EN\_H}$           | 1.5 | 1.8  | 2.1 | V          |                    |
| Logic Low Input Threshold                | $V_{INA\_L} /V_{PWM\_L}, V_{INB\_L}, V_{DIS\_L} /V_{EN\_L}$           | 0.8 | 1.1  | 1.4 | V          |                    |
| Input Hysteresis                         | $V_{INA\_HYS} /V_{PWM\_HYS}, V_{INB\_HYS}, V_{DIS\_HYS} /V_{EN\_HYS}$ |     | 0.7  |     | V          |                    |
| Output Side Characteristic               |   |     |      |     |            |                    |
| Logic High Output Voltage                | $V_{VDDA}-V_{OUTA\_H}, V_{VDDB}-V_{OUTB\_H}$                          |     | 0.1  |     | V          | $I_{out} = 100mA$  |
| Logic Low Output Voltage                 | $V_{OUTA\_L}, V_{OUTB\_L}$  |     | 35   |     | mV         | $I_{out} = -100mA$ |
| Output Source Resistance                 | $R_{OUTA\_H}, R_{OUTB\_H}$  |     | 1    |     | $\Omega$   | $I_{out} = 100mA$  |
| Output Sink Resistance                   | $R_{OUTA\_L}, R_{OUTB\_L}$  |     | 0.35 |     | $\Omega$   | $I_{out} = -100mA$ |
| Peak Output Source Current               | $I_{OUTA+}, I_{OUTB+}$  |     | 6    |     | A          |                    |
| Peak Output Sink Current                 | $I_{OUTA-}, I_{OUTB-}$  |     | 8    |     | A          |                    |

### 6.2. Switching Characteristics

VDDI=3.3V or 5V, VDDA=VDDB=15V, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at Ta=25°C.

| Parameter                                    | Symbol               | Min | Typ | Max | Unit | Comments   |
|--|----------------------|-----|-----|-----|------|--|
| Minimum Pulse Width                          | $t_{PWmin}$          |     | 15  | 25  | ns   |  |
| Propagation Delay                            | $t_{PDHL}, t_{PDLH}$ |     | 33  | 45  | ns   |  |
| Pulse Width Distortion $ t_{PDLH}-t_{PDHL} $ | $t_{PWD}$            |     |     | 9   | ns   |  |
| Channel to Channel Delay Matching            | $t_{DMLH}, t_{DMHL}$ |     |     | 6   | ns   |  |
| Programmed Deadtime                          | $t_{DT}$             | 160 | 200 | 240 | ns   | $t_{DT}(ns)=10 \cdot R(k\Omega)$ ; Test for R = 20k $\Omega$ |
| Output Rise Time (10% to 90%)                | $t_R$                |     | 15  |     | ns   | CL=1.8nF, VDDx=15V   |
| Output Fall Time (90% to 10%)                | $t_F$                |     | 15  |     | ns   | CL=1.8nF, VDDx=15V   |
| Shutdown Time from Disable True              | $t_{DIS}$            |     | 50  | 80  | ns   |  |
| Recovery Time from Disable False             | $t_{EN}$             |     | 50  | 80  | ns   |  |

|  |  |     |     |  |       |   |
|--|--|-----|-----|--|-------|---|
| VDDI Power-up Time Delay<br>(Time from VDDI = $V_{VDDI\_ON}$ to OUTA/B = INA/B)    | $t_{start\_VDDI}$                        |     | 12  |  | us    | INA or INB tied to VDDI                       |
| VDDA/B Power-up Time Delay<br>(Time from VDDA/B = $V_{VDD\_ON}$ to OUTA/B = INA/B) | $t_{start\_VDDA}$ ,<br>$t_{start\_VDDB}$ |     | 18  |  | us    | INA or INB tied to VDDI<br>$C_{OUTA/B}=1.8nF$ |
| Common Mode Transient Immunity   | CMTI                                     | 100 | 150 |  | kV/us | verified by design                            |

### 6.3. Typical Performance Characteristics

VDDI=3.3V or 5V, VDDA=VDDB=15V, TA = 25°C. Output has no load unless otherwise noted.

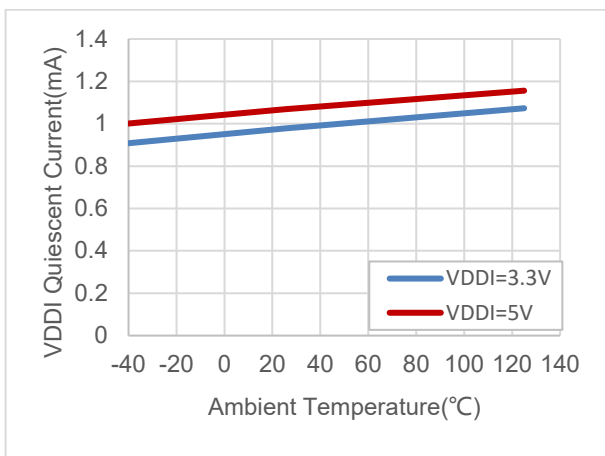


Figure 6.1 VDDI Quiescent Current vs Temperature

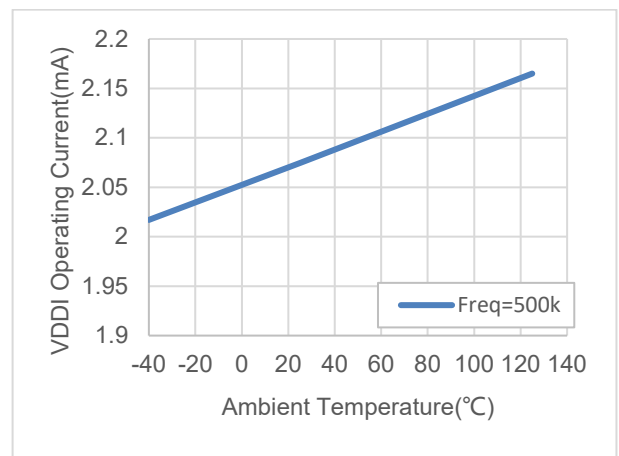


Figure 6.2 VDDI Operating Current vs Temperature

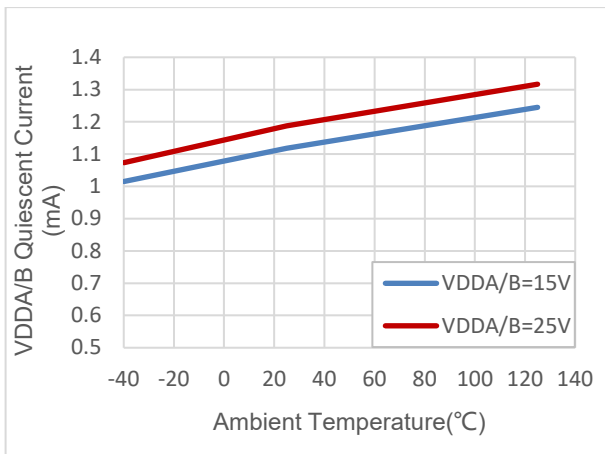


Figure 6.3 VDDA/B Quiescent Current vs Temperature

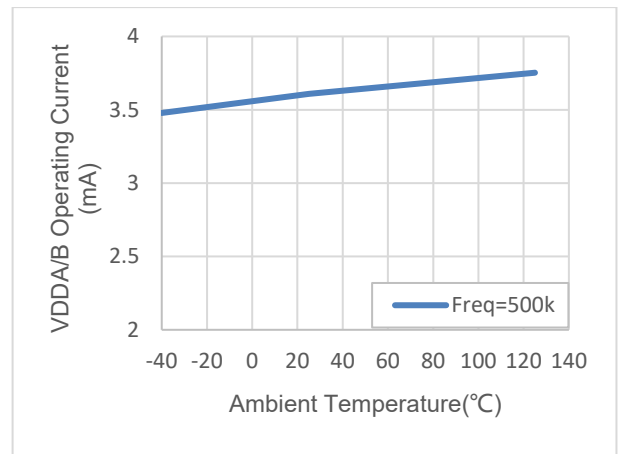


Figure 6.4 VDDA/B Operating Current vs Temperature

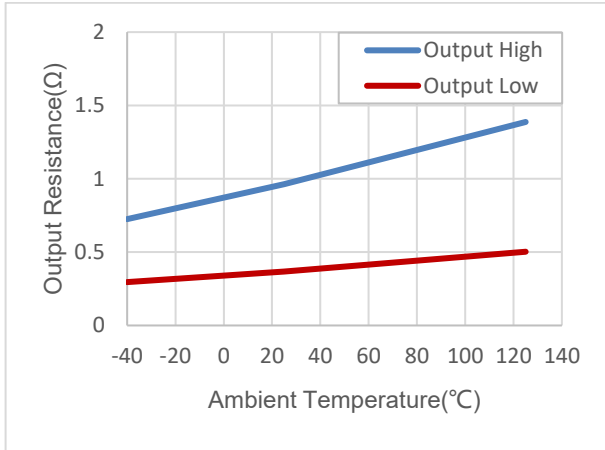


Figure 6.5 Output Resistance vs Temperature

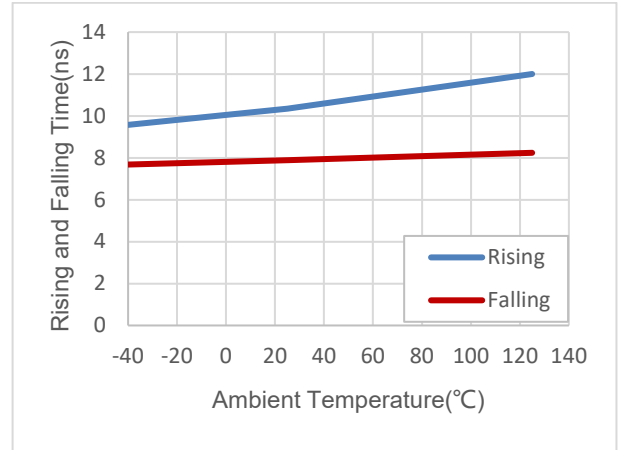


Figure 6.6 Typical Rise Time & Fall Time vs Temperature

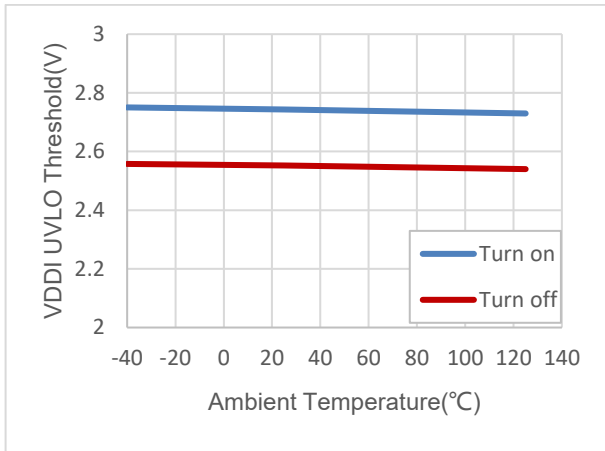


Figure 6.7 VDDI UVLO Threshold vs Temperature

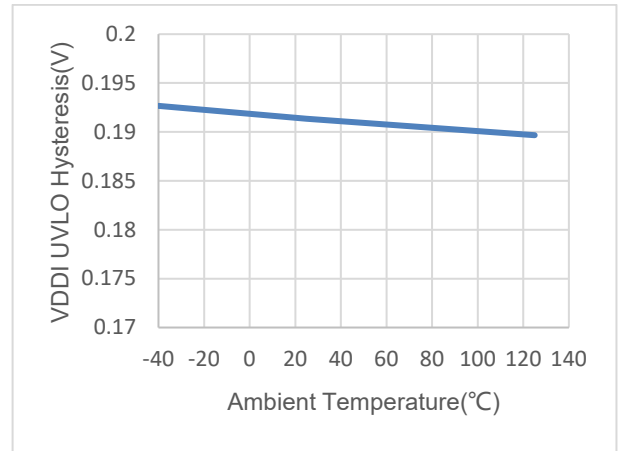


Figure 6.8 VDDI UVLO Hysteresis vs Temperature

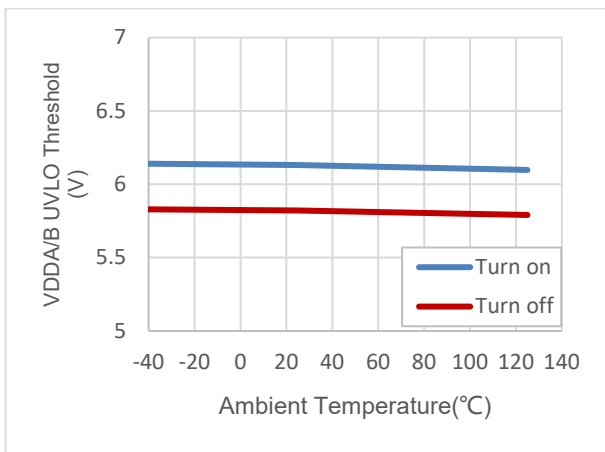


Figure 6.9 6V VDDA/B UVLO Threshold vs Temperature

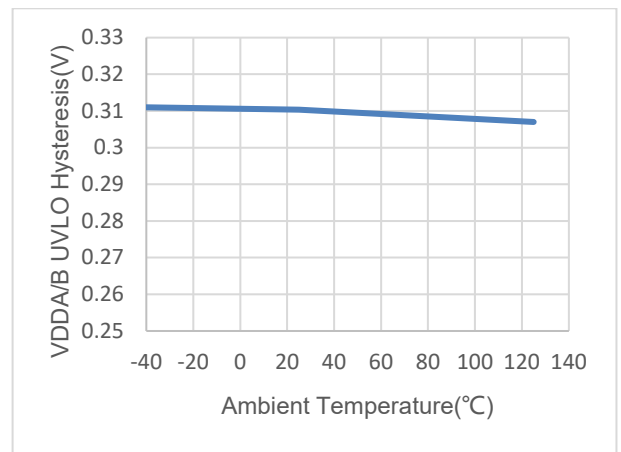


Figure 6.10 6V VDDA/B UVLO Hysteresis vs Temperature

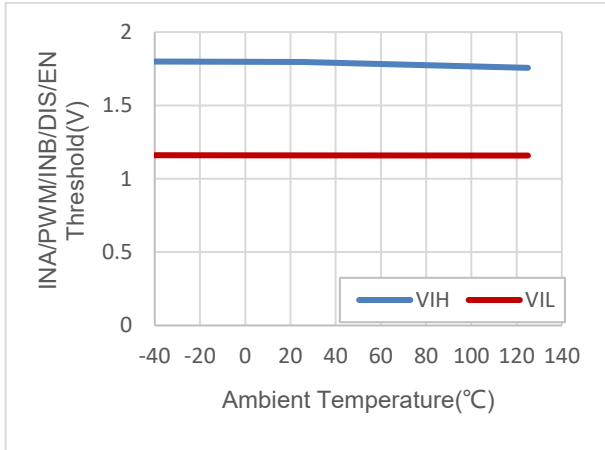


Figure 6.11 INA/PWM/INB/DIS/EN Threshold vs Temperature

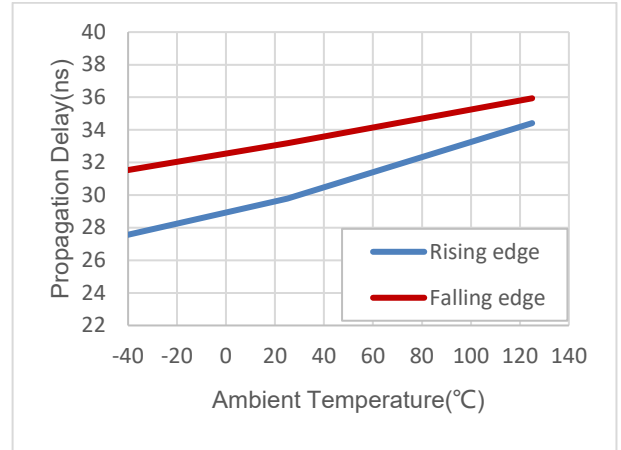


Figure 6.12 Propagation Delay vs Temperature

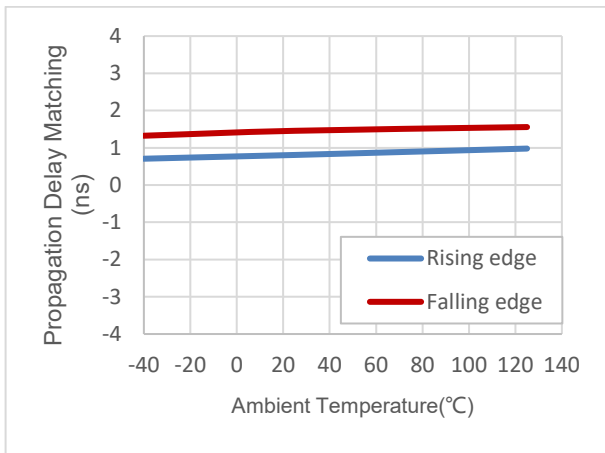


Figure 6.13 Propagation Delay Matching vs Temperature

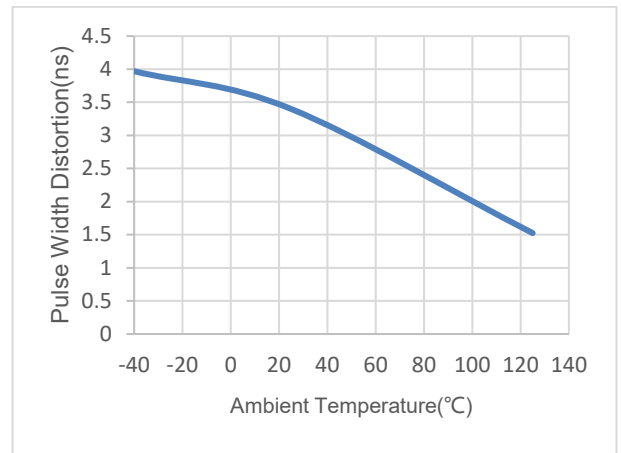


Figure 6.14 Pulse Width Distortion vs Temperature

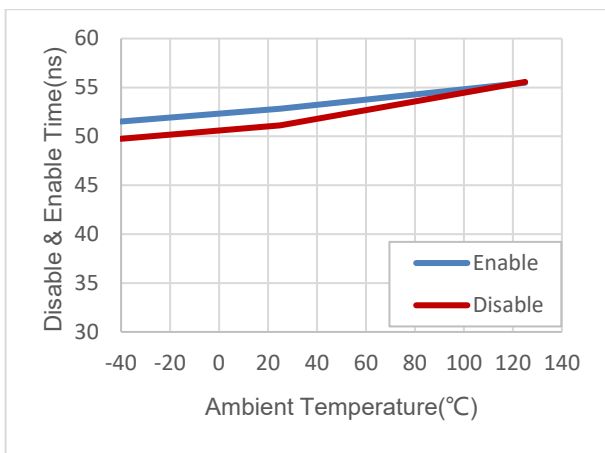


Figure 6.15 Disable & Enable Time vs Temperature

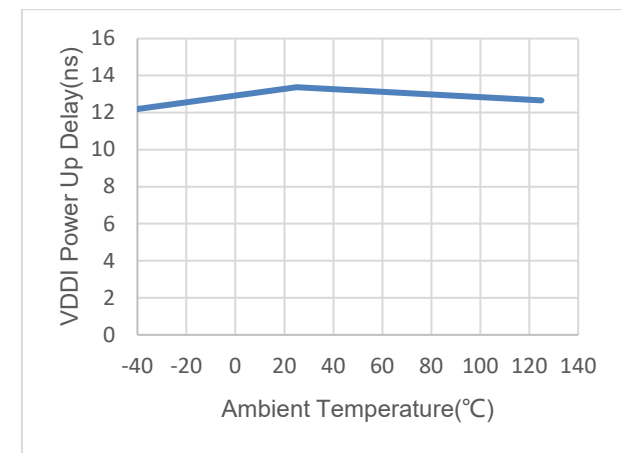


Figure 6.17 VDDI power up delay vs Temperature

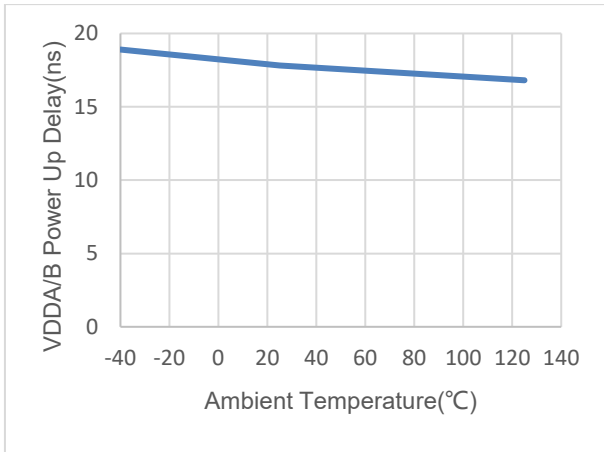


Figure 6.16 VDDA/B power up delay vs Temperature

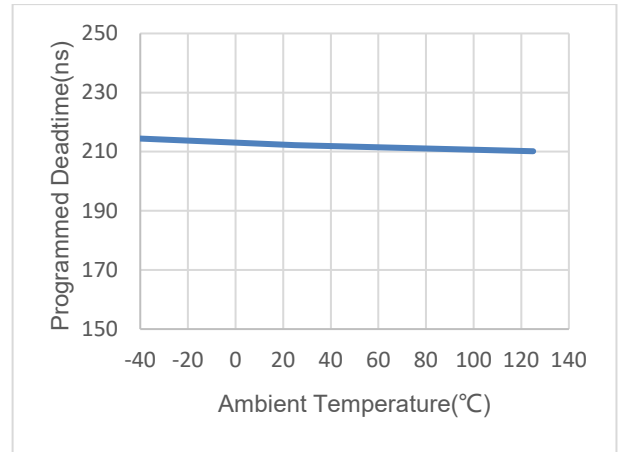


Figure 6.18 Deadtime (RDT=20kΩ) vs Temperature

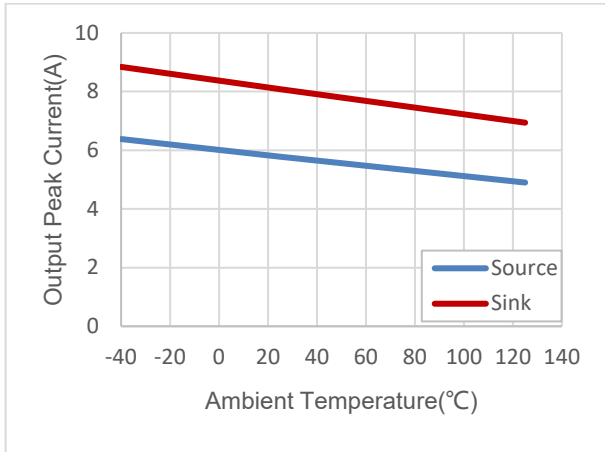


Figure 6.19 Peak current vs Temperature

### 6.4. Parameter Measurement Information

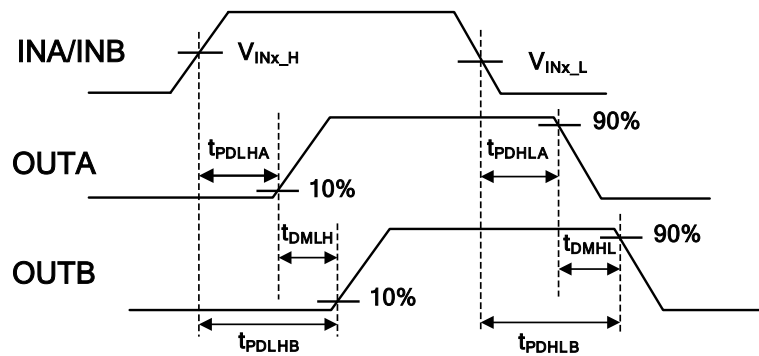


Figure 6.20 Propagation Delay and Channel to Channel Delay Match Time, connect DT to VDDI

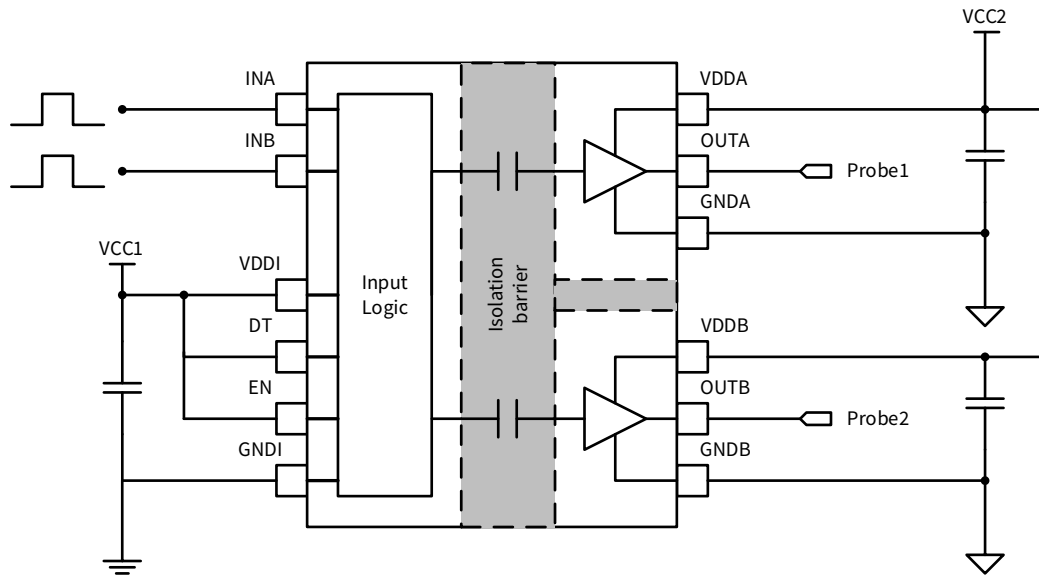


Figure 6.21 Channel to Channel Delay Match Test Circuit

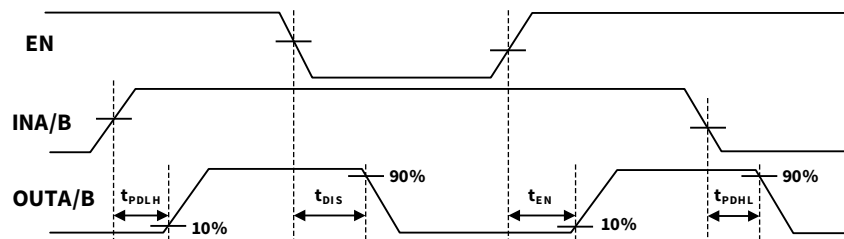


Figure 6.22 Disable Time and Enable Time (NSI6602N, NSI6622N)

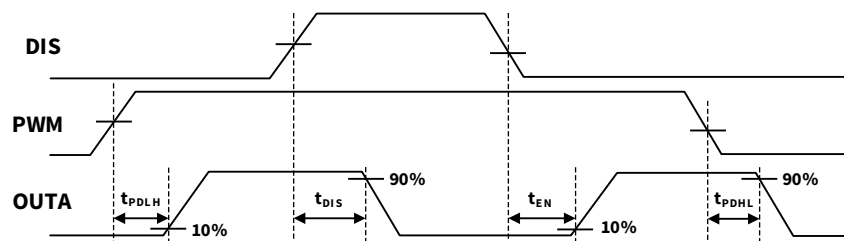


Figure 6.23 Disable Time and Enable Time (NSI6642)

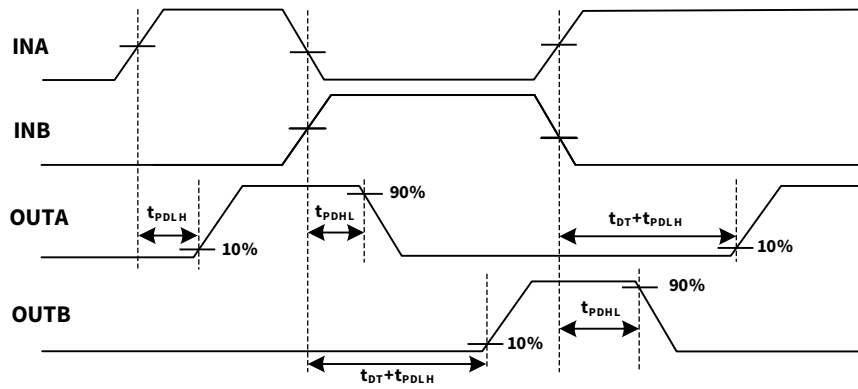


Figure 6.24 Deadtime, Determined by RDT (NSI6602N)

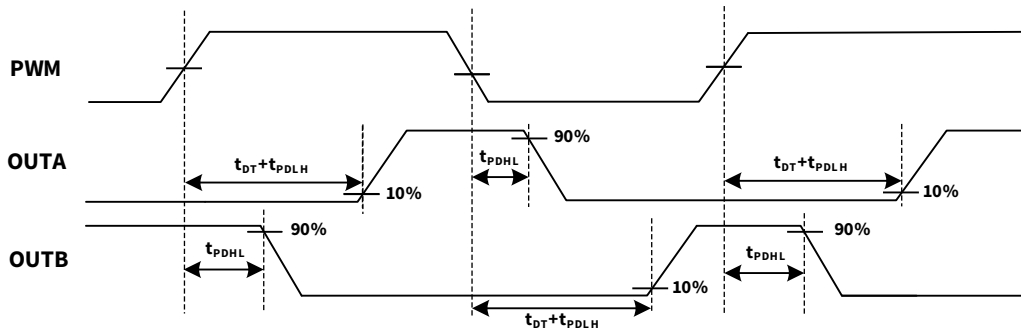


Figure 6.25 Deadtime, Determined by RDT (NSI6642)

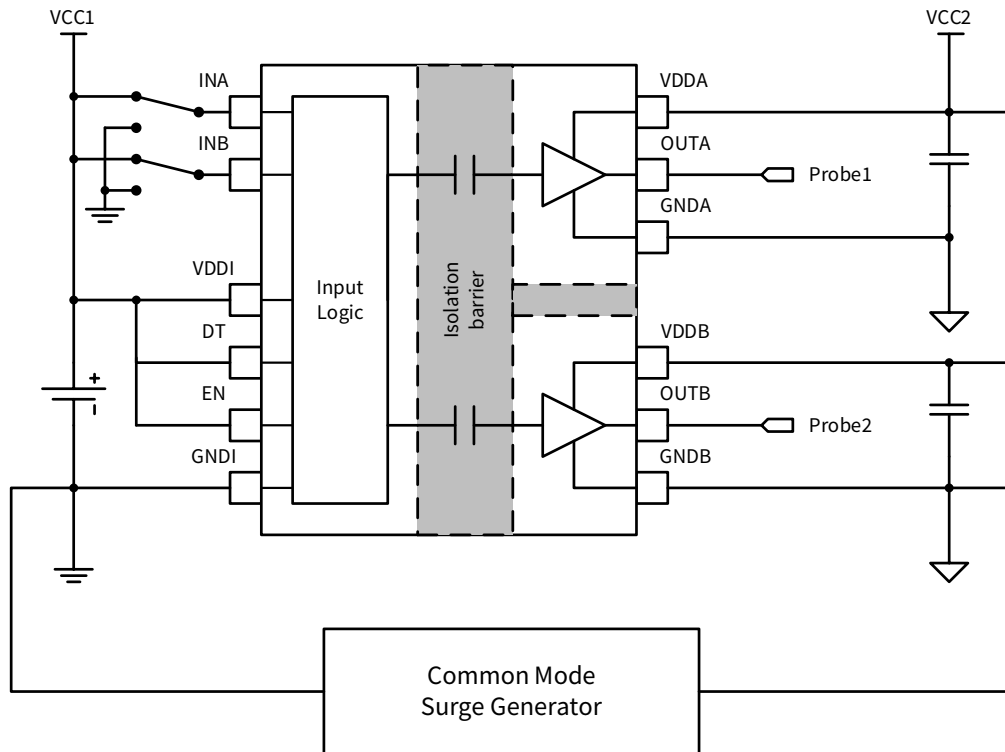


Figure 6.26 Common-Mode Transient Immunity Test Circuit

## 7. High Voltage Feature Description

### 7.1. Insulation Characteristics

| Description                          | Test Condition   | Symbol     | Value     |          |          | Unit       |
|--------------------------------------|--|------------|-----------|----------|----------|------------|
|                                      |  |            | LGA 13    | SOW16/14 | SOP16/14 |            |
| Min. External Air Gap (Clearance)    |  | CLR        | 3.5       | 8        | 4        | mm         |
| Min. External Tracking (Creepage)    |  | CPG        | 3.5       | 8        | 4        | mm         |
| Distance through the Insulation      |  | DTI        | 28        |          |          | um         |
| Comparative Tracking Index           | DIN EN 60112 (VDE 0303-11)   | CTI        | >600      |          |          | V          |
| Material Group                       | IEC 60664-1  |            | I         |          |          |            |
| Overvoltage Category per IEC60664-1  | For Rated Mains Voltage $\leq 150V_{rms}$  |            | I to III  | I to IV  | I to IV  |            |
|                                      | For Rated Mains Voltage $\leq 300V_{rms}$  |            | I to II   | I to IV  | I to III |            |
|                                      | For Rated Mains Voltage $\leq 600V_{rms}$  |            | I         | I to IV  | I to II  |            |
|                                      | For Rated Mains Voltage $\leq 1000V_{rms}$   |            | /         | I to III | /        |            |
| Climatic Category                    |  |            | 40/125/21 |          |          |            |
| Pollution Degree                     | per DIN VDE 0110, Table 1  |            | 2         |          |          |            |
| Maximum Working Isolation Voltage    | AC voltage   | $V_{IOWM}$ | 560       | 1000     | 700      | $V_{RMS}$  |
|                                      | DC voltage   |            | 792       | 1414     | 990      | $V_{DC}$   |
| Maximum Repetitive Isolation Voltage |  | $V_{IORM}$ | 792       | 1414     | 990      | $V_{peak}$ |
| Apparent Charge                      | Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$ , $t_{ini} = 60s$ , $V_{pd(m)}=1.2*V_{IORM}$ , $t_m=10s$ . | $q_{pd}$   | /         | <5       | /        | pC         |
|                                      | Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$ , $t_{ini}=60s$ , $V_{pd(m)}=1.6*V_{IORM}$ , $t_m=10s$ .          |            | /         |          | /        | pC         |
|                                      | Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}$ , $t_{ini}$                         |            | /         |          | /        | pC         |

| Description                         | Test Condition   | Symbol     | Value      |       |      | Unit       |
|-------------------------------------|--|------------|------------|-------|------|------------|
|                                     | =1s, $V_{pd(m)}=1.875 \cdot V_{IORM}$ ,<br>$t_m=1s$ (method b1) or<br>$V_{pd(m)}=V_{ini}$ ,<br>$t_m=t_{ini}$ (method b2)   |            |            |       |      |            |
| Apparent Charge                     | Method a, after<br>Input/output safety test<br>subgroup 2/3,<br>$V_{ini}=V_{IOTM}$ , $t_{ini}=60s$ ,<br>$V_{pd(m)}=1.2 \cdot V_{IORM}$ , $t_m=10s$   | $q_{pd}$   | <5         | /     | <5   | pC         |
|                                     | Method a, after<br>environmental tests<br>subgroup 1, $V_{ini}=V_{IOTM}$ ,<br>$t_{ini}=60s$ ,<br>$V_{pd(m)}=1.3 \cdot V_{IORM}$ , $t_m=10s$  |            |            | /     |      | pC         |
|                                     | Method b, routine test<br>(100% production) and<br>preconditioning (type<br>test); $V_{ini}=1.2 \cdot V_{IOTM}$ ,<br>$t_{ini}=1s$<br>$V_{pd(m)}=1.5 \cdot V_{IORM}$ , $t_m=1s$<br>(method b1) or<br>$V_{pd(m)}=V_{ini}$ ,<br>$t_m=t_{ini}$ (method b2) |            |            | /     |      | pC         |
| Maximum Transient Isolation Voltage | $t = 60 \text{ sec}$   | $V_{IOTM}$ | 3535       | 8000  | 4242 | $V_{peak}$ |
| Maximum impulse voltage             | Tested in air, 1.2/50us<br>waveform per<br>IEC62368-1  | $V_{imp}$  | /          | 6000  | 3500 | $V_{peak}$ |
| Maximum Surge Isolation Voltage     | Test method per<br>IEC62368-1, 1.2/50us<br>waveform, $V_{IOSM} \geq$<br>$V_{IMP} \times 1.3$   | $V_{IOSM}$ | 3500       | 10000 | 6000 | $V_{peak}$ |
| Isolation Resistance                | $V_{IO} = 500 \text{ V}$ , $T_{amb} = 25 \text{ }^\circ\text{C}$   | $R_{IO}$   | $>10^{12}$ |       |      | $\Omega$   |
|                                     | $V_{IO} = 500 \text{ V}$ , $T_{amb} = T_s$   |            | $>10^9$    |       |      | $\Omega$   |
|                                     | $V_{IO} = 500 \text{ V}$ , $100 \text{ }^\circ\text{C} \leq T_{amb} \leq 125 \text{ }^\circ\text{C}$   |            | $>10^{11}$ |       |      | $\Omega$   |
| Isolation Capacitance               | $f = 1\text{MHz}$  | $C_{IO}$   | 1.2        |       |      | pF         |
| Insulation Specification per UL1577 |  |            |            |       |      |            |
| Withstand Isolation Voltage         | $V_{TEST} = 1.2 \times V_{ISO}$ , $t = 1 \text{ sec}$ ,<br>100% production test  | $V_{ISO}$  | 2500       | 5700  | 3000 | $V_{rms}$  |

### 7.2. Safety-Limiting Values

Basic isolation safety-limiting values as outlined in VDE-0884-11 of NSI66x2x-xLAR (LGA13 5x5mm)

| Description | Test Condition | Side | Value | Unit |
|-------------|----------------|------|-------|------|
|-------------|----------------|------|-------|------|

|                                  |  |                    |      |                  |
|----------------------------------|--|--------------------|------|------------------|
| Safety Supply Power              | $R_{\theta JA} = 209.5 \text{ }^\circ\text{C/W}^1$ , $T_J = 150 \text{ }^\circ\text{C}$ , $T_A = 25 \text{ }^\circ\text{C}$                            | Input              | 90   | mW               |
|                                  |  | Driver A, Driver B | 254  | mW               |
|                                  |  | Total              | 598  | mW               |
| Safety Supply Current            | $R_{\theta JA} = 209.5 \text{ }^\circ\text{C/W}^1$ , $V_{DDA/B} = 15\text{V}$ , $T_J = 150 \text{ }^\circ\text{C}$ , $T_A = 25 \text{ }^\circ\text{C}$ | Driver A, Driver B | 17   | mA               |
|                                  | $R_{\theta JA} = 209.5 \text{ }^\circ\text{C/W}^1$ , $V_{DDA/B} = 25\text{V}$ , $T_J = 150 \text{ }^\circ\text{C}$ , $T_A = 25 \text{ }^\circ\text{C}$ | Driver A, Driver B | 10.2 | mA               |
| Safety Temperature <sup>2)</sup> |  |                    | 150  | $^\circ\text{C}$ |

- 1) Calculate with the junction-to-air thermal resistance,  $R_{\theta JA}$ , of LGA13 package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature ( $T_J$ ) specified for the device.

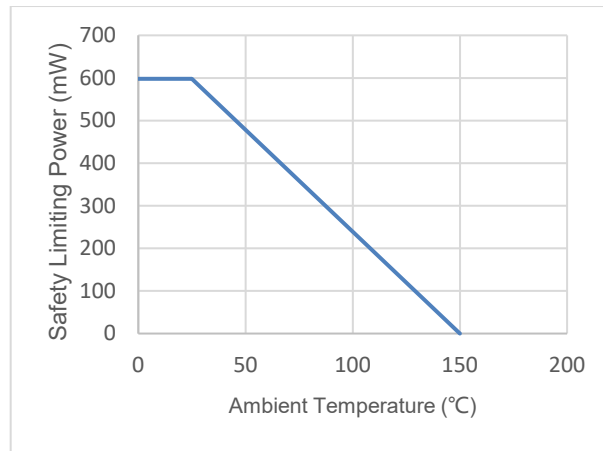


Figure 7.1 NSI66x2x-DLAR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17.

Reinforced isolation safety-limiting values as outlined in VDE-0884-11 of NSI66x2x-xSWxR (SOW16/SOW14)

| Description                      | Test Condition  | Side               | Value | Unit             |
|----------------------------------|---|--------------------|-------|------------------|
| Safety Supply Power              | $R_{\theta JA} = 97 \text{ }^\circ\text{C/W}^1$ , $T_J = 150 \text{ }^\circ\text{C}$ , $T_A = 25 \text{ }^\circ\text{C}$                            | Input              | 90    | mW               |
|                                  |   | Driver A, Driver B | 599   | mW               |
|                                  |   | Total              | 1288  | mW               |
| Safety Supply Current            | $R_{\theta JA} = 97 \text{ }^\circ\text{C/W}^1$ , $V_{DDA/B} = 15\text{V}$ , $T_J = 150 \text{ }^\circ\text{C}$ , $T_A = 25 \text{ }^\circ\text{C}$ | Driver A, Driver B | 40    | mA               |
|                                  | $R_{\theta JA} = 97 \text{ }^\circ\text{C/W}^1$ , $V_{DDA/B} = 25\text{V}$ , $T_J = 150 \text{ }^\circ\text{C}$ , $T_A = 25 \text{ }^\circ\text{C}$ | Driver A, Driver B | 24    | mA               |
| Safety Temperature <sup>2)</sup> |   |                    | 150   | $^\circ\text{C}$ |

- 1) Calculate with the junction-to-air thermal resistance,  $R_{\theta JA}$ , of SOW16/SOW14 package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature ( $T_J$ ) specified for the device.

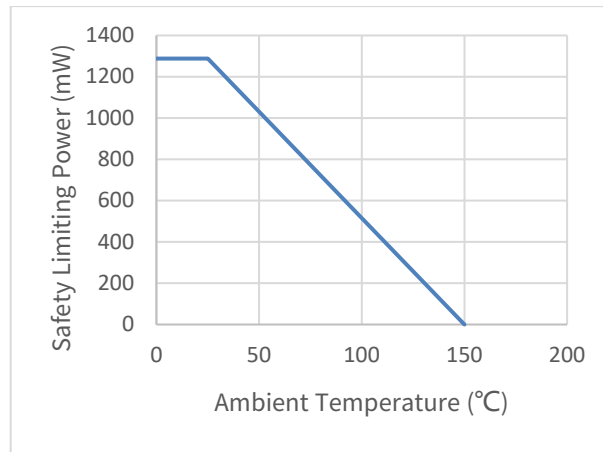


Figure 7.2 NSI66x2x-DSWR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17.

Basic isolation safety-limiting values as outlined in VDE-0884-11 of NSI66x2x-xSPxR (SOP16/SOP14)

| Description                      | Test Condition  | Side               | Value | Unit             |
|----------------------------------|---|--------------------|-------|------------------|
| Safety Supply Power              | $R_{\theta JA} = 150.5 \text{ } ^\circ\text{C/W}^1$ , $T_J = 150 \text{ } ^\circ\text{C}$ , $T_A = 25 \text{ } ^\circ\text{C}$                            | Input              | 90    | mW               |
|                                  |   | Driver A, Driver B | 370   | mW               |
|                                  |   | Total              | 830   | mW               |
| Safety Supply Current            | $R_{\theta JA} = 150.5 \text{ } ^\circ\text{C/W}^1$ , $V_{DDA/B} = 15\text{V}$ , $T_J = 150 \text{ } ^\circ\text{C}$ , $T_A = 25 \text{ } ^\circ\text{C}$ | Driver A, Driver B | 24.7  | mA               |
|                                  | $R_{\theta JA} = 150.5 \text{ } ^\circ\text{C/W}^1$ , $V_{DDA/B} = 25\text{V}$ , $T_J = 150 \text{ } ^\circ\text{C}$ , $T_A = 25 \text{ } ^\circ\text{C}$ | Driver A, Driver B | 14.8  | mA               |
| Safety Temperature <sup>2)</sup> |   |                    | 150   | $^\circ\text{C}$ |

- 1) Calculate with the junction-to-air thermal resistance,  $R_{\theta JA}$ , of SOP16/SOP14 package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature ( $T_J$ ) specified for the device.

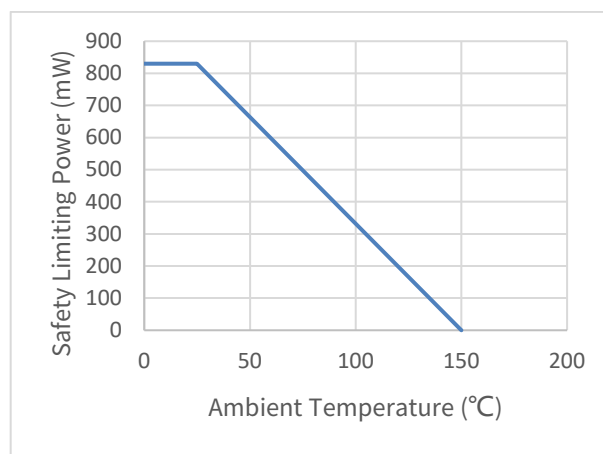


Figure 7.3 NSI66x2x-DSPxR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17.



### 7.3. Safety-Related Certifications

The NSI66x2x-DLAR(LGA13 5x5mm) are approved or pending approval by the organizations listed in table.

| UL                                   |   | VDE                               |                       | CQC                             |
|--------------------------------------|---|-----------------------------------|-----------------------|---------------------------------|
| UL1577 Component Recognition Program | Approved under CSA Component Acceptance Notice 5A | DIN EN IEC 60747-17 (VDE 0884-17) |                       | Certified according to GB4943.1 |
| Single 2500Vrms voltage              | Protection, Isolation                             | Single 2500Vrms voltage           | Protection, Isolation | Basic insulation                |
| E500602                              | E500602   | R50574061                         |                       | CQC21001289933                  |

The NSI66x2x -DSWR are approved or pending approval by the organizations listed in table.

| UL                                    |   | VDE  |                       | CQC                             |
|---------------------------------------|---|--|-----------------------|---------------------------------|
| UL 1577 Component Recognition Program | Approved under CSA Component Acceptance Notice 5A | Certified according to DIN EN IEC 60747-17 (VDE 0884-17) |                       | Certified according to GB4943.1 |
| Single 5700Vrms voltage               | Protection, Isolation                             | Single 5700Vrms voltage                                  | Protection, Isolation | Reinforced insulation           |
| E500602                               | E500602   | 40052820   |                       | CQC20001264939                  |

The NSI66x2x -DSWKR are approved or pending approval by the organizations listed in table.

| UL                                    |   | VDE  |                       | CQC                             |
|---------------------------------------|---|--|-----------------------|---------------------------------|
| UL 1577 Component Recognition Program | Approved under CSA Component Acceptance Notice 5A | Certified according to DIN EN IEC 60747-17 (VDE 0884-17) |                       | Certified according to GB4943.1 |
| Single 5700Vrms voltage               | Protection, Isolation                             | Single 5700Vrms voltage                                  | Protection, Isolation | Reinforced insulation           |
| E500602                               | E500602   | 40052820   |                       | CQC21001289932                  |

The NSI66x2x-DSPNR(SOP16) are approved or pending approval by the organizations listed in table.

| UL | VDE | CQC |
|----|-----|-----|
|----|-----|-----|

|                                       |                         |   |                         |  |                                 |
|---------------------------------------|-------------------------|---|-------------------------|--|---------------------------------|
| UL 1577 Component Recognition Program | Protection, Isolation   | Approved under CSA Component Acceptance Notice 5A | Protection, Isolation   | Certified according to DIN VDE V 0884-17   | Certified according to GB4943.1 |
| Single 3000Vrms voltage               | Single 3000Vrms voltage | Single 3000Vrms voltage                           | Single 3000Vrms voltage | Basic insulation at $V_{IORM}=990V_{peak}$<br>$V_{IOSM}=6000V_{peak}$<br>$V_{IOTM}=4242V_{peak}$ | Basic insulation                |
| E500602                               | E500602                 | E500602   | E500602                 | 40057024   | CQC21001289931                  |

## 8. Function Description

### 8.1. Overview

NSI66x2x is a high reliability dual channel isolated gate driver which could be designed in variety switching power and motor drive topologies. NSI66x2x has some useful protections, such as under voltage lock out (UVLO) for both input and output supply, enable function, deadtime control, default low output as input is floating. The functional circuit block diagram is shown as below:

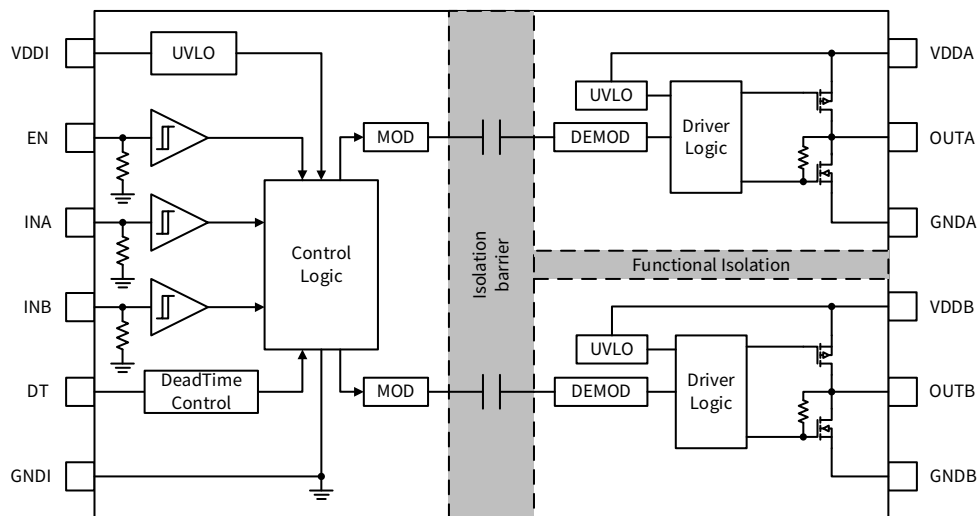


Figure 8.1 Functional Block Diagram (NSI6602N)

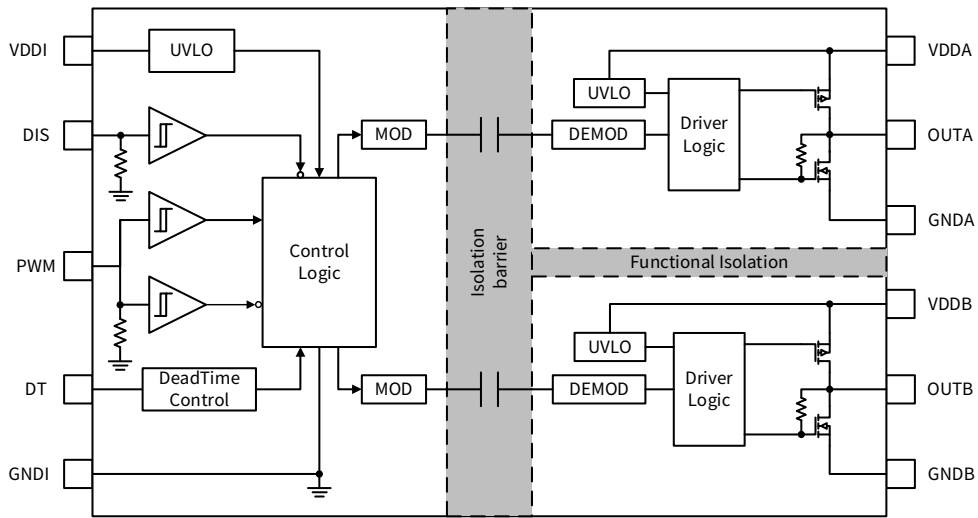


Figure 8.2 Functional Block Diagram (NSI6642)

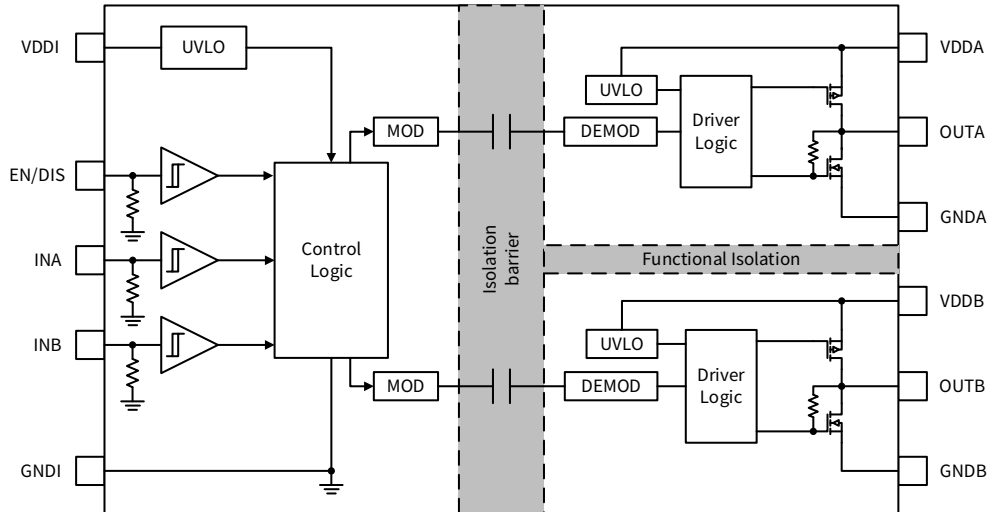


Figure 8.3 Functional Block Diagram (NSI6622x)

### 8.2. Undervoltage Lockout (UVLO)

The NSI66x2x has an internal under voltage lock out (UVLO) protection on both input and output supply circuit blocks. The driver output is held low by an active clamp circuit when the supply voltage of VDDI or VDDA/VDD B is lower than  $V_{VDD\_ON}$  at power-up status or lower than  $V_{VDD\_OFF}$  after power-up, regardless of the status of the input pins.

The VDDI and VDDA/B ULVO protections have hysteresis ( $V_{VDD\_HYS}$ ) to prevent chatter noise from VDD supply and allow small drops in supply power which are usually happened in startup.

### 8.3. Input and Output Logic Table

The table below consists of truth tables for the NSI66x2x families.

Table 8.1 Output status vs Input and Power status (NSI6602N)

| VDDI status | VDDA/B status | EN     | IN     |        | OUT |   | NOTE  |
|-------------|---------------|--------|--------|--------|-----|---|---|
|             |               |        | A      | B      | A   | B |   |
| PU          | PU            | H      | L      | H      | L   | H | If Deadtime function is used, output transits to high after the deadtime expires. |
| PU          | PU            | H      | H      | L      | H   | L |   |
| PU          | PU            | H      | H      | H      | H   | H | DT pin is pulled to VDDI.   |
| PU          | PU            | H      | H      | H      | L   | L | DT is left open or programmed with R <sub>DT</sub> .                              |
| PU          | PU            | H      | L or O | L or O | L   | L |   |
| PU          | PU            | L or O | X      | X      | L   | L | Device is disabled.   |
| PU          | PD            | X      | X      | X      | L   | L |   |
| PD          | PU            | X      | X      | X      | L   | L |   |

Table 8.2 Output status vs Input and Power status (NSI6642)

| VDDI status | VDDA/B status | DIS    | PWM    | OUT |   | NOTE  |
|-------------|---------------|--------|--------|-----|---|---|
|             |               |        |        | A   | B |   |
| PU          | PU            | L or O | L or O | L   | H | If Deadtime function is used, output transits to high after the deadtime expires. |
| PU          | PU            | L or O | H      | H   | L |   |
| PU          | PU            | H      | X      | L   | L | Device is disabled.   |
| PU          | PD            | X      | X      | L   | L |   |
| PD          | PU            | X      | X      | L   | L |   |

Table 8.3 Output status vs Input and Power status (NSI6622N)

| VDDI status | VDDA/B status | EN     | IN     |        | OUT |   | NOTE                |
|-------------|---------------|--------|--------|--------|-----|---|---------------------|
|             |               |        | A      | B      | A   | B |                     |
| PU          | PU            | H      | L      | H      | L   | H |                     |
| PU          | PU            | H      | H      | L      | H   | L |                     |
| PU          | PU            | H      | H      | H      | H   | H |                     |
| PU          | PU            | H      | L or O | L or O | L   | L |                     |
| PU          | PU            | L or O | X      | X      | L   | L | Device is disabled. |

|    |    |   |   |   |   |   |  |
|----|----|---|---|---|---|---|--|
| PU | PD | X | X | X | L | L |  |
| PD | PU | X | X | X | L | L |  |

Table 8.4 Output status vs Input and Power status (NSI6622V)

| VDDI status | VDDA/B status | DIS    | IN     |        | OUT |   | NOTE <sup>1)</sup>  |
|-------------|---------------|--------|--------|--------|-----|---|---------------------|
|             |               |        | A      | B      | A   | B |                     |
| PU          | PU            | L or O | L      | H      | L   | H |                     |
| PU          | PU            | L or O | H      | L      | H   | L |                     |
| PU          | PU            | L or O | H      | H      | H   | H |                     |
| PU          | PU            | L or O | L or O | L or O | L   | L |                     |
| PU          | PU            | H      | X      | X      | L   | L | Device is disabled. |
| PU          | PD            | X      | X      | X      | L   | L |                     |
| PD          | PU            | X      | X      | X      | L   | L |                     |

1) PD= Power Down; PU= Power Up; H= Logic High; L= Logic Low; O= Left Open; X= Irrelevant.

### 8.4. Programmable Deadtime (DT pin)

#### 8.4.1. Pulling the DT Pin to VDDI

This allows outputs match inputs completely and no deadtime is asserted.

#### 8.4.2. DT Pin Left Open or Connected to a Programming Resistor between DT and GNDI Pins

If the DT pin is left open, the deadtime duration ( $t_{DT}$ ) is set to <35ns.  $t_{DT}$  can be programmed by placing a resistor,  $R_{DT}$ , between the DT pin and GNDI. The appropriate  $R_{DT}$  value can be determined from Equation 1, where  $R_{DT}$  is in k $\Omega$  and  $t_{DT}$  in ns:

$$t_{DT} \approx 10 \times R_{DT} \tag{1}$$

The recommended value of  $R_{DT}$  is between from 1k $\Omega$  to 200k $\Omega$ . The steady state voltage at DT pin is about 0.8V and the DT pin current will be less than 10uA when  $R_{DT} = 100k\Omega$ . It is also recommended to parallel a ceramic capacitor, for example 2.2nF, with  $R_{DT}$  to achieve better noise immunity.

The programmed deadtime is activated by the input signal's falling edge to prevent shoot-through when the device is designed in an application of high side and low side driver. The details of input and output logic with deadtime are shown as Figure 8.4:

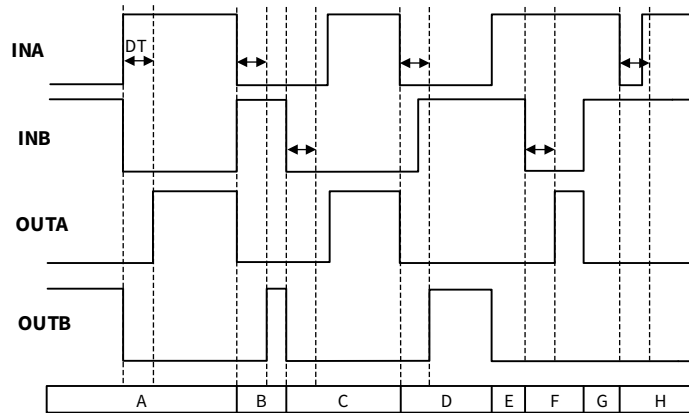


Figure 8.4 Input and Output Logic with the Programmed Deadtime (NSI6602N)

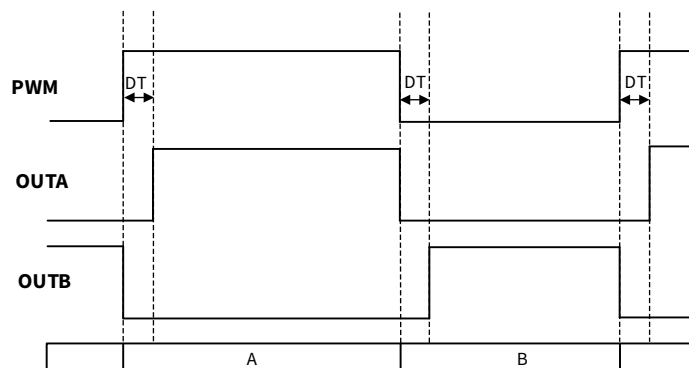


Figure 8.5 Input and Output Logic with the Programmed Deadtime (NSI6642)

| Condition   | Result  |
|---|---|
| A: INA goes high, and INB goes low.                                     | OUTB goes low immediately, then OUTA goes high after the programmed deadtime which is assigned at INB goes low. |
| B: INA goes low, and INB goes high.                                     | OUTA goes low immediately, then OUTB goes high after the programmed deadtime which is assigned at INA goes low. |
| C: INB goes low, then INA goes high after deadtime.                     | OUTB goes low immediately, then OUTA goes high immediately when INA goes high.                                  |
| D: INA goes low, then INB goes high before deadtime.                    | OUTA goes low immediately, then OUTB goes high after deadtime   |
| E: INA goes high, INB is still high.                                    | OUTB goes low immediately and OUTA keeps low.   |
| F: INA is still high, INB goes low.                                     | OUTA goes high after deadtime while INB is low and OUTB keeps low.  |
| G: INA is still high, INB goes high after deadtime                      | OUTA goes low immediately and OUTB keeps low.   |
| H: INA goes low then goes high before deadtime while INB is still high. | OUTA keeps low and OUTB keeps low because deadtime control.   |

### 8.5. ESD Protection

Figure 8.3 shows the multiple diodes involved in the ESD protection part of NSI66x2x.

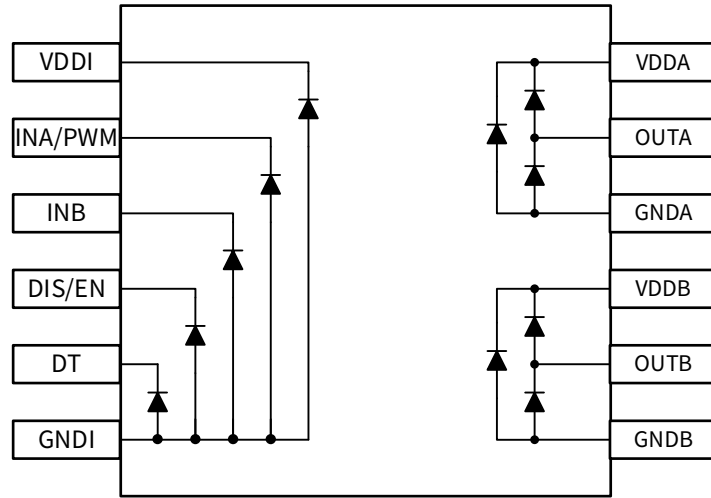


Figure 8.6 ESD Structure (NSI66x2x)

## 9. Application Note

### 9.1. Typical Application Circuit

The circuit shows a typical half-bridge configuration by using the driver NSI66x2x which could be used in several popular power converter topologies such as half-bridge/ full bridge / LLC isolated topologies, buck-boost topologies and 3-phase motor drive applications.

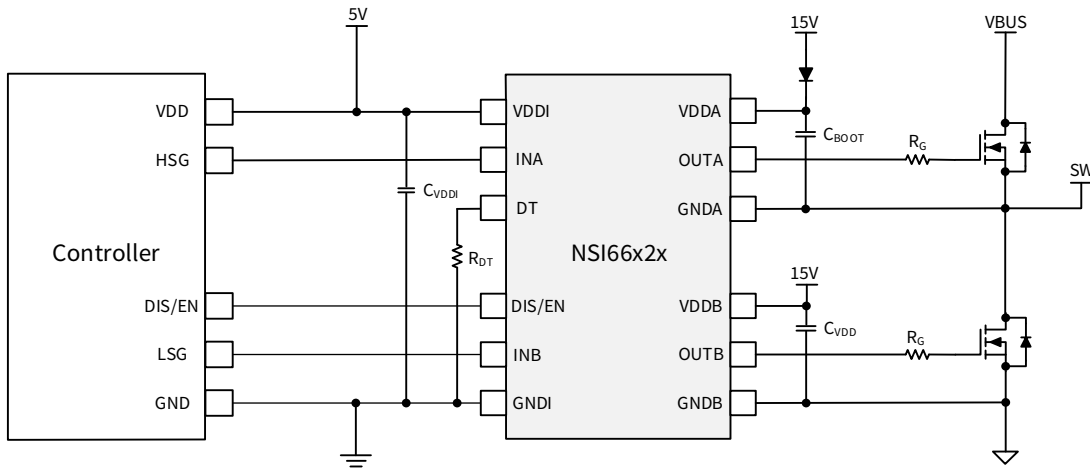


Figure 9.1 Typical Half-Bridge Application Schematic

### 9.2. PCB Layout

PCB layout is important to get optimal performance. Some key guidelines are given as below:

- Low-ESR and low-ESL bypass capacitors should be placed close to the device between pin VDDI to GNDI and pin VDDA/B to GNDA/B.

- There is high frequency switching current that charges and discharges the gate of external power transistor, leading to EMI and ring issues. The parasitic inductance of this loop should be minimized, by decreasing loop area and placing NSI66x2x close to power transistor.
- Large amount of copper should be placed at VDDA/B pin and GNDA/B pin for thermal dissipation.
- To ensure isolation performance between primary and secondary side, the space under the device should keep free from any plane, trace, pad or via.

### 10.Package information

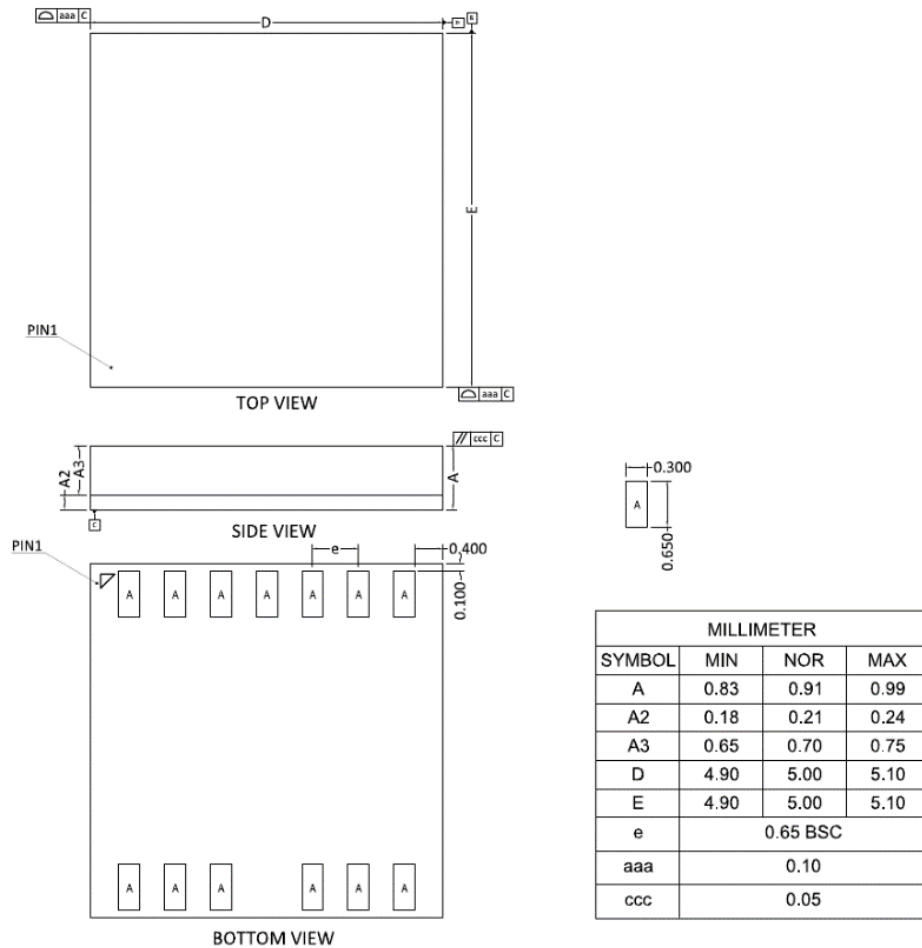


Figure 10.1 LGA13 5-mm x 5-mm Package Shape and Dimension

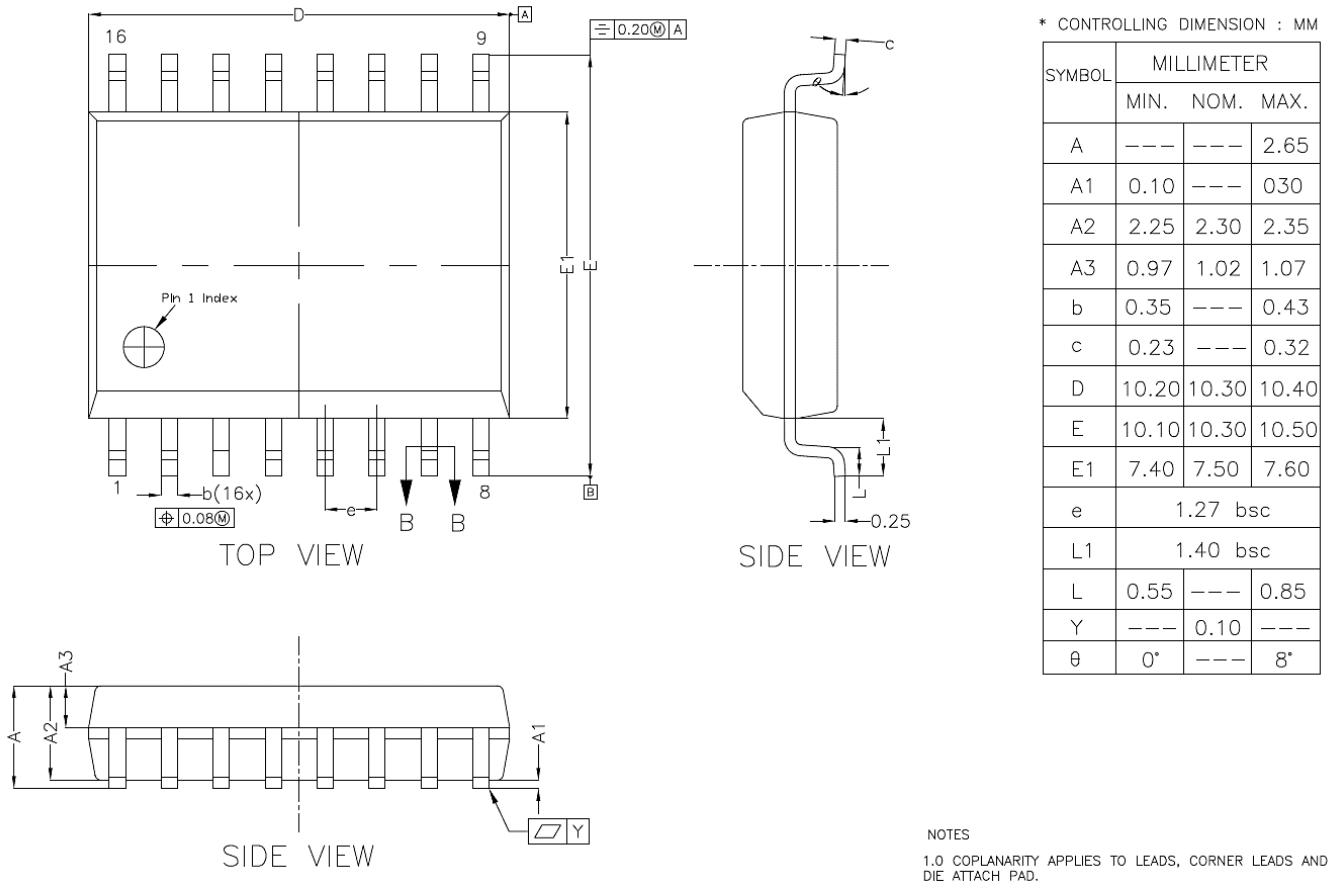


Figure 10.2 SOW16 Package Shape and Dimension

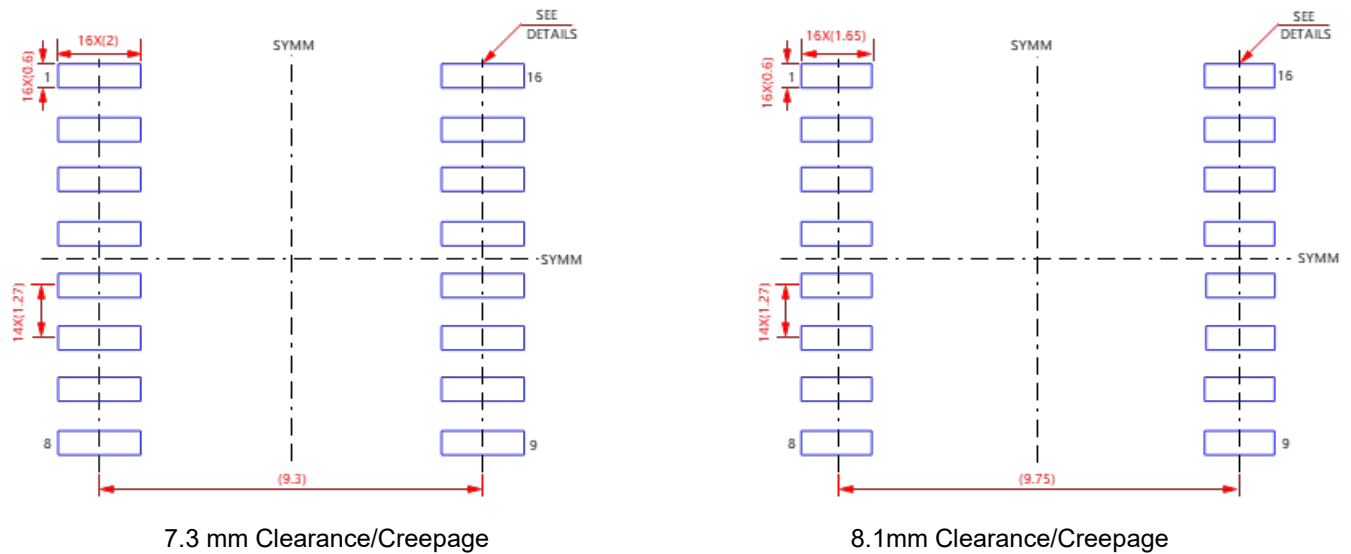


Figure 10.3 SOW16 Package Board Layout Example(mm)

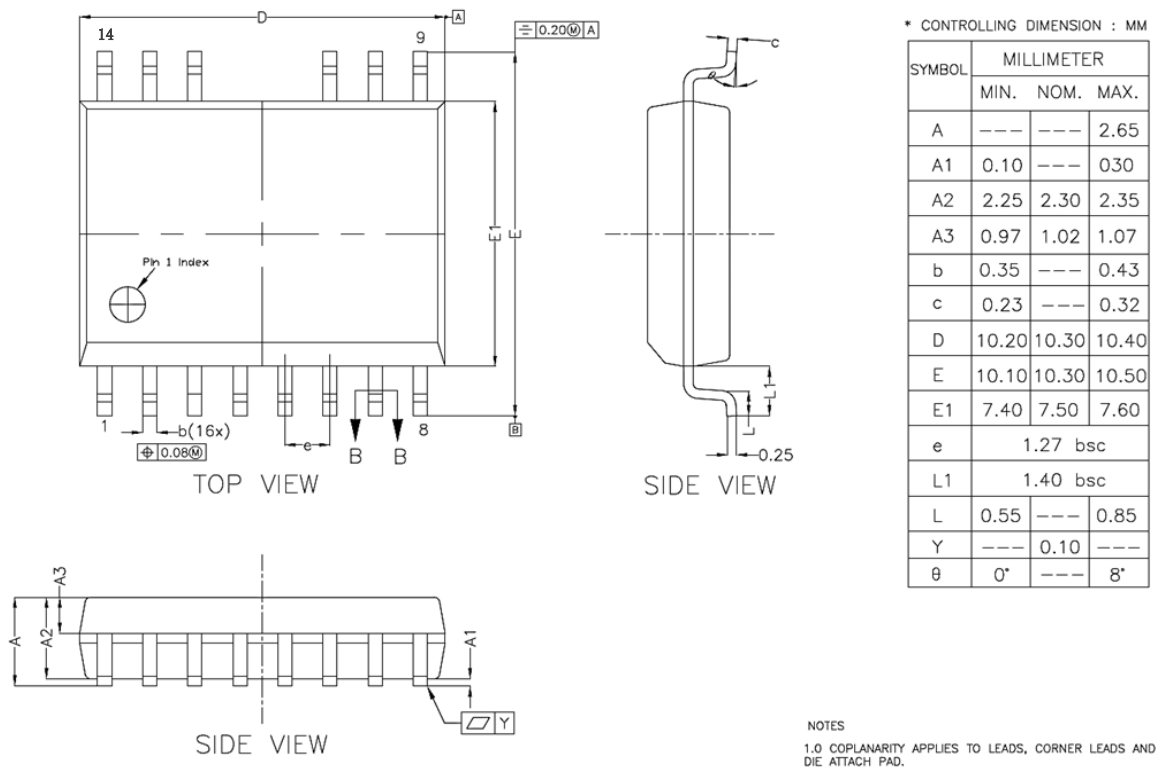


Figure 10.4 SOW14 Package Shape and Dimension

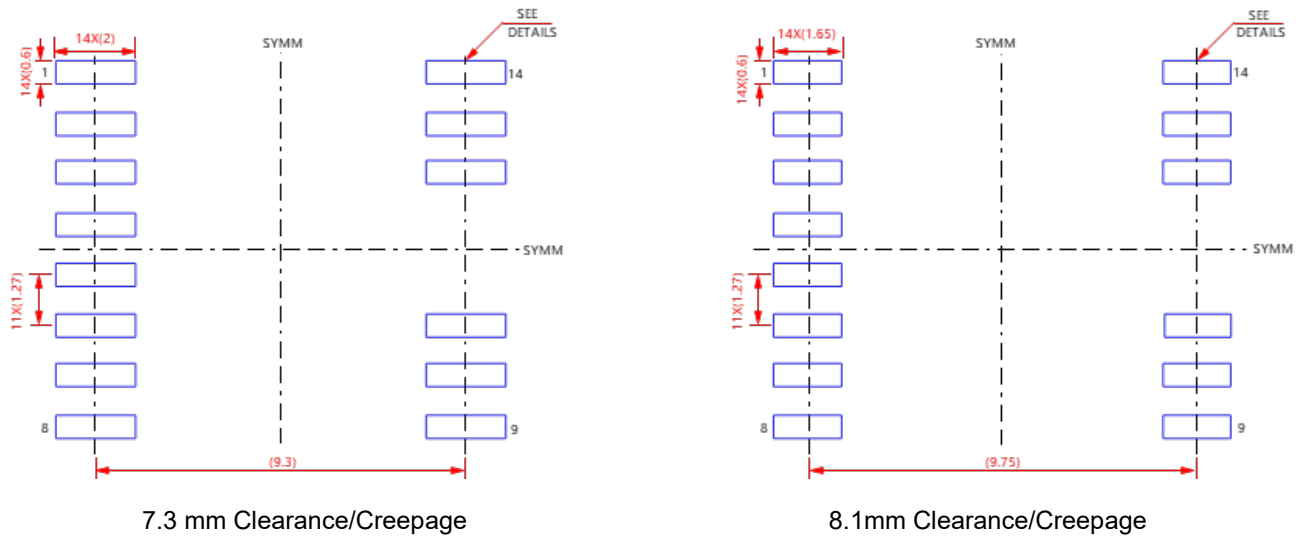


Figure 10.5 SOW14 Package Board Layout Example(mm)

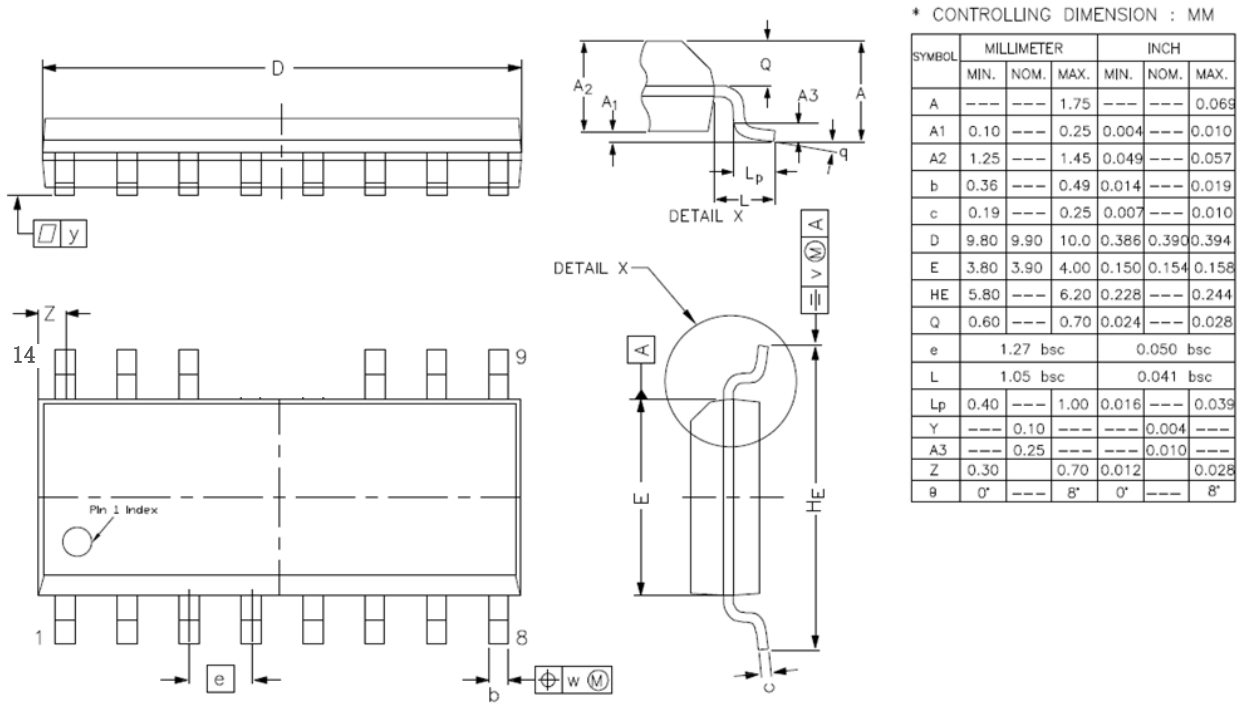


Figure 10.6 SOP14 Package Shape and Dimension

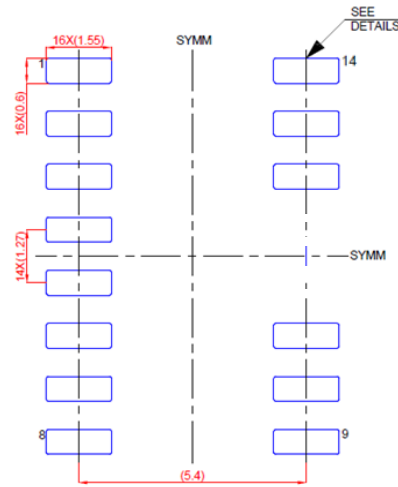
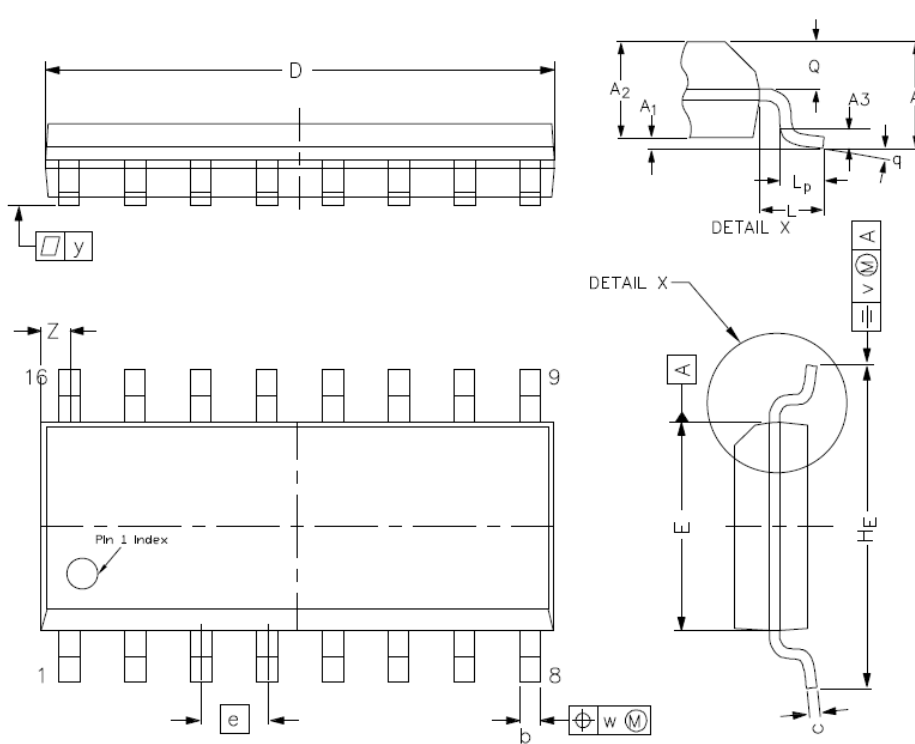


Figure 10.7 SOP14 Package Board Layout Example(mm)



\* CONTROLLING DIMENSION : MM

| SYMBOL | MILLIMETER |      |      | INCH      |       |       |
|--------|------------|------|------|-----------|-------|-------|
|        | MIN.       | NOM. | MAX. | MIN.      | NOM.  | MAX.  |
| A      | ----       | ---- | 1.75 | ----      | ----  | 0.069 |
| A1     | 0.10       | ---- | 0.25 | 0.004     | ----  | 0.010 |
| A2     | 1.25       | ---- | 1.45 | 0.049     | ----  | 0.057 |
| b      | 0.36       | ---- | 0.49 | 0.014     | ----  | 0.019 |
| c      | 0.19       | ---- | 0.25 | 0.007     | ----  | 0.010 |
| D      | 9.80       | 9.90 | 10.0 | 0.386     | 0.390 | 0.394 |
| E      | 3.80       | 3.90 | 4.00 | 0.150     | 0.154 | 0.158 |
| HE     | 5.80       | ---- | 6.20 | 0.228     | ----  | 0.244 |
| Q      | 0.60       | ---- | 0.70 | 0.024     | ----  | 0.028 |
| e      | 1.27 bsc   |      |      | 0.050 bsc |       |       |
| L      | 1.05 bsc   |      |      | 0.041 bsc |       |       |
| Lp     | 0.40       | ---- | 1.00 | 0.016     | ----  | 0.039 |
| Y      | ----       | 0.10 | ---- | ----      | 0.004 | ----  |
| A3     | ----       | 0.25 | ---- | ----      | 0.010 | ----  |
| Z      | 0.30       | ---- | 0.70 | 0.012     | ----  | 0.028 |
| θ      | 0°         | ---- | 8°   | 0°        | ----  | 8°    |

Figure 10.8 SOP16 Package Shape and Dimension

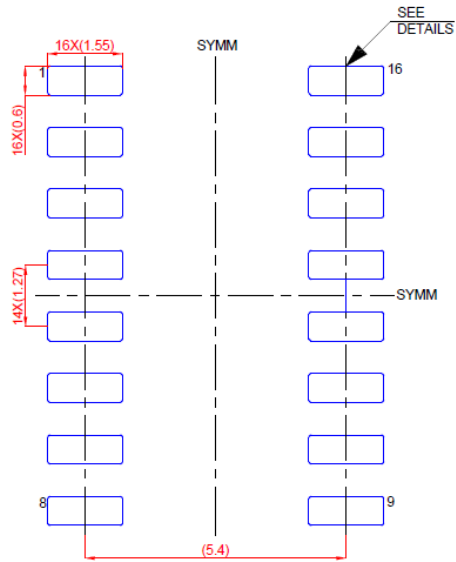


Figure 10.9 SOP16 Package Board Layout Example(mm)

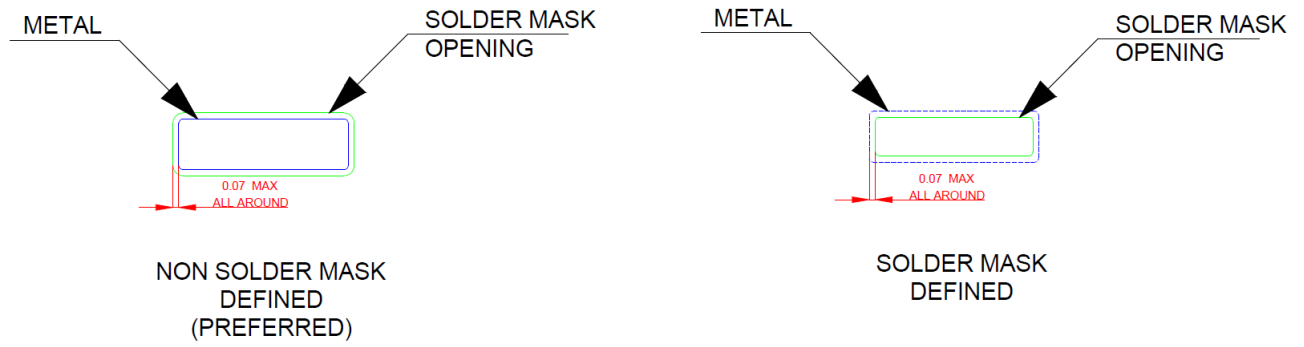


Figure 10.10 Solder Mask Details(mm)

11. Ordering Information

| Part No.        | Isolation Rating (kV <sub>RMS</sub> ) | Driver-side UVLO TYP. | Temperature  | Body Size (mm) | Package      | MSL | SPQ  |
|-----------------|---------------------------------------|-----------------------|--------------|----------------|--------------|-----|------|
| NSI6602NA-DLAR  | 2.5                                   | 6V                    | -40 to 125°C | 5X5X0.91       | LGA13(5x5mm) | 3   | 3000 |
| NSI6602NA-DSWR  | 5.7                                   | 6V                    | -40 to 125°C | 10.3X7.5X2.65  | SOW16        | 2   | 1000 |
| NSI6602NA-DSWKR | 5.7                                   | 6V                    | -40 to 125°C | 10.3X7.5X2.65  | SOW14        | 2   | 1000 |
| NSI6602NA-DSPNR | 3.0                                   | 6V                    | -40 to 125°C | 9.9X3.9X1.75   | SOP16        | 2   | 2500 |
| NSI6602NA-DSPOR | 3.0                                   | 6V                    | -40 to 125°C | 9.9X3.9X1.75   | SOP14        | 2   | 2500 |
| NSI6602NB-DLAR  | 2.5                                   | 8V                    | -40 to 125°C | 5X5X0.91       | LGA13(5x5mm) | 3   | 3000 |
| NSI6602NB-DSWR  | 5.7                                   | 8V                    | -40 to 125°C | 10.3X7.5X2.65  | SOW16        | 2   | 1000 |
| NSI6602NB-DSWKR | 5.7                                   | 8V                    | -40 to 125°C | 10.3X7.5X2.65  | SOW14        | 2   | 1000 |
| NSI6602NB-DSPNR | 3.0                                   | 8V                    | -40 to 125°C | 9.9X3.9X1.75   | SOP16        | 2   | 2500 |
| NSI6602NB-DSPOR | 3.0                                   | 8V                    | -40 to 125°C | 9.9X3.9X1.75   | SOP14        | 2   | 2500 |
| NSI6602NC-DLAR  | 2.5                                   | 13V                   | -40 to 125°C | 5X5X0.91       | LGA13(5x5mm) | 3   | 3000 |
| NSI6602NC-DSWR  | 5.7                                   | 13V                   | -40 to 125°C | 10.3X7.5X2.65  | SOW16        | 2   | 1000 |
| NSI6602NC-DSWKR | 5.7                                   | 13V                   | -40 to 125°C | 10.3X7.5X2.65  | SOW14        | 2   | 1000 |
| NSI6602NC-DSPNR | 3.0                                   | 13V                   | -40 to 125°C | 9.9X3.9X1.75   | SOP16        | 2   | 2500 |
| NSI6602NC-DSPOR | 3.0                                   | 13V                   | -40 to 125°C | 9.9X3.9X1.75   | SOP14        | 2   | 2500 |
| NSI6602ND-DLAR  | 2.5                                   | 4V                    | -40 to 125°C | 5X5X0.91       | LGA13(5x5mm) | 3   | 3000 |
| NSI6602ND-DSWR  | 5.7                                   | 4V                    | -40 to 125°C | 10.3X7.5X2.65  | SOW16        | 2   | 1000 |
| NSI6602ND-DSWKR | 5.7                                   | 4V                    | -40 to 125°C | 10.3X7.5X2.65  | SOW14        | 2   | 1000 |
| NSI6602ND-DSPNR | 3.0                                   | 4V                    | -40 to 125°C | 9.9X3.9X1.75   | SOP16        | 2   | 2500 |
| NSI6602ND-DSPOR | 3.0                                   | 4V                    | -40 to 125°C | 9.9X3.9X1.75   | SOP14        | 2   | 2500 |
| NSI6642A-DLAR   | 2.5                                   | 6V                    | -40 to 125°C | 5X5X0.91       | LGA13(5x5mm) | 3   | 3000 |
| NSI6642A-DSWR   | 5.7                                   | 6V                    | -40 to 125°C | 10.3X7.5X2.65  | SOW16        | 2   | 1000 |
| NSI6642A-DSWKR  | 5.7                                   | 6V                    | -40 to 125°C | 10.3X7.5X2.65  | SOW14        | 2   | 1000 |
| NSI6642A-DSPNR  | 3.0                                   | 6V                    | -40 to 125°C | 9.9X3.9X1.75   | SOP16        | 2   | 2500 |
| NSI6642A-DSPOR  | 3.0                                   | 6V                    | -40 to 125°C | 9.9X3.9X1.75   | SOP14        | 2   | 2500 |

|                 |     |     |              |               |              |   |      |
|-----------------|-----|-----|--------------|---------------|--------------|---|------|
| NSI6642B-DLAR   | 2.5 | 8V  | -40 to 125°C | 5X5X0.91      | LGA13(5x5mm) | 3 | 3000 |
| NSI6642B-DSWR   | 5.7 | 8V  | -40 to 125°C | 10.3X7.5X2.65 | SOW16        | 2 | 1000 |
| NSI6642B-DSWKR  | 5.7 | 8V  | -40 to 125°C | 10.3X7.5X2.65 | SOW14        | 2 | 1000 |
| NSI6642B-DSPNR  | 3.0 | 8V  | -40 to 125°C | 9.9X3.9X1.75  | SOP16        | 2 | 2500 |
| NSI6642B-DSPOR  | 3.0 | 8V  | -40 to 125°C | 9.9X3.9X1.75  | SOP14        | 2 | 2500 |
| NSI6642C-DLAR   | 2.5 | 13V | -40 to 125°C | 5X5X0.91      | LGA13(5x5mm) | 3 | 3000 |
| NSI6642C-DSWR   | 5.7 | 13V | -40 to 125°C | 10.3X7.5X2.65 | SOW16        | 2 | 1000 |
| NSI6642C-DSWKR  | 5.7 | 13V | -40 to 125°C | 10.3X7.5X2.65 | SOW14        | 2 | 1000 |
| NSI6642C-DSPNR  | 3.0 | 13V | -40 to 125°C | 9.9X3.9X1.75  | SOP16        | 2 | 2500 |
| NSI6642C-DSPOR  | 3.0 | 13V | -40 to 125°C | 9.9X3.9X1.75  | SOP14        | 2 | 2500 |
| NSI6642D-DLAR   | 2.5 | 4V  | -40 to 125°C | 5X5X0.91      | LGA13(5x5mm) | 3 | 3000 |
| NSI6642D-DSWR   | 5.7 | 4V  | -40 to 125°C | 10.3X7.5X2.65 | SOW16        | 2 | 1000 |
| NSI6642D-DSWKR  | 5.7 | 4V  | -40 to 125°C | 10.3X7.5X2.65 | SOW14        | 2 | 1000 |
| NSI6642D-DSPNR  | 3.0 | 4V  | -40 to 125°C | 9.9X3.9X1.75  | SOP16        | 2 | 2500 |
| NSI6642D-DSPOR  | 3.0 | 4V  | -40 to 125°C | 9.9X3.9X1.75  | SOP14        | 2 | 2500 |
| NSI6622NA-DLAR  | 2.5 | 6V  | -40 to 125°C | 5X5X0.91      | LGA13(5x5mm) | 3 | 3000 |
| NSI6622NA-DSWR  | 5.7 | 6V  | -40 to 125°C | 10.3X7.5X2.65 | SOW16        | 2 | 1000 |
| NSI6622NA-DSWKR | 5.7 | 6V  | -40 to 125°C | 10.3X7.5X2.65 | SOW14        | 2 | 1000 |
| NSI6622NA-DSPNR | 3.0 | 6V  | -40 to 125°C | 9.9X3.9X1.75  | SOP16        | 2 | 2500 |
| NSI6622NA-DSPOR | 3.0 | 6V  | -40 to 125°C | 9.9X3.9X1.75  | SOP14        | 2 | 2500 |
| NSI6622NB-DLAR  | 2.5 | 8V  | -40 to 125°C | 5X5X0.91      | LGA13(5x5mm) | 3 | 3000 |
| NSI6622NB-DSWR  | 5.7 | 8V  | -40 to 125°C | 10.3X7.5X2.65 | SOW16        | 2 | 1000 |
| NSI6622NB-DSWKR | 5.7 | 8V  | -40 to 125°C | 10.3X7.5X2.65 | SOW14        | 2 | 1000 |
| NSI6622NB-DSPNR | 3.0 | 8V  | -40 to 125°C | 9.9X3.9X1.75  | SOP16        | 2 | 2500 |
| NSI6622NB-DSPOR | 3.0 | 8V  | -40 to 125°C | 9.9X3.9X1.75  | SOP14        | 2 | 2500 |
| NSI6622NC-DLAR  | 2.5 | 13V | -40 to 125°C | 5X5X0.91      | LGA13(5x5mm) | 3 | 3000 |
| NSI6622NC-DSWR  | 5.7 | 13V | -40 to 125°C | 10.3X7.5X2.65 | SOW16        | 2 | 1000 |
| NSI6622NC-DSWKR | 5.7 | 13V | -40 to 125°C | 10.3X7.5X2.65 | SOW14        | 2 | 1000 |

|                 |     |     |              |               |              |   |      |
|-----------------|-----|-----|--------------|---------------|--------------|---|------|
| NSI6622NC-DSPNR | 3.0 | 13V | -40 to 125°C | 9.9X3.9X1.75  | SOP16        | 2 | 2500 |
| NSI6622NC-DSPOR | 3.0 | 13V | -40 to 125°C | 9.9X3.9X1.75  | SOP14        | 2 | 2500 |
| NSI6622ND-DLAR  | 2.5 | 4V  | -40 to 125°C | 5X5X0.91      | LGA13(5x5mm) | 3 | 3000 |
| NSI6622ND-DSWR  | 5.7 | 4V  | -40 to 125°C | 10.3X7.5X2.65 | SOW16        | 2 | 1000 |
| NSI6622ND-DSWKR | 5.7 | 4V  | -40 to 125°C | 10.3X7.5X2.65 | SOW14        | 2 | 1000 |
| NSI6622ND-DSPNR | 3.0 | 4V  | -40 to 125°C | 9.9X3.9X1.75  | SOP16        | 2 | 2500 |
| NSI6622ND-DSPOR | 3.0 | 4V  | -40 to 125°C | 9.9X3.9X1.75  | SOP14        | 2 | 2500 |
| NSI6622VA-DLAR  | 2.5 | 6V  | -40 to 125°C | 5X5X0.91      | LGA13(5x5mm) | 3 | 3000 |
| NSI6622VA-DSWR  | 5.7 | 6V  | -40 to 125°C | 10.3X7.5X2.65 | SOW16        | 2 | 1000 |
| NSI6622VA-DSWKR | 5.7 | 6V  | -40 to 125°C | 10.3X7.5X2.65 | SOW14        | 2 | 1000 |
| NSI6622VA-DSPNR | 3.0 | 6V  | -40 to 125°C | 9.9X3.9X1.75  | SOP16        | 2 | 2500 |
| NSI6622VA-DSPOR | 3.0 | 6V  | -40 to 125°C | 9.9X3.9X1.75  | SOP14        | 2 | 2500 |
| NSI6622VB-DLAR  | 2.5 | 8V  | -40 to 125°C | 5X5X0.91      | LGA13(5x5mm) | 3 | 3000 |
| NSI6622VB-DSWR  | 5.7 | 8V  | -40 to 125°C | 10.3X7.5X2.65 | SOW16        | 2 | 1000 |
| NSI6622VB-DSWKR | 5.7 | 8V  | -40 to 125°C | 10.3X7.5X2.65 | SOW14        | 2 | 1000 |
| NSI6622VB-DSPNR | 3.0 | 8V  | -40 to 125°C | 9.9X3.9X1.75  | SOP16        | 2 | 2500 |
| NSI6622VB-DSPOR | 3.0 | 8V  | -40 to 125°C | 9.9X3.9X1.75  | SOP14        | 2 | 2500 |
| NSI6622VC-DLAR  | 2.5 | 13V | -40 to 125°C | 5X5X0.91      | LGA13(5x5mm) | 3 | 3000 |
| NSI6622VC-DSWR  | 5.7 | 13V | -40 to 125°C | 10.3X7.5X2.65 | SOW16        | 2 | 1000 |
| NSI6622VC-DSWKR | 5.7 | 13V | -40 to 125°C | 10.3X7.5X2.65 | SOW14        | 2 | 1000 |
| NSI6622VC-DSPNR | 3.0 | 13V | -40 to 125°C | 9.9X3.9X1.75  | SOP16        | 2 | 2500 |
| NSI6622VC-DSPOR | 3.0 | 13V | -40 to 125°C | 9.9X3.9X1.75  | SOP14        | 2 | 2500 |
| NSI6622VD-DLAR  | 2.5 | 4V  | -40 to 125°C | 5X5X0.91      | LGA13(5x5mm) | 3 | 3000 |
| NSI6622VD-DSWR  | 5.7 | 4V  | -40 to 125°C | 10.3X7.5X2.65 | SOW16        | 2 | 1000 |
| NSI6622VD-DSWKR | 5.7 | 4V  | -40 to 125°C | 10.3X7.5X2.65 | SOW14        | 2 | 1000 |
| NSI6622VD-DSPNR | 3.0 | 4V  | -40 to 125°C | 9.9X3.9X1.75  | SOP16        | 2 | 2500 |
| NSI6622VD-DSPOR | 3.0 | 4V  | -40 to 125°C | 9.9X3.9X1.75  | SOP14        | 2 | 2500 |

## 12. Tape and Reel Information

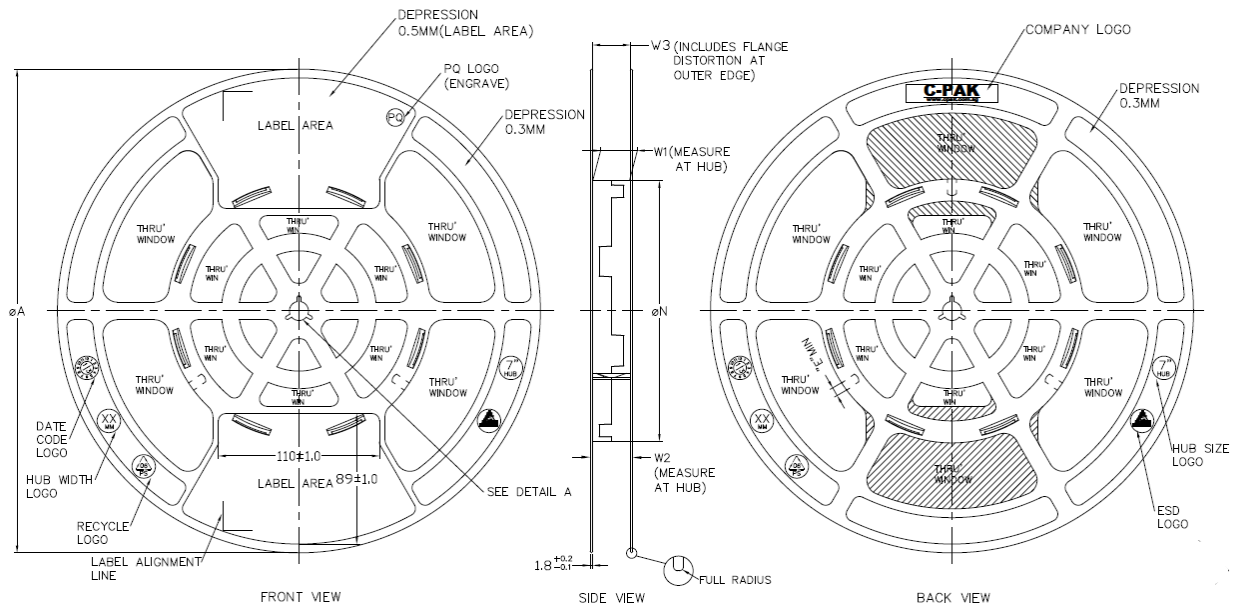


Figure 12.1 Tape Information

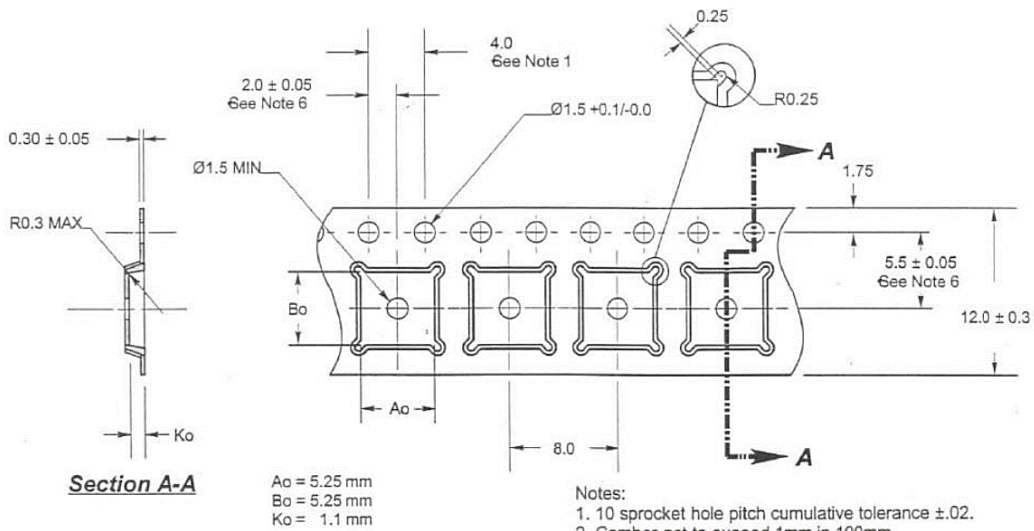
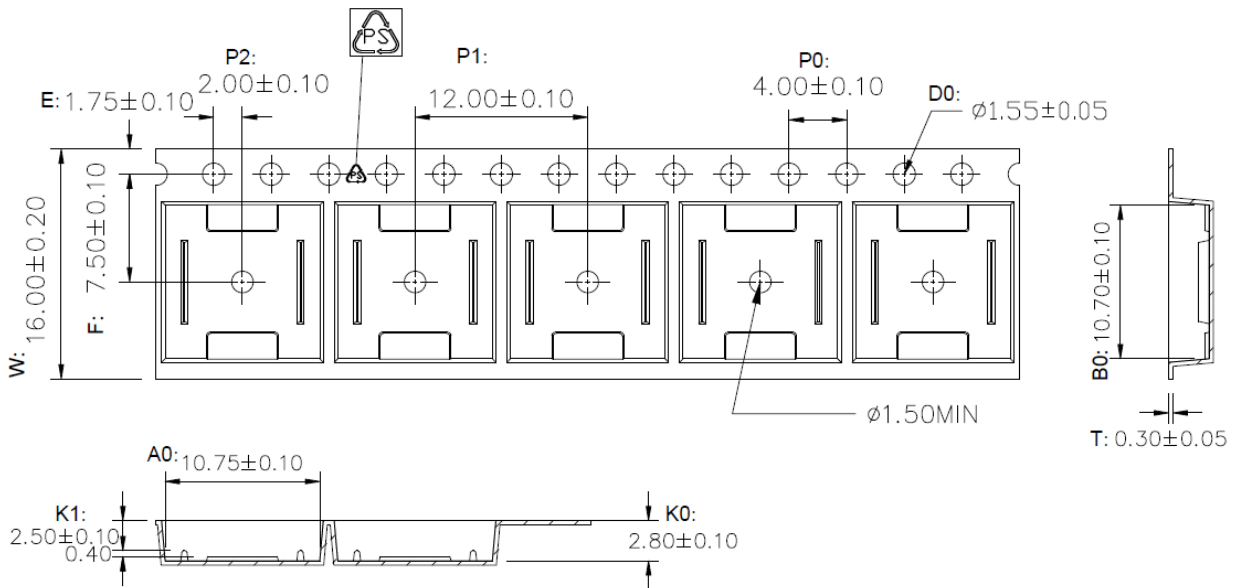


Figure 12.2 LGA13 Reel Information



1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.20$ .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy .
4. All dimensions meet EIA-481 requirements.
5. Thickness :  $0.30 \pm 0.05$ mm.
6. Packing length per 22" reel : 378 Meters.(N=122)
7. Component load per 13" reel : 1000 pcs.

Figure 12.3 SOW16/SOW14 Reel Information

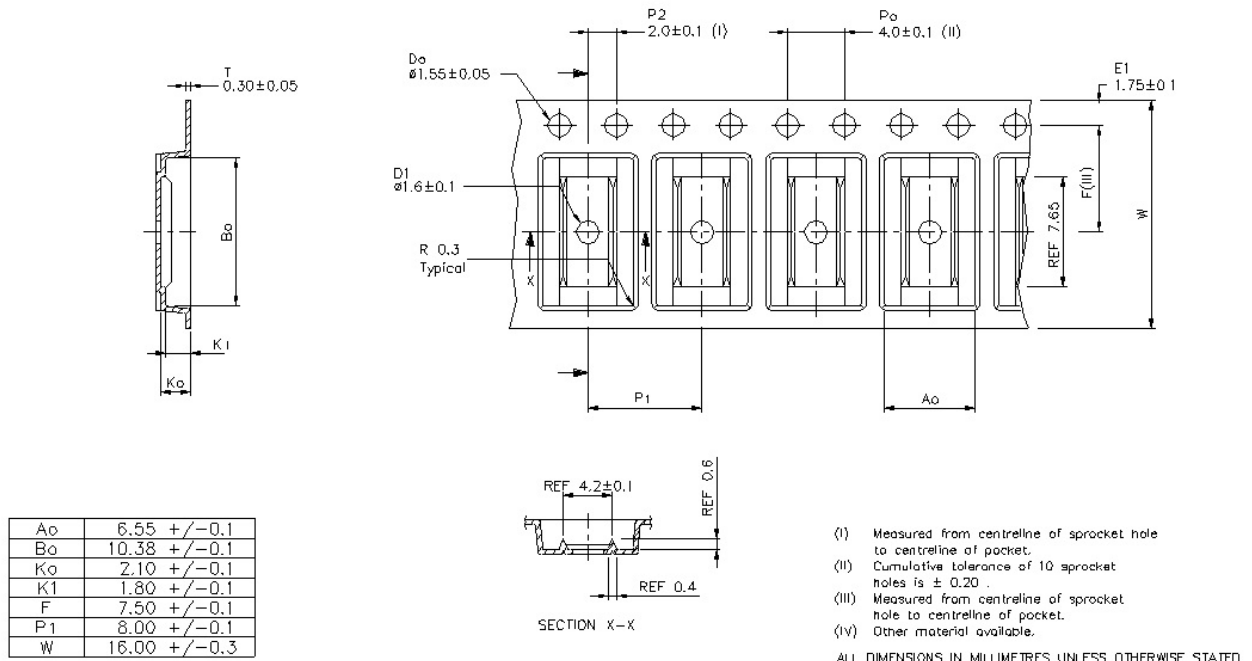


Figure 12.4 SOP16/SOP14 Reel Information

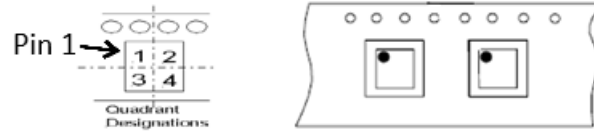


Figure 12.5 Quadrant Designation for Pin1 Orientation in Tape

### 13.Revision History

| <b>Revision</b> | <b>Description</b>  | <b>Date</b> |
|-----------------|---|-------------|
| 1.0             | Initial version   | 2023/7/10   |
| 1.1             | 1. Update the PIN description of DT.<br>2. Modify the isolation safety-limiting values.<br>3. Update the number of safety - related certifications. | 2025/1/13   |

## **IMPORTANT NOTICE**

The information given in this document (the “Document”) shall in no event be regarded as any warranty or authorization of, express or implied, including but not limited to accuracy, completeness, merchantability, fitness for a particular purpose or infringement of any third party’s intellectual property rights.

Users of this Document shall be solely responsible for the use of NOVOSENSE’s products and applications, and for the safety thereof. Users shall comply with all laws, regulations and requirements related to NOVOSENSE’s products and applications, although information or support related to any application may still be provided by NOVOSENSE.

This Document is provided on an “AS IS” basis, and is intended only for skilled developers designing with NOVOSENSE’s products. NOVOSENSE reserves the rights to make corrections, modifications, enhancements, improvements or other changes to the products and services provided without notice. NOVOSENSE authorizes users to use this Document exclusively for the development of relevant applications or systems designed to integrate NOVOSENSE’s products. No license to any intellectual property rights of NOVOSENSE is granted by implication or otherwise. Using this Document for any other purpose, or any unauthorized reproduction or display of this Document is strictly prohibited. In no event shall NOVOSENSE be liable for any claims, damages, costs, losses or liabilities arising out of or in connection with this Document or the use of this Document.

For further information on applications, products and technologies, please contact NOVOSENSE ([www.novosns.com](http://www.novosns.com)).

**Suzhou NOVOSENSE Microelectronics Co., Ltd**