NOVOSENSE

NSI6601xE

Single-Channel Isolated Gate Driver

Datasheet (EN) 1.0

Product Overview

The NSI6601xE is a family of single-channel isolated gate drivers designed to drive IGBTs, power MOSFETs and SiC MOSFETs in many applications. The NSI6601AE provides split output that controls the rise and fall times individually. The NSI6601ME connects the gate of the transistor to an internal clamp to prevent false turn-on caused by Miller current. It can source and sink 10A peak current.

The NSI6601xE is available in SOP8 or SOW8 package, and can support 3000VRMS and 5700VRMS isolation per UL1577 respectively. System robustness is supported by 150kV/μs minimum common-mode transient immunity (CMTI).

The driver operates with a maximum supply voltage of 32V, while the input-side accepts supply voltage from 3.1V to 17V. Under voltage lock-out (UVLO) protection is supported by all the power supply voltage pins.

Because of high driving current ability, excellent robustness, wide supply voltage range and fast signal propagation, NSI6601xE is suitable for high reliability, high power density and highly efficient switching power system.

Key Features

- Isolated single-channel driver
- Miller Clamp options (NSI6601MEB/MEC/MED/MEF)
- Split output (NSI6601AEB/AEC/AED/AEF)
- Input side supply voltage: 3.1V to 17V
- Driver side supply voltage: up to 32V with 5V, 8V, 12V and 17V UVLO options
- 10A peak source and sink output current
- Minimum CMTI: ±150kV/μs
- 85ns typical propagation delay
- Operation ambient temperature: -40°C ~125°C
- RoHS & REACH compliance
- Lead-free component, suitable for lead-free soldering profile: 260°C, MSL3

Safety Regulatory Approvals

- UL recognition: Isolation rating of 3000VRMS SOP8 and 5700VRMS SOW8 for 1 minute per UL1577
- DIN EN IEC 60747-17(VDE V 0884-17):2021-10
- CSA component notice 5A
- CQC certification per GB4943.1-2011

Applications

- Isolated DC/DC and AC/DC Power Supplies
- High Voltage PFC
- Solar Inverters
- Motor Drives and EV Charging
- UPS and Battery Chargers

Block Diagram

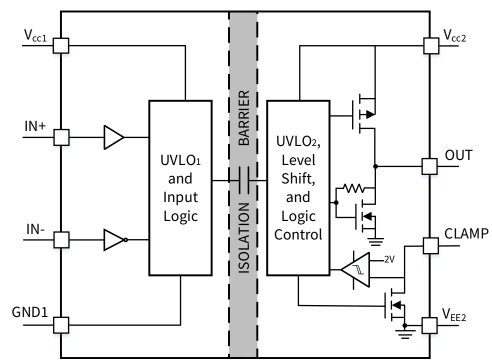

Figure 0.1 NSI6601ME Diagram

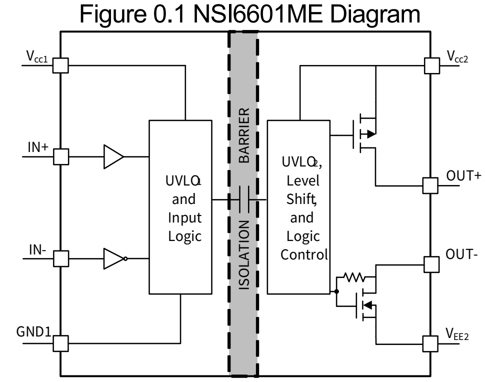

Figure 0.2 NSI6601AE Diagram

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1. Pin Configuration and Function

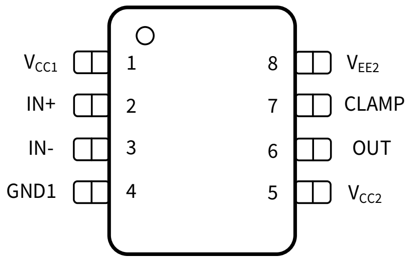


Figure 1.1 NSI6601ME Versions
(Top View)

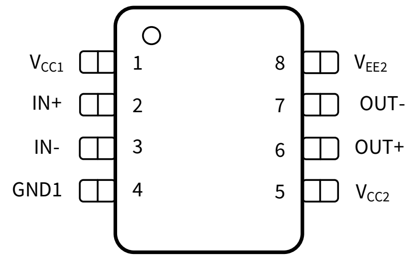


Figure 1.2 NSI6601AE Versions
(Top View)

Table 1.1 NSI6601xE Pin Configuration and Description

Pin Name	***Pin NO.***		***Function***
	NSI6601ME	*NSI6601AE*	
V_{CC1}	1	1	Input-side supply rail
IN+	2	2	Non-inverted input signal with internal pull down to GND1
IN-	3	3	Inverted input signal with internal pull up to VCC1
GND1	4	4	Input-side ground reference
V_{CC2}	5	5	Positive output supply rail
OUT	6	/	Gate Driver Output
CLAMP	7	/	Active Miller-Clamp input
OUT+	/	6	Gate Driver pull-up Output
OUT-	/	7	Gate Driver pull-down Output
V_{EE2}	8	8	Driver-side ground reference

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
Input Side Supply Voltage	V_{CC1}-GND1	-0.3	18	V
Input Signal Voltage	V_{IN+}-GND1, V_{IN-}-GND1	-0.3	18	V
Driver Side Supply Voltage	V_{CC2}-V_{EE2}	-0.3	35	V
Output Signal Voltage	V_{OUT}-V_{EE2}, V_{CLAMP}-V_{EE2}, V_{OUT+}-V_{EE2+}, V_{OUT-}-V_{EE2}	-0.3	V_{CC2}+0.3	V
Operating Junction Temperature	T_J	-40	150	°C
Storage Temperature	T_{stg}	-65	150	°C

3. ESD Ratings

Ratings		Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD ● All pins	±2000	V
	Charged device model (CDM), per AEC-Q100-011-RevB ● All pins	±1500	V

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
Input Side Supply Voltage	V_{CC1}-GND1	3.1	17	V
Input Signal Voltage	V_{IN+}-GND1, V_{IN-}-GND1	-0.3	17	V
Driver Side Supply Voltage	V_{CC2}-V_{EE2} (NSI6601MEB/AEB)	9.5	32	V
	V_{CC2}-V_{EE2} (NSI6601MEC/AEC)	13.5	32	
	V_{CC2}-V_{EE2} (NSI6601MED/AED)	6	32	
	V_{CC2}-V_{EE2} (NSI6601MEF/AEF)	18.5	32	
Ambient Temperature	T_A	-40	125	°C

5. Thermal Information

Parameters	Symbol	SOP8	SOW8	Unit
Junction–to-ambient thermal resistance(1)	R_{JA}	120	110	°C/W
Junction–to-top characterization parameter(2)	Ψ_{JT}	38	18	°C/W

1) Tested using High Effective Thermal Conductivity Test Board (2s2p) described in JESD51-7
2) Tested following the environment described in JESD51-7

6. Specifications

6.1. DC Electrical Characteristics

Use V_{CC1}=5V, with a bypass capacitor of 1μF from V_{CC1} to GND1, and V_{CC2}=15V with a capacitor of 10μF from V_{CC2} to V_{EE2} where V_{EE2}=GND2. Positive and negative symbols represent the current into and out of the specified terminal (unless otherwise noted).

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply Currents						
Input Supply Quiescent Current	I_{CC1}		0.9	1.5	mA	V_{IN+}= GND1, V_{IN-}=5V
Output Supply Quiescent Current	I_{CC2}		1.3	2.2	mA	V_{IN+}= GND1, V_{IN-}=GND1
Input Side Supply UVLO Threshold						
VCC1 UVLO Rising Threshold	V_{CC1_ON}		2.9	3.1	V	V_{IN+}=5V, V_{IN-}=GND1
VCC1 UVLO Falling Threshold	V_{CC1_OFF}	2.55	2.78		V	V_{IN+}=5V, V_{IN-}=GND1
VCC1 UVLO Hysteresis1)	V_{CC1_HYS}		0.12		V	
Driver Side Supply UVLO Threshold (NSI6601MEB/AEB 8V UVLO Level)						
VCC2 UVLO Rising Threshold	V_{CC2_ON}	8.1	8.5	8.9	V	V_{IN+}=5V, V_{IN-}=GND1
VCC2 UVLO Falling Threshold	V_{CC2_OFF}	7.6	8	8.4	V	V_{IN+}=5V, V_{IN-}=GND1
VCC2 UVLO Hysteresis1)	V_{CC2_HYS}		0.5		V	
Driver Side Supply UVLO Threshold (NSI6601MEC/AEC 12V UVLO Level)						
VCC UVLO Rising Threshold	V_{CC2_ON}	11.4	12	12.6	V	V_{IN+}=5V, V_{IN-}=GND1
VCC UVLO Falling Threshold	V_{CC2_OFF}	10.4	11	11.6	V	V_{IN+}=5V, V_{IN-}=GND1
VCC UVLO Hysteresis1)	V_{CC2_HYS}		1		V	
Driver Side Supply UVLO Threshold (NSI6601MED/AED 5V UVLO Level)						
VCC UVLO Rising Threshold	V_{CC2_ON}	4.5	5	5.5	V	V_{IN+}=5V, V_{IN-}=GND1
VCC UVLO Falling Threshold	V_{CC2_OFF}	4.0	4.5	5.0	V	V_{IN+}=5V, V_{IN-}=GND1
VCC UVLO Hysteresis1)	V_{CC2_HYS}		0.5		V	

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Driver Side Supply UVLO Threshold (NSI6601MEF/AEF 17V UVLO Level)						
VCC UVLO Rising Threshold	V_{CC2_ON}	16.3	17	17.7	V	V_{IN+}=5V, V_{IN-}=GND1
VCC UVLO Falling Threshold	V_{CC2_OFF}	15.3	16	16.7	V	V_{IN+}=5V, V_{IN-}=GND1
VCC UVLO Hysteresis[1)]	V_{CC2_HYS}		1		V	
Input Pin Characteristics						
Logic High Input Threshold (IN+, IN-)	V_{IN+H}, V_{IN-H}		0.55×V_{CC1}	0.7×V_{CC1}	V	
Logic Low Input Threshold (IN+, IN-)	V_{IN+L}, V_{IN-L}	0.3×V_{CC1}	0.45×V_{CC1}		V	
Input Hysteresis Voltage (IN+, IN-)[1)]	V_{IN_hys}		0.1×V_{CC1}		V	
IN+ Input Current	I_{IN+}		55	70	μA	V_{IN+}= V_{CC1}
IN- Input Current	I_{IN-}	-70	-55		μA	V_{IN-}=GND1

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Output Pin Characteristics						
High Level Output Voltage (V_{CC2}-V_{OUT}) [1)]	V_{OH}		35		mV	I_{OUT}=-50mA, V_{IN+}=High, V_{IN-}=Low.
Low Level Output Voltage (OUT) [1)]	V_{OL}		20		mV	I_{CLAMP}=50mA,V_{IN+}=Low, V_{IN-}=High.
Output Pull-up Resistance[1)]	R_{OH}		0.7		Ω	V_{OH}/50mA.
Output Pull-down Resistance[1)]	R_{OL}		0.4		Ω	V_{OL}/50mA.
Peak Source Current[1)]	I_{OH}		10		A	V_{IN+}=High, V_{IN-}=Low, pulse width<10μs.
Peak Sink Current[1)]	I_{OL}		10		A	V_{IN+}=Low, V_{IN-}=High, pulse width<10μs.
Active Miller Clamp (NSI6601ME)						
Clamp Low Level Voltage[1)]	V_{LL_CLAMP}		70		mV	I_{CLAMP}=20mA,V_{IN-}=V_{IN+}=Low.
Clamp Threshold Voltage[1)]	V_{CLAMP_TH}		2	2.3	V	Referred to V_{EE2}.
Low Level Clamp Current (Peak) [1)]	I_{LL_CLAMP}		5		A	V_{IN-}=V_{IN+}=Low, V_{CLAMP}=15V pulse.
Clamp Delay Falling[1)]	T_{CD}		46		ns	
Short Circuit Clamping						
Clamping Voltage (OUT) (V_{OUT+}-V_{CC2} for NSI6601AE, V_{OUT}-V_{CC2} for NSI6601ME) [1)]	V_{CLP_OUT}		0.3		V	I_{OUT}=500mA with t_{pulse}=10μs, V_{IN+}=High, V_{IN-}=Low.

Clamping Voltage (CLAMP) (V_{CLAMP}-V_{CC2},NSI6601ME) 1)	V_{CLP_CLAMP}		1.2		V	I_{CLAMP}=500mA with t_{pulse}=10μs, V_{IN+}=High, V_{IN-}=Low.
			0.7		V	I_{CLAMP}=20mA, V_{IN+}=High, V_{IN-}=Low .
Active Pulldown						
Active Pulldown Voltage on CLAMP (V_{CLAMP} to V_{EE2}) 1)	V_{ACTPD}		2.1		V	I_{CLAMP}=500mA, V_{CC1}= V_{CC2}=Open.

(1) Not test covered, guaranteed by characterization.

6.2. Switching Characteristics

Switching characteristics are measured by using V_{CC1}=5V, 1μF capacitor from V_{CC1} to GND1, and V_{CC2}=15V with 10μF bypass capacitor from V_{CC2} to V_{EE2}, T_A =-40°C to 125°C (unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Minimum Pulse Width	t_{PWmin}		30	60	ns	
Propagation Delay	t_{pLH}	50	85	110	ns	C_{LOAD}=100pF
Propagation Delay	t_{pHL}	50	85	110	ns	C_{LOAD}=100pF
Pulse Width Distortion $\|t_{PLH}-t_{PHL}\|$	t_{PWD}		2	25	ns	C_{LOAD}=100pF
Output Rise Time (20% to 80%)	t_R		10	20	ns	C_{LOAD}=1nF
Output Fall Time (80% to 20%)	t_F		10	18	ns	C_{LOAD}=1nF
Common Mode Transient Immunity 2)	CMTI	150			kV/μs	

(2)Not test covered, guaranteed by design.

6.3. Typical Performance Characteristics

Typical characteristics are measured by using V_{CC1}=5V, 1μF capacitor from V_{CC1} to GND1, and V_{CC2}=15V with 10μF bypass capacitor from V_{CC2} to V_{EE2} T_J =-40°C to 125°C (unless otherwise noted).

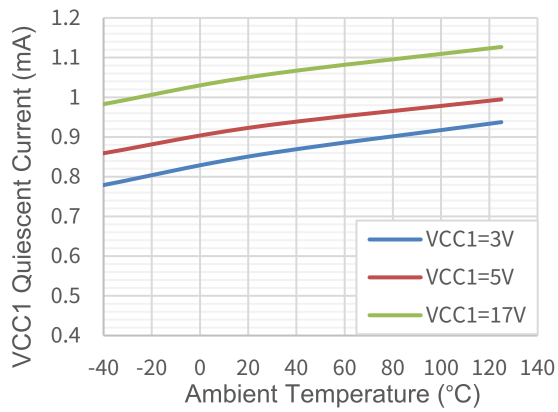


Figure 6.1 Input supply quiescent current Vs. Temperature

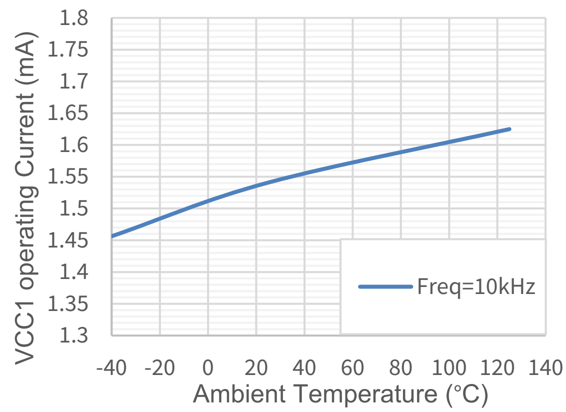


Figure 6.2 Input supply operating current Vs. Temperature

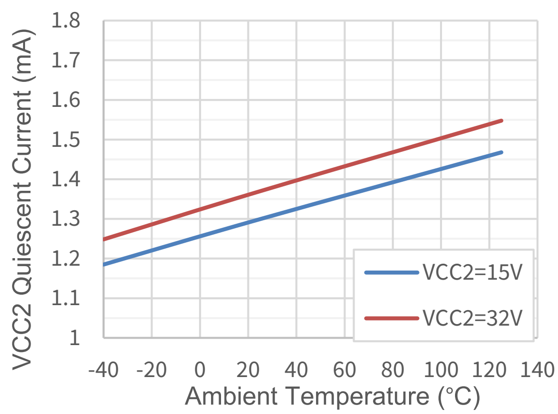


Figure 6.3 Output supply quiescent current Vs. Temperature

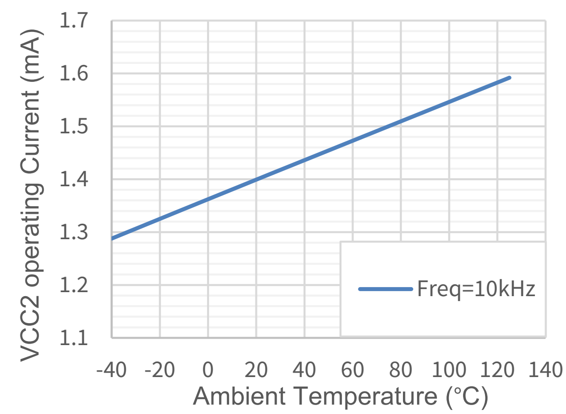


Figure 6.4 Output supply operating current Vs. Temperature

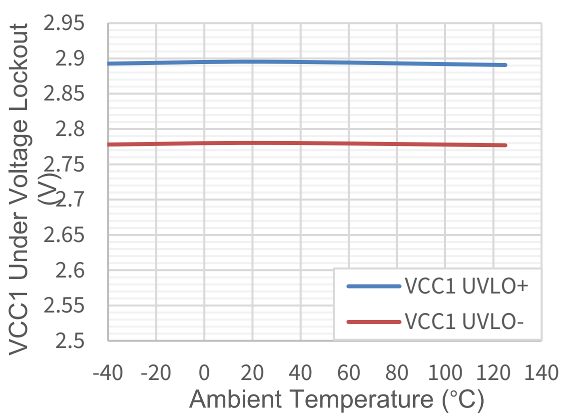


Figure 6.5 VCC1 UVLO Threshold Vs. Temperature

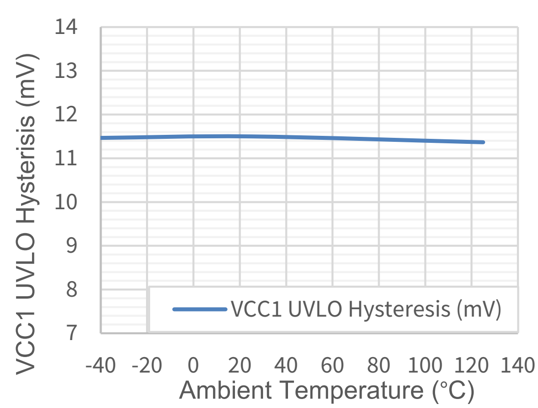


Figure 6.6 VCC1 UVLO Hysteresis Vs. Temperature

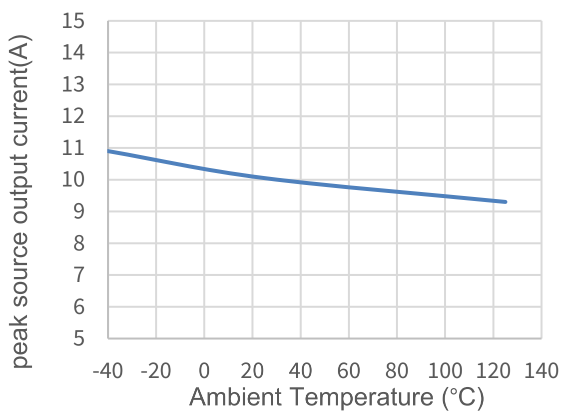


Figure 6.7 Peak Source Output Current Vs. Temperature

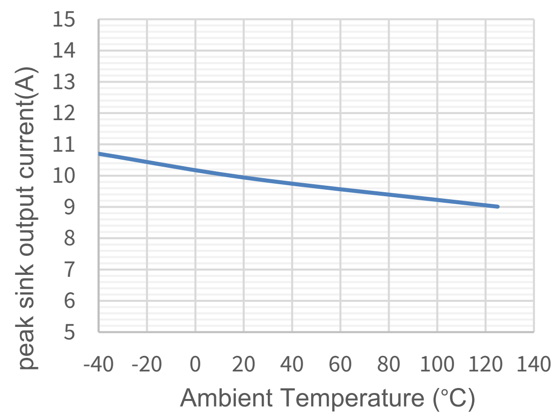


Figure 6.8 Peak Sink Output Current Vs. Temperature

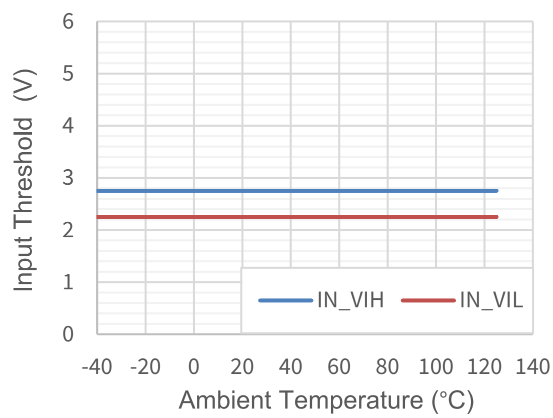


Figure 6.9 Input Threshold Vs. Temperature

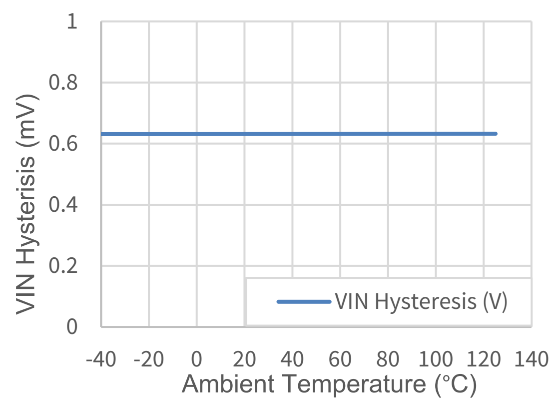


Figure 6.10 Input Hysteresis Vs. Temperature

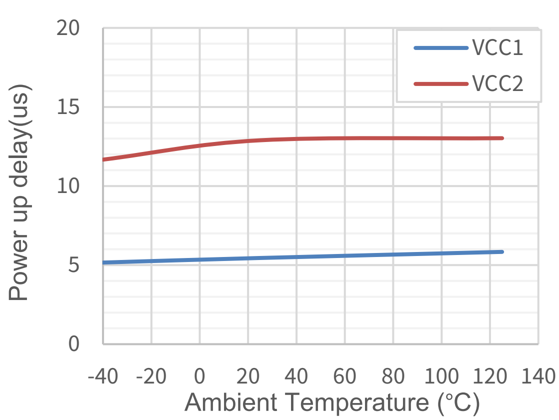


Figure 6.11 Power up Delay Vs. Temperature

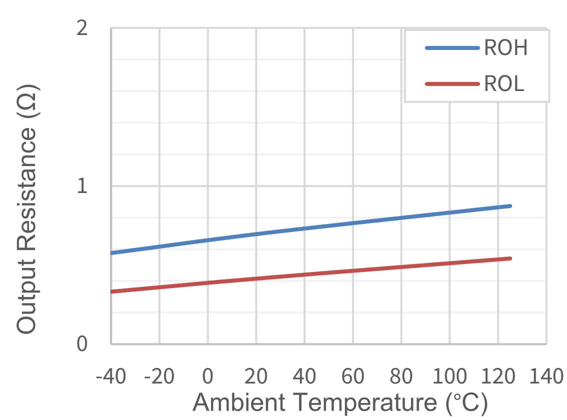


Figure 6.12 Output Resistance Vs. Temperature

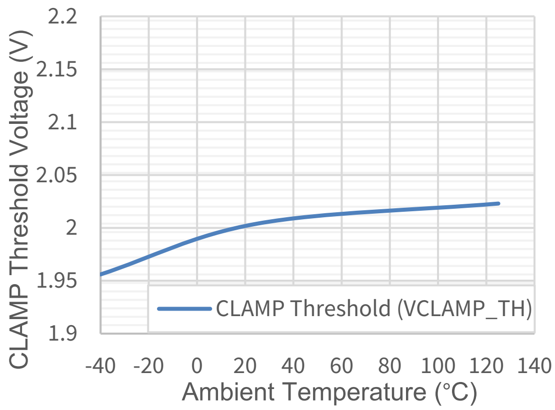


Figure 6.13 CLAMP Threshold Voltage Vs. Temperature

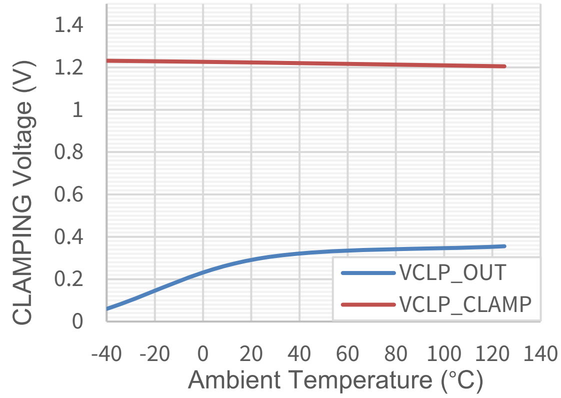


Figure 6.14 CLAMPING Voltage Vs. Temperature

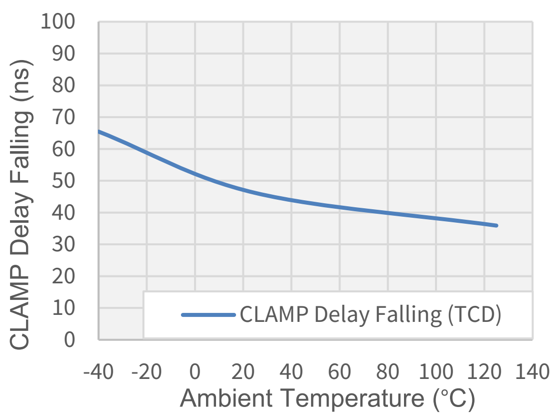


Figure 6.15 CLAMP Delay Falling Vs. Temperature

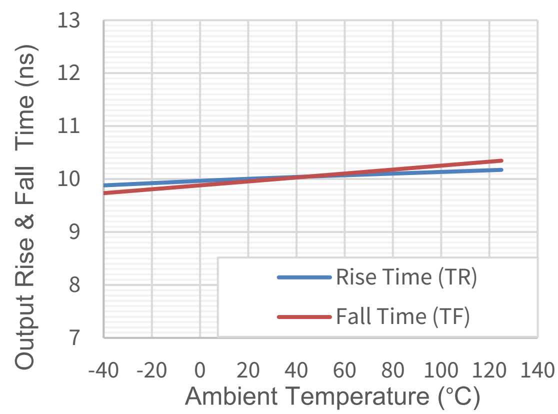


Figure 6.16 Output rise and fall time Vs. Temperature

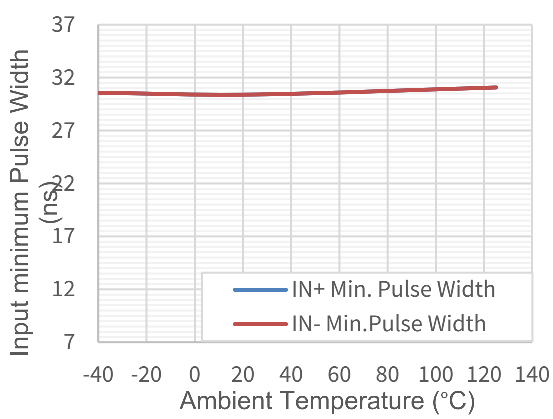


Figure 6.17 Minimum Pulse Width Vs. Temperature

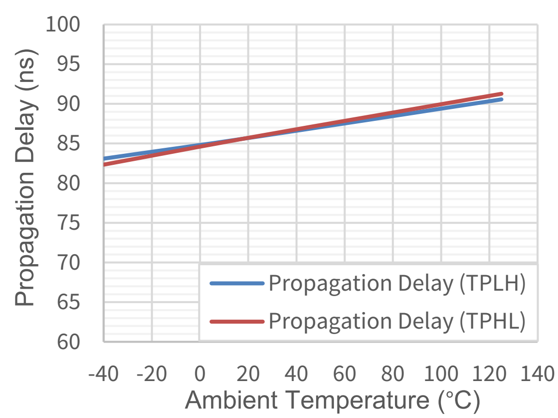


Figure 6.18 Propagation Delay Vs. Temperature

6.4. Parameter Measurement Information

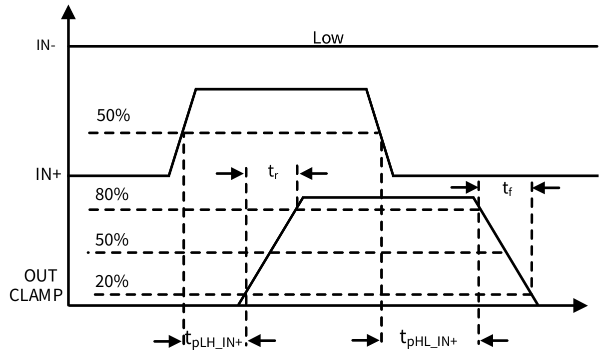


Figure 6.19 Propagation Delay, Rise Time and Fall Time (For Non-Inverting Configuration)

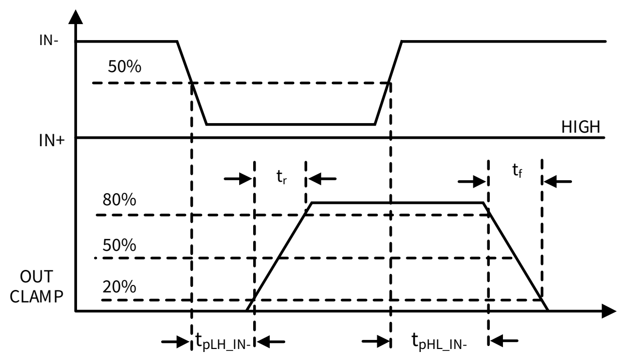


Figure 6.20 Propagation Delay, Rise Time and Fall Time (For Inverting Configuration)

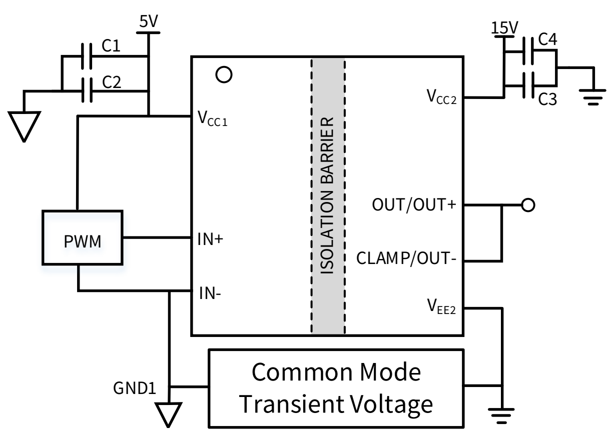


Figure 6.21 Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	Symbol	SOP8	SOW8	Unit	Comments
Min. External Air Gap (Clearance)	CLR	4.0	8.0	mm	Shortest pin-to-pin distance through air
Min. External Tracking (Creepage)	CPG	4.0	8.0	mm	Shortest pin-to-pin distance across the package surface
Distance Through the Insulation	DTI	20	20	μm	Minimum internal gap
Tracking Resistance (Comparative Tracking Index)	CTI	>600	>600	V	
Material Group		I	I		IEC 60664-1

7.2. Insulation Specificationfor SOP8 Package

Description	Test Condition	Symbol	Value	Unit
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150 V_{RMS}		I to IV	
	For Rated Mains Voltage ≤ 300 V_{RMS}		I to III	
Climatic Category			40/125/21	
Pollution Degree			2	
DIN EN IEC 60747-17(VDE 0884-17)				
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	700	V_{RMS}
	DC voltage		990	V_{DC}
Maximum Repetitive Peak Isolation Voltage		V_{IORM}	990	V_{PEAK}
Apparent Charge	Input to Output Test Voltage, Method B1, $V_{pd(m)}=V_{IORM}\times1.5$, 100% production test, $t_{ini}=t_m=1s$	q_{pd}	<5	pC
	Method A , After Environmental Tests Subgroup 1,$V_{pd(m)}=V_{IORM}\times1.2$, $t_{ini}=60s$, $t_m=10s$			pC
	After Input and Output Safety Test Subgroup 2 and Subgroup 3,$V_{pd(m)}=V_{IORM}\times1.2$,$t_{ini}=60s$, $t_m=10s$			pC
Maximum Transient Isolation Voltage	t = 60s	V_{IOTM}	4242	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50μs waveform per IEC62368-1	V_{imp}	3000	V
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50μs waveform, VIOSM≥VIMP × 1.3	V_{IOSM}	6000	V_{PEAK}
Isolation Resistance	V_{IO} =500V at $T_A=T_S=25°C$	R_{IO}	$>10^{12}$	Ω
	V_{IO} =500V at $T_A=T_S=150°C$		$>10^{9}$	Ω
	V_{IO} =500V at $100°C\leq T_A\leq125°C$		$>10^{11}$	Ω
Isolation Capacitance	f = 1MHz	C_{IO}	0.6	pF
UL1577				
Insulation voltage per UL	$V_{TEST} = V_{ISO}$, t = 60s (qualification),$V_{TEST} = 1.2\times V_{ISO}$,t = 1s(100% production test)	V_{ISO}	3000	V_{RMS}

7.3. Safety Limiting Values for SOP8 Package

Description	Test Condition	Symbol	Value		Unit
Maximum Safety Temperature		T_S	150		°C
Maximum Safety Power Dissipation	$R_{\theta JA}$=120°C/W, T_J=150°C, T_A=25°C	P_S	Total	1.04	W
			Input Side	0.05	
			Output Side	0.99	
Maximum Safety Current	$R_{\theta JA}$=120°C/W, V_{CC2}=15V, T_J=150°C, T_A=25°C	I_S	Output Side	66	mA
	$R_{\theta JA}$=120°C/W, V_{CC2}=30V, T_J=150°C, T_A=25°C		Output Side	33	

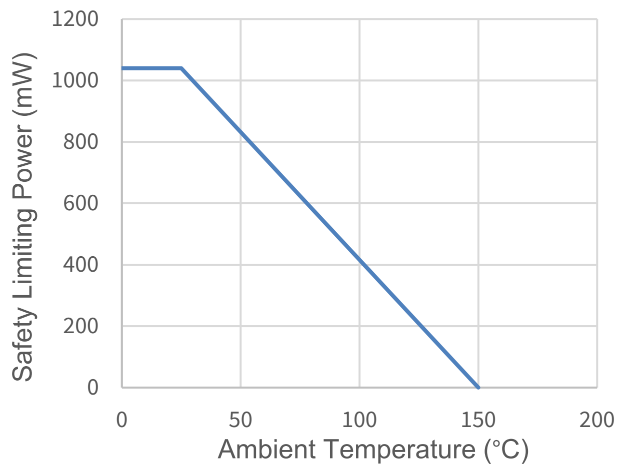


Figure 7.1 Thermal Derating Curve for Limiting Power per DIN VDE V 0884-17 for SOP8 Package

7.4. Regulatory Information for SOP8 Package

UL		VDE	CQC
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1-2022
Single Protection, 3000V_{RMS} Isolation Voltage	Single Protection, 3000V_{RMS} Isolation voltage	Basic Insulation V_{IORM}=990V_{PEAK}, V_{IOTM}=4242V_{PEAK}, V_{IOSM}=6000V_{PEAK}	Basic Insulation
E500602		pending	pending

7.5. Insulation Specification for SOW8 Package

Description	Test Condition	Symbol	Value	Unit
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 600V_{RMS}		I to III	
	For Rated Mains Voltage ≤ 1000V_{RMS}		I to II	
Climatic Category			40/125/21	
Pollution Degree			2	
DIN EN IEC 60747-17(VDE 0884-17)				
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	1500	V_{RMS}
	DC voltage		2121	V_{DC}
Maximum Repetitive Peak Isolation Voltage		V_{IORM}	2121	V_{PEAK}
Apparent Charge	Method B1,$V_{pd(m)}$=V_{IORM}×1.875, 100% production test, t_{ini}=t_m=1s	q_{pd}	<5	pC
	Method A , After Environmental Tests Subgroup 1,$V_{pd(m)}$=V_{IORM}×1.6, t_{ini}=60s, t_m=10s			pC
	Method A , After Input and Output Safety Test Subgroup 2 and Subgroup 3,$V_{pd(m)}$=V_{IORM}×1.2, t_{ini}=60s, t_m=10s, partial discharge <5pC			pC
Maximum Transient Isolation Voltage	t = 60s	V_{IOTM}	8000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50us waveform per IEC62368-1	V_{imp}	6000	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1,1.2/50us waveform, VIOSM≥VIMP × 1.3	V_{IOSM}	10000	V_{PEAK}
Isolation Resistance	V_{IO} =500V at T_A=T_S=25°C	R_{IO}	>10^{12}	Ω
	V_{IO} =500V at T_A=T_S=150°C		>10^{9}	Ω
	V_{IO} =500V at 100°C≤T_A≤125°C		>10^{11}	Ω
Isolation Capacitance	f = 1MHz	C_{IO}	1	pF
UL1577				
Insulation voltage per UL	V_{TEST} = V_{ISO}, t = 60s (qualification),V_{TEST} = 1.2×V_{ISO},t = 1s(100% production test)	V_{ISO}	5700	V_{RMS}

7.6. Safety Limiting Values for SOW8 Package

Description	Test Condition	Symbol	Value		Unit
Maximum Safety Temperature		T_S	150		°C
Maximum Safety Power Dissipation	$R_{\theta JA}$=110°C/W, T_J=150°C, T_A=25°C	P_S	Total	1.14	W
			Input Side	0.05	
			Output Side	1.09	
Maximum Safety Current	$R_{\theta JA}$=110°C/W, V_{CC2}=15V, T_J=150°C, T_A=25°C	I_S	Output Side	73	mA
	$R_{\theta JA}$=110°C/W, V_{CC2}=30V, T_J=150°C, T_A=25°C		Output Side	36	

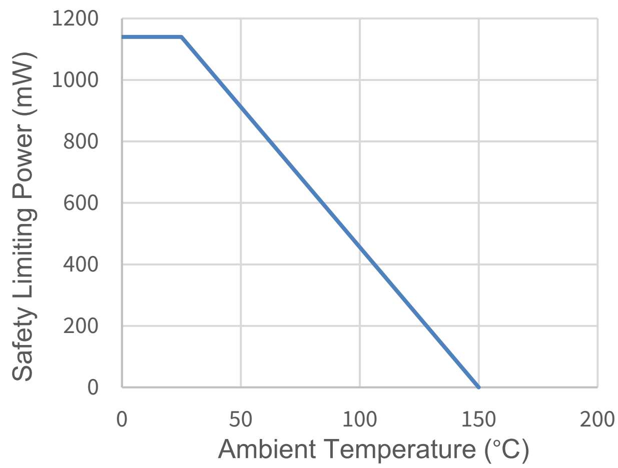


Figure 7.2 Thermal Derating Curve for Limiting Power per DIN VDE V 0884-11 for SOW8 Package

7.7. Regulatory Information for SOW8 Package

UL		VDE	CQC
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1-2022
Single Protection, 5700V_{RMS} Isolation Voltage	Single Protection, 5700V_{RMS} Isolation voltage	Reinforced Insulation V_{IORM}=2121V_{PEAK}, V_{IOTM}=8000V_{PEAK}, V_{IOSM}=10000V_{PEAK}	Reinforced Insulation
E500602		40052820	CQC20001264938

8. Function Description

8.1. Overview

The NSI6601xE family of highly reliable isolated gate driver has 4V, 9V and 12V UVLO versions, which is suitable to drive MOSFET, IGBT, and SiC. The NSI6601xE is available in SOP8 narrow body and wide body package, which can support 3000VRMS or 5700VRMS isolation per UL1577. System robustness is supported by 150kV/μs minimum common-mode transient immunity (CMTI).

The functional block diagram of NSI6601ME is shown in Figure 8.1 and function block diagram of NSI6601AE is shown in Figure 8.2. Two input pins with non-inverting and inverting logic support interlock and shoot through protection. Low resistance of high side and low side MOSFET in the output stage ensures high driving capability. Split outputs help to control the rise and fall time individually. Active pull-down feature is implemented to protect power transistor. Miller clamp feature of NSI6601ME can help prevent false turn-on of power transistors caused by Miller current

The isolation barrier inside NSI6601xE is based on capacitive isolation. The signal across the isolation barrier is transmitted through OOK (on-off keying) modulation technique with key benefits of high noise immunity and low radiation EMI. The transmitter sends a high-frequency carrier across the isolation barrier to represent one digital state and sends no signal to represent the other digital state. As shown in Figure 8.3, the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side.

8.2. Functional Block Diagram

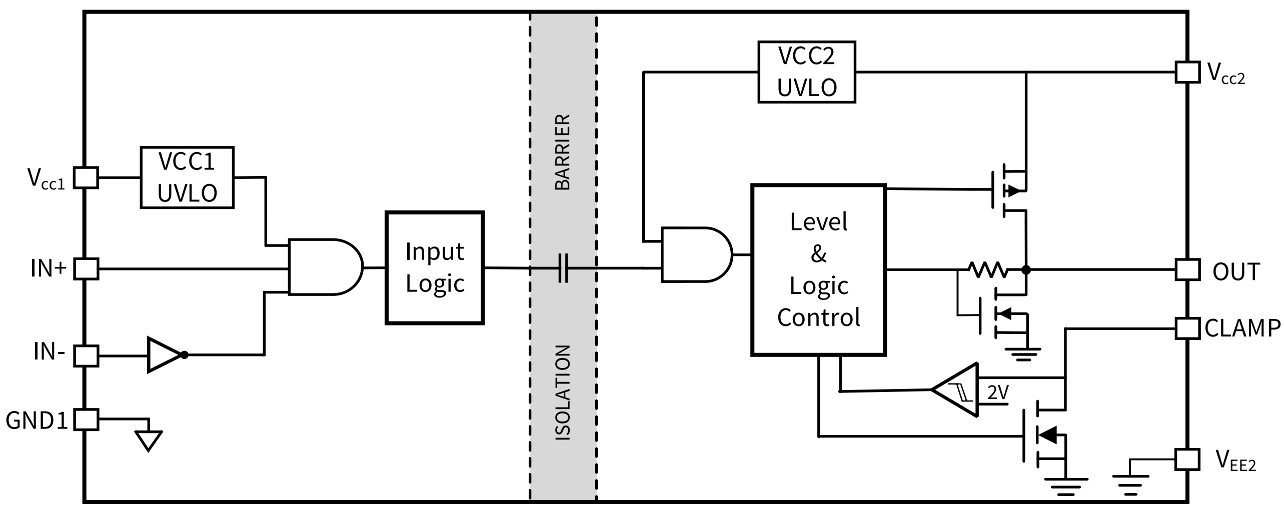


Figure 8.1 NSI6601MEB/MEC/MED Functional Block Diagram

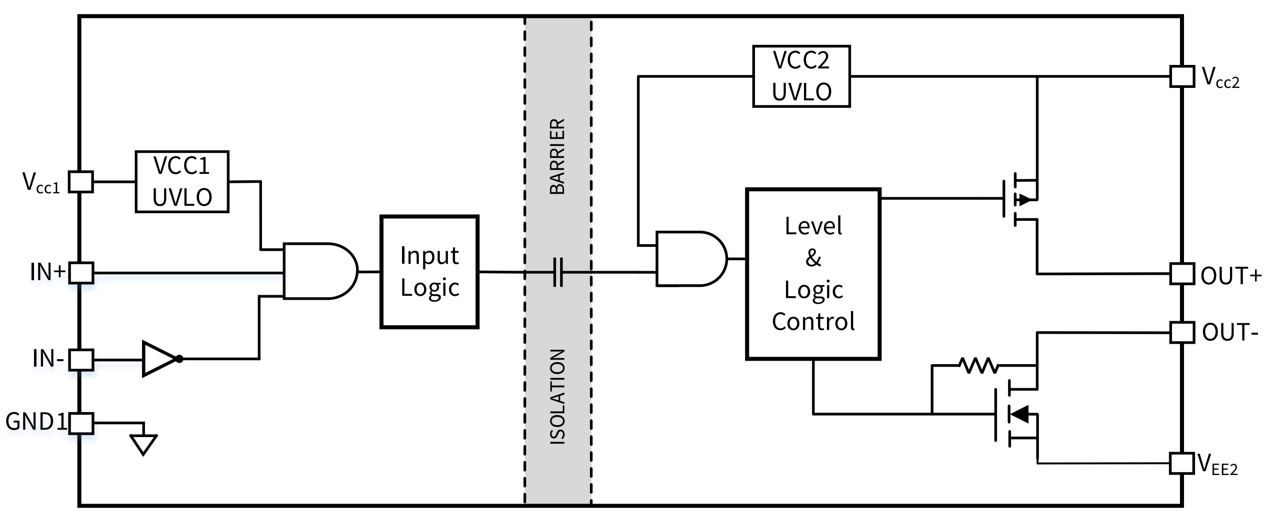


Figure 8.2 NSI6601AEB/AEC/AED Functional Block Diagram

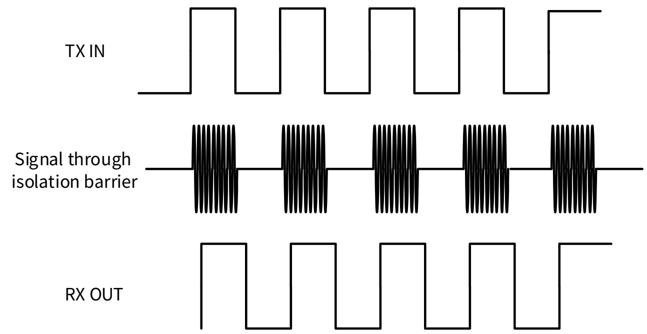


Figure 8.3 OOK based Modulation

8.3. Truth Tables

Table 8.1 Driver Function Table (1)

V_{CC1} status	V_{CC2} status	Inputs		Output status			Comment
		IN+	IN-	OUT	OUT+	OUT-	
PU	PU	H	L	H	H	Hi-Z	
PU	PU	L	H	L	Hi-Z	L	
PU	PU	H	H	L	Hi-Z	L	Interlock protection
PU	PU	L	L	L	Hi-Z	L	
PD	PU	X	X	L	Hi-Z	L	
PU	PD	X	X	L	Hi-Z	L	Active pull-down
PD	PD	X	X	L	Hi-Z	L	Active pull-down

(1) PD = Powered Down; PU = Powered Up; H = Logic High; L= Logic Low; X= Irrelevant;Hi-Z=High Resistance

The IN+ pin is internally pulled down to GND1, while IN- pin is internally pulled up to VCC1, making the output of NSI6601xE low by default. To improve noise immunity, grounding an input or tying to VCC1 is recommended.

8.4. Output Stage

The NSI6601xE has a P-channel MOSFET to pull up the OUT pin when turning on external power transistor. The measurement result R_{OH} represents the on-resistance of P-channel MOSFET. The equivalent pull-up resistance of NSI6601xE is ROH. The result is quite small, indicating the strong driving capability of NSI6601xE.

The pull-down structure of NSI6601xE is simply composed of an N-channel MOSFET with on-resistance of R_{OL}. The result is quite small, indicating the strong driving capability of NSI6601xE.

Typical values of pull-up and pulldown internal resistance are listed in Table 8.2.

Table 8.2 NSI6601xE Output Stage On-Resistance

Device Option	R_{OH}	R_{OL}	R_{CLAMP}	Unit
NSI6601ME	0.7	0.4	0.4	Ω
NSI6601AE	0.7	0.4	NA	Ω

In miller-clamp output configuration as shown in Figure 8.4, the pulldown structure works as two parallel N-channel MOSFETs structure when the CLAMP and OUT pins connect to the gate of the IGBT or MOSFET.

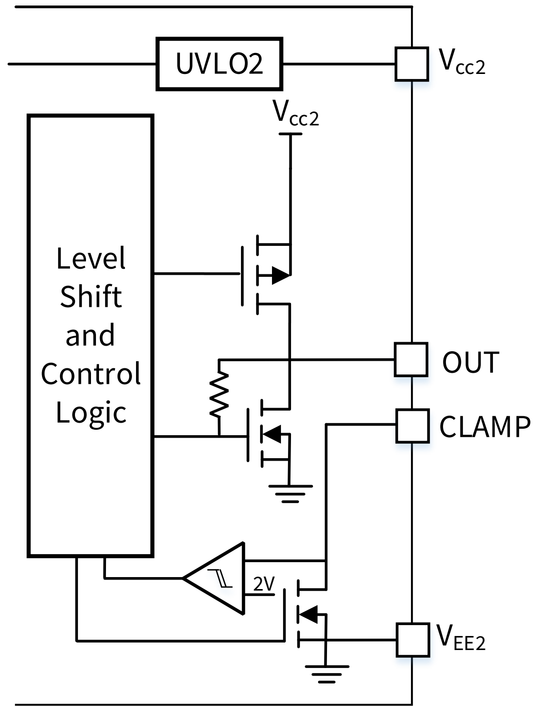


Figure 8.4 NSI6601ME Output Stage

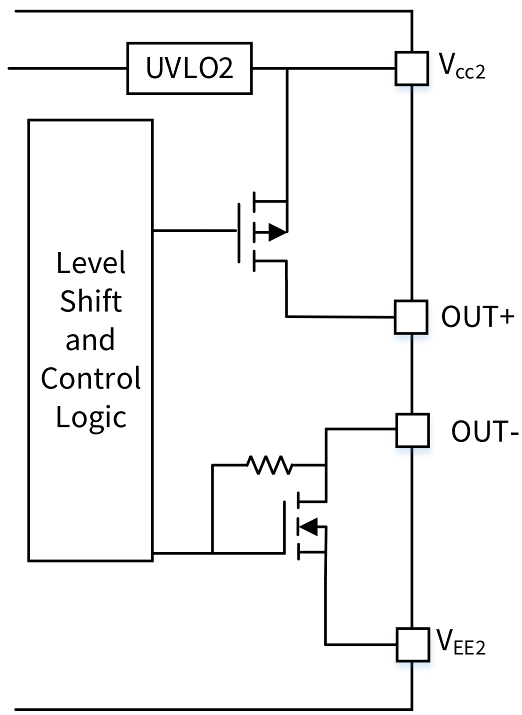


Figure 8.5 NSI6601AE Output Stage

8.5. V_{CC1}, and V_{CC2} Under Voltage Lock Out (UVLO)

The NSI6601xE has an internal under voltage lock out (UVLO) protection on both input and output side source blocks. The driver output is held low by an active clamp circuit when the supply voltage of VCC1 or VCC2 is lower than VCC_ON at power-up status or lower than VCC2-OFF after power-up, regardless of the status of the input pins.

The VCC1_GND1 and VCC2_VEE2 ULVO protections have hysteresis (VCC1_HYS & VCC2_HYS) to prevent chatter noise from VCC supply and allow small drops in supply power which usually occur in startup. It also prevents sags in the VCC, cause by sudden increase in ICC current while system commences switching.

8.6. Active Pull-Down

This function helps to pull the IGBT or MOSFET gate to the off-state when VCC2 is not connected to the power supply. This feature prevents the false turn-on of OUT and CLAMP pins by clamping the output to approximately 2V.

8.7. Short Circuit Clamping

Short circuit is used to clamp the driver output voltage as well as to pull the miller clamp pins to a bit higher than VCC2. This function helps to protect the gate of a MOSFET or IGBT from overvoltage breakdown. The short circuit clamping is implemented by adding an additional circuit between the dedicated pins and the VCC2. The internal diode circuitry can conduct 500mA current to the supply for 10µs.Use of external schottky diode may be added to improve the current capability and tighter clamping.

8.8. Active Miller Clamp of NSI6601ME

The active miller clamp function helps to prevent the false turn-on of the power switches caused by the miller current in applications such as half bridge configuration, where switched off IGBT turns to dynamically turn-on during turn on period of the opposite IGBT. It usually happens when a unipolar power supply is used. To avoid such false turn-on of switches a miller clamp allows sinking the miller current across a low impedance path in this dv/dt situation. During turn-off the gate voltage is monitored and the power-switch gate voltage is clamped to less than 2V referred to VEE2. The clamp is designed for a miller current in the same range as the nominal output current.

9. Application Note

9.1. Typical Application Circuit

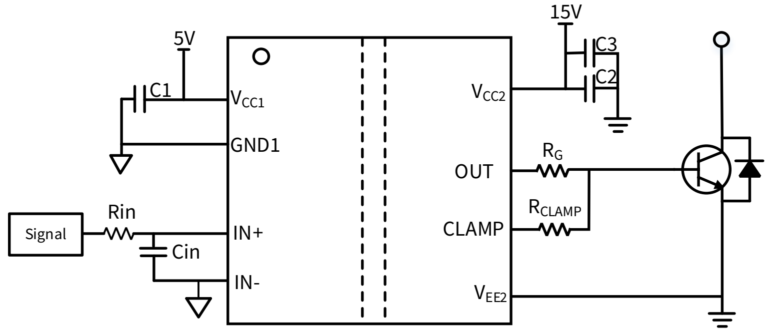


Figure 9.1 NSI6601ME Typical Application Circuit

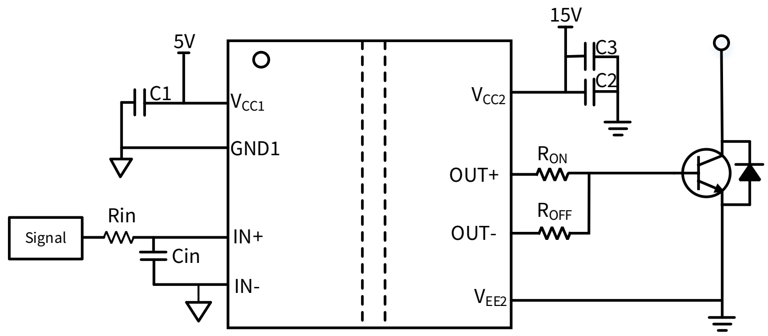


Figure 9.2 NSI6601AE Typical Application Circuit

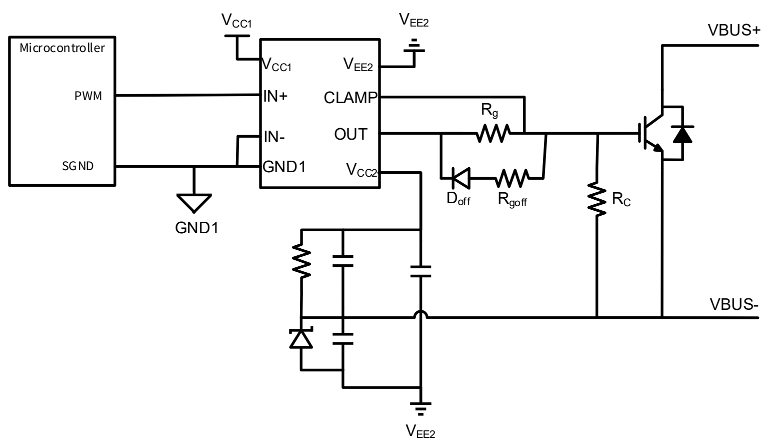


Figure 9.3 Negative Voltage Driving circuit using NSI6601ME

Bypassing capacitors for V_{CC1} and V_{CC2} supplies are needed to achieve reliable performance. To filter noise, 0.1µF/50V ceramic capacitor is recommended to be placed as close as possible to NSI6601xE, both at V_{CC1} and V_{CC2} side. For V_{CC2} supply, additional 10µF/50V ceramic capacitor is recommended, to support high peak currents when turning on external power transistor. If the V_{CC1} or V_{CC2} power supply is located long distance from the IC, larger capacitance is needed.

The input filter composed by Rin and Cin can be used if input PWM has ring due to long traces or bad PCB layout. However, it will introduce longer propagation delay.

9.2. Interlock Protection

For applications to drive power transistors in half bridge configuration, two NSI6601xE can be used. Interlock protection is possible as shown in Figure 9.4&Figure 9.5. If the controller has some mistake, leading to negative dead time, the output PWM of NSI6601xE is adjusted to avoid power transistor shoot through.

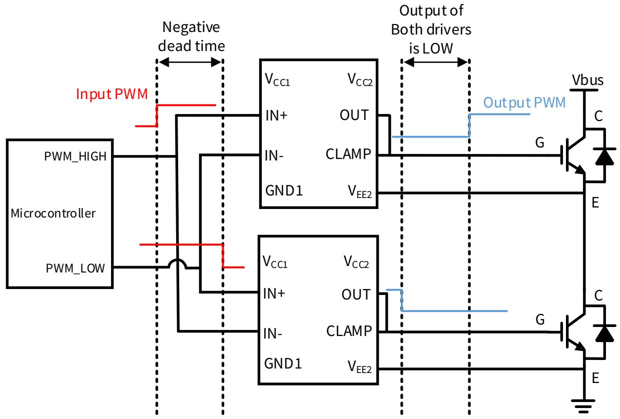


Figure 9.4 Interlock Protection using NSI6601ME

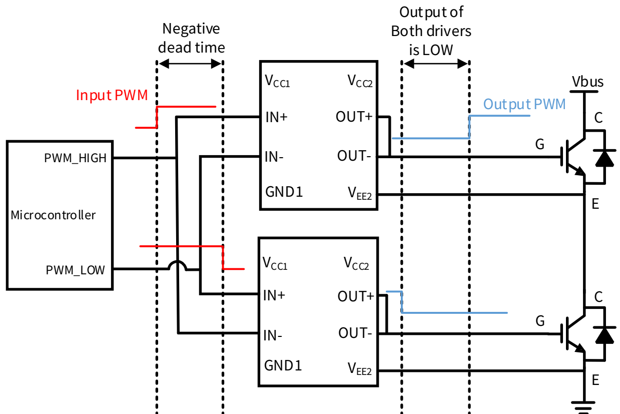


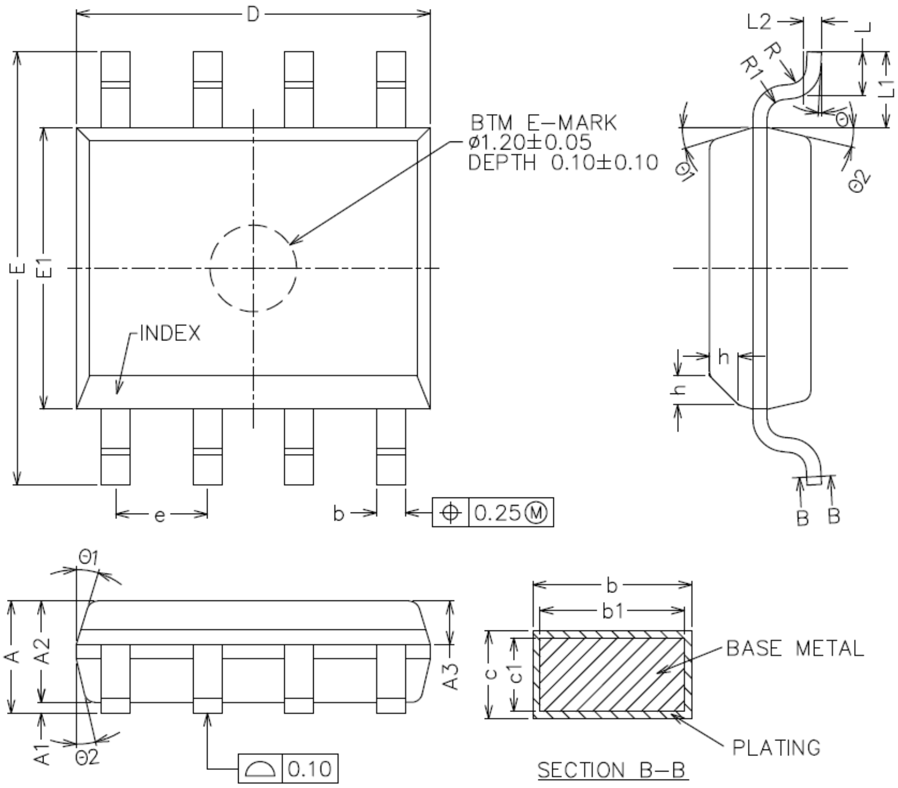
Figure 9.5 Interlock Protection using NSI6601AE

9.3. PCB Layout

Careful PCB layout is essential for optimal performance. Some key guidelines are:

- The bypass capacitors should be placed close to NSI6601xE, between V_{CC1} to GND1, or V_{CC2} to V_{EE2}.
- There is high switching current that charges and discharges the gate of external power transistor, leading to EMI and ring issues. The parasitic inductance of this loop should be minimized, by decreasing loop area and place NSI6601 close to power transistor.
- Place large amount of copper connecting to V_{EE2} pin and V_{CC2} pin for thermal dissipation, with priority on V_{EE2} pin. If the system has multi V_{EE2} or V_{CC2} layers, use multiple vias of adequate size for connection.
- To ensure isolation performance between primary and secondary side, the space under the chip should be kept free from planes, traces, pads or via.

10. Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.05	–	0.25
A2	1.30	1.40	1.50
A3	0.50	0.60	0.70
b	0.38	–	0.47
b1	0.37	0.40	0.43
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.17	1.27	1.37
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
Θ	0°	–	8°
Θ1	15°	17°	19°
Θ2	11°	13°	15°

Figure 10.1 SOP8 Package Shape and Dimension in millimeters

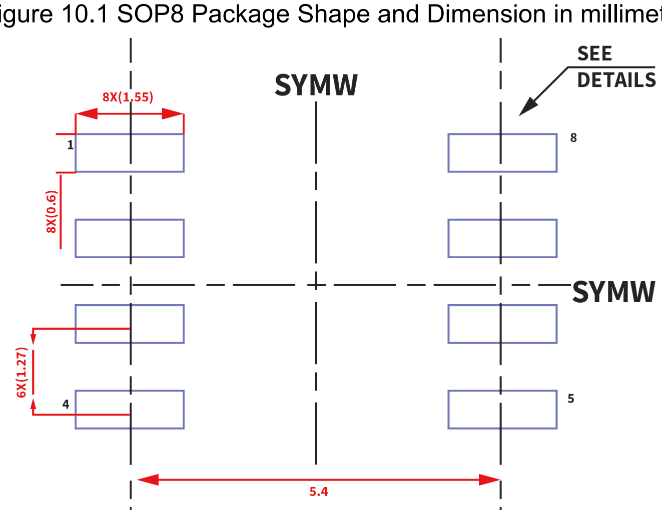


Figure 10.2 Land Pattern Example of SOP8(mm)

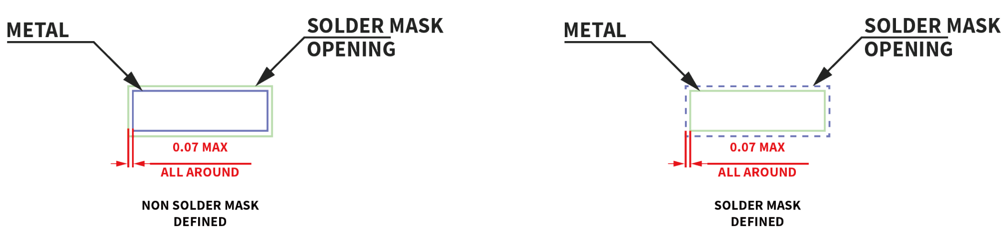
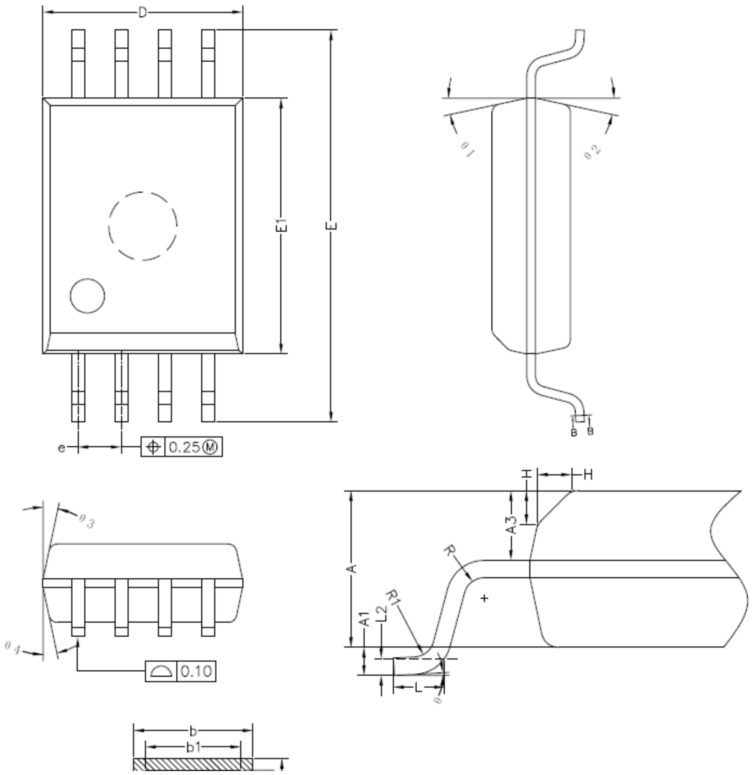


Figure 10.3 Solder Mask Detail of SOP8(mm)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL		MIN	NOM	MAX
A		—	—	2.85
A1		0.31	0.41	0.51
A2		2.20	2.30	2.40
A3		0.97	1.02	1.07
b	PURE Sn	0.33	—	0.47
	NiPdAu	0.33	—	0.44
b1		0.33	0.38	0.43
c	PURE Sn	0.22	—	0.32
	NiPdAu	0.22	—	0.29
c1		0.22	0.25	0.28
D		5.75	5.85	5.95
E		11.30	11.50	11.70
E1		7.40	7.50	7.60
e		1.17	1.27	1.37
H		0.40	0.50	0.60
L		0.55	0.75	0.90
L1		2.00REF		
L2		0.25BSC		
R		0.07	—	—
R1		0.07	—	—
θ		0°	—	8°
θ1		10°	12°	14°
θ2		10°	12°	14°
θ3		10°	12°	14°
θ4		10°	12°	14°

NOTES:

1.ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

2.TOP INDEX E−MARK ø1.00±0.10, DEPTH $0.10^{+0.15}_{-0.08}$, BOTTOM E−MARK ø2.00±0.10, DEPTH $0.15^{+0.15}_{-0.13}$.

Figure 10.4 SOW8 Package Shape and Dimension in millimeters

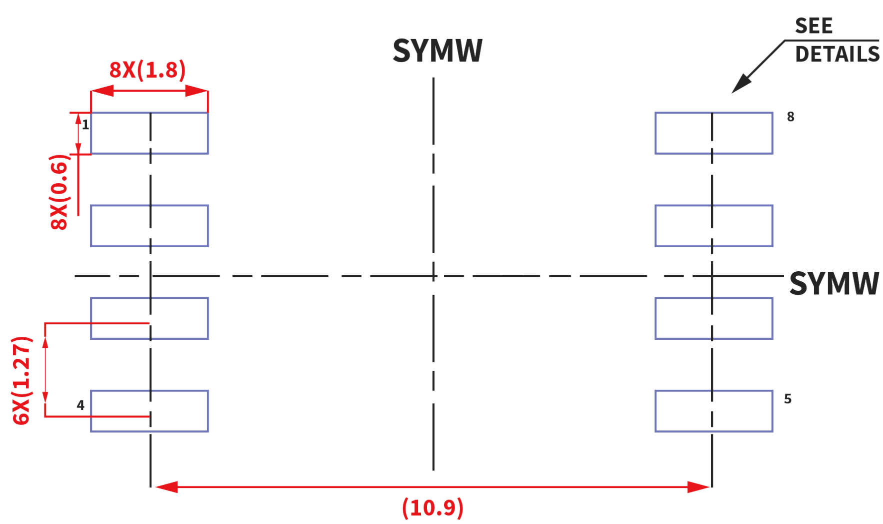


Figure 10.5 Land Pattern Example of SOW8(mm)

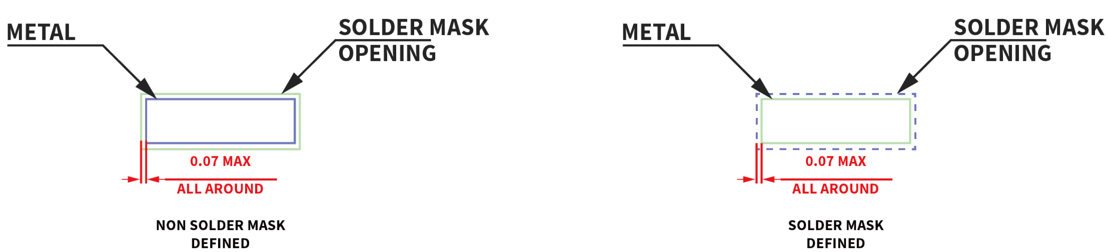


Figure 10.6 Solder Mask Detail of SOW8(mm)

11. Ordering Information

Part Number	*Isolation Rating (kV)*	*UVLO Level*	*Temperature*	*MSL*	*Package Type*	*Auto-motive*	MPQ	*SPQ*
NSI6601MEB-DSPR	3	9V	-40 to 125°C	3	SOP8	NO	2500	2500
NSI6601MEC-DSPR	3	12V	-40 to 125°C	3	SOP8	NO	2500	2500
NSI6601MED-DSPR	3	5V	-40 to 125°C	3	SOP8	NO	2500	2500
NSI6601MEF-DSPR	3	17V	-40 to 125°C	3	SOP8	NO	2500	2500
NSI6601MEB-DSWVR	5	9V	-40 to 125°C	3	SOW8	NO	1000	1000
NSI6601MEC-DSWVR	5	12V	-40 to 125°C	3	SOW8	NO	1000	1000
NSI6601MED-DSWVR	5	5V	-40 to 125°C	3	SOW8	NO	1000	1000
NSI6601MEF-DSWVR	5	17V	-40 to 125°C	3	SOW8	NO	1000	1000
NSI6601AEB-DSPR	3	9V	-40 to 125°C	3	SOP8	NO	2500	2500
NSI6601AEC-DSPR	3	12V	-40 to 125°C	3	SOP8	NO	2500	2500
NSI6601AED-DSPR	3	5V	-40 to 125°C	3	SOP8	NO	2500	2500
NSI6601AEF-DSPR	3	17V	-40 to 125°C	3	SOP8	NO	2500	2500
NSI6601AEB-DSWVR	5	9V	-40 to 125°C	3	SOW8	NO	1000	1000
NSI6601AEC-DSWVR	5	12V	-40 to 125°C	3	SOW8	NO	1000	1000
NSI6601AED-DSWVR	5	5V	-40 to 125°C	3	SOW8	NO	1000	1000
NSI6601AEF-DSWVR	5	17V	-40 to 125°C	3	SOW8	NO	1000	1000

12. Documentation Support

Part Number	***Product Folder***	***Datasheet***	***Technical Documents***	***Isolated Driver Selection Guide***
NSI6601xE	tbd	tbd	tbd	tbd

13. Tape and Reel Information

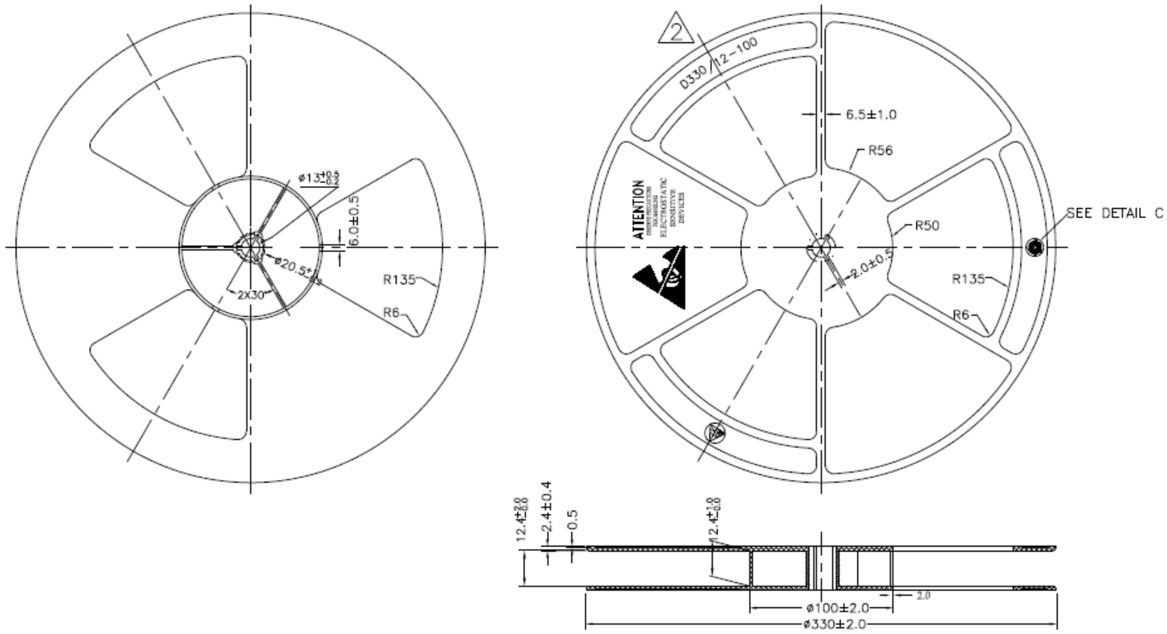


Figure 13.1 Tape Information

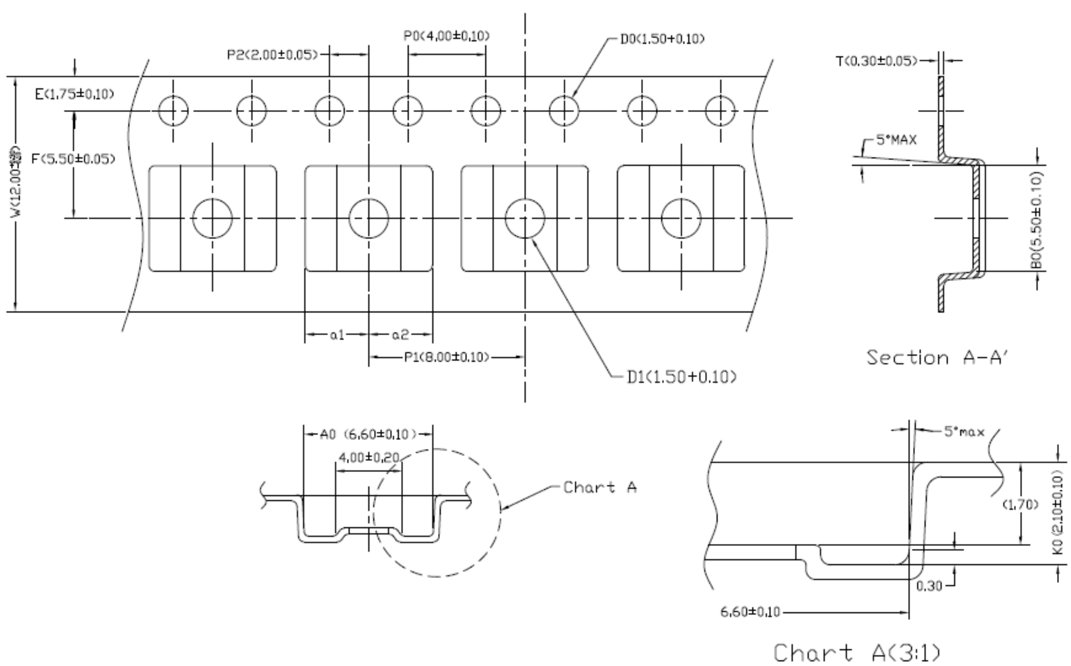


Figure 13.2 Reel Information of SOP8

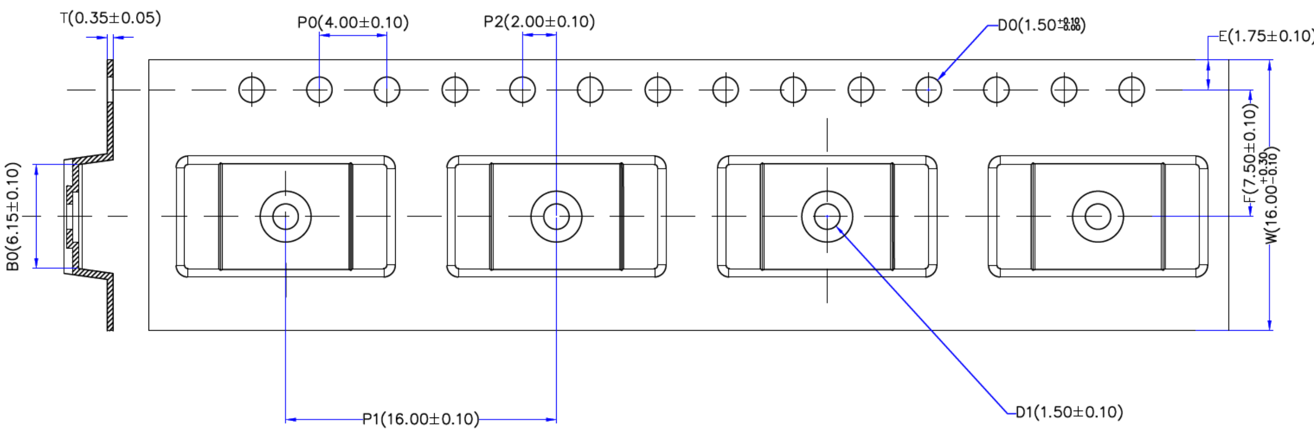


Figure 12.3 Reel Information of SOW8

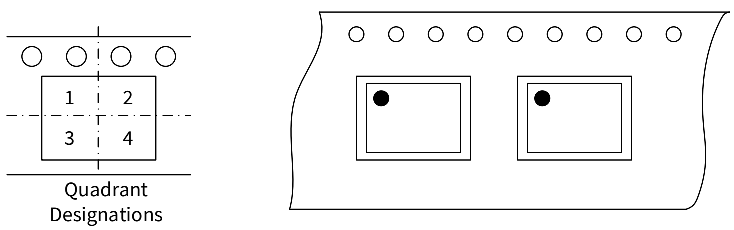


Figure 12.4 Quadrant Designation for Pin1 Orientation in Tape

14. Revision History

Revision	Description	Date
1.0	Initial version	2026/4/24

IMPORTANT NOTICE

For further information on applications, products and technologies, please contact NOVOSENSE (www.novosns.com).

Suzhou NOVOSENSE Microelectronics Co., Ltd