NOVOSENSE

NSI22C11

High Speed, Reinforced/Basic Isolated Comparator with Dual Output

Datasheet (EN) 1.1

Product Overview

NSI22C11 is a high-speed isolated comparator with output separated from input based on the NOVOSENSE capacitive isolation technology Adaptive OOK®. The NSI22C11 is an isolated single-ended comparator with both open-drain and push-pull output. The short response time of NSI22C11 makes it highly suitable for over-voltage protection application. The high common-mode transient immunity ensures that the device is able to provide accurate protection even in the presence of high-power switching such as in motor control applications.

NSI22C11 have an adjustable input reference threshold from 0.5V to 2V. The reference can be set by an external voltage source or the 100μA internal current source flowing through an external resistor.

The fail-safe function (missing VDD1 detection) simplifies system-level design and diagnostics. The NSI22C11 supports basic isolation with SOP8 narrow body package and reinforced isolation with SOW8 wide body package.

Key Features

- Up to 5000V_{RMS} Insulation Voltage
- 3.1V to 27V wide input side power supply
- Adjustable input reference threshold:
  - 0.5V to 2V
- Analog input voltage range: 0V to 2.7V
- Internal threshold reference:100μA ±2% error (Max)
- Accurate trigger threshold: ±0.25% error (Max)
- Fast propagation time: 0.4μs (typ)
- High CMTI: 150kV/μs (Typ)
- System-Level Diagnostic Features:
  - VDD1 monitoring
- Operation Temperature: -40°C~125°C
- RoHS-Compliant Packages:
  - SOW8 wide body (SOP8 300mil)
  - SOP8 narrow body (SOP 150mil)

Safety Regulatory Approvals

- UL recognition:
  - SOW8: 5000V_{rms} for 1 minute per UL1577
  - SOP8: 3000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- AC motor controls
- Power and solar inverters
- Uninterruptible Power Suppliers
- DC/DC converters

Device Information

Part Number	Package	Body Size
NSI22C11-DSWVR	SOW8(300mil)	5.85mm × 7.50mm
NSI22C11-DSPR	SOP8(150mil)	4.90mm × 3.90mm

Functional Block Diagrams

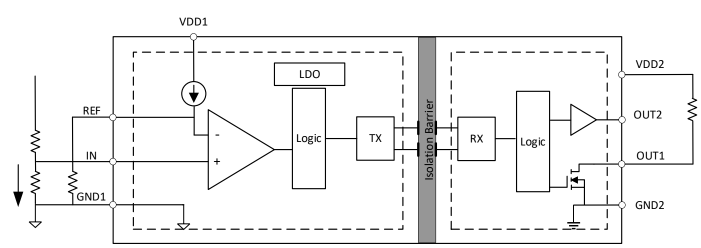

Figure 1. NSI22C11 Block Diagram

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1. Pin Configuration and Functions

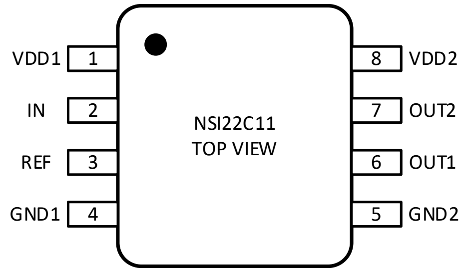


Figure 1.1 NSI22C11 Package

Table 1.1 NSI22C11 Pin Configuration and Description

NSI22C11 PIN NO.	SYMBOL	FUNCTION
1	VDD1	Power supply for input side (3.1V to 27V)
2	IN	Analog input (Single-ended Positive)
3	REF	Internal reference current output (threshold voltage is 0.5~2V)
4	GND1	Ground 1, the ground reference for input side
5	GND2	Ground 2, the ground reference for output side
6	OUT1	Open-drain output (pulled down when $V_{IN}>V_{REF}$)
7	OUT2	Push-pull output (pulled down when $V_{IN}>V_{REF}$)
8	VDD2	Power supply for output side (2.7V to 5.5V)

2. Absolute Maximum Ratings[1]

Parameters	Symbol	Min	Typ	Max	Unit
Input Side Power Supply Voltage (VDD1 to GND1)	VDD1	-0.3		35	V
Output Side Power Supply Voltage (VDD2 to GND2)	VDD2	-0.3		6.5	V
Input Voltage	IN	GND1-6		5.5	V
Reference Voltage	REF	GND1-0.5		6.5	V
Output Voltage	OUT2, OUT1	GND2-0.5		VDD2+0.5	V
Input current per IO pin	I_{IN}	-10		10	mA
Junction Temperature	T_J	-40		150	°C
Storage Temperature	T_{STG}	-55		150	°C

(1) The device cannot operate beyond the listed Absolute Maximum Ratings to prevent permanent device damage. The device is not fully functional if operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings. Long-time stress of the absolute maximum conditions may affect the device lifetime.

3. ESD Ratings

Parameters	Test Condition	Value	Unit
Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2.0	kV
	Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±1.0	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply					
Side1 Power Supply	VDD1	3.1	5.0	27	V
Side2 Power Supply	VDD2	2.7	3.3	5.5	V
Input Configuration					
Window threshold voltage	V_{REF}[1]	0.5		2	V
Analog input voltage	V_{IN}[2]	0		2.7	V
Filter capacitance on REF pin	C_{REF}		100		nF
Output Configuration					
Output voltage	V_{out}	0		VDD2	V
Sinking current limit per OUT pin	I_{sink}			12	mA

Parameters	Symbol	Min	Typ	Max	Unit
Sourcing current limit for OUT2	I_{source}			10	mA
Temperature					
Operating Ambient Temperature	T_A	-40		125	°C

(1) Exceeding the recommended VREF will lead to inaccurate reference threshold.

(2) Exceeding the recommended VIN will lead to leakage current.

5. Thermal Information

Parameters	Symbol	SOW8	SOP8	Unit
Junction–to-ambient thermal resistance	$R_{\theta JA}$	86	137.7	°C/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	28	54.9	°C/W
Junction-to-board thermal resistance	$R_{\theta JB}$	42	71.7	°C/W
Junction–to-top characterization parameter	Ψ_{JT}	4	12	°C/W
Junction-to-board characterization parameter	Ψ_{JB}	42	46	°C/W

6. Specifications

6.1. Electrical Characteristics

(VDD1 = 3.1V~27V, VDD2 =2.7V~5.5V, V_{REF} = 0.5V ~ 2V, V_{IN} = 0V ~2.7V, and TA = -40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 3.3V, TA = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Input Side Supply Voltage	VDD1	3.1	5.0	27	V	
Output Side Supply Voltage	VDD2	2.7	3.3	5.5	V	
Input Side Supply Voltage Undervoltage Threshold	$VDD1_{UV+}$		2.9		V	rising
	$VDD1_{UV-}$		2.8		V	falling
Output Side Supply Voltage Undervoltage Threshold	$VDD2_{UV+}$		2.3		V	rising
	$VDD2_{UV-}$		2.1			falling
Input Side Supply Current	IDD1		1.8	4.6	mA	
Output Side Supply Current	IDD2		1.4	4.5 (1)	mA	R_{PULLUP}=4.7kΩ
Analog Input and Output						
REF Window threshold	V_{REF}	0.5		2	V	Falling input threshold
REF threshold error	E_{REF}	-0.25		0.25	%	V_{REF}=2V

Parameters	***Symbol***	***Min***	***Typ***	***Max***	***Unit***	***Comments***
Internal REF current source	I_{REF}	98	100	102	µA	
Input hysteresis voltage	V_{HYS}		12		mV	Rising input threshold - Falling input threshold
Input resistance	R_{IN}		1		GΩ	At V_{IN} pin
Input bias current	I_{BIAS}		10		pA	
Input capacitance	C_{IN}		2		pF	At V_{IN} pin
High-level output voltage	V_{OH}	VDD2-0.3			V	Isource ≤4mA, for push-pull output OUT2
Low-level output voltage	V_{OL}	0		GND1+0.7	V	
Output leakage current	I_{LKG}		10	300	nA	V_{PULLUP}=5V
Output current limit per OUT pin	I_{sink}[2]			12	mA	VDD2=5V, sinking
	I_{source}			10	mA	VDD2=5V, sourcing of OUT2
Common-mode transient immunity	CMTI	75	150		kV/µs	R_{PULLUP}=10kΩ
Timing						
Deglitch time [3]	t_d		200		ns	V_{od}=20mV, C_L=15pF
Propagation delay [3]	t_{PD}		0.4		µs	V_{od}=20mV, C_L=15pF
			0.3	0.6	µs	V_{od}=100mV, C_L=15pF
Output fall time of OUT1	t_f		2	10	ns	C_L=15pF
Output rise/fall time of OUT2	t_r/t_f		2	10	ns	C_L=15pF
VDD1 Blanking time	t_{blk}		160		µs	
VDD1 Failsafe delay time	t_{fd}		120		µs	
VDD1 startup time	t_{s1}		50		µs	VDD1 step to 3.1V, VDD2≥3.0V
VDD2 startup time	t_{s2}		10		µs	VDD2 step to 3.0V, VDD1≥3.1V

(1) The output supply current is tested with the open-drain output pulled up to the supply voltage.

(2) The sink current range of the open-drain output to satisfy the low-level output voltage range, 0~ GND1+0.7 V.

(3) The Deglitch time and Propagation delay are tested with VIN rising from V_{REF} - V_{od} to V_{REF} + V_{od}.

6.2. Timing Diagrams

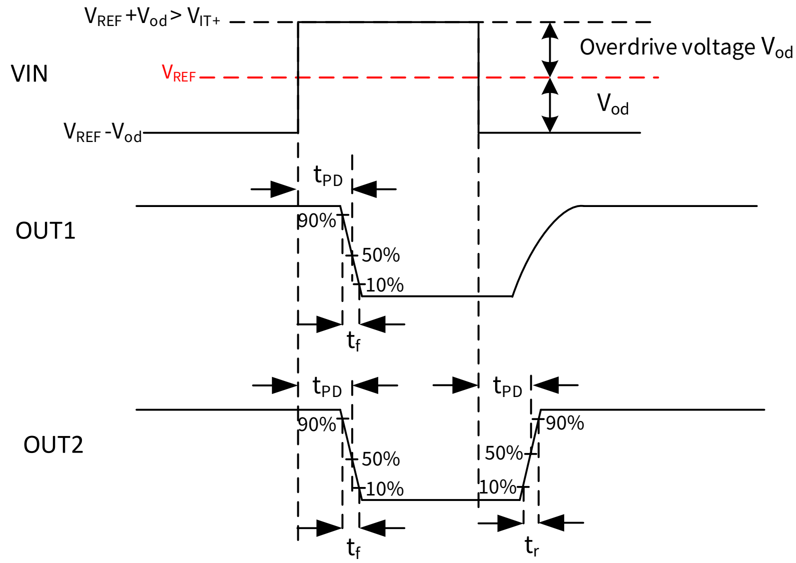


Figure 6.1 Propagation Delay and Output Fall Time Definition

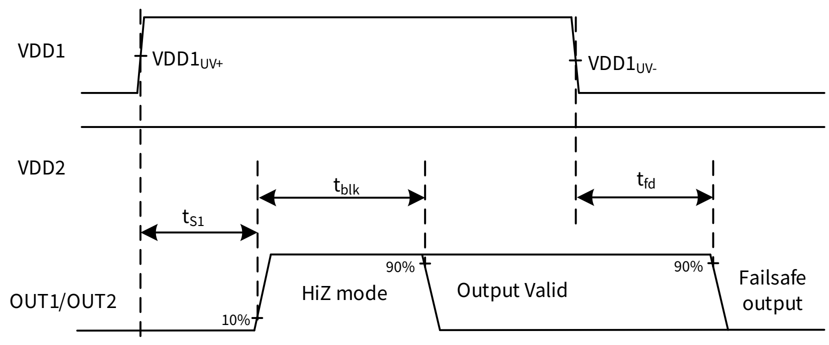


Figure 6.2 VDD1 Startup and Failsafe Process

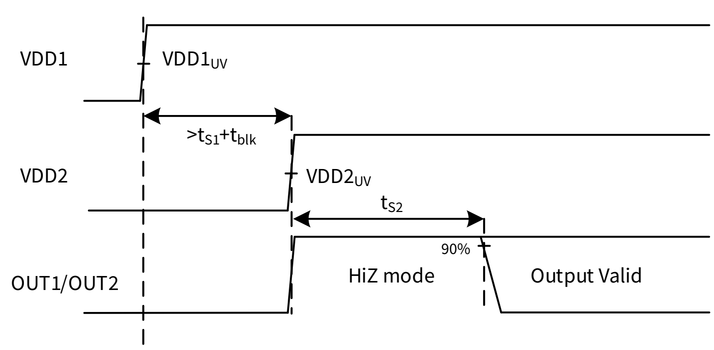


Figure 6.3 VDD2 Startup Process

6.3. Typical Performance Characteristics

Unless otherwise noted, test at VDD1 = 5V, VDD2 = 3.3V, V_{IN}= 0V, V_{REF} = 1V, T_A = 25°C.

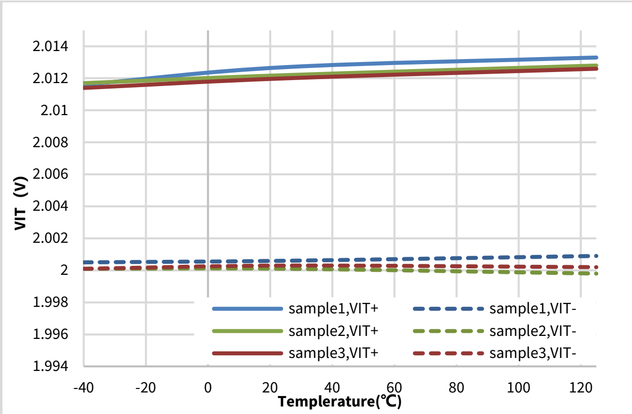


Figure 6.4 Trip Threshold of Comparator vs Temperature (V_{REF} = 2V)

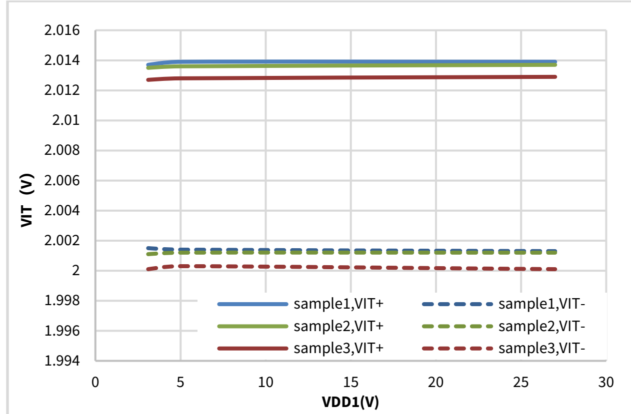


Figure 6.5 Trip Threshold of Comparator vs Input Side Supply Voltage (V_{REF} = 2V)

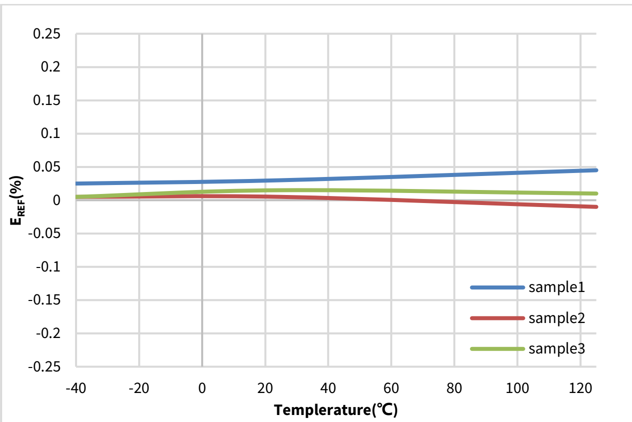


Figure 6.6 E_{REF} of Comparator vs Temperature (V_{REF} = 2V)

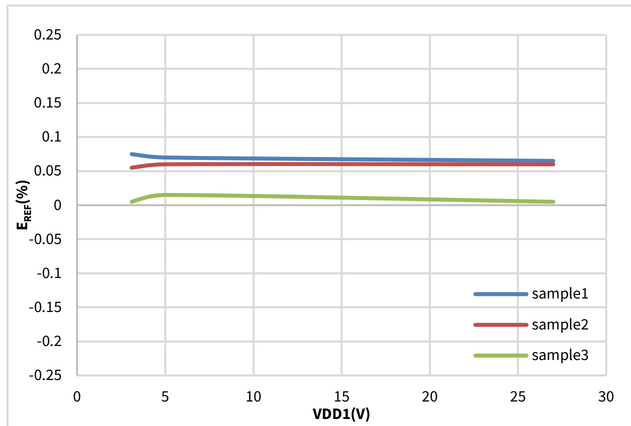


Figure 6.7 E_{REF} of Comparator vs Input Side Supply Voltage (V_{REF} = 2V)

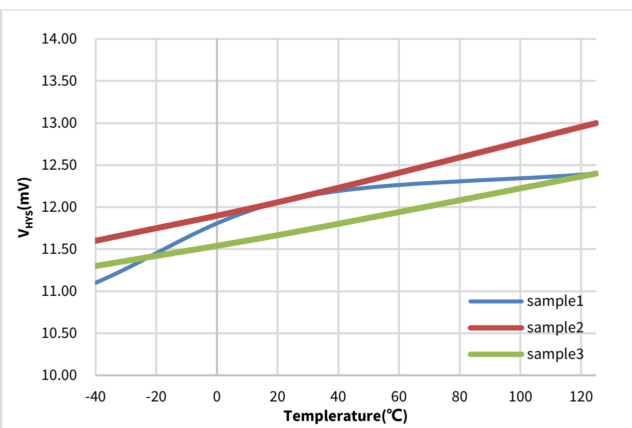


Figure 6.8 V_{HYS} of Comparator vs Temperature

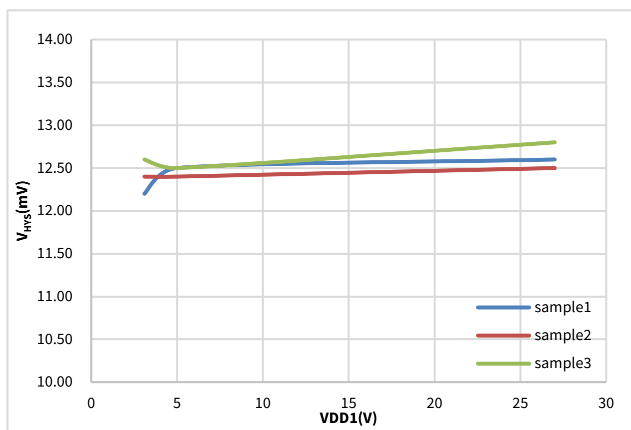


Figure 6.9 V_{HYS} of Comparator vs Input Side Supply Voltage

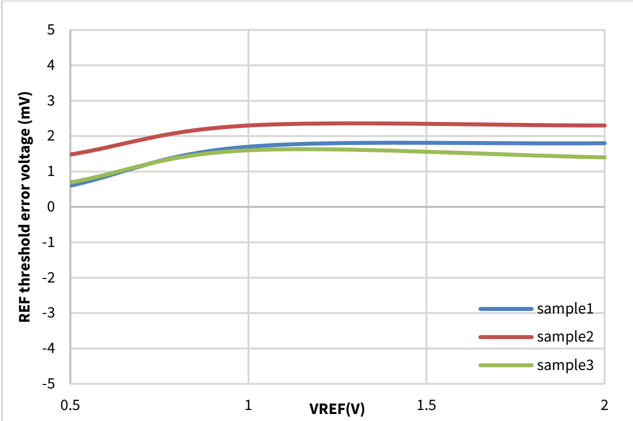


Figure 6.10 REF threshold error voltage of Comparator vs V_{REF}

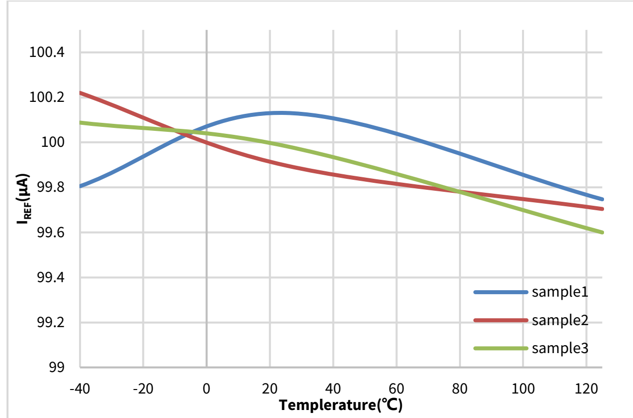


Figure 6.11 I_{REF} vs Temperature

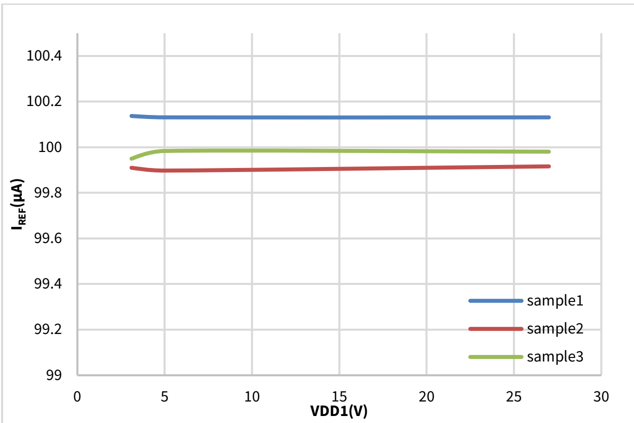


Figure 6.12 V_{HYS} of Positive Comparator vs Temperature

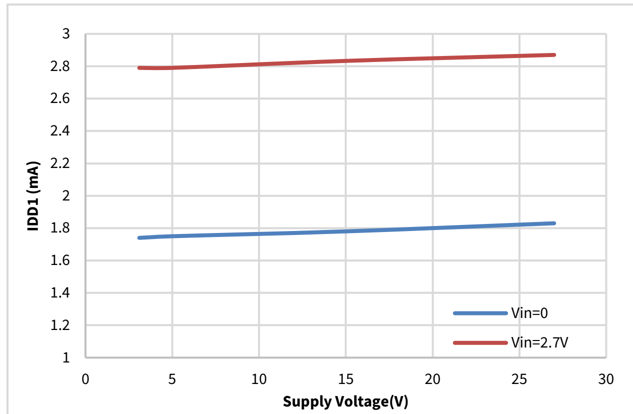


Figure 6.13 IDD1 vs Supply Voltage

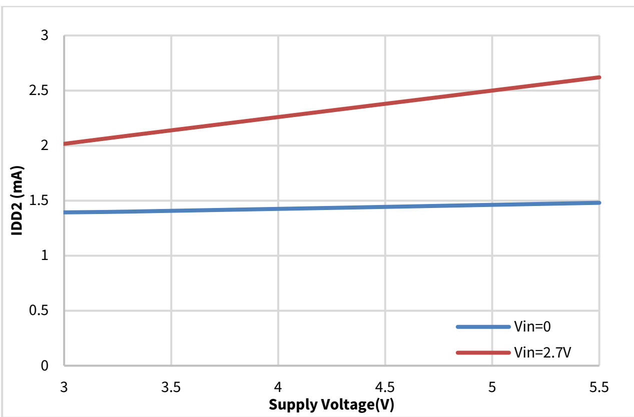


Figure 6.14 IDD2 vs Supply Voltage

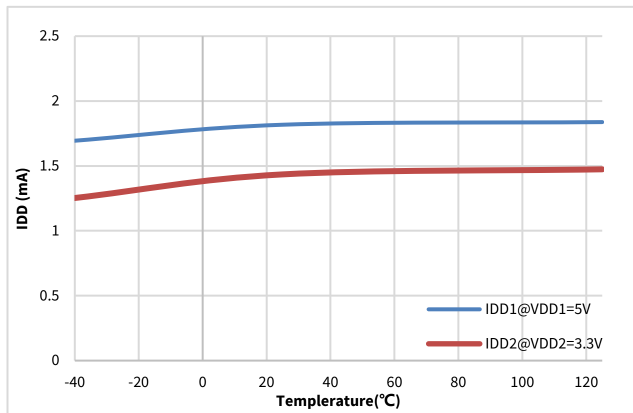


Figure 6.15 IDD vs Temperature (V_{in}=0V)

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value		Unit	Comments
		SOP8	SOW8		
Minimum External Clearance	CLR	4	8	mm	IEC 60664-1:2007
Minimum External Creepage	CPG	4	8	mm	IEC 60664-1:2007
Distance Through Insulation	DTI	27		μm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600		V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I			IEC 60664-1

Description	Test Condition	Value	
		SOP8	SOW8
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	I to IV	I to IV
	For Rated Mains Voltage ≤ 300Vrms	I to III	I to IV
	For Rated Mains Voltage ≤ 600Vrms	I to II	I to IV
	For Rated Mains Voltage ≤ 1000Vrms	I	I to III
Climatic Classification		40/125/21	
Pollution Degree per DIN VDE 0110		2	

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value		Unit
			SOP8	SOW8	
DIN EN IEC 60747-17 (VDE 0884-17)					
Maximum repetitive isolation voltage		V_{IORM}	990	2121	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	700	1500	V_{RMS}
	DC Voltage		990	2121	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, V_{ini}=V_{IOTM}, t_{ini} = 60 s , $V_{pd(m)}$=1.2*V_{IORM}, t_m=10s.	q_{pd}	/	<5	pC
	Method a, after environmental tests subgroup 1, V_{ini}=V_{IOTM}, t_{ini}=60s ,$V_{pd(m)}$=1.6*V_{IORM}, t_m=10s				pC

Description	*Test Condition*	*Symbol*	*Value*		*Unit*
			SOP8	*SOW8*	
	Method b, V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd\ (m)}$=1.875*V_{IORM}, t_m=1s（method b1）or $V_{pd(m)}$=V_{ini}, t_m=t_{ini}(method b2)				pC
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, V_{ini}=V_{IOTM}, t_{ini} = 60 s , $V_{pd(m)}$=1.2*V_{IORM}, t_m=10s.	q_{pd}	<5	/	pC
	Method a, after environmental tests subgroup 1, V_{ini}=V_{IOTM}, t_{ini}=60s ,$V_{pd(m)}$=1.3*V_{IORM}, t_m=10s				pC
	Method b, V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd\ (m)}$=1.5*V_{IORM}, t_m=1s（method b1）or $V_{pd(m)}$=V_{ini}, t_m=t_{ini}(method b2)				pC
Maximum transient isolation voltage	t = 60sec	V_{IOTM}	4242	8000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50μs waveform per IEC62368-1	V_{IMP}	3000	6250	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50μs waveform, V_{IOSM}≥V_{IMP} × 1.3	V_{IOSM}	6000	10000	V_{PEAK}
Isolation resistance	V_{IO} =500V, T_{amb}=25°C	R_{IO}	$>10^{12}$	$>10^{12}$	Ω
	V_{IO} =500V, 100℃ ≤ T_{amb} ≤ 125°C	R_{IO}	$>10^{11}$	$>10^{11}$	Ω
	V_{IO} =500V, T_{amb}=T_s	R_{IO}	$>10^{9}$	$>10^{9}$	Ω
Isolation capacitance	f = 1MHz	C_{IO}	0.8	0.8	pF
Safety total power dissipation	V_I = 5.5V, T_J = 150 °C, T_A = 25 °C	Ps	907	1453	mW
Safety input, output, or supply current	θ_{JA} = 137.7°C /W for SOP8, V_I = 5.5V, T_J = 150 °C, T_A = 25°C	Is	165	/	mA
	θ_{JA} = 86°C/W for SOW8, V_I = 5.5V, T_J = 150 °C, T_A = 25 °C		/	264	mA
Maximum safety temperature		Ts	150	150	°C
UL1577					
Insulation voltage per UL	V_{TEST} = V_{ISO}, t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO}, t = 1 s	V_{ISO}	3000	5000	V_{RMS}

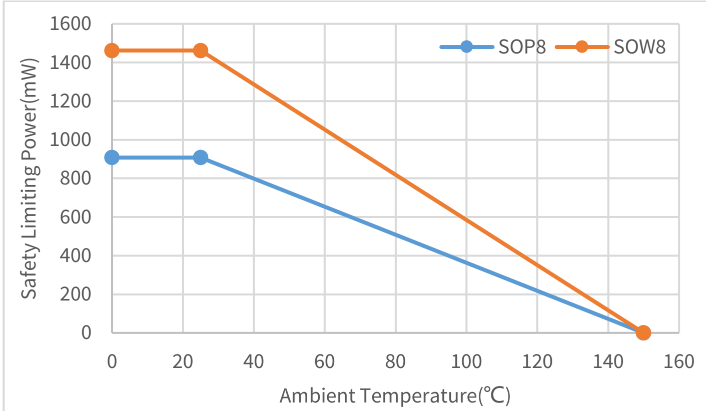


Figure 7.1 NSI22C11 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE 0884-17

7.3. Regulatory Information

The NSI22C11-DSWVR are approved or pending approval by the organizations listed in table.

UL		VDE	CQC	TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1
Single Protection, 5000V_{rms} Isolation voltage	Single Protection, 5000V_{rms} Isolation voltage	Reinforce Insulation V_{IORM}=2121 V_{PEAK} V_{IOTM}=8000 V_{PEAK} V_{IOSM}=10000 V_{PEAK}	Reinforced insulation	5000Vrms for 1min
E500602	E500602	40052820	CQC20001264938	R50574061

The NSI22C11-DSPR are approved or pending approval by the organizations listed in table.

UL		VDE	CQC	TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1
Single Protection, 3000V_{rms} Isolation voltage	Single Protection, 3000V_{rms} Isolation voltage	Basic Insulation V_{IORM}=990 V_{PEAK} V_{IOTM}=4242 V_{PEAK} V_{IOSM}=6000 V_{PEAK}	Basic insulation	3000Vrms for 1min
E500602	E500602	40057024	CQC20001264940	R50574061

8. Function Description

8.1. Overview

The NSI22C11 is a high-speed basic or reinforced isolated comparator with adjustable internal reference threshold. It is an isolated single-ended comparator with both open-drain and push-pull output, as shown in Figure 8.1. The input stage of the device drives a comparator to convert input signal to binary signal. The internal reference threshold can be adjusted by changing the external resistance that internal current source flows through. The driver (called TX in the Functional Block

Diagram) transfers the output of the comparator across the isolation barrier that separates the input side and output side voltage domains. For NSI22C11, the received binary signals are processed and output in the open-drain (OUT1 pin) and push-pull (OUT2 pin) form. When V_{IN} >V_{REF}, the open-drain output OUT1 and push-pull output OUT2 are actively pulled low. When V_{IN} drops below V_{REF}, the open-drain output OUT1 releases to the external pull-up level, and the push-pull output OUT2 is actively driven high.

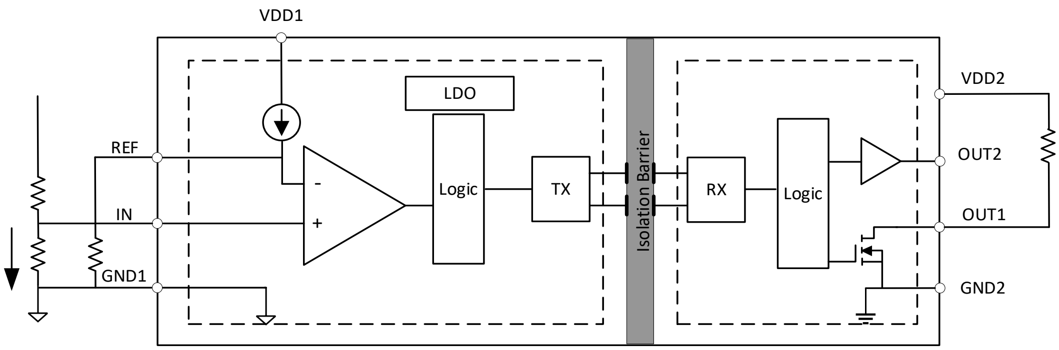


Figure 8.1 Function Block Diagram of NSI22C11

8.2. Analog input

The NSI22C11 is a single-ended comparator with input range of 0~2.7V. The input voltage and REF voltage are compared to generate the output. The output is pulled down when the input voltage exceeds the reference voltage and releases when the input voltage falls back below the reference voltage.

8.3. Reference input

The voltage of REF pin V_{REF} determines the internal reference threshold of the comparator. There are two ways to set V_{REF}. It is recommended to place an external resistor between the REF pin to GND1. The 100μA internal current source flows through the external resistor, which generates a high precision voltage reference. In addition, REF pin can be driven by an external voltage source to set the internal reference threshold. NSI22C11 has a positive threshold from 0.5V to 2V. Do not drive REF pin outside the recommended range to avoid the unintentional output.

Place an external capacitor between the REF pin to GND1 to filter the voltage of REF pin. When powered up, the capacitor is charged by the 100μA internal current source to V_{REF}. The output is not valid until charging is completed. The larger the capacitance, the higher the reference voltage, the longer V_{REF} settling time. If V_{REF} settling time exceeds the sum of VDD1 startup time t_{s1} and blanking time t_{blk}, there will be an invalid output until V_{REF} reaches the expected value, as is shown in Figure 8.2. Tests show that the external capacitor of less than 2.2nF do not cause false output during VDD1 startup. While the capacitance value is too small for filtering performance in noisy applications. It is recommended to select 100nF capacitor between the REF pin to GND1 to achieve better filtering performance and take some measures to avoid false alarms during powerup, such as priority power-on of VDD1 or additional design for setup blanking time.

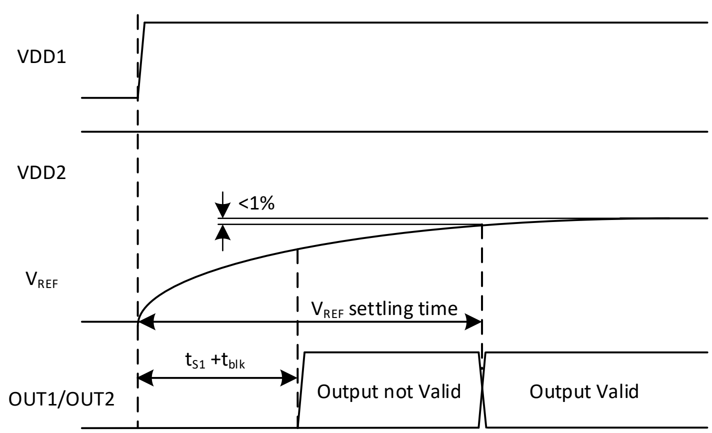


Figure 8.2 Output during V_{REF} Settling Time

8.4. Digital Output

The switching characteristics of NSI22C11 are shown in Figure 8.3.

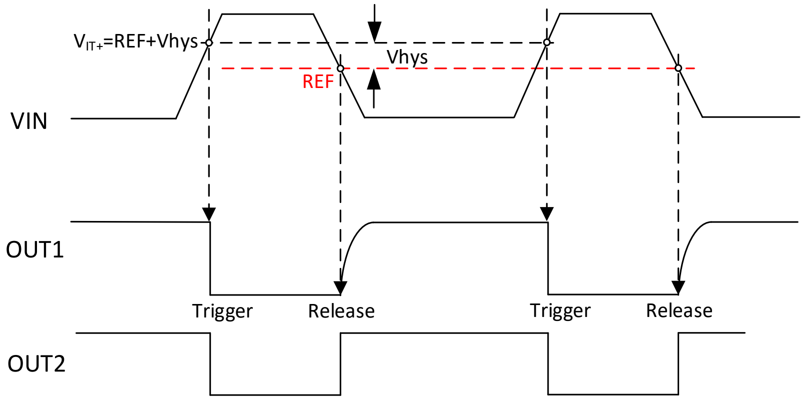


Figure 8.3 Switching Characteristic of NSI22C11

The NSI22C11 provides two output forms, an open-drain output and a push-pull output. The open-drain output (OUT1 pin) is pulled down when the input voltage rises above V_{IT+} (V_{REF}+V_{HYS}) and releases when the input voltage falls below V_{REF}. The push-pull output (OUT2 pin) is actively driven low when the input voltage rises above V_{IT+} (V_{REF}+V_{HYS}) and is actively driven high when the input voltage falls below V_{REF}. The hysteresis voltage V_{HYS} (typical value of 10mV) makes the comparator have better immunity in noisy environment without the need to add a positive feedback circuit to create hysteresis.

It should be noted that the CMTI (Common-mode transient immunity) performance of the open-drain output is related to the pullup resistance and load capacitance. When a common-mode transient event with high dV/dt occurs, the open-drain output may be pulled down because of interference signal coupled from parasitic capacitance between the high side and the low side. The lower pullup resistance enhances immunity. Additionally, a capacitor can be placed between the output pins and GND2 pin to improve the CMTI performance. However, the load capacitance extends the output fall time and is preferably less than 1nF.

In addition, NSI22C11 integrates some diagnostic measures and offers a failsafe output to simplify system-level design. The failsafe output is low-level voltage and it will be activated when the undervoltage of VDD1 is detected (VDD1< $VDD1_{UV}$), as is shown in Figure 8.4. When the undervoltage of VDD2 is detected (VDD2< $VDD2_{UV}$), the open-drain output is always high as it is pulled up to VDD2 through a resistor.

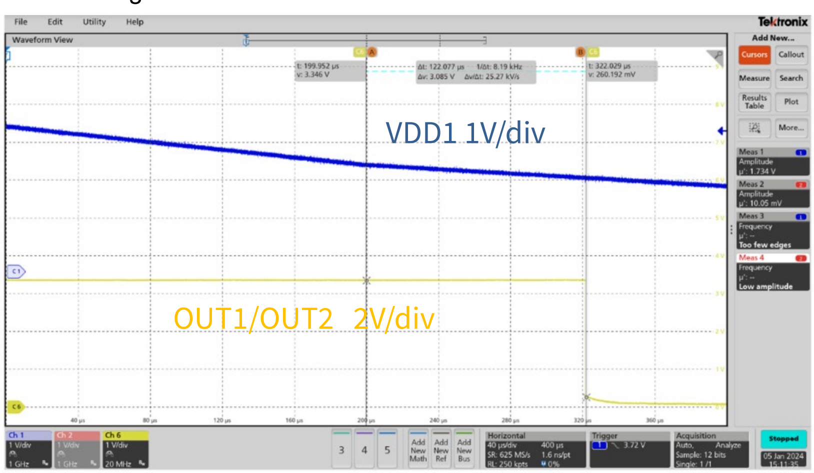


Figure 8.4 Typical Failsafe output when VDD1 undervoltage

9. Application Note

9.1. Typical Application Circuit

The NSI22C11 is highly suitable for over-voltage or over-temperature protection application such as AC motor controls because of its short response time. The typical application circuit is shown in Figure 9.1.

The DC bus voltage is divided by a resistance network, and the divided voltage is applied to the input of the NSI22C11 through a capacitor filter. An external resistor paralleled with a 100nF capacitor is placed between the REF pin to GND1 to generate the reference voltage of the comparator. The open-drain output OUT1 is pulled up through a resistor. A capacitor can be placed between the OUT1 pin and GND2 pin to improve the CMTI performance. Both open-drain output OUT1 and push-pull output OUT2 can be sent to the MCU as protective signals.

The current sensing and protection circuits of the motor drive are also shown in Figure 9.1. Refer to the datasheets of NSI22C12 and NSI300 for detailed information.

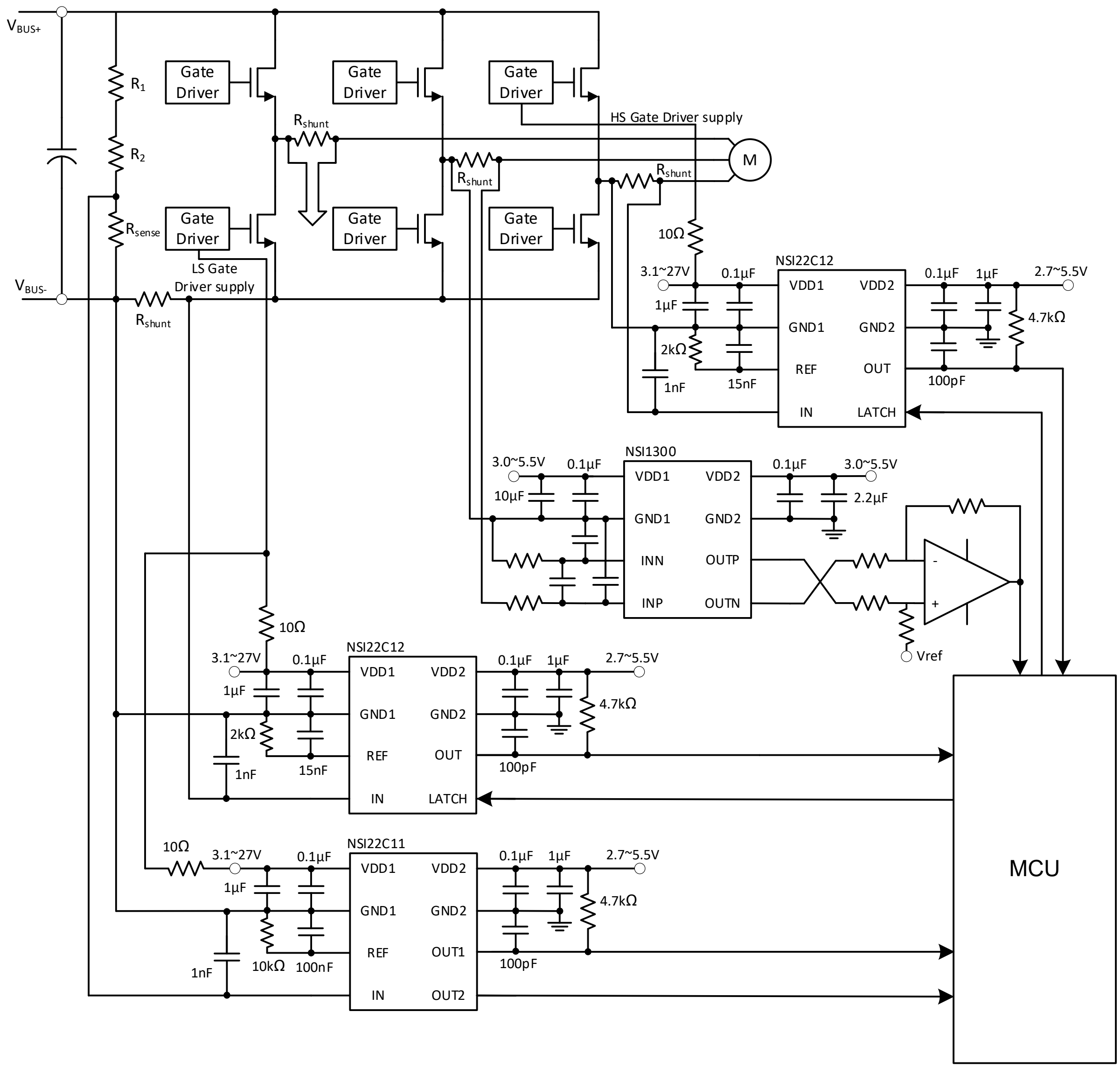


Figure 9.1 Typical application circuit of NSI22C1x in AC motor controls

9.2. Power Supply Recommendations

The NSI22C11 requires a 0.1μF capacitor paralleled with a 1μF capacitor between VDD1 and GND1, VDD2 and GND2 for power supply decoupling.

A 10Ω resistor is recommended in serious with the high-side power supply for current limiting and better filtering in the applications that the high side is powered by a noisy high-voltage power supply. For example, for DC bus voltage monitoring of the motor drive, the LS gate driver supply can be multiplexed as the high-side power supply.

9.3. PCB Layout

There are some key guidelines or considerations for optimizing performance in PCB layout:

- The NSI22C11 requires a 0.1μF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the VDD pin. If better filtering is required, an additional 1~10μF capacitor may be used.

- Kelvin rules is recommended for the connection between shunt resistor to the NSI22C11. Because of the Kelvin connection, any voltage drops across the trace and leads should have no impact on the measured voltage.
- Place the sensing resistor close to the IN pin and keep the layout of the input voltage and the sampling GND1 symmetrical and run very close to each other to the input of the NSI22C11. This minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal.
- Place the external reference resistor and its filter capacitor as close as possible to the REF pin for a stable reference voltage.

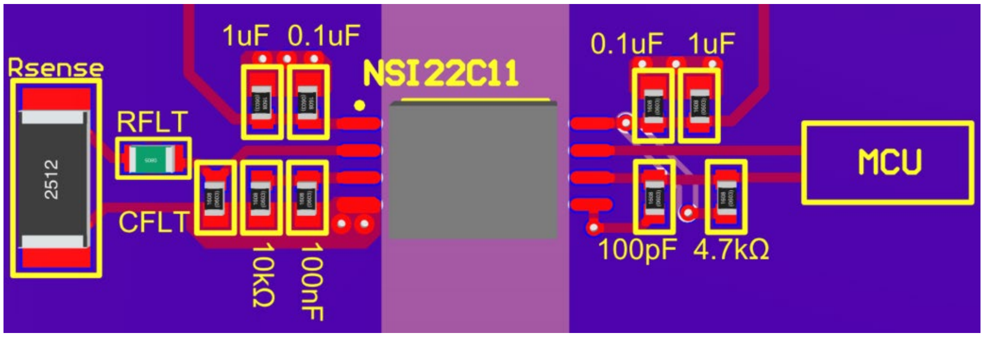
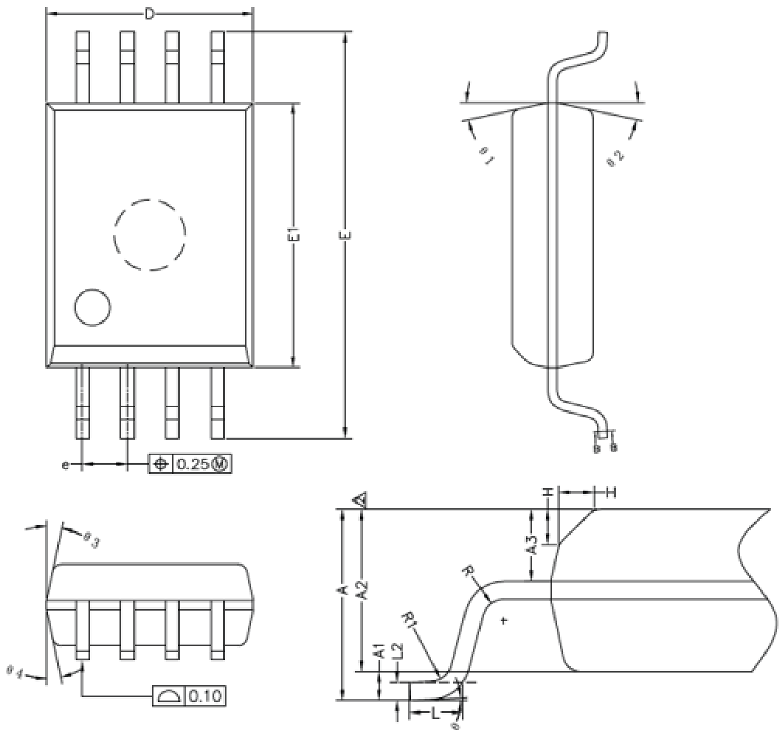
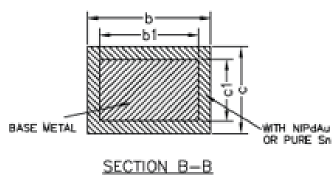


Figure 9.2 PCB layout example of NSI22C11

10. Package Information





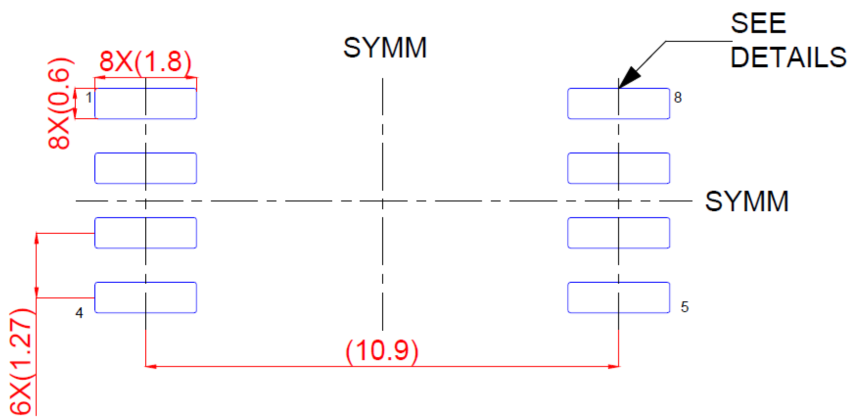
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL		MIN	NOM	MAX
A		–	–	2.85
A1		0.31	0.41	0.51
A2		2.20	2.30	2.40
A3		0.97	1.02	1.07
b	PURE Sn	0.33	–	0.47
	NiPdAu	0.33	–	0.44
b1		0.33	0.38	0.43
c	PURE Sn	0.22	–	0.32
	NiPdAu	0.22	–	0.29
c1		0.22	0.25	0.28
D		5.75	5.85	5.95
E		11.30	11.50	11.70
E1		7.40	7.50	7.60
e		1.17	1.27	1.37
H		0.40	0.50	0.60
L		0.55	0.75	0.90
L1		2.00REF		
L2		0.25BSC		
R		0.07	–	–
R1		0.07	–	–
θ		0°	–	8°
θ1		10°	12°	14°
θ2		10°	12°	14°
θ3		10°	12°	14°
θ4		10°	12°	14°

NOTES:

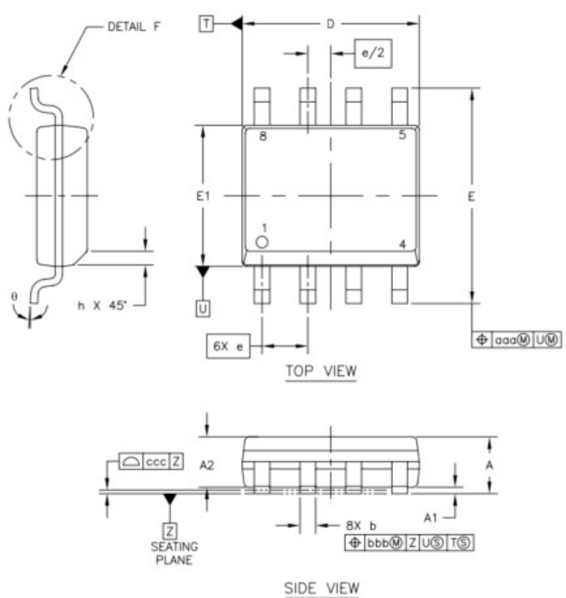
1. ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. TOP INDEX E-MARK ø1.00±0.10, DEPTH $0.10^{+0.15}_{-0.08}$, BOTTOM E-MARK ø2.00±0.10, DEPTH $0.15^{+0.15}_{-0.13}$.

Figure 10.1 SOW8 Package Shape and Dimension in millimeters



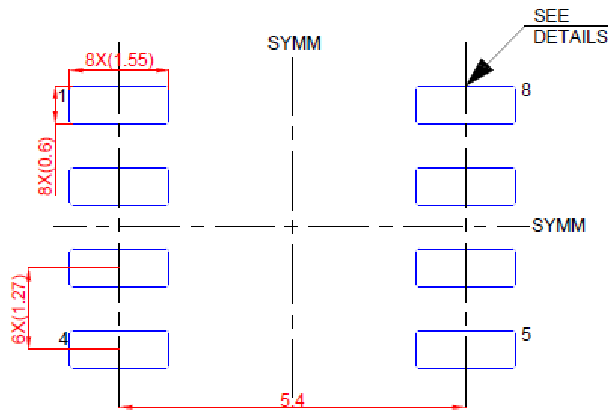
LAND PATTERN EXAMPLE(mm)
9.1 mm NOMINAL
CLEARANCE/CREEPAGE

Figure 10.2 SOW8 Package Board Layout Example

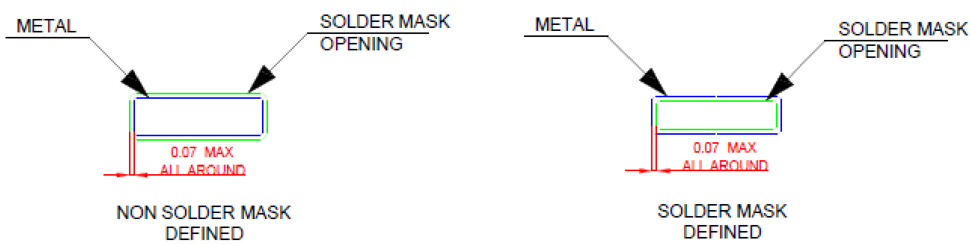


DESCRIPTION	SYMBOL	INCH			MILLIMETER		
		MIN	NOM	MAX	MIN	NOM	MAX
TOTAL THICKNESS	A	.053		.069	1.35		1.75
STAND OFF	A1	.004		.010	0.10		0.25
MOLD THICKNESS	A2	.049		---	1.25		---
LEAD WIDTH	b	.014		.019	0.35		0.49
L/F THICKNESS	c	.007		.010	0.19		0.25
BODY SIZE	D	.189		.197	4.80		5.00
	E1	.150		.157	3.80		4.00
	E	.228		.244	5.80		6.20
LEAD PITCH	e	.050 BSC			1.27 BSC		
	L	.016		.049	0.40		1.25
	h	.010		.020	0.25		0.50
	θ	0°		7°	0°		7°
	θ1	5°		15°	5°		15°
	θ2	2°	7°	12°	2°	7°	12°
LEAD EDGE OFFSET	aaa	.010			0.25		
LEAD OFFSET	bbb	.010			0.25		
COPLANARITY	ccc	.004			0.10		

Figure 10.3 SOP8 package shape and dimension in millimeters



LAND PATTERN EXAMPLE(mm)



SOLDER MASK DETAILS

Figure 10.4 SOP8 Package Board Layout Example

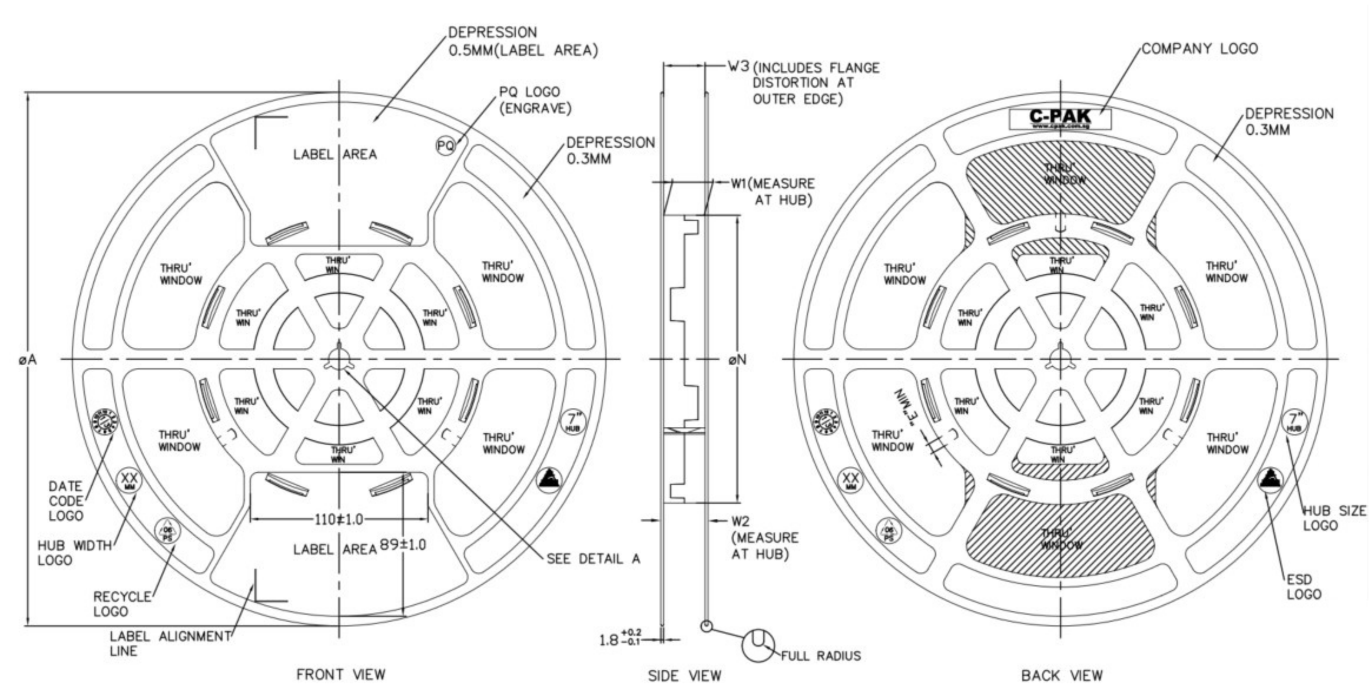
11. Ordering Information

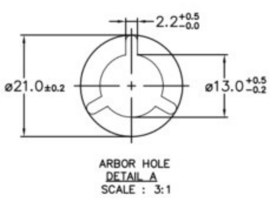
Part No.	Isolation Rating(kV)	REF Range(V)	Moisture Sensitivity Level	Temperature	Package Type	Package Drawing	SPQ	Release to Market
NSI22C11-DSPR	3	0.5~ 2	Level-3	-40 to 125°C	SOP8 (150mil)	SOP8	2500	NO
NSI22C11 -DSWVR	5	0.5~ 2	Level-3	-40 to 125°C	SOP8 (300mil)	SOW8	1000	YES

12. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NSI22C11	Click here	Click here	Click here	Click here

13. Tape and Reel Information





PRODUCT SPECIFICATION

TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	$8.4^{+1.5}_{-0.0}$	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	$12.4^{+2.0}_{-0.0}$	18.4		5.5
16MM	330	178	$16.4^{+2.0}_{-0.0}$	22.4		5.5
24MM	330	178	$24.4^{+2.0}_{-0.0}$	30.4		5.5
32MM	330	178	$32.4^{+2.0}_{-0.0}$	38.4		5.5

SURFACE RESISTIVITY

LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{3} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES

Figure 13.1 Reel Information

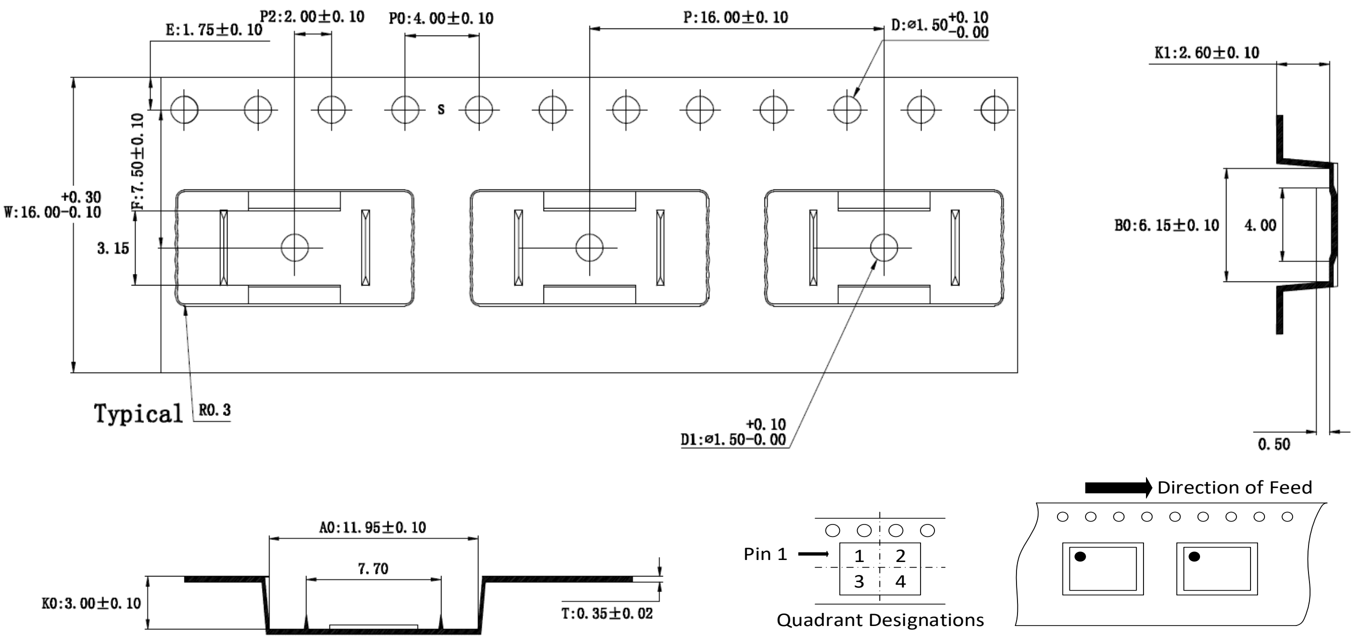
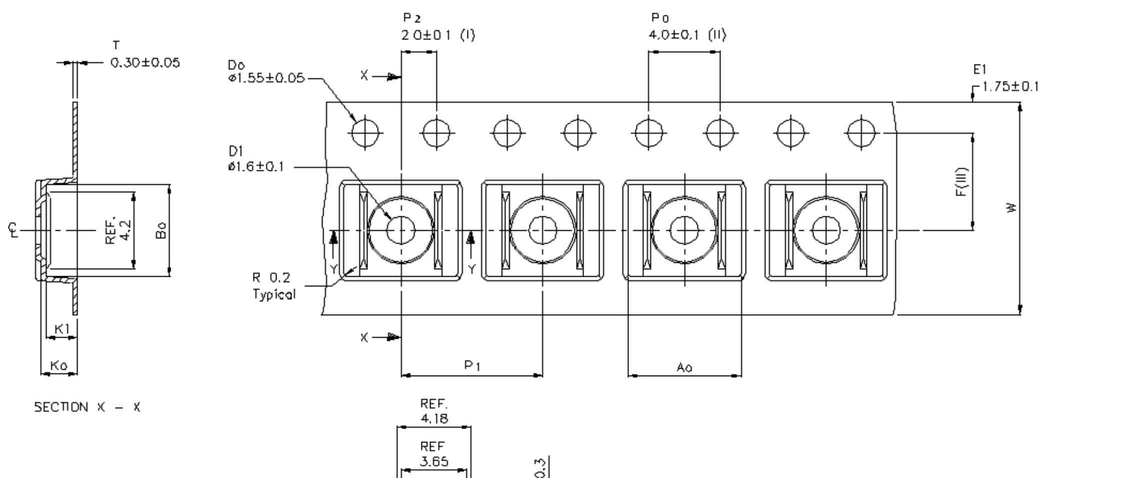


Figure 13.2 Tape Information of SOP8(300mil)



Ao	6.50	+/− 0.1
Bo	5.30	+/− 0.1
Ko	2.20	+/− 0.1
K1	1.90	+/− 0.1
F	5.50	+/− 0.1
P1	8.00	+/− 0.1
W	12.00	+/− 0.3

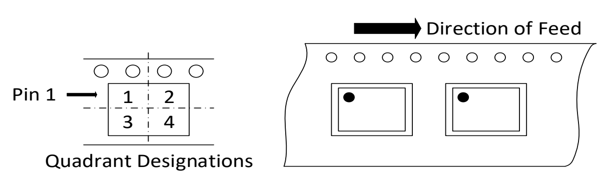


Figure 13.3 Tape Information of SOP8(150mil)

14. Revision History

Revision	Description	Date
1.0	Initial release	2024/8/15
1.1	Update Figure 10.1 SOW8 Package Shape and Dimension in millimeters.	2025/6/17

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