NSI1611S50
High Reliability Reinforced Isolated Amplifier
Datasheet (EN) 1.0

Product Overview

The NSI1611S50 is a high-performance isolated amplifier with output separated from input based on NOVOSENSE capacitive isolation technology, which provides the amplifier with exceptional resistance to magnetic interference.

The device accepts a single-ended voltage input of 0.01-4V and provides a single-ended output which can help to reduce the external differential to single ended amplifier. The low offset and gain drift ensure the accuracy over the entire temperature range.

The NSI1611S50 features high input impedance, making it an ideal choice for applications where large resistive dividers are used or when connecting any high-impedance voltage signal source to the input.

The high common-mode transient immunity ensures that the device is able to provide accurate and reliable measurements even in the presence of high-power switching such as in motor control applications.

Key Features

- Up to 5700V_{rms} Insulation voltage
- 0.01~4V linear Input Voltage Range
- Single-Ended Output with Adjustable Gain:
  - Gain = 0.2* V_{REFIN}
  - VREFIN = 5.0V recommended for best accuracy
- Low Offset Error and Drift:
  ±1.5mV (Max), ±45μV/°C (Max)
- Low Gain Error and Drift:
  ±0.25% (Max), ±35ppm/°C (Max)
- Low Nonlinearity and Drift:
  ±0.04% (Max), ±1ppm/°C (Typ)
- SNR: 82dB (Typ, BW=10kHz), 71dB (Typ, BW=100kHz)
- Wide bandwidth: 330kHz (Typ)
- High CMTI: 150kV/μs (Typ)
- Operation Temperature: -40°C ~125°C
- RoHS-Compliant Packages: SOP8(300mil)

Safety Regulatory Approvals

- UL recognition: 5700V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Motor Drives
- Server Power Supply Units
- Energy Storage Systems
- Solar Inverters
- Charging Piles

Device Information

Part Number	Package	Body Size
NSI1611S50-DSWVR	SOP8(300mil)	5.85mm × 7.50mm

Functional Block Diagrams

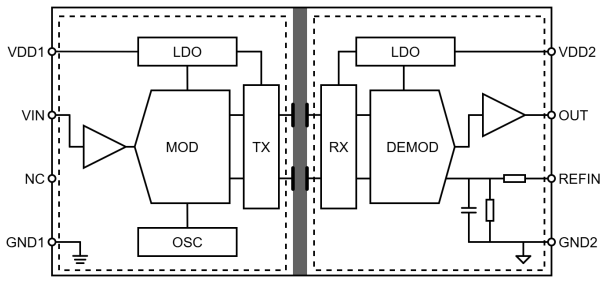

Figure 1. NSI1611S50 Block Diagram

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1. Pin Configuration and Functions

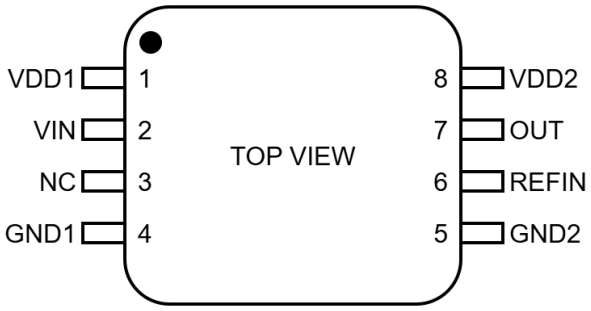


Figure 1.1 NSI1611S50 Package(Not to scale)

Table 1.1 NSI1611S50 Pin Configuration and Description

NSI1611S50 PIN NO.	*SYMBOL*	*FUNCTION*
1	VDD1	Input side power supply
2	VIN	Single ended analog input
3	NC	Not internally connected, connecting to GND1 recommended
4	GND1	Input side ground
5	GND2	Output side ground
6	REFIN	Reference voltage input, connect to recommended voltage for best accuracy
7	OUT	Single-ended analog output
8	VDD2	Output side power supply

2. Absolute Maximum Ratings(1)

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	VDDx to GNDx	-0.3		6.5	V
Analog Input Voltage	VIN	GND-0.5		VDD1+0.5	V
Analog Output Voltage	OUT	GND-0.5		VDD2+0.5	V
Reference Input Voltage	REFIN	GND-0.5		VDD2+0.5	V
Input current per IO Pin	I_{IN}	-10		10	mA
Junction Temperature	T_J	-40		150	°C
Storage Temperature	T_{STG}	-55		150	°C

(1) The device cannot operate beyond the listed Absolute Maximum Ratings to prevent permanent device damage. The device is not fully functional if operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings. Long-time stress of the absolute maximum conditions may affect the device lifetime.

3. ESD Ratings

Parameters	Test Condition	Value	Unit
Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2.0	kV
	Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1.0	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Power supply voltage	VDD1 to GND1	4.5	5.0	5.5	V
	VDD2 to GND2(1)	3.0	5.0	5.5	V
Input voltage before clipping output	$V_{Clipping}$		4.3		V
Linear differential input full scale voltage	V_{FSR}	0.01		4	V
Operating ambient temperature	T_A	-40		125	°C
Reference input voltage	V_{REFIN}(2)	3.0	5.0	5.5	V

(1) Voltage of VDD2 must be higher than that of REFIN to ensure sufficient headroom for VOUT to output the required voltage.

(2) V_{REFIN} = 5.0V for best accuracy performance, refer to section 6.1 for details.

5. Thermal Information

Parameters	*Symbol*	*SOP8(300mil)*	*Unit*
Junction–to-ambient thermal resistance	$R_{\theta JA}$	86	°C/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	28	°C/W
Junction-to-board thermal resistance	$R_{\theta JB}$	42	°C/W
Junction–to-top characterization parameter	Ψ_{JT}	4	°C/W
Junction-to-board characterization parameter	Ψ_{JB}	42	°C/W

6. Specifications

6.1. Electrical Characteristics of NSI1611S50

(Minimum and maximum specifications apply across the following conditions: VDD1 = 4.5 ~ 5.5V, VDD2 = 4.5 ~ 5.5V, INP =0.01V to 4V, V_{REFIN} = 5.0V T_A = -40°C to 125°C. Unless otherwise noted, Typical values are measured at VDD1 = VDD2 = 5V, T_A = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Input side supply voltage	VDD1	4.5	5	5.5	V	
Input side supply current	IDD1		7.2	9	mA	
Output side supply voltage	VDD2	4.5	5	5.5	V	
Output side supply current	IDD2		4.7	6	mA	
Input side VDD undervoltage detection threshold voltage	$VDD1_{UV}$	3.9	4.1	4.2	V	VDD1 rising threshold
		3.7	3.8	3.9	V	VDD1 falling threshold
Output side VDD undervoltage detection threshold voltage	$VDD2_{UV}$	2.6	2.7	2.8	V	VDD2 rising threshold
		2.3	2.4	2.5	V	VDD2 falling threshold
Analog Input						
Input offset voltage	V_{OS}	-1.5	±0.3	1.5	mV	V_{IN} = 0.01V, V_{REFIN} = 5.0V, at T_A = 25°C
		-5	±1.2	5	mV	V_{IN} = 0.01V, V_{REFIN} = 3.3V, at T_A = 25°C
Input offset drift (1)	TCV_{OS}	-45	±10	45	μV/°C	
Single-ended input resistance	R_{IN}		1		GΩ	
Input capacitance	C_I		5		pF	Single-ended input capacitance, fin=250kHz
Input offset current	I_{IO}		10		nA	VIN = GND1
REFIN input resistance	R_{REFIN}		100		kΩ	
Analog Output						
Nominal Gain	Gain		0.2*V_{REFIN}		V/V	
Gain error	E_G	-0.25%	±0.05%	0.25%		at T_A = 25°C
Gain error thermal drift (1)	TCE_G	-35	±10	35	ppm/°C	
Nonlinearity		-0.04%	±0.01%	0.04%		
Nonlinearity drift (1)			±1		ppm/°C	
Total harmonic distortion (3)	THD		-80		dB	V_{IN} = 0.01~4Vpp, f_{IN} = 10kHz, BW = 100kHz
Output noise			270		$μV_{RMS}$	VIN = GNDI, BW = 100kHz

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Signal to noise ratio	SNR		82		dB	V_{IN} = 0.01~4Vpp, f_{IN} = 1kHz, BW = 10kHz
	SNR		71		dB	V_{IN} = 0.01~4Vpp, f_{IN} = 10kHz, BW = 100kHz, 1MHz filter
Input clipping output voltage	$V_{clipout}$		4.3		V	V_{IN}>=$V_{Clipping}$
Output bandwidth	BW		330		kHz	
Power supply rejection ratio (2) of VDD1	$PSRR_{dc}$		-90		dB	PSRR vs VDD1, from 3.0~5.5V at DC
	$PSRR_{ac}$		-80		dB	PSRR vs VDD1, 100mV and 10kHz ripple
Power supply rejection ratio (2) of VDD2	$PSRR_{dc}$		-90		dB	PSRR vs VDD2, from 3.0~5.5V at DC
	$PSRR_{ac}$		-76		dB	PSRR vs VDD2, 100mV and 10kHz ripple
Output resistance	R_{OUT}		0.2		Ω	
Swing to GND2	V_{swing}			5	mV	V_{IN} = 0V, RL = 10kΩ
Mode selection threshold of REFIN	V_{th_refin}	1.75		2.5	V	V_{REFIN}>V_{th_refin} for ratiometric gain mode
Output limit current	I_{lim}		±14		mA	
Common-mode transient immunity	CMTI	100	150		kV/μs	Common-mode transient immunity
Timing						
Rising time of OUT	t_r		1.1		μs	
Falling time of OUT	t_f		1.1		μs	
VIN to OUT signal delay (50% - 50%)	t_{PD}		1.5	1.9	μs	
Analog setting time	t_{AS}		50	100	μ s	VDD step to 5.0 V, to OUT valid, 0.1% settling

(1) The temperature drift is calculated within the whole temperature range (-40°C to 125°C).

(2) Input referred.

(3) THD is defined as the ratio of the sum of the rms value of first five higher harmonics to the amplitude of the fundamental (input referred).

(4) Not test covered, guaranteed by characterization.

(5) Not test covered, guaranteed by design.

6.2. Timing Diagrams

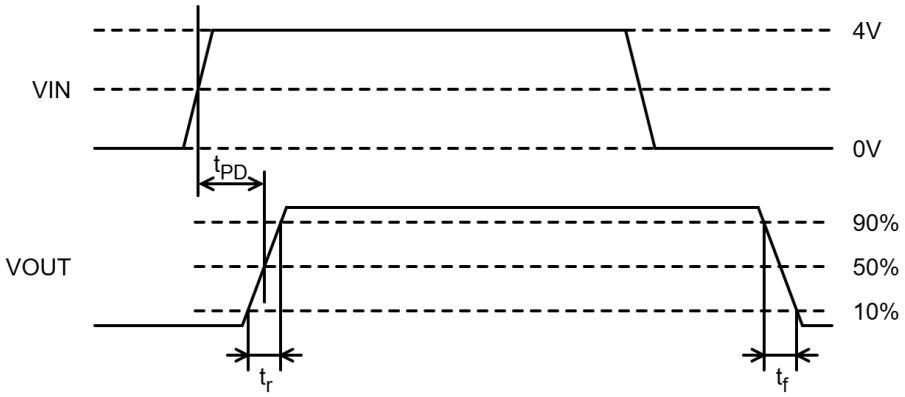


Figure 6.1 Propagation Delay and Output Fall Time Definition

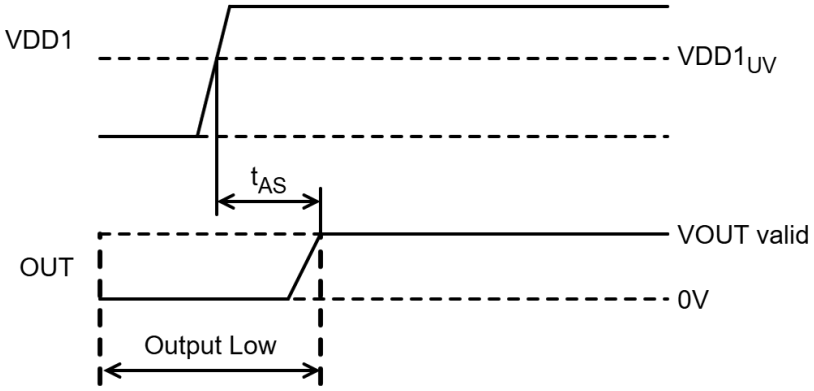


Figure 6.2 Analog Settling Time Definition

6.3. Typical Performance Characteristics

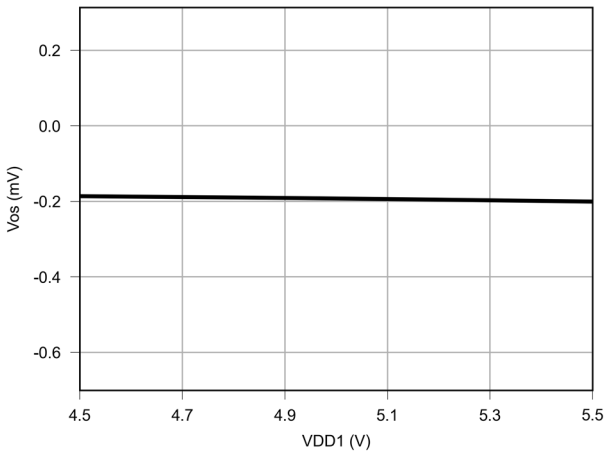


Figure 6.3 Vos vs VDD1

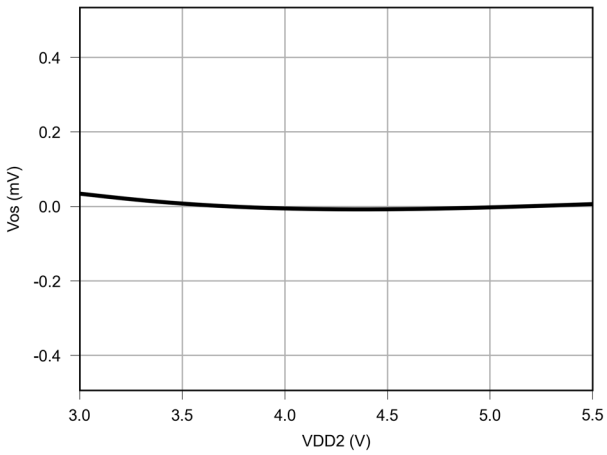


Figure 6.4 Vos vs VDD2

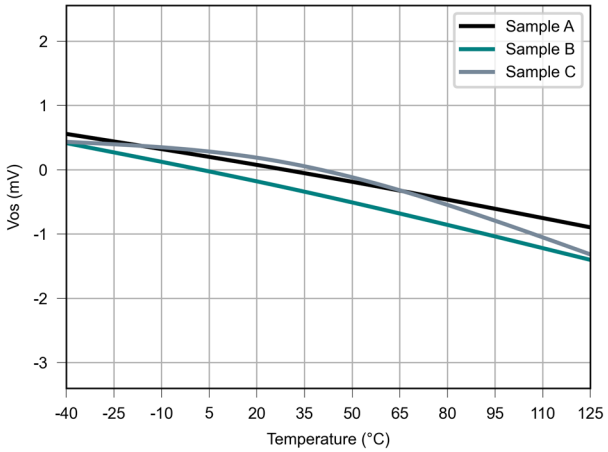


Figure 6.5 Vos vs Temperature

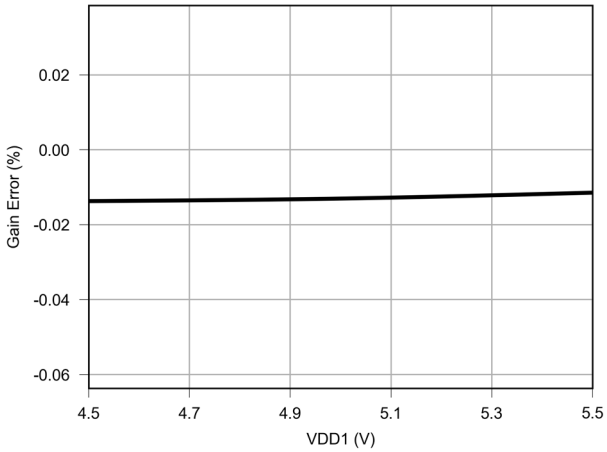


Figure 6.6 EG vs VDD1

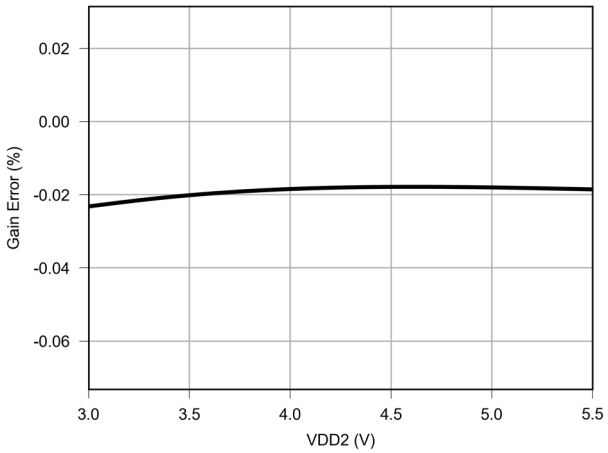


Figure 6.7 EG vs VDD2

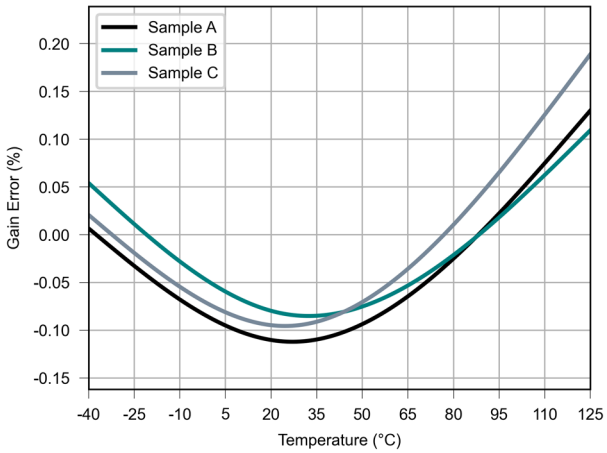


Figure 6.8 EG vs Temperature

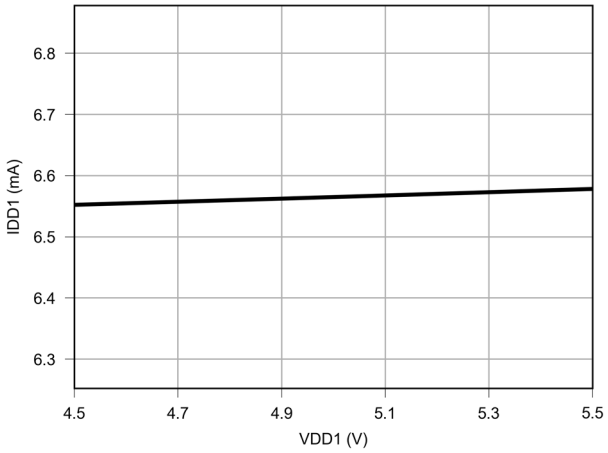


Figure 6.9 IDD1 vs VDD1

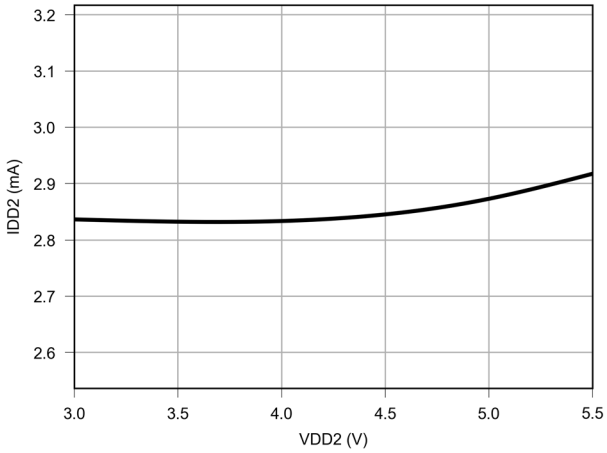


Figure 6.10 IDD2 vs VDD2

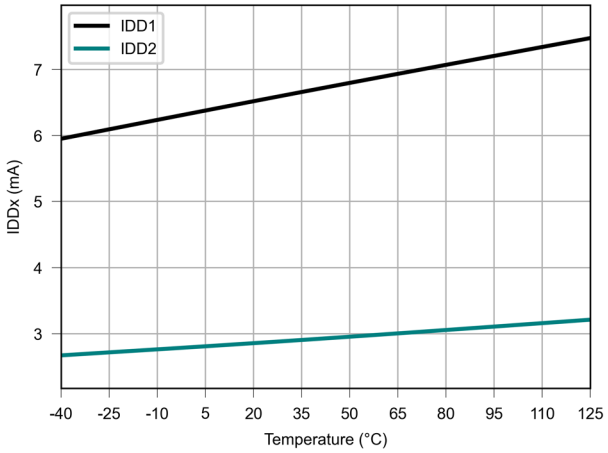


Figure 6.11 IDDx vs Temperature

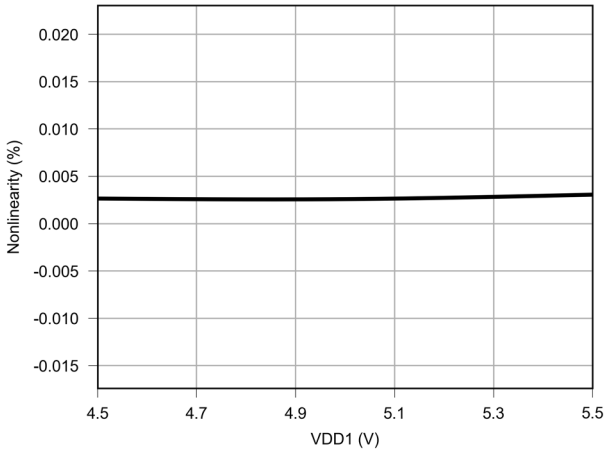


Figure 6.12 Nonlinearity vs VDD1

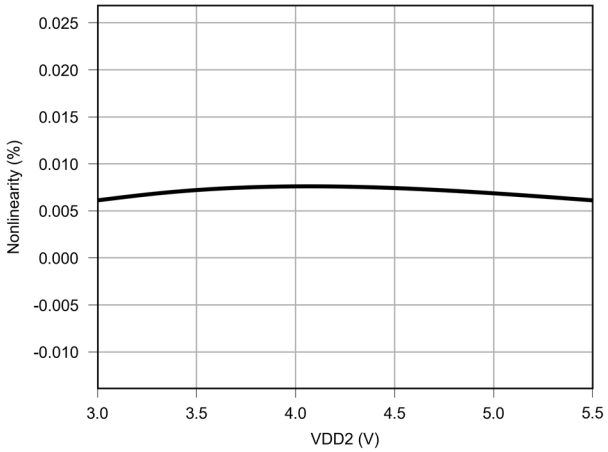


Figure 6.13 Nonlinearity vs VDD2

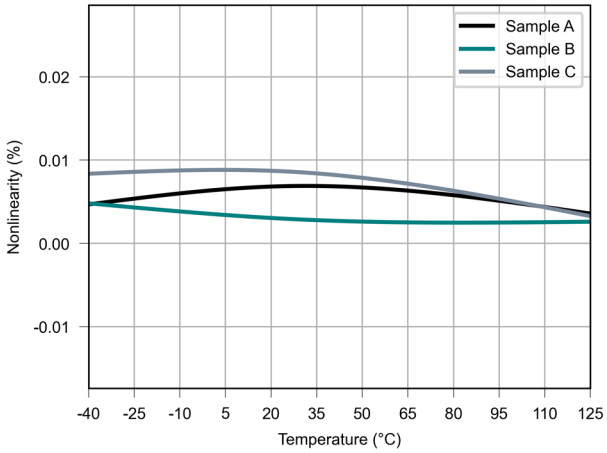


Figure 6.14 Nonlinearity vs Temperature

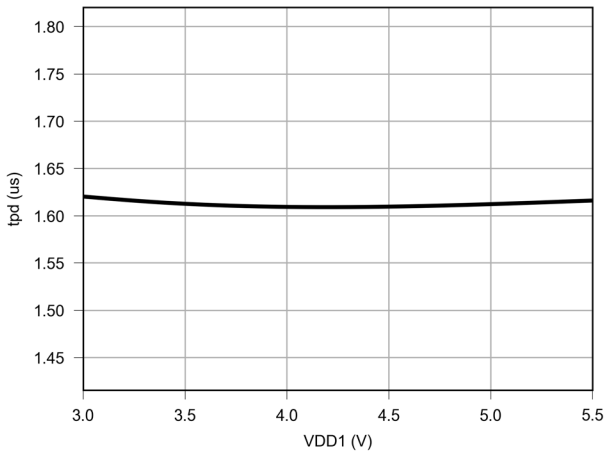


Figure 6.15 Propagation Delay vs VDD1

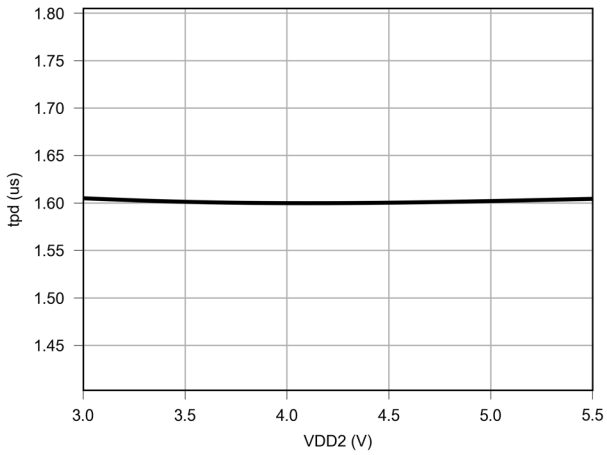


Figure 6.16 Propagation Delay vs VDD2

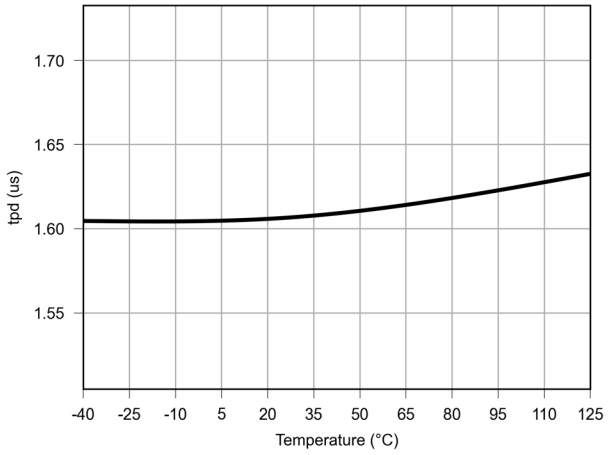


Figure 6.17 Propagation Delay vs Teperature

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value	Unit	Comments
Minimum External Clearance	CLR	8.5	mm	IEC 60664-1
Minimum External Creepage	CPG	8.5	mm	IEC 60664-1
Distance Through Insulation	DTI	18	μm	Distance through insulation (internal clearance – capacitive signal isolation)
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

Description	Test Condition	Value
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	I to IV
	For Rated Mains Voltage ≤ 300Vrms	I to IV
	For Rated Mains Voltage ≤ 600Vrms	I to III
Climatic Classification		40/125/21
Pollution Degree per DIN VDE 0110		2

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value	Unit
DIN EN IEC 60747-17 (VDE 0884-17)				
Maximum repetitive isolation voltage		V_{IORM}	1500	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	1060	V_{RMS}
	DC Voltage		1500	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, t_{ini} = 60 s , $V_{pd(m)}=1.2*V_{IORM}$, t_m=10s.	q_{pd}	<5	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, t_{ini}=60s ,$V_{pd(m)}=1.6*V_{IORM}$, t_m=10s			pC
	Method b, $V_{ini}=1.2*V_{IOTM}$, t_{ini}=1s $V_{pd\ (m)}=1.875*V_{IORM}$, t_m=1s（method b1）or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$(method b2)			pC
Maximum transient isolation voltage	t = 60sec	V_{IOTM}	8000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50μs waveform per IEC62368-1	V_{IMP}	7700	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50μs waveform, $V_{IOSM}≥V_{IMP}$ × 1.3	V_{IOSM}	10000	V_{PEAK}

Description	Test Condition	Symbol	Value	Unit
Isolation resistance	V_{IO} =500V, T_{amb}=25°C	R_{IO}	>10^{12}	Ω
	V_{IO} =500V, 100°C ≤ T_{amb} ≤ 125°C	R_{IO}	>10^{11}	Ω
	V_{IO} =500V, T_{amb}=T_s	R_{IO}	>10^{9}	Ω
Isolation capacitance	f = 1MHz	C_{IO}	0.8	pF
Safety total power dissipation	V_I = 5.5V, T_J = 150 °C, T_A = 25 °C	Ps	1430	mW
Safety input, output, or supply current	θ_{JA} = 82°C/W for SOW8, V_I = 5.5V, T_J = 150 °C, T_A = 25 °C	Is	260	mA
Maximum safety temperature		Ts	150	°C
UL1577				
Insulation voltage per UL	V_{TEST} = V_{ISO}, t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO}, t = 1s	V_{ISO}	5700	V_{RMS}

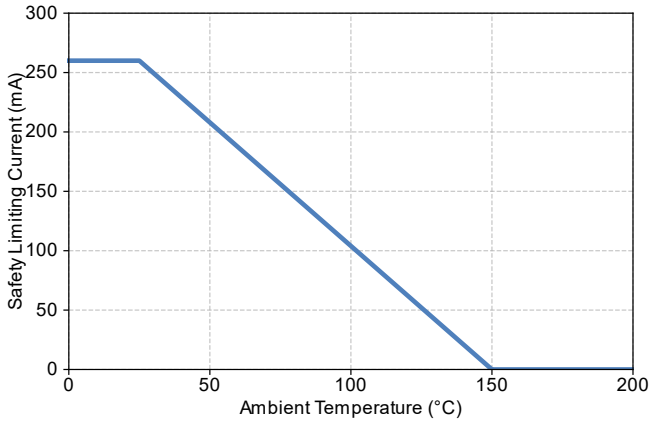


Figure 7.1 NSI1611S50 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

7.3. Regulatory Information

The NSI1611S50-DSWVR are approved or pending approval by the organizations listed in table.

UL		*CQC*	*TUV*	
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to GB4943.1	Certified According to EN IEC 62368-1	DIN EN IEC 60747-17 (VDE 0884-17)
Single Protection, 5700V_{rms} Isolation voltage	Single Protection, 5700V_{rms} Isolation voltage	Reinforced insulation	5700Vrms for 1min	Reinforce Insulation V_{IORM}=1500 V_{PEAK} V_{IOTM}=8000 V_{PEAK} V_{IOSM}=10000 V_{PEAK}
Pending	Pending	Pending	Pending	Pending

8. Function Description

8.1. Overview

The NSI1611S50 is a high-performance isolated amplifier with an input range of 0.01~4V and a single-ended output. The buffer at the input port ensures the input impedance is high enough for large resistive dividers input. Subsequently, the analog signal is modulated to a digital waveform to transfer through the isolation barrier. Both the modulator and the isolator drivers (designated as TX in the functional block diagram) are clocked by the inside oscillator. The isolator receiver (designated as RX in the functional block diagram) receives the modulated waveform and restores it to an analog form.

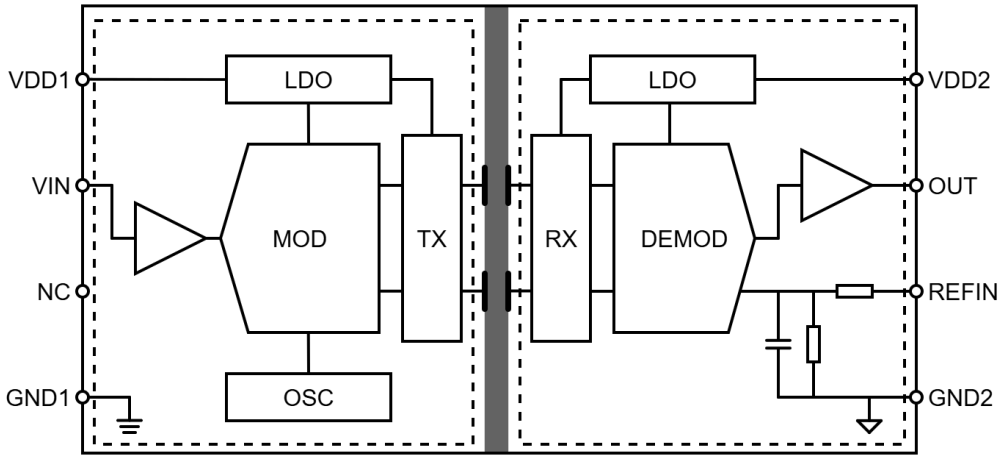


Figure 8.1 Function Block Diagram of NSI1611S50

8.2. Analog Input

There are two restrictions on the analog input signals VIN

- If the input voltage exceeds the range from GND1–0.5V to VDD1+0.5V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on.
- The linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (V_{FSR}). V_{FSR} is 0.01V to 4V for NSI1611S50, specified in Recommended Operating Conditions section.

8.3. Analog Output

The NSI1611S50 outputs a single-ended voltage relative to GND2. The voltage gain from input to output can be configured by the voltage on the pin REFIN. When REFIN is connected to an external reference voltage above 2.5V, the NSI1611S50 has a dynamic output voltage range proportional to the voltage of REFIN. The input to output curve is shown in Figure 8.2 and the output follows Equation 1

$$VOUT = 0.2 \times V_{REFIN} \times V_{IN} \quad \text{Equation 1}$$

The NSI1611S50 is trimmed under the condition that the voltage of REFIN is a precision 5.0V. It is highly recommended that the customers utilize the NSI1611S50 under the same condition for optimal accuracy performance. When the pin REFIN is applied with 5.0V, the nominal gain of NSI1611S50 is 1V/V.

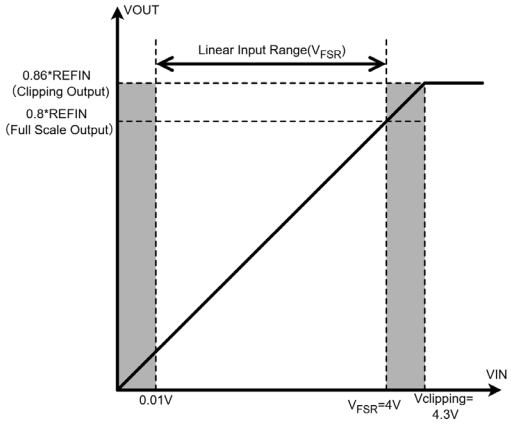


Figure 8.2 Input to Output Transfer Curve of the NSI1611S50

8.4. Accuracy Guaranteed Range and Output Voltage Swing

The accuracy of NSI1611S50 is not guaranteed when input voltage approaches zero volt, as the output buffer requires a minimum headroom above GND2. However, the device still retains the ability to provide an output close to zero volt, which is guaranteed by the parameter V_{swing}. As shown in Figure 8.3, all specs are tested and guaranteed from 0.01V to maximum input voltage. When input voltage is below 0.01V, the output voltage still follows input voltage while not all specs are covered in final test. The minimum voltage this device can output is tested and denoted as V_{swing}.

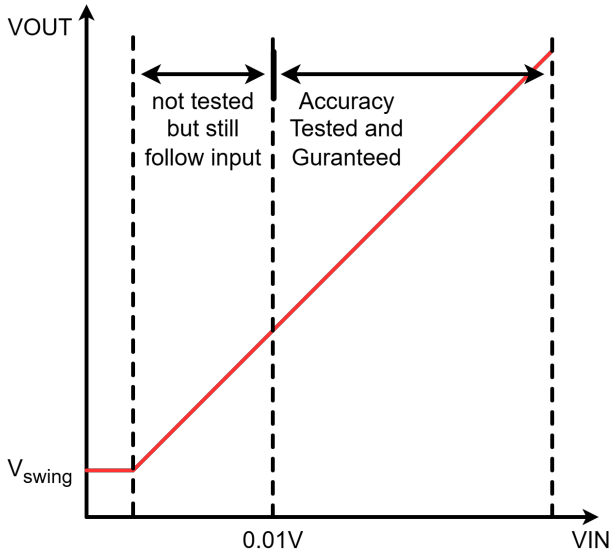


Figure 8.3 Output Curve near zero voltage (not to scale)

8.5. Device Operating States

The NSI1611S50 can operate in the following states:

- **Missing low-side power supply state**: This state is entered when the low-side supply (VDD2) drops below the $VDD2_{UV}$ threshold. In this state, the device is unresponsive, and the output (OUT) is in a high-impedance (Hi-Z) state.
- **Missing high-side power supply state**: When the low-side of the device (VDD2) is properly powered and within the recommended operating conditions, but the high-side power supply (VDD1) is below the $VDD1_{UV}$ threshold, the OUT pin is driven to GND2.
- **Analog input overrange state**: With both VDD1 and VDD2 operating within the recommended conditions, if the analog input voltage (V_{IN}) exceeds the maximum clipping voltage (VClipping, MAX), the device outputs Vclipping at the OUT pin.

- **Normal operating state**: When VDD1, VDD2, and V_{IN} all fall within their respective recommended operating ranges, the device enters normal operation, and the output delivers a voltage proportional to the input voltage and REFIN voltage.

OPERATING STATES	*VDD1*	*VDD2*	*V_{IN}*	*DESCRIPTION*
Missing low-side power supply state	No effect	VDD2 < $VDD2_{UV}$	No effect	The output (OUT) is in a high-impedance (Hi-Z) state.
Missing high-side power supply state	VDD1 < $VDD1_{UV}$	Valid(1)	No effect	The OUT pin is driven to GND2.
Analog input overrange state	Valid(1)	Valid(1)	V_{IN} > $V_{cilpping}$	The device outputs the clipping voltage: $V_{clipping}$ * Gain
Normal operating state	Valid(1)	Valid(1)	Valid(1)	The device outputs a voltage according to Equation(1)

(1) Valid denotes operation within the recommended operating conditions.

Figure 8.4 illustrates the operating states under different kinds of combination of power supply states.

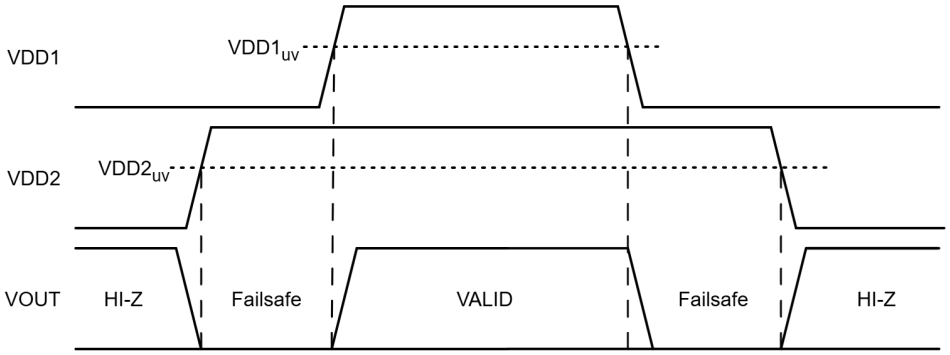


Figure 8.4 Waveform of NSI1611S50 when power fails

9. Application Note

9.1. Typical Application Circuit

Figure 9.1 illustrates a typical application example of NSI1611S50. On the input side, the HV_BUS voltage is divided down to 0.01~4V level across the bottom resistor of a high-impedance resistive divider. VDD1 needs a power supply from 4.5V to 5.5V. A 0.1uF capacitor and a 10uF capacitor in parallel on VDDx are recommended to improve EOS and stability. On the output side, NSI1611S50 provides an output proportional to the HV_BUS voltage

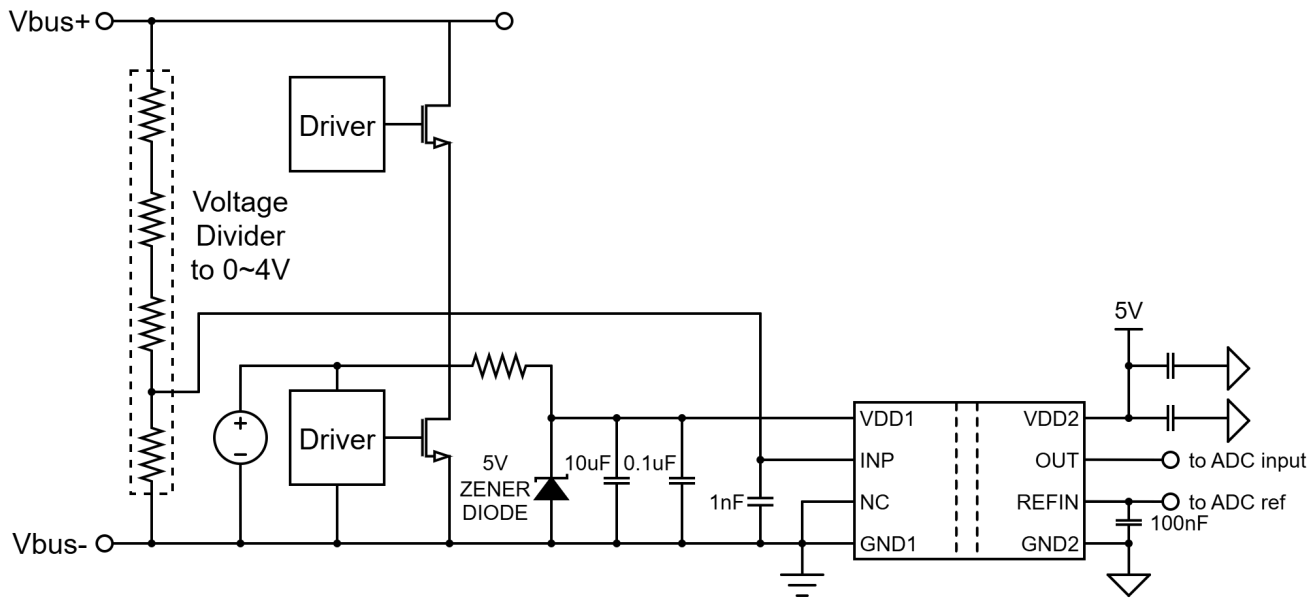


Figure 9.1 Typical Application Diagram of NSI1611S50

9.2. High Voltage Dividing Resistor Selection

Two restrictions should be considered when choosing the proper value of the voltage-dividing resistors:

- The current through the resistor should be within its rated range. Using Ohm law to calculate the cross current (I_{cross} = V_{max}/R_{total});
- The divided input voltage value should not exceed the linear input range of NSI1611S50, in which case the output may be clipped.

9.3. Accuracy Related Parameters

Parameters related to the accuracy performance are explained in this section, including Vos and its drift, EG and its drift, Nonlinearity. Other immunity parameters that affect accuracy like PSRR are also included.

9.3.1. Input Offset V_{OS} and Gain Error E_G

Vos and EG are the most significant factors influencing accuracy. The ideal curve and actual curve are shown in Figure 9.2.

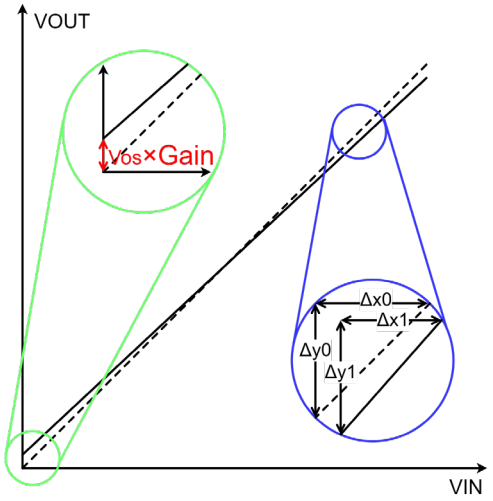


Figure 9.2 Vos and EG diagram

V_{OS} means the input offset voltage when input is 0.01V for NSI1611S. The tested output should be divided by nominal gain as Vos is defined as the offset voltage referred to input (See Equation 2).

$$Vos=Vo/Nominal\ Gain-0.01V \quad \text{Equation 2}$$

where

- Vo is the output voltage tested when input is 0.01V for NSI1611S50.
- Nominal Gain is 0.2 * V_{REFIN}
- Gain is the magnification of the amplifier, and the definition formula is shown in Equation 2. EG means the difference between actual and ideal slope. It should be noted that EG is tested across the whole input range to minimize test error (See Equation 4).

$$Gain=\frac{\Delta y1}{\Delta x1}=\frac{Vo1-Vo2}{Vin1-Vin2} \quad \text{Equation 3}$$

$$E_G=\frac{Gain-Nominal\ Gain}{Nominal\ Gain}\times 100\% \quad \text{Equation 4}$$

- where Vin1 and Vin2 are the lower and upper limit of the input FSR separately, Vo1 and Vo2 are the output voltage corresponding to Vin1 and Vin2.

9.3.2.Input Offset Drift TCV_{OS} and Gain Error Thermal Drift TCE_G

Input offset drift TCV_{OS} means the drift of V_{OS} over the whole operating temperature range, which is calculated as Equation 5.

$$TCVos=\frac{Vos_{max}-Vos_{min}}{TempRange} \quad \text{Equation 5}$$

where

- Vos_{max} and Vos_{min} are the maximum and minimum offset voltage over the whole operating ambient temperature range.
- TempRange covers the whole operating temperature, from -40°C to 125°C.

Gain error thermal drift TCE_G is the drift of E_G over the whole operating temperature range, which is calculated as Equation 6.

$$TCE_G=\frac{E_{Gmax}-E_{Gmin}}{TempRange} \quad \text{Equation 6}$$

where E_{Gmax} and E_{Gmin} are the maximum and minimum Gain Error over the whole temperature.

Both TCV_{OS} and TCE_G should be multiplied by the direction of temperature drift.

9.3.3.Nonlinearity

Nonlinearity describes the deviation between the actual output and the ideal linear output. Calculate the peak-to-peak value of the error between the actual output and the fitting curve, and nonlinearity is expressed as the ratio of half of the peak-to-peak error to the full-scale range of the output voltage (See Equation 7).

$$\text{Nonlinearity}=\frac{\text{Error\_pkpk}}{2\times V_{OFSR}}\times 100\% \qquad \text{Equation 7}$$

where

- Error_pkpk is the peak-to-peak value of the error between the actual output and the fitting curve.
- V_{OFSR} represents the full-scale range of the output voltage.

9.3.4.Power-Supply Rejection Ratio

Power-Supply Rejection Ratio (PSRR) describes the level of the output error (input inferred) which is affected by the variation of power supply. PSRR is defined in dB and calculated as Equation 8.

$$\text{PSRR}=20\times\log_{10}\left(\frac{V_{O\_var}}{\text{Nominal Gain}\times VDD_{var}}\right) \qquad \text{Equation 8}$$

Where V_{O_var} and VDD_{var} are respectively the variation value of the output voltage and the supply voltage.

9.3.5.Total Error Calculation

The total error is contributed by parameters discussed above. It is helpful to know the respective contribution of all different parameters when something is wrong about system current sensing. This section will introduce the calculation method of total error.

Parameters which mainly affect sensing accuracy are Vos, EG and Nonlinearity and their drift. PSRR is not a dominant factor in most cases. However, PSRR can be a concern when the power supply has high-frequency ripple, in which case a larger decoupling capacitor and a better layout are highly recommended (Refer to Section 9.4).

The error introduced by Vos and its drift can be calculated as:

$$\text{Error\_Vos}=\frac{Vos_{max}+TCV_{os}\times\Delta T}{V_{IN}}\times 100\% \qquad \text{Equation 9}$$

where

- Vosmax is the maximum value of input offset voltage at 25°C.
- TCV_{os} is the maximum drift of input offset voltage over the whole working temperature.
- ΔT is the range of temperature variation.
- V_{IN} is the input voltage in the application.

The error introduced by E_G and TCE_G can be calculated as：

$$\text{Error\_}E_G=E_G+TCE_G\times\Delta T \qquad \text{Equation 10}$$

where

- E_G is the maximum value of Gain Error when the temperature is 25°C.
- TCE_G is the maximum drift of Gain Error over the whole temperature.
- The error introduced by Nonlinearity is $\text{Nonlinearity}_{max}$, the maximum value of Nonlinearity in the entire temperature range, - 40°C to 125°C.

The total error sensing error is expressed as:

$$\text{Total\_Error}=\sqrt{\text{Error\_Vos}^2+\text{Error\_}E_G{}^2+\text{Nonlinearity}_{max}{}^2} \qquad \text{Equation 11}$$

For example, consider an NSI1611S50 with the sensing input voltage of 0~4V and a - 40°C to 85°C temperature range. The total error calculation is shown in Table 9.1.

Table 9.1 Total Error Calculation of NSI1611S50 (-40°C to 85°C)

Error Component	Symbol	Equation	Error at Vin=0.4V	Error at Vin=4.0V
Input offset error	Error_Vos	$Error\_Vos=\frac{Vos_{max}+TCV_{os}\times\Delta T}{V_{IN}}\times100\%=\frac{\pm1.5mV\pm45\mu V/°C\times60°C}{V_{IN}}\times100\%$	±1.05%	±0.105%
Gain error	Error_E_G	$Error\_E_G=E_G+TCE_G\times\Delta T=\pm0.25\%\pm35ppm/°C\times60°C$	±0.46%	±0.46%
Nonlinearity	$Nonlinearity_{max}$	$Nonlinearity_{max}=\pm0.04\%$	±0.04%	±0.04%
Total error	Total_Error	$Total\_Error=\sqrt{Error\_Vos^2+Error\_E_G{}^2+Nonlinearity_{max}{}^2}$	±1.147%	±0.474%

Since the input offset voltage is independent of input voltage, it becomes the dominant factor of the total error when the input voltage is low. To improve the system accuracy, especially under low-input applications, it is recommended to perform software zero-point calibration and gain error calibration. With system-level calibration, the total error can also be reduced significantly. The reduced error is calculated as Table 9.2.

Table 9.2 Total Error Calculation with Software Calibration of NSI1611S50 (- 40°C to 85°C)

Error Component	Symbol	Equation	Error at Vin=0.4 V	Error at Vin=4.0V
Input offset error	Error_Vos	$Error\_Vos=\frac{TCV_{os}\times\Delta T}{V_{IN}}\times100\%=\frac{\pm45\mu V/°C\times60°C}{V_{IN}}\times100\%$	±0.675%	±0.0675%
Gain error	Error_E_G	$Error\_E_G=TCE_G\times\Delta T=\pm35ppm/°C\times60°C$	±0.21%	±0.21%
Nonlinearity	$Nonlinearity_{max}$	$Nonlinearity_{max}=\pm0.04\%$	±0.04%	±0.04%
Total error	Error	$Total\_Error=\sqrt{Error\_Vos^2+Error\_E_G{}^2+Nonlinearity_{max}{}^2}$	±0.708%	±0.224%

The maximum total error with and without calibration is shown in Figure 9.3, considering 0~4V input as full input range, NSI1611S50 can achieve <0.75% error at more than 10% input voltage(Vin≥0.4V) with software calibration, and <1.2% error at more than 10% load(Vin≥0.4V) without software calibration.

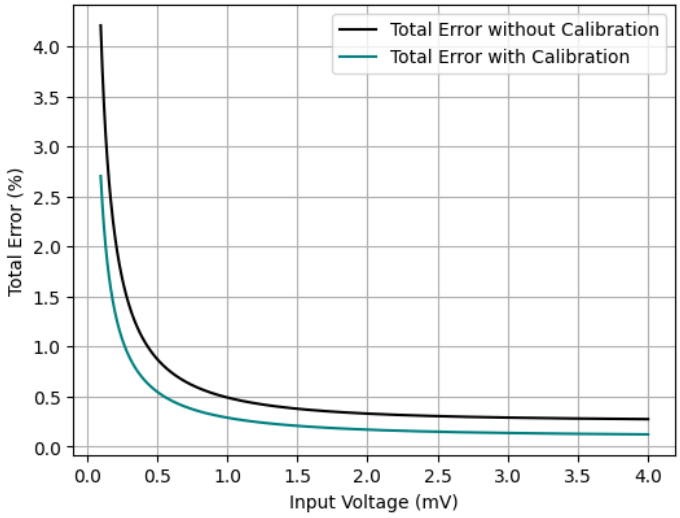


Figure 9.3 Total Error Over - 40°C to 85°C vs Input Voltage

9.4. PCB Layout

Figure 9.4 shows a typical layout example of NSI1611S50. To enhance power supply noise immunity and EOS robustness, it is recommended to use a low-ESR 100nF capacitor (C2, C4) in parallel with a low-ESR 1 μF capacitor (C1, C3). These capacitors should be positioned as close as possible to the power supply pins, and the smaller-value capacitors should be in the inner place as they usually have a lower ESR and better immunity to high-frequency interference.

An additional capacitor(C5) is recommended to be added in parallel with lower side divided resistor(R3). The capacitor is also recommended to be positioned as close as possible to the input pin VIN.

An input RC filter (R5 and C7) is recommended to be added to the REFIN pin. The passband of internal input filter is about 100kHz, a lower bandwidth may provide better result in case of interference.

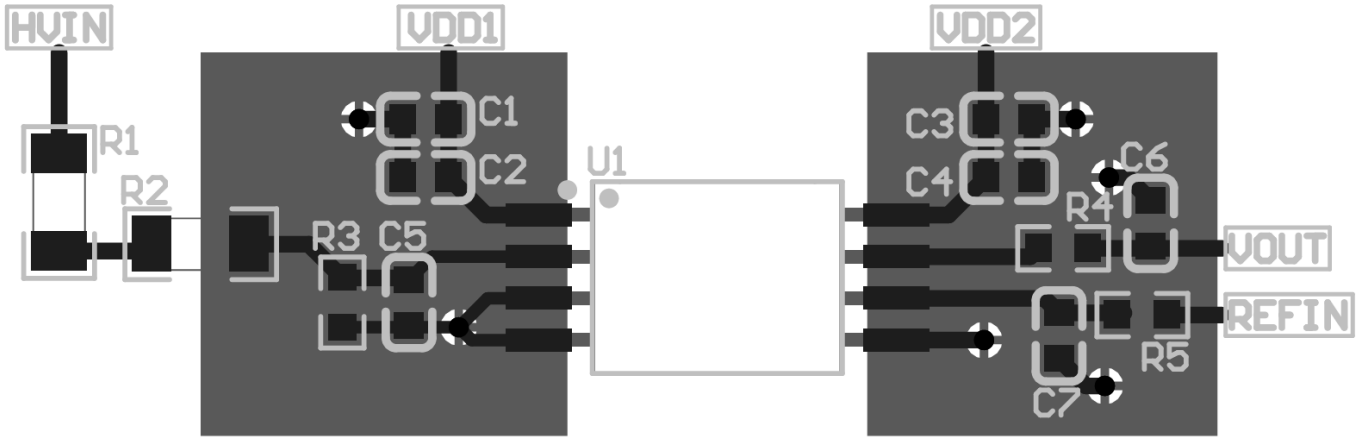
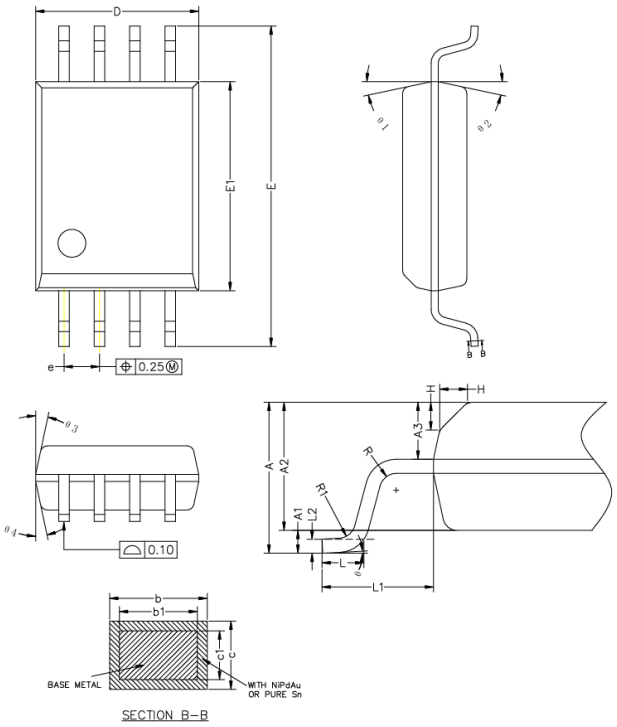


Figure 9.4 PCB layout example of NSI1611S50

10. Package Information

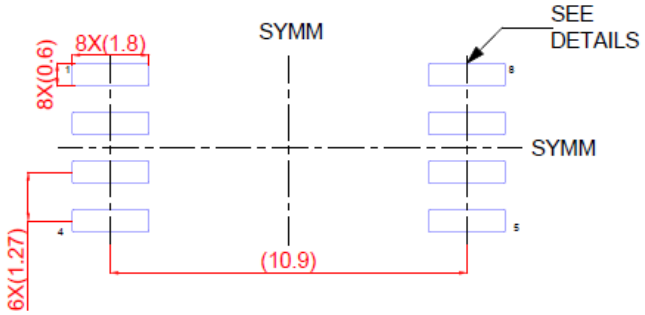


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	2.85
A1	0.31	0.41	0.51
A2	2.20	2.30	2.40
A3	0.97	1.02	1.07
b PURE Sn	0.33	–	0.47
NiPdAu	0.31	–	0.51
b1	0.29	–	0.43
c PURE Sn	0.22	–	0.35
NiPdAu	0.13	–	0.33
c1	0.11	–	0.31
D	5.75	5.85	5.95
E	11.25	11.50	11.75
E1	7.40	7.50	7.60
e		1.27BSC	
H		0.50REF	
L	0.50	–	1.00
L1		2.00REF	
L2		0.25BSC	
R		0.07REF	
R1		0.07REF	
θ	0°	–	8°
θ1		12°REF	
θ2		12°REF	
θ3		12°REF	
θ4		12°REF	

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.1 SOW8 package shape and dimension in millimeters



LAND PATTERN EXAMPLE(mm)
9.1 mm NOMINAL
CLEARANCE/CREEPAGE

SOLDER MASK DETAILS

Figure 10.2 SOW8 Package Board Layout Example

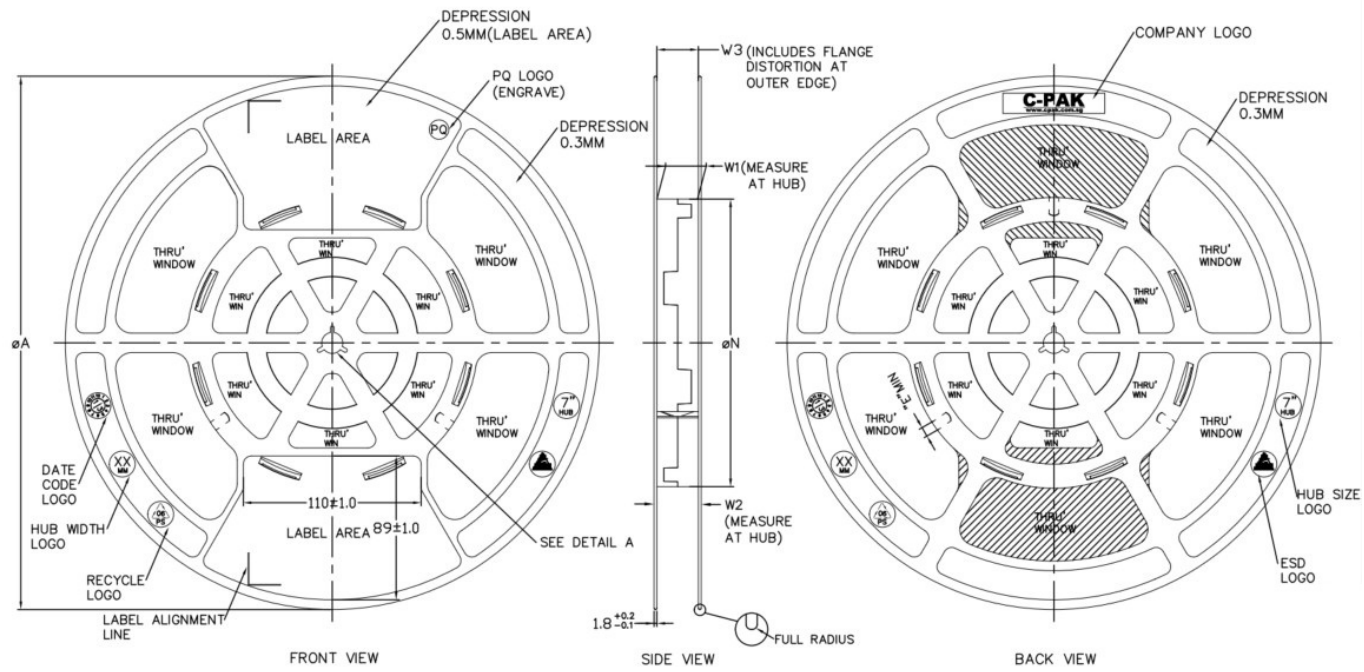
11. Ordering Information

Part No.	Isolation Rating(kV)	Linear Input Range	MSL	Device Marking	Temperature	Package Type	Package Drawing	SPQ	MPQ
NSI1611S50-DSWVR	5.7	0.01 ~ 4V	Level-3	NSi1611S50D	-40 to 125℃	SOP8 (300mil)	SOW8	1000	1000

12. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NSI1611S50	Click here	Click here	Click here	Click here

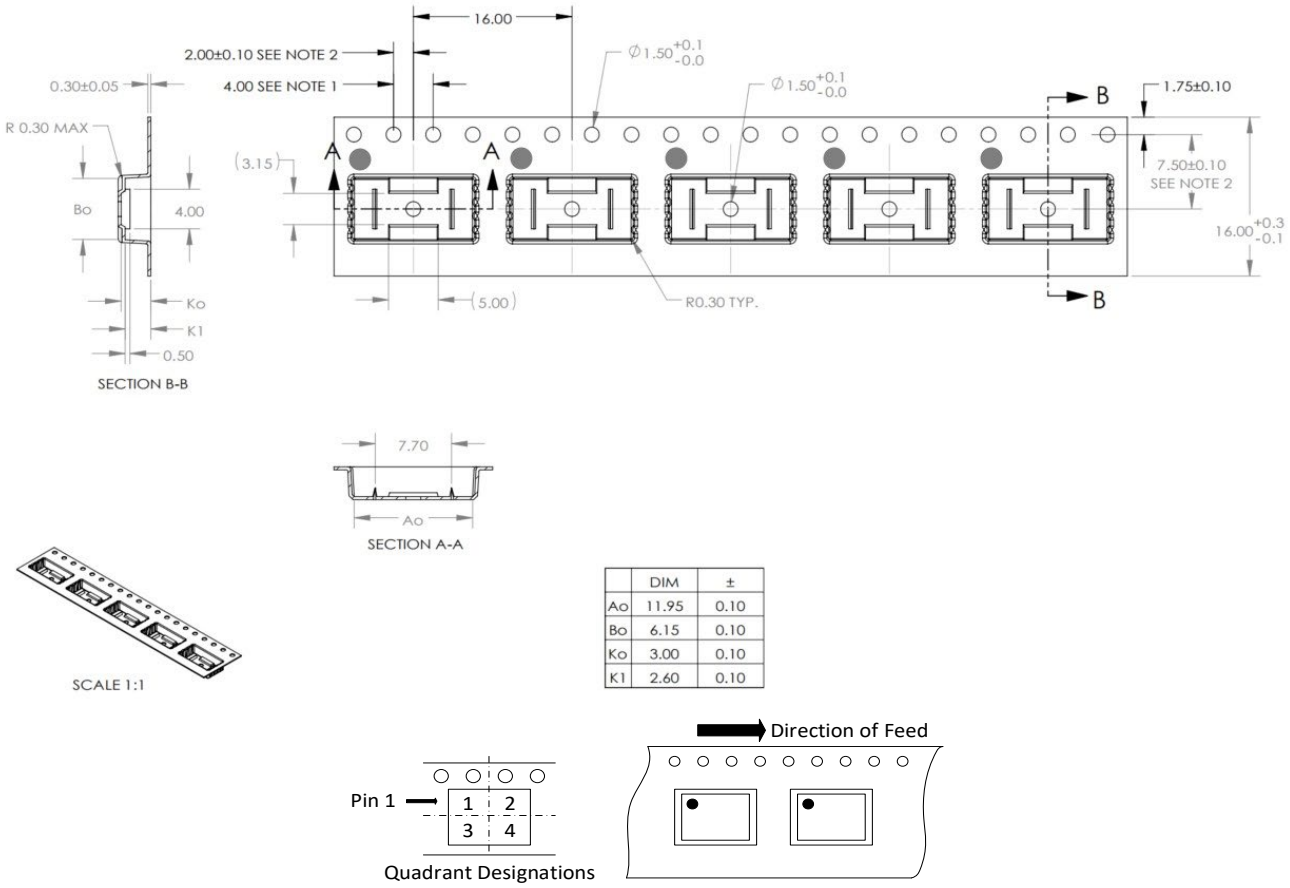
13. Tape and Reel Information



PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4	18.4		5.5
16MM	330	178	16.4	22.4		5.5
24MM	330	178	24.4	30.4		5.5
32MM	330	178	32.4	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{9} TO 10^{12}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{9}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{5} TO 10^{9}	ANTISTATIC (COATED)	ALL TYPES

Figure 13.1 Tape Information



	DIM	±
Ao	11.95	0.10
Bo	6.15	0.10
Ko	3.00	0.10
K1	2.60	0.10

Figure 13.2 Reel Information of SOP8(300mil)

14. Revision History

Revision	Description	Date
1.0	Initial Version.	2026/3/18

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