

High Reliability Reinforced Isolated Sigma-Delta Modulator with LVDS Interface

Product Overview

The NSI1305/6L is a high reliability reinforced isolated Σ - Δ modulator with LVDS digital interface. The device has a linear differential input signal range of $\pm 50\text{mV}$ or $\pm 250\text{mV}$. The differential input is ideally suited to shunt resistor-based current sensing in high voltage applications where isolation is required.

The analog input is amplified and continuously sampled by a second-order Σ - Δ modulator and converted to a high speed, single bit data stream. Both the input clock and the output data are LVDS interface conformed to TIA/EIA-644-A LVDS Standard. The output data is synchronous to the external clock with a frequency range from 5MHz to 21MHz. By using an appropriate digital filter (such as sinc3 filter) to decimate the bitstream, the device can achieve 16 bits resolution and an 86dB/82.5dB signal to noise ratio (SNR) at 78.125kSPS with a 20MHz master clock.

The fail-safe functions including input common-mode overvoltage detection and missing AVDD detection simplify system-level design and diagnostics.

Key Features

- Up to 5000V_{RMS} Insulation Voltage
- Clock frequency: 5MHz to 21MHz
- $\pm 50\text{mV}$ or $\pm 250\text{mV}$ Linear Input Voltage Range
- Low voltage differential signaling interface
- Excellent DC Performance:
 - Offset Error: $\pm 50\mu\text{V}$ or $\pm 100\mu\text{V}$ (Max)
 - Offset Drift: $-1.3\sim 1.3\mu\text{V}/^\circ\text{C}$ (Max)
 - Gain Error: $\pm 0.2\%$ (Max)
 - Gain Drift: $\pm 40\text{ppm}/^\circ\text{C}$ (Max)
- SNR: 82.5dB or 86dB (Typ)
- High CMTI: 150kV/ μs (Typ)

- Conforms to TIA/EIA-644-A LVDS Standard
- System-Level Diagnostic Features:
 - AVDD monitoring
 - Input common-mode overvoltage detection
- Operation Temperature: $-40^\circ\text{C}\sim 125^\circ\text{C}$
- RoHS-Compliant Package: SOP16(300mil)

Safety Regulatory Approvals

- UL recognition: up to 5000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Industrial Motor Drives
- Power and solar inverters
- Uninterruptible Power Suppliers

Device Information

Part Number	Package	Body Size
NSI1306Lx-DSWR	SOP16(300mil)	10.30mm × 7.50mm
NSI1305Lx-DSWR	SOP16(300mil)	10.30mm × 7.50mm

Functional Block Diagrams

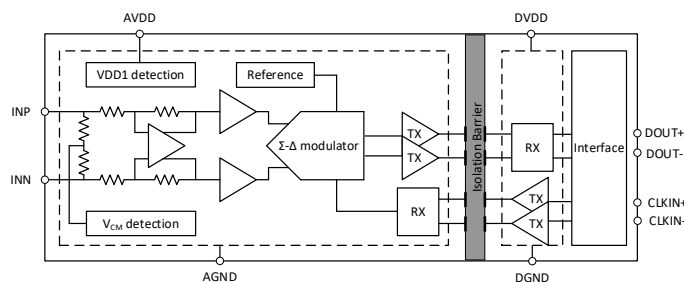


Figure 1. NSI1305/6L Block Diagram

INDEX

1. PIN CONFIGURATION AND FUNCTIONS	3
2. ABSOLUTE MAXIMUM RATINGS⁽¹⁾	5
3. ESD RATINGS	5
4. RECOMMENDED OPERATING CONDITIONS	5
5. THERMAL INFORMATION	6
6. SPECIFICATIONS	6
6.1. ELECTRICAL CHARACTERISTICS: NSI1305/6L05	6
6.2. ELECTRICAL CHARACTERISTICS: NSI1305/6L25	7
6.3. TIMING CHARACTERISTICS	9
6.4. TYPICAL PERFORMANCE CHARACTERISTICS	10
7. HIGH VOLTAGE FEATURE DESCRIPTION	14
7.1. INSULATION AND SAFETY RELATED SPECIFICATIONS	14
7.2. INSULATION CHARACTERISTICS	14
7.3. REGULATORY INFORMATION	15
8. FUNCTION DESCRIPTION	16
8.1. OVERVIEW	16
8.2. ANALOG INPUT	16
8.3. DIGITAL INPUT	16
8.4. DIGITAL OUTPUT	16
8.5. FAIL-SAFE OUTPUT	17
9. APPLICATION NOTE	18
9.1. TYPICAL APPLICATION CIRCUIT	18
9.2. SHUNT RESISTOR SELECTION	18
9.3. DIGITAL FILTER	19
9.4. PCB LAYOUT	19
10. PACKAGE INFORMATION	21
11. ORDERING INFORMATION	22
12. DOCUMENTATION SUPPORT	22
13. TAPE AND REEL INFORMATION	23
14. REVISION HISTORY	24

1. Pin Configuration and Functions

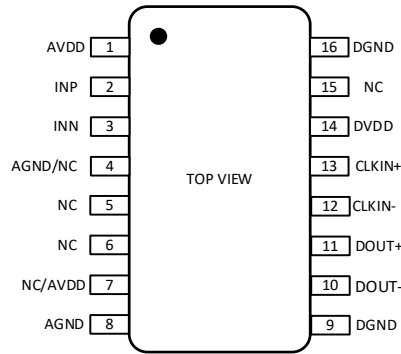


Figure 1.1 NSI1305/6L Package (SOP16(300mil))

Table 1.1 NSI1305/6L Pin Configuration and Description

NSI1305/6L PIN NO.	SYMBOL	FUNCTION
1	AVDD	Power supply for analog side (3.0V to 5.5V)
2	INP	Positive analog input (±250mV recommended for NSI1305/6L25 and ±50mV recommended for NSI1305/6L05)
3	INN	Negative analog input
4	AGND/NC	This pin is internally connected to pin 8 and can be tied to AGND or leave floating.
5	NC	Not internally connected, this pin can be left floating or tied to AVDD, AGND
6	NC	Not internally connected, this pin can be left floating or tied to AVDD, AGND
7	NC/AVDD	This pin is internally connected to pin 1 and can be left floating or tied to AVDD
8	AGND	Analog input ground reference
9	DGND	Digital output ground reference
10	DOUT-	Inverted modulator data output
11	DOUT+	Modulator data output
12	CLKIN-	Inverted modulator clock input
13	CLKIN+	Modulator clock input
14	DVDD	Power supply for digital side (3.0V to 5.5V)
15	NC	Not internally connected, this pin can be left floating or tied to DVDD, DGND
16	DGND	Digital ground reference

Table 1.2 NSI1305/6 Device Comparison Table

<i>PART NUMBER</i>	<i>LINEAR INPUT VOLTAGE RANGE</i>	<i>DIFFERENTIAL INPUT RESISTANCE</i>	<i>DIGITAL OUTPUT INTERFACE</i>
NSI1305L05	±50mV	4.9kΩ	LVDS (clock falling edge effective)
NSI1305L25	±250mV	22kΩ	
NSI1306L05	±50mV	4.9kΩ	LVDS (clock rising edge effective)
NSI1306L25	±250mV	22kΩ	

2. Absolute Maximum Ratings⁽¹⁾

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage ⁽²⁾	AVDD, DVDD	-0.3		6.5	V
Analog Input Voltage	INP, INN	AGND-6		AVDD+0.5	V
Digital Input Voltage	CLKIN+, CLKIN-	DGND-0.5		DVDD+0.5	V
Digital Output Voltage	DOUT+, DOUT-	DGND-0.5		DVDD+0.5	V
Output current per Output Pin	I _o	-10		10	mA
Junction Temperature	T _J	-40		150	°C
Storage Temperature	T _{STG}	-55		150	°C

(1) The device cannot operate beyond the listed Absolute Maximum Ratings to prevent permanent device damage. The device is not fully functional if operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings. Long-time stress of the absolute maximum conditions may affect the device lifetime.

(2) VDD1 to GND1, VDD2 to GND2

3. ESD Ratings

Parameters	Test Condition	Value	Unit
Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2.0	kV
	Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1.0	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Analog Side Power Supply	AVDD	3.0	5.0	5.5	V
Digital Side Power Supply	DVDD	3.0	3.3	5.5	V
NSI1305/6L05	Differential input voltage before clipping output	V _{Clipping}		±64	mV
	Linear differential input full scale voltage	V _{FSR}	-50	50	mV
	Operating common-mode input voltage	V _{CM}	-0.032		0.8
NSI1305/6L25	Differential input voltage before clipping output	V _{Clipping}		±320	mV
	Linear differential input full scale voltage	V _{FSR}	-250	250	mV
	Operating common-mode input voltage	V _{CM}	-0.16		0.8
Operating Ambient Temperature	T _A	-40		125	°C

5. Thermal Information

Parameters	Symbol	SOP16(300mil)	Unit
Junction-to-ambient thermal resistance	$R_{\theta JA}$	82	°C/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	42	°C/W
Junction-to-board thermal resistance	$R_{\theta JB}$	46	°C/W
Junction-to-top characterization parameter	Ψ_{JT}	12	°C/W
Junction-to-board characterization parameter	Ψ_{JB}	46	°C/W

6. Specifications

6.1. Electrical Characteristics: NSI1305/6L05

(AVDD = 3.0V ~ 5.5V, DVDD = 3.0V ~ 5.5V, INP = -50mV to +50mV, and INN = AGND = 0V, T_A = -40°C to 125°C and sinc³ filter with OSR=256. Unless otherwise noted, Typical values are at CLKIN=20MHz, AVDD = 5V, DVDD = 3.3V, T_A = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Analog Side Supply Voltage	AVDD	3.0	5.0	5.5	V	
Digital Side Supply Voltage	DVDD	3.0	3.3	5.5	V	
Analog Side Supply Current	IAVDD		11.5	15	mA	
Digital Side Supply Current	IDVDD		7.5		mA	
AVDD undervoltage detection threshold voltage	AVDD _{UV}	2	2.5	3	V	AVDD falling
Analog Input						
Common-mode overvoltage detection level	V _{CMov}	0.9			V	Detection level has a typical hysteresis of 96 mV
Common-mode rejection ratio	CMRR _{dc}		-95		dB	INP = INN, $f_{IN} = 0$ Hz, $V_{CM min} \leq V_{IN} \leq V_{CM max}$
	CMRR _{ac}		-99		dB	INP = INN, $f_{IN} = 10$ kHz, $V_{CM min} \leq V_{IN} \leq V_{CM max}$
Single-ended input resistance	R _{IN}		4.75		kΩ	INN = AGND
Differential input resistance	R _{IND}		4.9		kΩ	
Input capacitance	C _I		2		pF	
Input bias current	I _{IB}	-24	-23	-20	μA	INP = INN = AGND, $I_{IB} = (I_{IBP} + I_{IBN}) / 2$
Input bias current drift ⁽¹⁾	TCI _{IB}		±2		nA/°C	
Common-mode transient immunity	CMTI	100	150		kV/μs	Common-mode transient immunity

Parameters	Symbol	Min	Typ	Max	Unit	Comments
DC Accuracy						
Differential nonlinearity	DNL	-0.99		0.99	LSB	
Integral nonlinearity	INL	-4	±1	4	LSB	
Offset error	E _o	-50	±2.5	50	μV	INP = INN = AGND, at T _A = 25°C
Offset error thermal drift ⁽¹⁾	TCE _o	-0.5	±0.15	0.5	μV/°C	
Gain error	E _G	-0.2%	±0.005%	0.2%		at T _A = 25°C
Gain error thermal drift ⁽¹⁾	TCE _G	-30	±10	30	ppm/°C	
Power supply rejection ratio ⁽²⁾	PSRR		-106		dB	PSRR vs AVDD, at DC
			-104		dB	PSRR vs AVDD, 100mV and 10kHz ripple
AC Accuracy						
Signal to noise ratio	SNR	78	82.5		dB	f _{IN} = 1kHz
Signal to noise and distortion	SINAD	77	82.5		dB	f _{IN} = 1kHz
Total harmonic distortion ⁽³⁾	THD		-96	-84	dB	f _{IN} = 1kHz
Spurious-free dynamic range	SFDR		100		dB	f _{IN} = 1kHz
Digital Input / Output (LVDS logic)						
Output differential voltage	V _{OD}	250	350	450	mV	
Output common mode voltage	V _{OC}	1.125	1.23	1.375	V	
Output short circuit current	I _{OC}		3.5		mA	
Input differential voltage	V _{ID}	100	350	600	mV	RLOAD=100Ω
Input common mode voltage	V _{IC}	0.05	1.25	3.25	V	V _{ID} =100mV
Receiver input current	I _{IN}	-20	0	20	μA	V _{IN} ≤3.3V

(1) The temperature drift is calculated with the whole temperature range (-40°C to 125°C).

(2) Input referred.

(3) THD is defined as the ratio of the sum of the rms value of first five higher harmonics to the amplitude of the fundamental (input referred).

6.2. Electrical Characteristics: NSI1305/6L25

(AVDD = 3.0V ~ 5.5V, DVDD = 3.0V ~ 5.5V, INP = -250mV to +250mV, and INN = AGND = 0V, T_A = -40°C to 125°C and sinc³ filter with OSR=256. Unless otherwise noted, Typical values are at CLKIN=20MHz, AVDD = 5V, DVDD = 3.3V, T_A = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Analog Side Supply Voltage	AVDD	3.0	5.0	5.5	V	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Digital Side Supply Voltage	DVDD	3.0	3.3	5.5	V	
Analog Side Supply Current	IAVDD		11.4	15.1	mA	
Digital Side Supply Current	IDVDD		7.5	9	mA	
AVDD undervoltage detection threshold voltage	AVDD _{UV}	1.8	2.3	2.7	V	AVDD falling
Analog Input						
Common-mode overvoltage detection level	V _{CMov}	0.9			V	Detection level has a typical hysteresis of 96 mV
Common-mode rejection ratio	CMRR _{dc}		-106		dB	INP = INN, f _{IN} = 0 Hz, V _{CM min} ≤ VIN ≤ V _{CM max}
	CMRR _{ac}		-104		dB	INP = INN, f _{IN} = 10 kHz, V _{CM min} ≤ VIN ≤ V _{CM max}
Single-ended input resistance	R _{IN}		19		kΩ	INN = AGND
Differential input resistance	R _{IND}		22		kΩ	
Input capacitance	C _I		2		pF	
Input bias current	I _{IB}	-24	-18	-12	μA	INP = INN = AGND, I _{IB} = (I _{IBP} + I _{IBN}) / 2
Input bias current drift ⁽¹⁾	TC _{I_{IB}}		±1		nA/°C	
Common-mode transient immunity	CMTI	100	150		kV/μs	Common-mode transient immunity
DC Accuracy						
Differential nonlinearity	DNL	-0.99		0.99	LSB	
Integral nonlinearity	INL	-4	±1	4	LSB	
Offset error	E _O	-100	±4.5	100	μV	INP = INN = AGND, at T _A = 25°C
Offset error thermal drift ⁽¹⁾	TCE _O	-1.3	±0.15	1.3	μV/°C	
Gain error	E _G	-0.2%	±0.005%	0.2%		at T _A = 25°C
Gain error thermal drift ⁽¹⁾	TCE _G	-40	±20	40	ppm/°C	
Power supply rejection ratio ⁽²⁾	PSRR		-100		dB	PSRR vs AVDD, at DC
			-90		dB	PSRR vs AVDD, 100mV and 10kHz ripple
AC Accuracy						
Signal to noise ratio	SNR	82	86		dB	f _{IN} = 1kHz
Signal to noise and distortion	SINAD	82	86		dB	f _{IN} = 1kHz

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Total harmonic distortion ⁽³⁾	THD		-95	-85	dB	$f_{IN} = 1\text{kHz}$
Spurious-free dynamic range	SFDR		100		dB	$f_{IN} = 1\text{kHz}$
Digital Input / Output (LVDS logic)						
Output differential voltage	V_{OD}	250	350	450	mV	
Output common mode voltage	V_{OC}	1.125	1.23	1.375	V	
Output short circuit current	I_{OC}		3.5		mA	
Input differential voltage	V_{ID}	100	350	600	mV	$R_{LOAD}=100\Omega$
Input common mode voltage	V_{IC}	0.05	1.25	3.25	V	$V_{ID}=100\text{mV}$
Receiver input current	I_{IN}	-20	0	20	μA	$V_{IN}\leq 3.3\text{V}$

(1) The temperature drift is calculated with the whole temperature range (-40°C to 125°C).

(2) Input referred.

(3) THD is defined as the ratio of the sum of the rms value of first five higher harmonics to the amplitude of the fundamental (input referred).

6.3. Timing Characteristics

(AVDD = 3.0V ~ 5.5V, DVDD = 3.0V ~ 5.5V, $T_A = -40^\circ\text{C}$ to 125°C and sinc³ filter with OSR=256. Unless otherwise noted, Typical values are at CLKIN=20MHz, AVDD = 5V, DVDD = 3.3V, $T_A = 25^\circ\text{C}$)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
CLKIN clock frequency	f_{CLKIN}	5		21	MHz	
CLKIN clock period	t_{CLKIN}	47.6		200	ns	
Clock duty ratio	Duty	40%	50%	60%		
Rising edge of CLKIN to DOUT valid delay	t_D		11	15	ns	$C_{LOAD} = 5\text{pF}$
Analog setting time	t_{AS}		0.5		ms	AVDD step to 3.0 V with DVDD $\geq 3.0\text{V}$, to DOUT valid, 0.1% settling

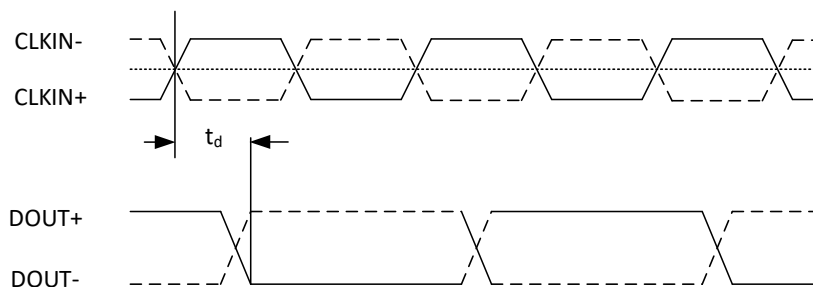


Figure 6.1 Digital Input and Output Timing (NSI1306L CLKIN rising edge effective)

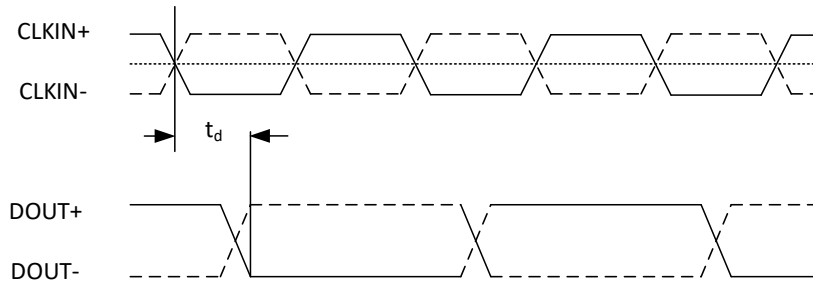


Figure 6.2 Digital Input and Output Timing (NSI1305L CLKIN falling edge effective)

6.4. Typical Performance Characteristics

Unless otherwise noted, test at AVDD = 5V, DVDD = 3.3V, Vin = -250mV to 250mV (NSI1305/6L25) or -50mV to 50mV (NSI1305/6L05), CLKIN=20MHz, and sinc³ filter with OSR=256.

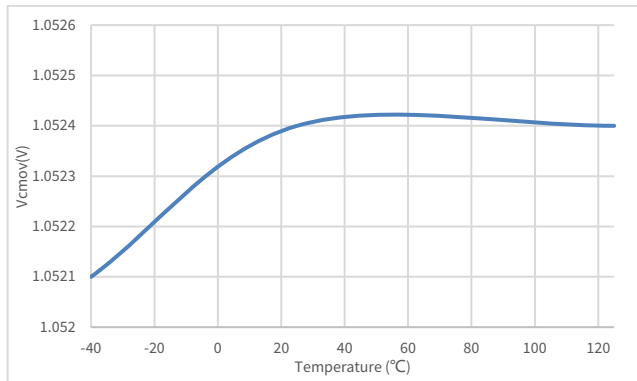


Figure 6.3 Common-Mode Overtolerance Detection Level vs Temperature

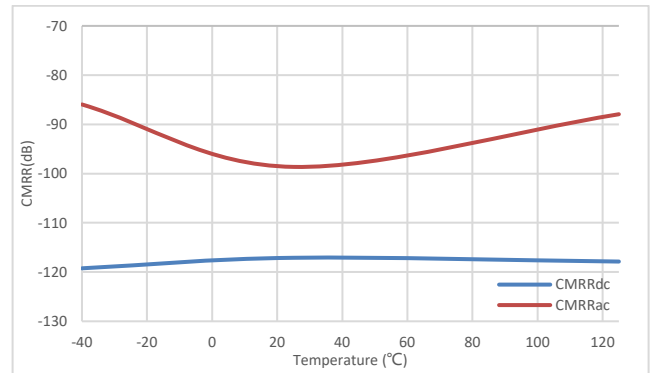


Figure 6.6 Common-Mode Rejection Ratio vs Temperature

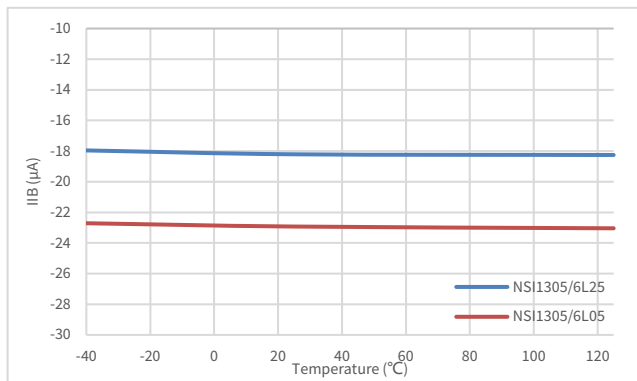


Figure 6.4 Input Bias Current vs Temperature

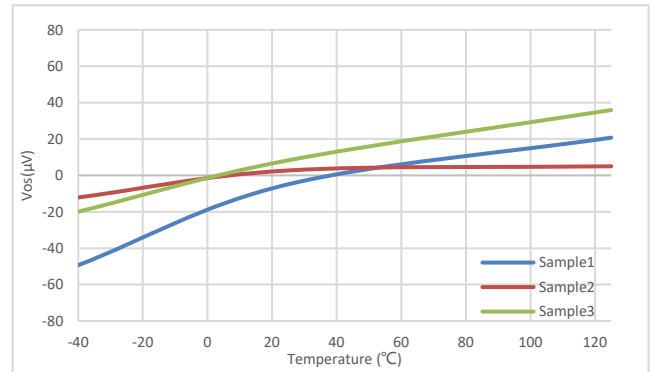


Figure 6.7 Input Offset Voltage vs Temperature (NSI1305/6L25)

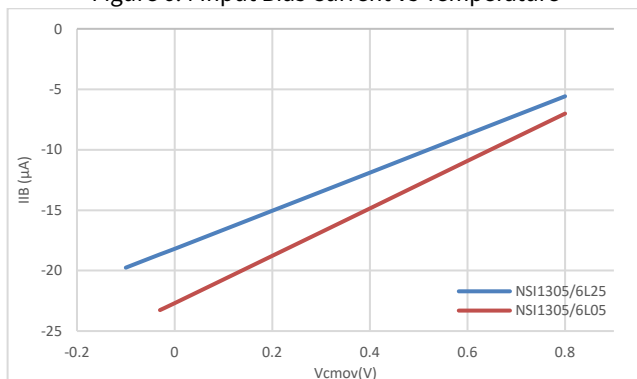


Figure 6.5 Input Bias Current vs Common-Mode voltage

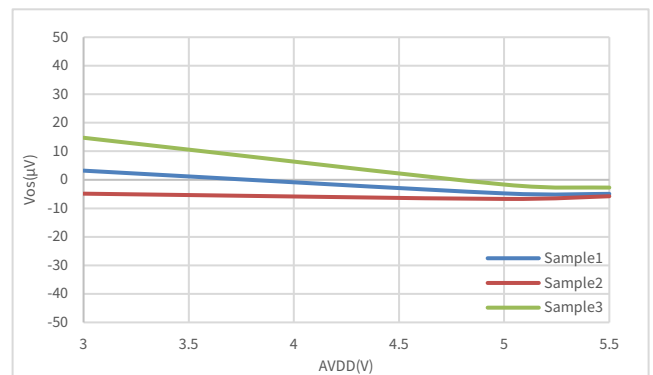


Figure 6.8 Input Offset Voltage vs Analog Side Supply Voltage (NSI1305/6L25)

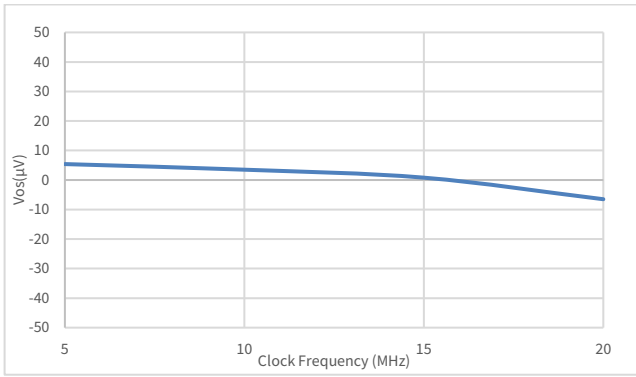


Figure 6.9 Input Offset Voltage vs Clock Frequency (NSI1305/6L25)

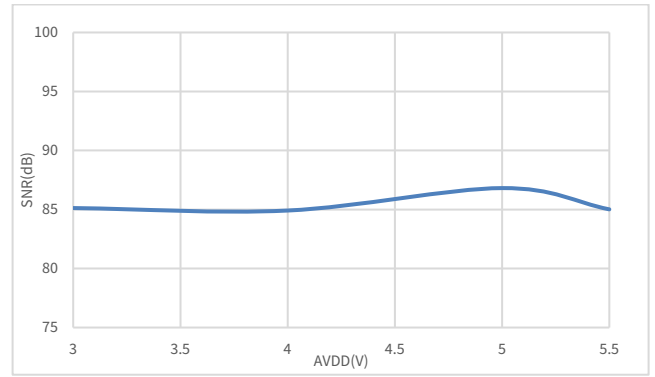


Figure 6.13 Signal-to-Noise Ratio vs Analog Side Supply Voltage (NSI1305/6L25)

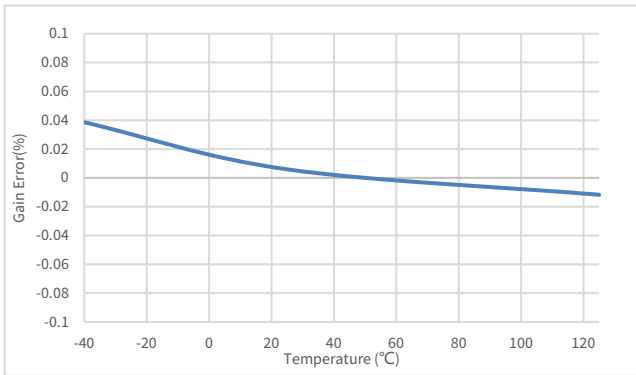


Figure 6.10 Gain Error vs Temperature

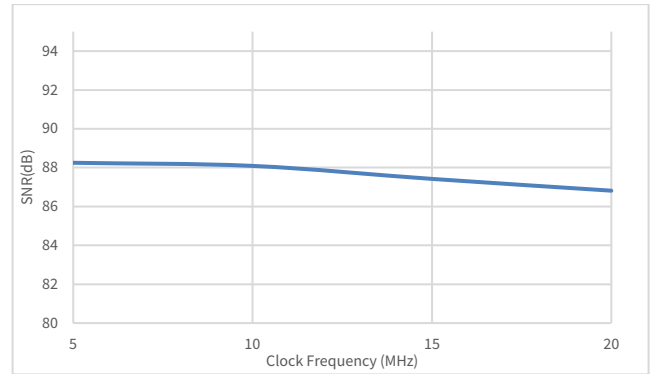


Figure 6.14 Signal-to-Noise Ratio vs Clock Frequency (NSI1305/6L25)

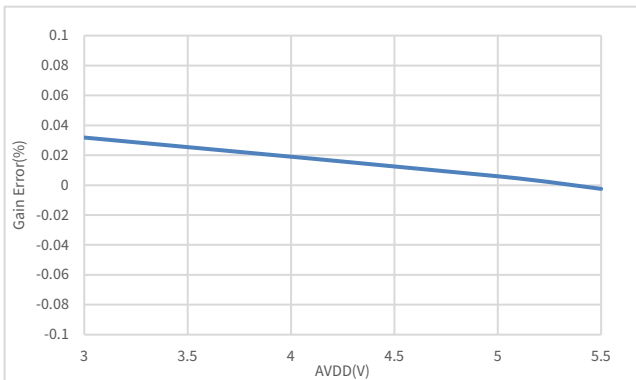


Figure 6.11 Gain Error vs Analog Side Supply Voltage

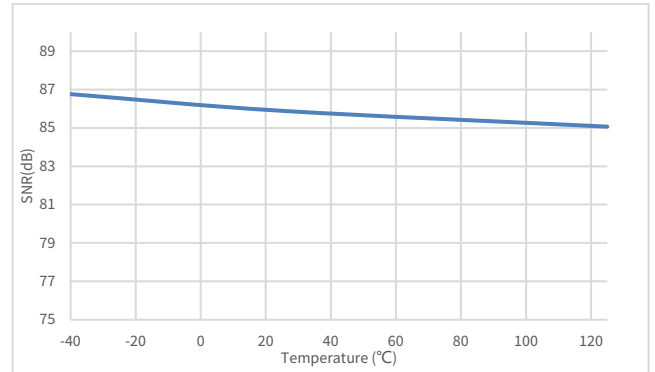


Figure 6.15 Signal-to-Noise Ratio vs Temperature (NSI1305/6L25)

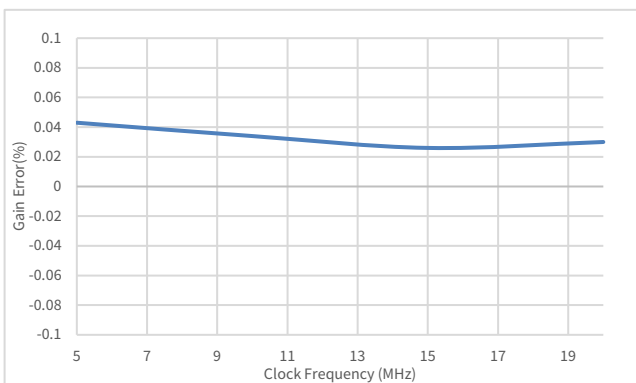


Figure 6.12 Gain Error vs Clock Frequency

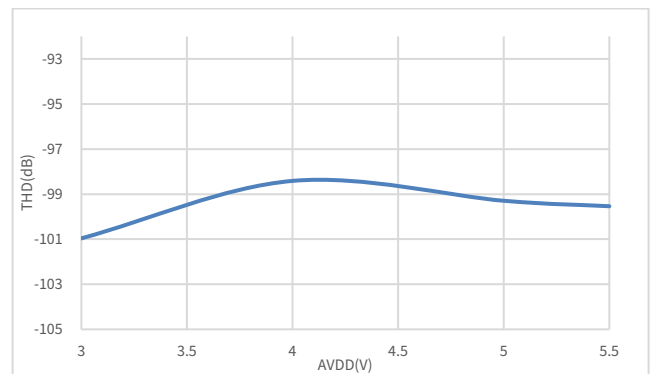


Figure 6.16 Total Harmonic Distortion vs Analog Side Supply Voltage (NSI1305/6L25)

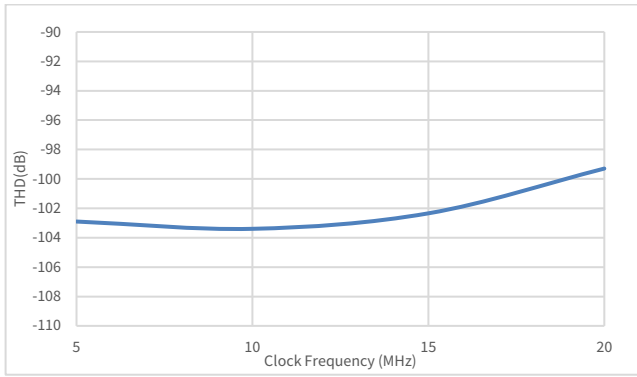


Figure 6.17 Total Harmonic Distortion vs Clock Frequency (NSI1305/6L25)

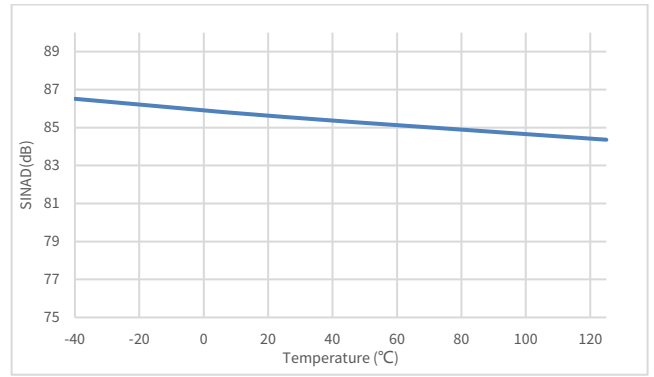


Figure 6.21 Signal-to-Noise + Distortion vs Temperature (NSI1305/6L25)

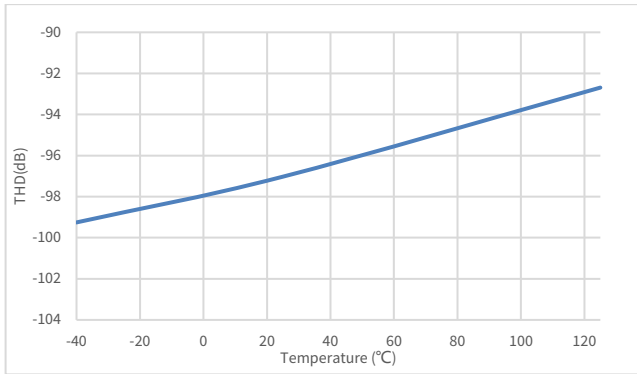


Figure 6.18 Total Harmonic Distortion vs Temperature (NSI1305/6L25)

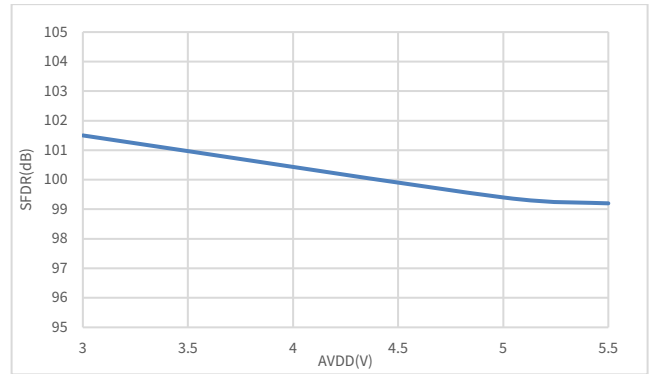


Figure 6.22 Spurious-Free Dynamic Range vs Analog Side Supply Voltage (NSI1305/6L25)

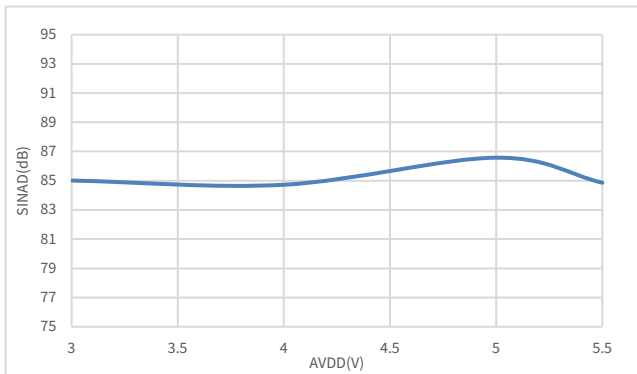


Figure 6.19 Signal-to-Noise + Distortion vs Analog Side Supply Voltage (NSI1305/6L25)

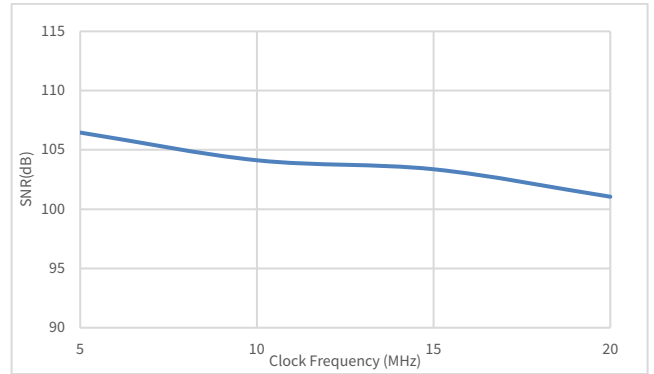


Figure 6.23 Spurious-Free Dynamic Range vs Clock Frequency (NSI1305/6L25)

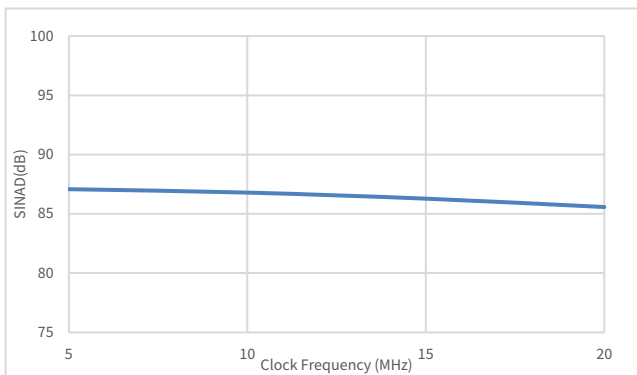


Figure 6.20 Signal-to-Noise + Distortion vs Clock Frequency (NSI1305/6L25)

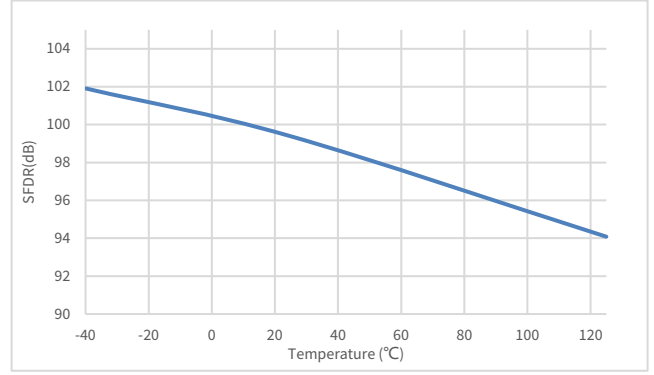


Figure 6.24 Spurious-Free Dynamic Range vs Temperature (NSI1305/6L25)

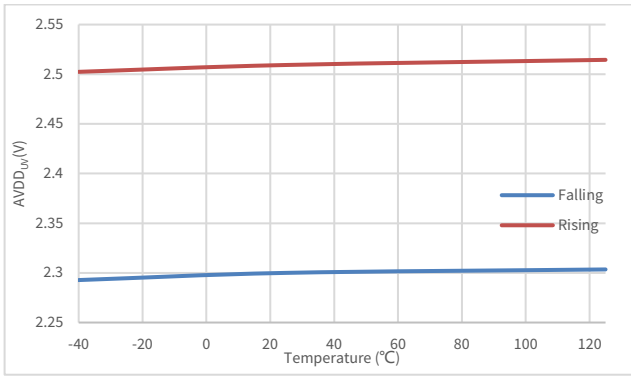


Figure 6.25 Analog Side Under-Voltage Detection Level vs Temperature

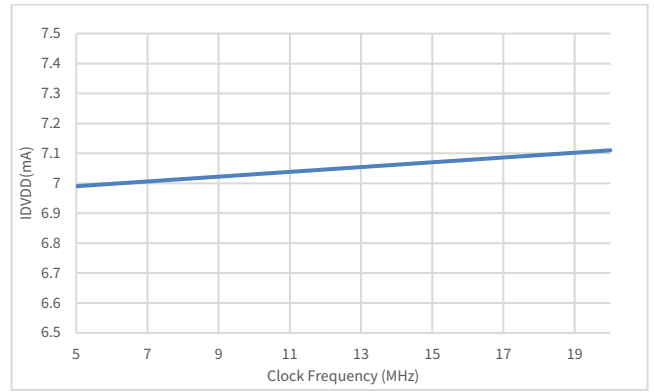


Figure 6.29 Digital Side Supply Current vs Clock Frequency

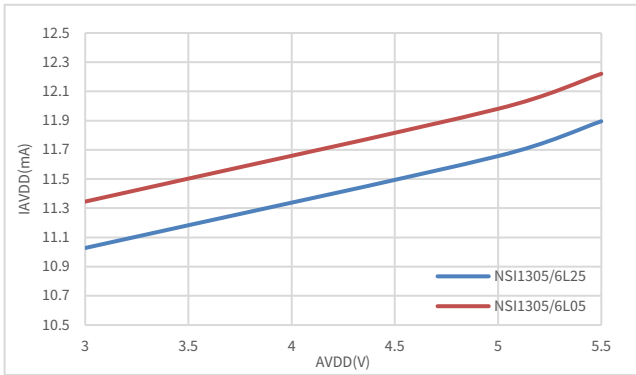


Figure 6.26 Analog Side Supply Current vs Supply Voltage

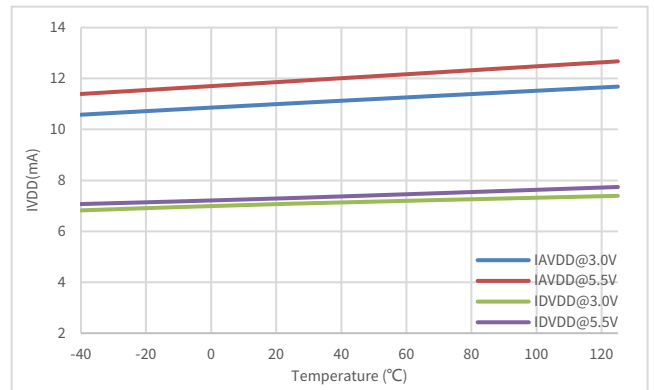


Figure 6.30 Supply Current vs Temperature (NSI1305/6L25)

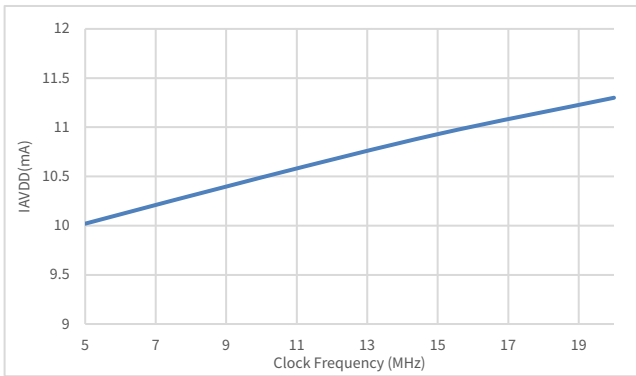


Figure 6.27 Analog Side Supply Current vs Clock Frequency (NSI1305/6L25)

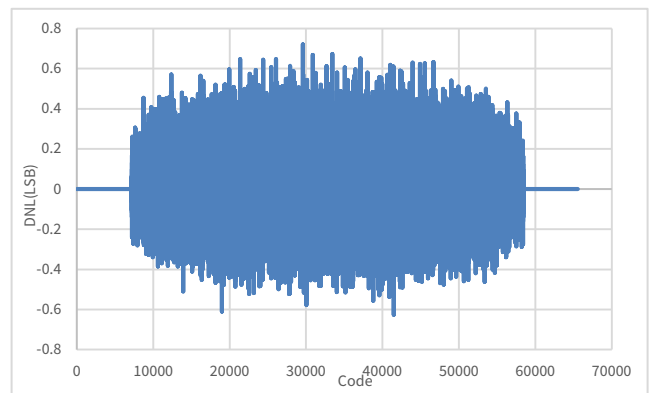


Figure 6.31 Typical Differential Nonlinearity

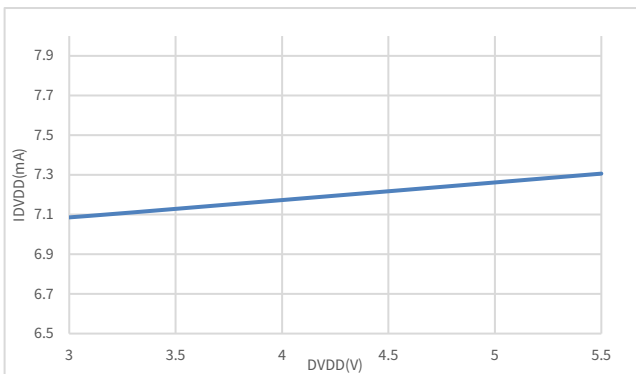


Figure 6.28 Digital Side Supply Current vs Supply Voltage

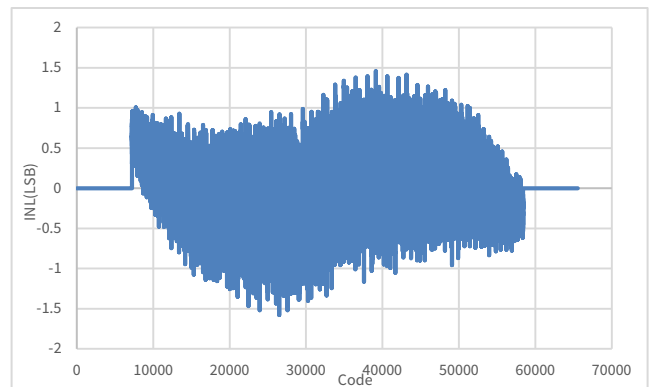


Figure 6.32 Typical Integral Nonlinearity

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value	Unit	Comments
Minimum External Clearance	CLR	8	mm	IEC 60664-1:2007
Minimum External Creepage	CPG	8	mm	IEC 60664-1:2007
Distance Through Insulation	DTI	28	μm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

Description	Test Condition	Value
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	I to IV
	For Rated Mains Voltage ≤ 300Vrms	I to IV
	For Rated Mains Voltage ≤ 600Vrms	I to IV
	For Rated Mains Voltage ≤ 1000Vrms	I to III
Climatic Classification		40/125/21
Pollution Degree per DIN VDE 0110		2

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value	Unit
DIN EN IEC 60747-17 (VDE 0884-17)				
Maximum repetitive isolation voltage		V_{IORM}	2121	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	1500	V_{RMS}
	DC Voltage		2121	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, $t_{ini}=60s$, $V_{pd(m)}=1.2*V_{IORM}$, $t_m=10s$.	q_{pd}	<5	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, $t_{ini}=60s$, $V_{pd(m)}=1.6*V_{IORM}$, $t_m=10s$			pC
	Method b, $V_{ini}=1.2*V_{IOTM}$, $t_{ini}=1s$ $V_{pd(m)}=1.875*V_{IORM}$, $t_m=1s$ (method b1) or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$ (method b2)			pC
Maximum transient isolation voltage	$t = 60sec$	V_{IOTM}	8000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50μs waveform per IEC62368-1	V_{IMP}	6250	V_{PEAK}

Description	Test Condition	Symbol	Value	Unit
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50µs waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$	V_{IOSM}	10000	V_{PEAK}
Isolation resistance	$V_{IO} = 500V, T_{amb} = 25^{\circ}C$	R_{IO}	$>10^{12}$	Ω
	$V_{IO} = 500V, 100^{\circ}C \leq T_{amb} \leq 125^{\circ}C$	R_{IO}	$>10^{11}$	Ω
	$V_{IO} = 500V, T_{amb} = T_s$	R_{IO}	$>10^9$	Ω
Isolation capacitance	$f = 1MHz$	C_{IO}	0.8	pF
Safety total power dissipation	$V_I = 5.5V, T_J = 150^{\circ}C, T_A = 25^{\circ}C$	P_s	1524	mW
Safety input, output, or supply current	$\theta_{JA} = 82^{\circ}C/W$ for SOW8, $V_I = 5.5V, T_J = 150^{\circ}C, T_A = 25^{\circ}C$	I_s	277	mA
Maximum safety temperature		T_s	150	$^{\circ}C$
UL1577				
Insulation voltage per UL	$V_{TEST} = V_{ISO}, t = 60$ s (qualification), $V_{TEST} = 1.2 \times V_{ISO}, t = 1$ s	V_{ISO}	5000	V_{RMS}

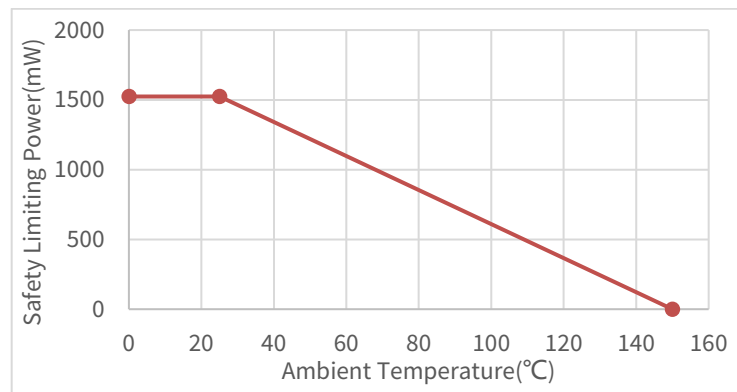


Figure 7.1 NSI1305/6L Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

7.3. Regulatory Information

The NSI1305/6L are approved or pending approval by the organizations listed in table.

UL		VDE	CQC
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1
Single Protection, 5000V _{rms} Isolation voltage	Single Protection, 5000V _{rms} Isolation voltage	Reinforce Insulation $V_{IORM} = 2121 V_{PEAK}$ $V_{IOTM} = 8000 V_{PEAK}$ $V_{IOSM} = 10000 V_{PEAK}$	Reinforced insulation
E500602	E500602	40052820	CQC20001264939

8. Function Description

8.1. Overview

The NSI1305/6L is a high performance isolated modulator with fully-differential input and LVDS digital interface. The fully-differential input is ideally suited to shunt current monitoring in high voltage applications where isolation is required. The analog input is continuously sampled by a second-order Σ - Δ modulator in the device, which is driven by a pre-stage fully-differential amplifier in the device. With the internal voltage reference and clock signal transferred across the isolation barrier from the external clock, the modulator converts the analog input signal to a digital bitstream. The drivers (called TX in the Functional Block Diagram) transfer the output of the modulator across the isolation barrier, as shown in the Functional Block Diagram. Both the input clock and the output data are LVDS interface conformed to TIA/EIA-644-A LVDS Standard.

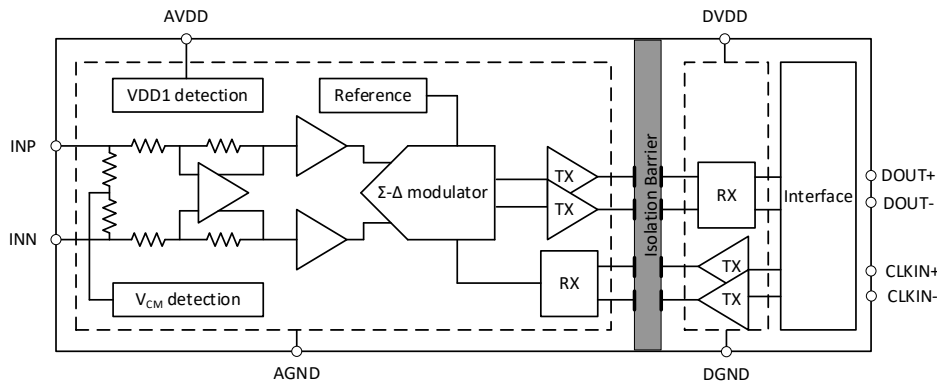


Figure 8.1 Function Block Diagram

8.2. Analog Input

There are two restrictions on the analog input signals (VINP and VINN).

- If the input voltage exceeds the range AGND – 6 V to AVDD + 0.5 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on.
- The linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

8.3. Digital Input

The digital input refers to clock signal which provides the clock for modulator conversion and output data frame clock. The clock signal should be supplied by an external source in the form of LVDS signal with a frequency range from 5MHz to 21MHz.

8.4. Digital Output

The digital output provides a stream of ones and zeros that can accurately represent the analog input voltage. Within the linear input range, the density of ones in the bitstream is proportional to the input voltage.

Ideally for a 0V input signal, the modulator outputs a bitstream with 50% high time. For a 250mV input signal (for the NSI1305/6L25), the modulator outputs a bitstream with 89.06% high time. For a -250mV input signal (for the NSI1305/6L25), the modulator outputs a bitstream with 10.94% high time. Figure 8.2 shows the data output vs isolated modulator input voltage.

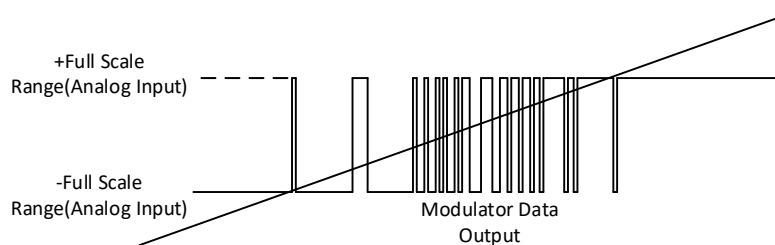


Figure 8.2 data output vs input voltage

Within full-scale input range, Equation 8.1 calculates the ones and zeros density of uncoded data for input voltage:

$$\text{Density} = (V_{IN} + V_{CLIPPING}) / (2 * V_{CLIPPING}) \tag{Equation 8.1}$$

If an overrange input signal is applied to the NSI1305/6L ($V_{IN} \geq V_{clipping}$), the output generates a single 0 or 1 every 128 clock cycles, as shown in Figure 8.3 and Figure 8.4.

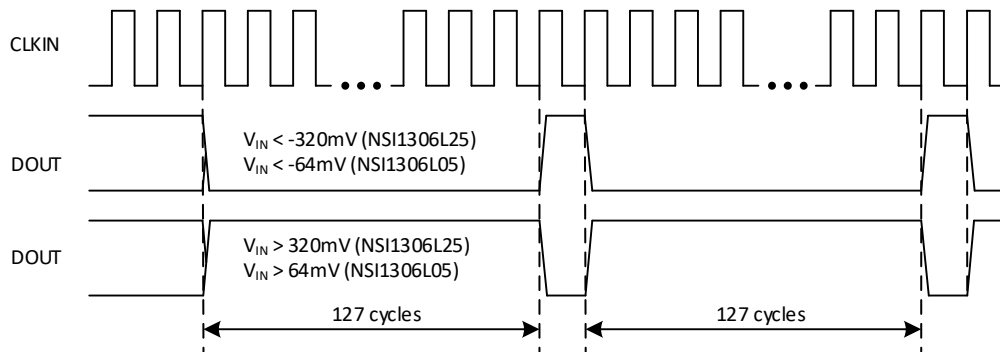


Figure 8.3 Overrange Bitstream Output of NSI1306L

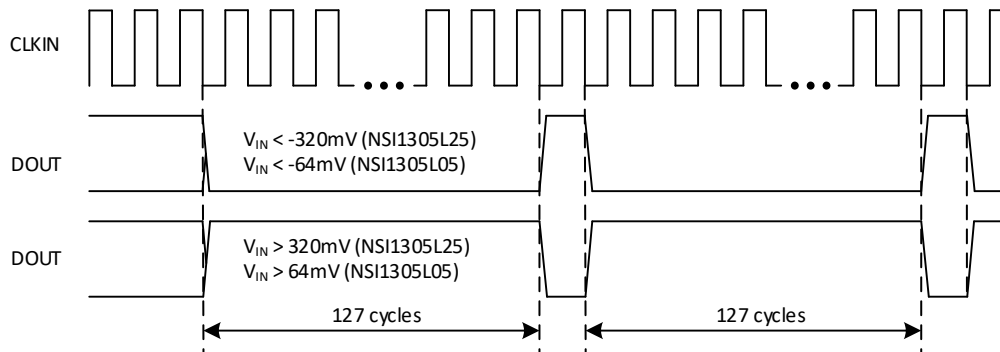


Figure 8.4 Overrange Bitstream Output of NSI1305L

8.5. Fail-safe Output

The NSI1305/6L integrates some diagnostic measures and offers a fail-safe output to simplify system-level design. The fail-safe function will be activated in following conditions:

- When the undervoltage of AVDD is detected ($AVDD < AVDD_{UV}$), DOUT pin output a bitstream of all logic zeros, as shown in Figure 8.5 and Figure 8.6.
- When the overvoltage of common-mode input voltage is detected ($V_{CM} > V_{CMov}$), DOUT pin output a bitstream of all logic ones, as shown in Figure 8.5 and Figure 8.6.

NOTE: If both of the above faults occur at the same time, DOUT pin output a bitstream of all logic zeros. (AVDD missing has a higher priority).

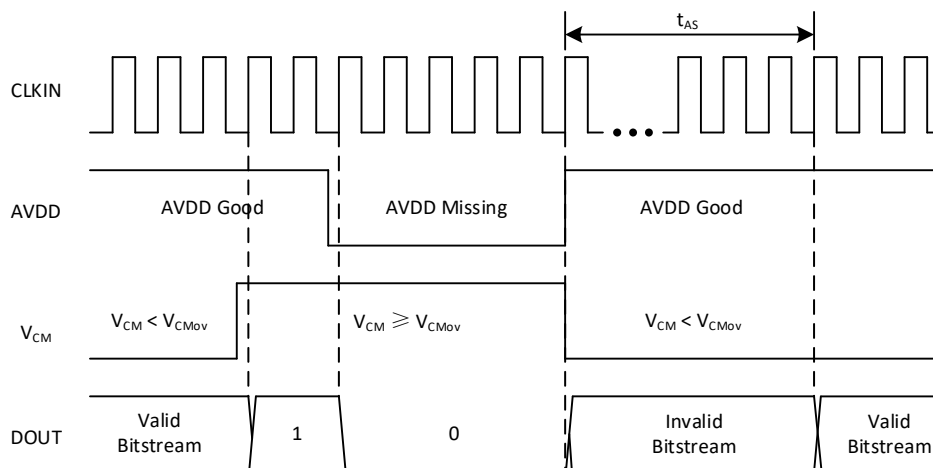


Figure 8.5 Fail-safe Bitstream Output of NSI1306L

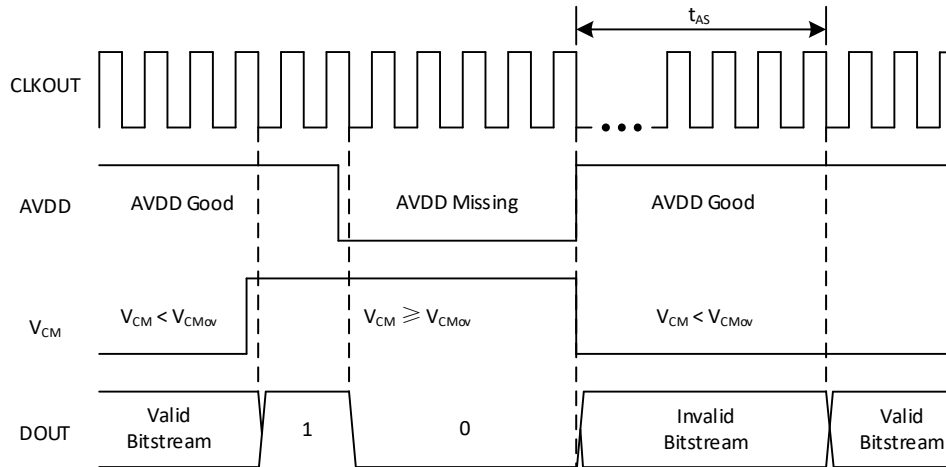


Figure 8.6 Fail-safe Bitstream Output of NSI1305L

9. Application Note

9.1. Typical Application Circuit

The NSI1305/6L is ideally suited to shunt resistor-based current sensing in high voltage applications such as frequency inverters. The typical application circuit is shown in Figure 9.1.

The voltage across the shunt resistor R_{sense} is applied to the differential input of NSI1305/6L through a RC filter. The internal second-order sigma-delta modulator converts the analog input to a single-bit output stream. The external digital system provides a clock source for the modulator and a digital filter for decimation and quantization noise filtering. Besides, a 100Ω termination resistor must be located near the input of the receiver.

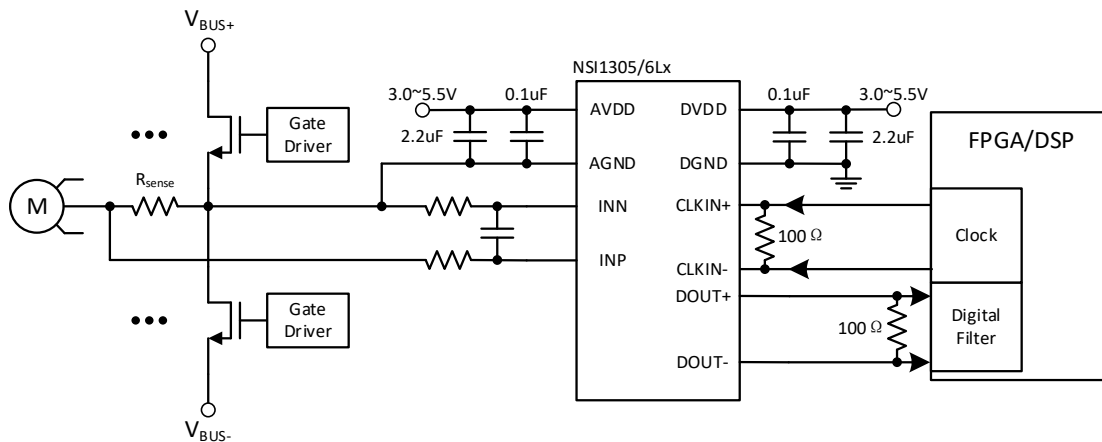


Figure 9.1 Typical application circuit in phase current sensing

9.2. Shunt Resistor Selection

Choosing a particular shunt resistor is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller sense resistor decreases power dissipation, while larger sense resistor can improve measure accuracy by utilizing the full input range of isolated amplifier.

There are two other factors should be considered when selecting the shunt resistor:

- The voltage-drop caused by the rated current range must not exceed the recommended linear input voltage range: $V_{SHUNT} \leq FSR$.

- The voltage-drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $V_{SHUNT} \leq V_{Clipping}$.

9.3. Digital Filter

The Σ - Δ modulator has characteristics of noise shaping. Most of the quantization noise is pushed from a low frequency to a higher frequency.

In order to reduce higher-frequency quantization noise, the modulator output is fed to the digital low-pass filter. Subsequently, the signal of interest passes through to the output of the digital filter, while much of the higher-frequency quantization noise is filtered out.

The digital filter serves another function – decimation. It creates a digital output code from the bitstream that the modulator outputs. The ratio of the modulator rate (f_{MOD}) of the delta-sigma modulator to its output data rate (f_{DR}) is the oversampling ratio (OSR). The relationship between f_{DR} and f_{MOD} is:

$$f_{DR} = f_{MOD} / OSR \tag{Equation 9.1}$$

A sinc3 filter is recommended since it's simple and requires less hardware resources. Equation 8.2 describes the transfer function of a sinc filter.

$$H(Z) = \left(\frac{1 - (1-Z^{-DR})}{DR (1-Z^{-1})} \right)^N \tag{Equation 9.2}$$

where:

DR is the decimation rate;

N is the sinc filter order.

The filter can be implemented in an FPGA or DSP. The sinc filter creates a digital output code by taking a multi-order moving average of the modulator output over a certain number of modulator clock periods.

The higher the decimation rate, the higher the conversion accuracy, and the lower the output data rate. So, there is a trade-off between accuracy and data rate. All the characterization in this datasheet is tested with a sinc3 filter with an oversampling ratio (OSR) of 256.

The output data size is expressed in Equation 8.3. The 16 most significant bits are used to return a 16-bit result.

$$Data\ Size = N \times \log_2 DR \tag{Equation 9.3}$$

The filter characteristics for a third-order sinc filter are summarized in Table 8.1.

Table 8.1 Sinc3 Filter Characteristics for 20 MHz CLKIN

Decimation Rate (DR)	Data Output Rate (kHz)	Data Size (bits)	Filter Response (kHz)
32	625	15	163.7
64	312.5	18	81.8
128	156.2	21	40.9
256	78.1	24	20.4
512	39.1	27	10.2

9.4. PCB Layout

There are some key guidelines or considerations for optimizing performance in PCB layout:

- NSI1305/6L requires a 0.1 μ F bypass capacitor between AVDD and AGND, DVDD and DGND. The capacitor should be placed as close as possible to the VDD pin. If better filtering is required, an additional 1~10 μ F capacitor may be used.
- Kelvin rules is recommended for the connection between shunt resistor to NSI1305/6L. Because of the Kelvin connection, any voltage drops across the trace and leads should have no impact on the measured voltage.
- Place the shunt resistor close to the INP and INN inputs and keep the layout of both connections symmetrical and run very close to each other to the input of the NSI1305/6L. This minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal.

- Place the 100Ω termination resistor as close as possible to the CLKIN+, CLKIN- inputs of the device to achieve highest signal integrity. If LVDS receiver is not integrated, an additional termination resistor is required as close as possible to the LVDS data inputs of the MCU or filter device.

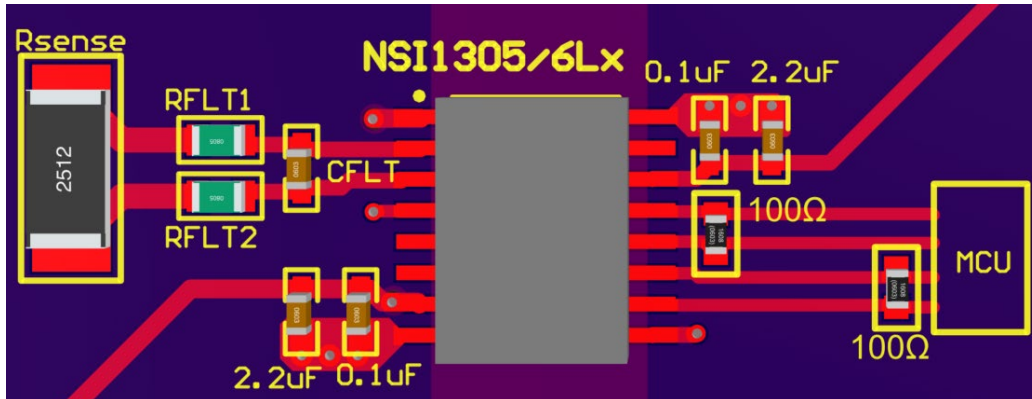


Figure 9.2 PCB layout example of NSI1305/6L

10. Package Information

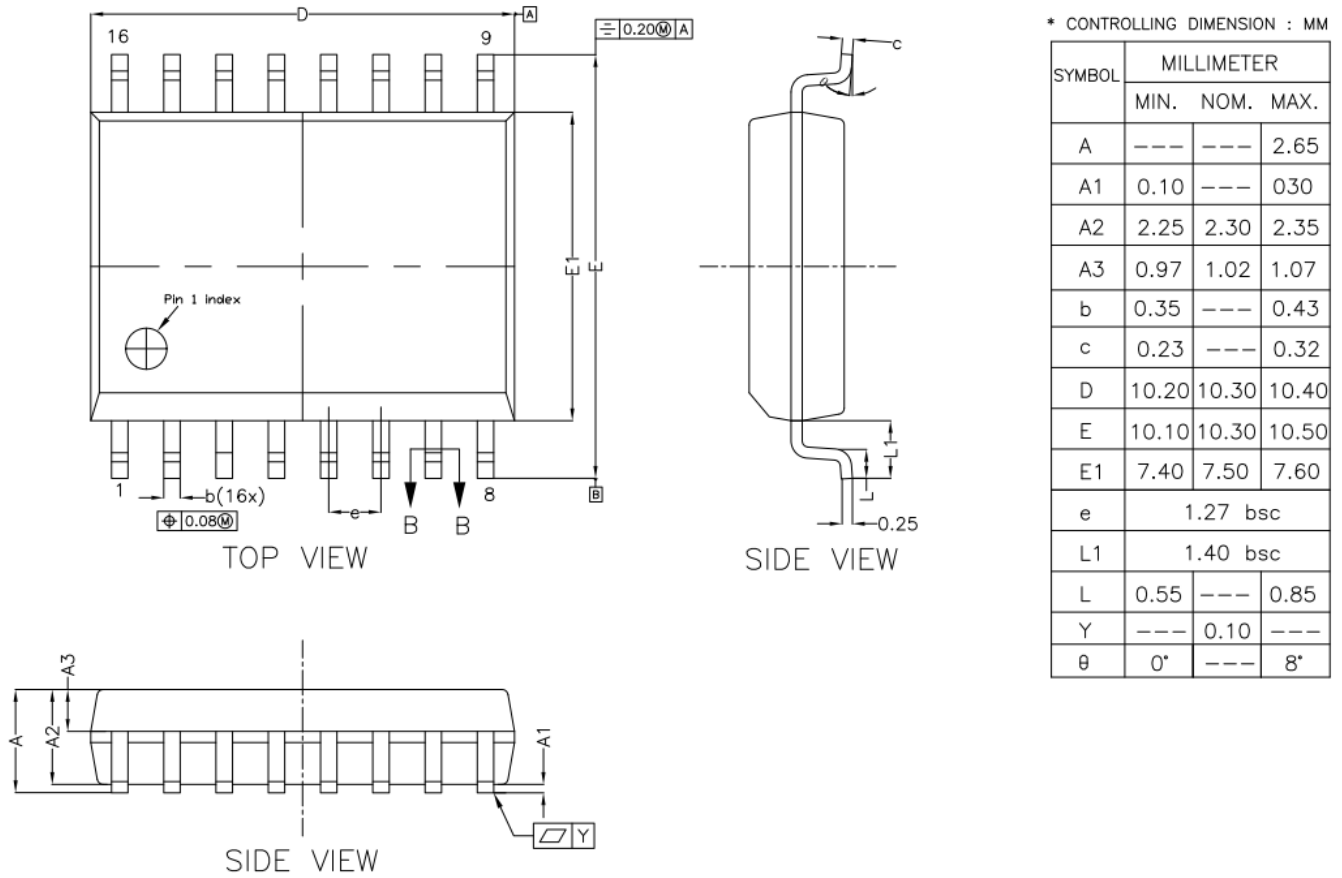


Figure 10.1 SOW16 package shape and dimension in millimeters

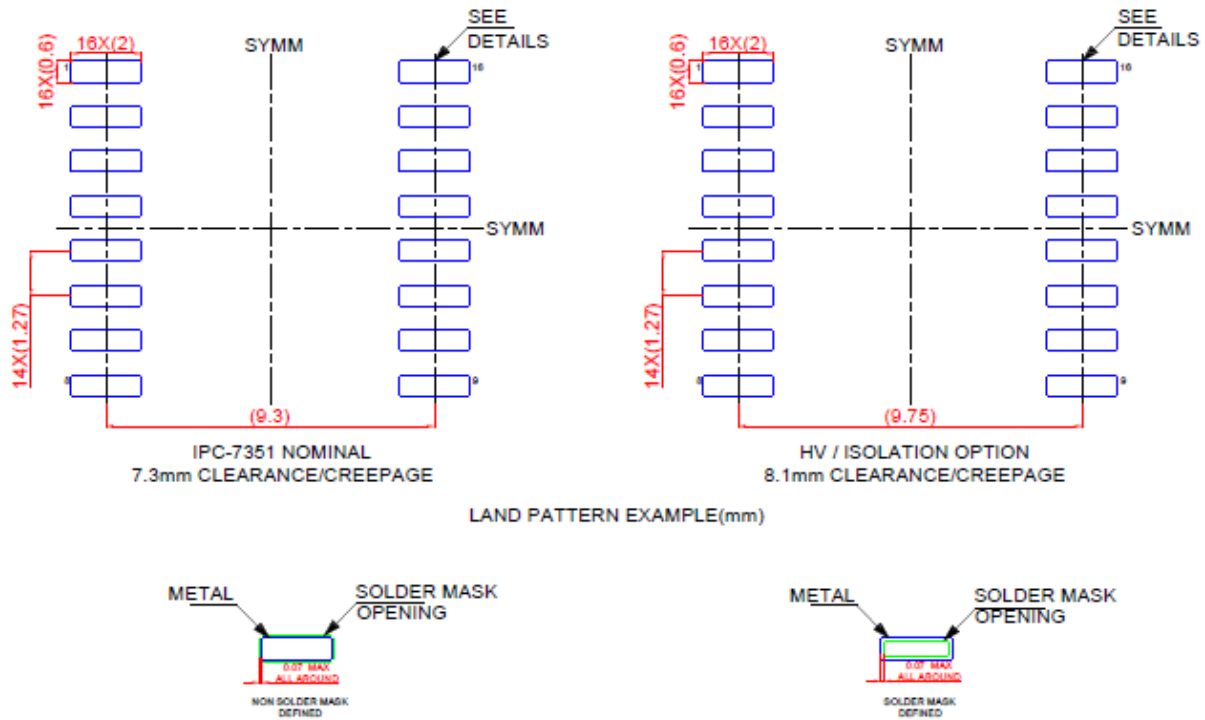


Figure 10.2 SOW16 Package Board Layout Example

11. Ordering Information

Part No.	Isolation Rating(kV)	Linear Input Range(mV)	Moisture Sensitivity Level	Temperature	Automotive	Package Type	Package Drawing	SPQ
NSI1306L05 -DSWR	5	-50 ~ 50	Level-2	-40 to 125°C	NO	SOP16 (300mil)	SOW16	1000
NSI1306L25 -DSWR	5	-250 ~ 250	Level-2	-40 to 125°C	NO	SOP16 (300mil)	SOW16	1000
NSI1305L05 -DSWR	5	-50 ~ 50	Level-2	-40 to 125°C	NO	SOP16 (300mil)	SOW16	1000
NSI1305L25 -DSWR	5	-250 ~ 250	Level-2	-40 to 125°C	NO	SOP16 (300mil)	SOW16	1000

12. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NSI1305/6L	Click here	Click here	Click here	Click here

13. Tape and Reel Information

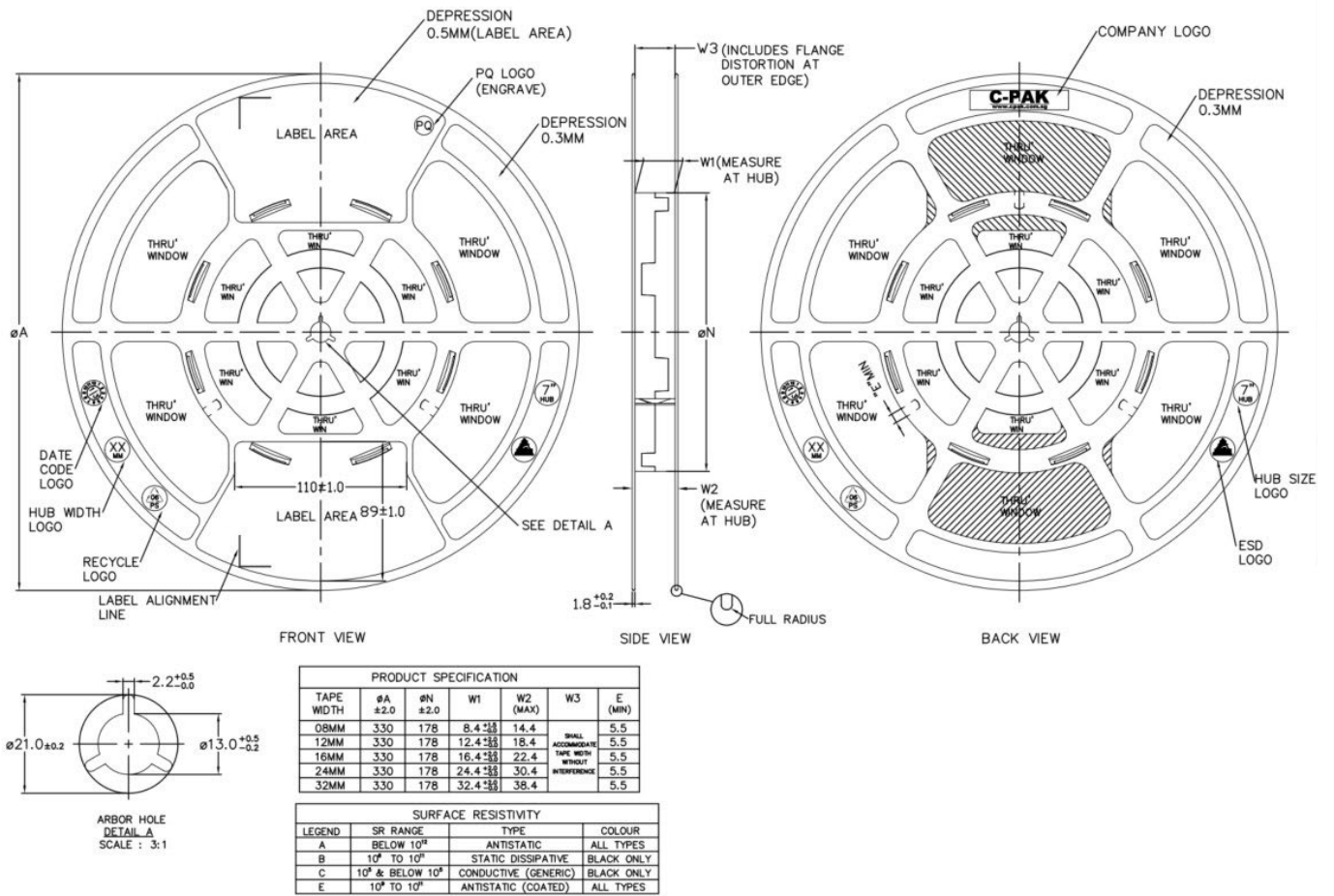


Figure 13.1 Tape Information

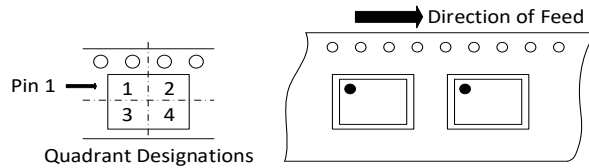
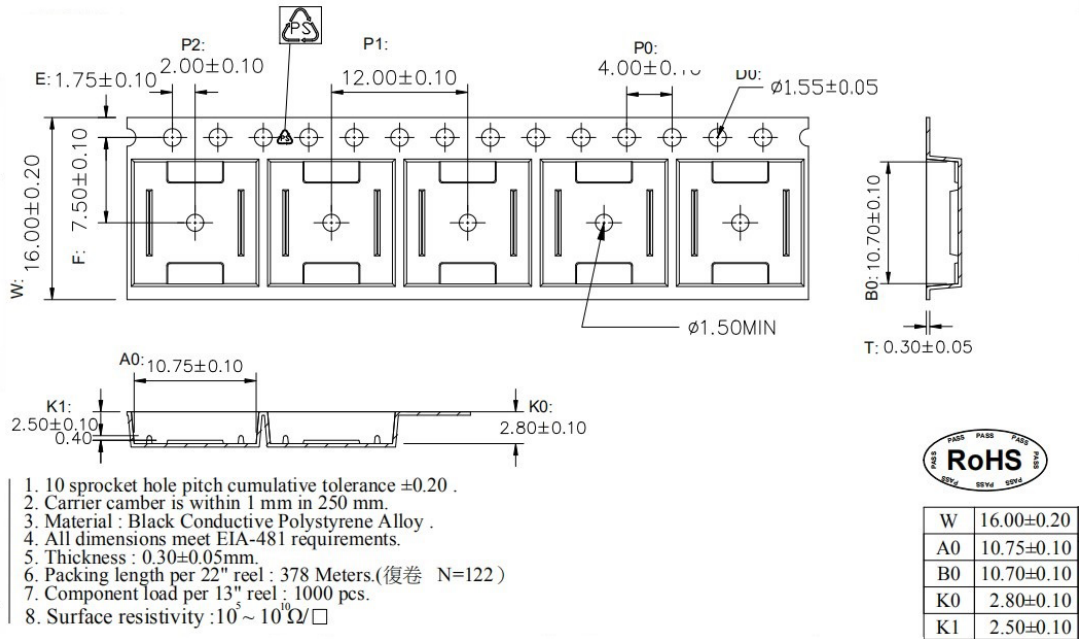


Figure 13.2 Reel Information of SOP16(300mil)

14. Revision History

Revision	Description	Date
1.0	Initial Release	2024/2/8

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