

Product Overview

The NSI1303 is a high performance Σ - Δ modulator with output separated from input based on the NOVOSENSE capacitive isolation technology. The device has a linear differential input signal range of $\pm 50\text{mV}$ ($\pm 64\text{mV}$ full-scale) or $\pm 250\text{mV}$ ($\pm 320\text{mV}$ full-scale). The differential input is ideally suited to shunt resistor-based current sensing in high voltage applications where isolation is required.

The analog input is amplified and continuously sampled by a second-order Σ - Δ modulator and converted to a high speed, single bit data stream. The output bit-stream of the NSI1303 is synchronized to the internally generated clock. NSI1303 can achieve 16 bits resolution and an 85dB (typ) signal to noise ratio (SNR) at 78.125kSPS by using an appropriate digital filter (such as sinc3 filter) to decimate the bitstream from 20MHz internal sampling clock.

The fail-safe functions including input common-mode overvoltage detection and missing AVDD detection simplify system-level design and diagnostics.

Key Features

- Up to 5700V_{RMS} Insulation Voltage
- 10MHz and 20MHz internal clock frequency options
- $\pm 50\text{mV}$ or $\pm 250\text{mV}$ Linear Input Voltage Range
- Excellent DC Performance:
 - Offset Error: $\pm 50\mu\text{V}$ or $\pm 100\mu\text{V}$ (Max)
 - Offset Drift: $\pm 1\mu\text{V}/^\circ\text{C}$ (Max)
 - Gain Error: $\pm 0.2\%$ (Max)
 - Gain Drift: $\pm 40\text{ppm}/^\circ\text{C}$ (Max)
- High CMTI: 150kV/ μs (Typ)
- System-Level Diagnostic Features:
 - AVDD monitoring
 - Input common-mode overvoltage detection
- Operation Temperature: $-40^\circ\text{C} \sim 125^\circ\text{C}$

- RoHS-Compliant Packages:
 - SOP8(300mil)
 - SOP16(300mil)

Safety Regulatory Approvals

- UL recognition per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Shunt current monitoring
- AC motor controls
- Uninterruptible Power Suppliers
- Automotive onboard chargers

Device Information

Part Number	Package	Body Size
NSI1303M/Dx-DSWVR	SOP8(300mil)	5.85mm × 7.50mm
NSI1303M/Dx-DSWR	SOP16(300mil)	10.30mm × 7.50mm

Functional Block Diagrams

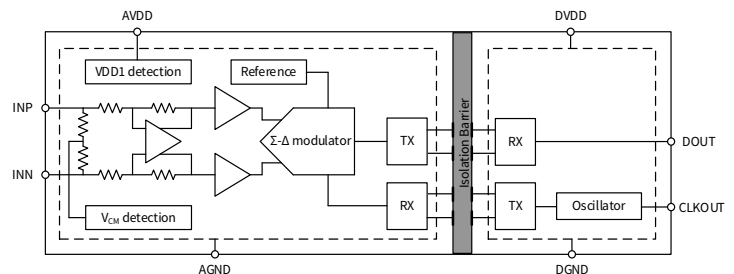


Figure 1. NSI1303M/Dx Block Diagram

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1. Pin Configuration and Functions

Table 1.1 NSI1303M/Dx Device Comparison Table

PART NUMBER	LINEAR INPUT VOLTAGE RANGE	DIFFERENTIAL INPUT RESISTANCE	INTERNAL CLOCK FREQUENCY	DIGITAL OUTPUT INTERFACE
NSI1303M01	±50mV	4.9kΩ	10MHz	Uncoded CMOS (clock rising edge effective)
NSI1303M21	±250mV	22kΩ		
NSI1303M02	±50mV	4.9kΩ	20MHz	
NSI1303M22	±250mV	22kΩ		
NSI1303D01	±50mV	4.9kΩ	10MHz	Uncoded CMOS (clock falling edge effective)
NSI1303D21	±250mV	22kΩ		
NSI1303D02	±50mV	4.9kΩ	20MHz	
NSI1303D22	±250mV	22kΩ		

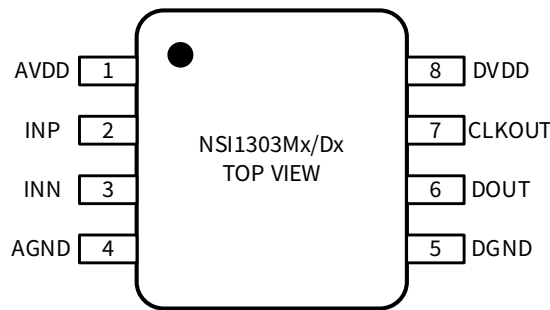


Figure 1.1 NSI1303Mx/Dx Package (SOP8(300mil))

Table 1.2 NSI1303 Pin Configuration and Description (SOP8(300mil))

NSI1303M/Dx PIN NO.	SYMBOL	FUNCTION
1	AVDD	Power supply for analog side (3.0V to 5.5V)
2	INP	Positive analog input (±250mV recommended for NSI1303x2x and ±50mV recommended for NSI1303x0x)
3	INN	Negative analog input
4	AGND	Analog ground reference
5	DGND	Digital ground reference
6	DOUT	Modulator data output
7	CLKOUT	Modulator clock output, 10 MHz (on NSI1303M/Dx1) or 20 MHz (on NSI1303M/Dx2) nominal
8	DVDD	Power supply for digital side (3.0V to 5.5V)

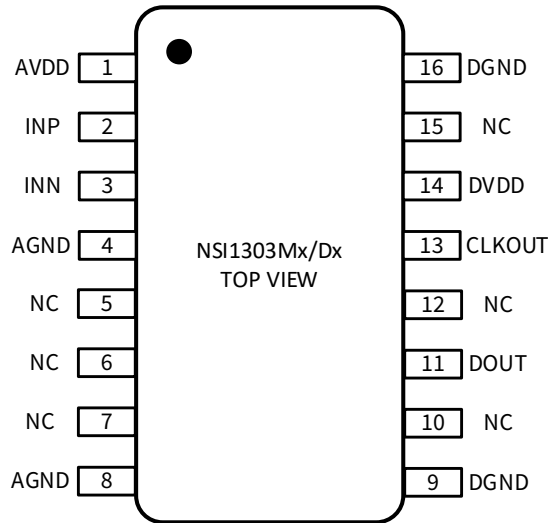


Figure 1.2 NSI1303Mx/Dx Package (SOP16(300mil))

Table 1.3 NSI1303M/Dx Pin Configuration and Description (SOP16(300mil))

NSI1303M/Dx PIN NO.	SYMBOL	FUNCTION
1	AVDD	Power supply for analog side (3.0V to 5.5V)
2	INP	Positive analog input ($\pm 250\text{mV}$ recommended for NSI1303x2x and $\pm 50\text{mV}$ recommended for NSI1303x0x)
3	INN	Negative analog input
4	AGND	Analog ground reference
5	NC	Not internally connected, this pin can be left floating or tied to AVDD, AGND
6	NC	Not internally connected, this pin can be left floating or tied to AVDD, AGND
7	NC	Internally connected to AVDD, this pin can be left floating or tied to AVDD
8	AGND	Analog ground reference
9	DGND	Digital ground reference
10	NC	Not internally connected, this pin can be left floating or tied to DVDD, DGND
11	DOUT	Modulator data output
12	NC	Not internally connected, this pin can be left floating or tied to DVDD, DGND
13	CLKOUT	Modulator clock output, 10 MHz (on NSI1303M/Dx1) or 20 MHz (on NSI1303M/Dx2) nominal
14	DVDD	Power supply for digital side (3.0V to 5.5V)
15	NC	Not internally connected, this pin can be left floating or tied to DVDD, DGND
16	DGND	Digital ground reference

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	AVDD, DVDD	-0.3		6.5	V
Analog Input Voltage	INP, INN	AGND-6		AVDD+0.5	V
Digital Output Voltage	DOUT,CLKOUT	DGND-0.5		DVDD+0.5	V
Output current per Output Pin	I _o	-10		10	mA
Operating Temperature	T _{OPR}	-40		125	°C
Junction Temperature	T _J	-40		150	°C
Storage Temperature	T _{STG}	-55		150	°C

3. ESD Ratings

Parameters	Test Condition	Value	Unit
Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4.0	kV
	Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1.0	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Analog Side Power Supply	AVDD	3.0	5.0	5.5	V
Digital Side Power Supply	DVDD	3.0	3.3	5.5	V
NSI1303x01/2	Differential input voltage before clipping output	V _{Clipping}	±64		mV
	Linear differential input full scale voltage	V _{FSR}	-50	50	mV
	Operating common-mode input voltage	V _{CM}	-0.032	0.8	V
NSI1303x21/2	Differential input voltage before clipping output	V _{Clipping}	±320		mV
	Linear differential input full scale voltage	V _{FSR}	-250	250	mV
	Operating common-mode input voltage	V _{CM}	-0.16	0.8	V
Operating Ambient Temperature	T _A	-40		125	°C

5. Thermal Information

Parameters	Symbol	SOP8(300mil)	SOP16(300mil)	Unit
Junction-to-ambient thermal resistance	$R_{\theta JA}$	86	82	°C/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	28	42	°C/W
Junction-to-board thermal resistance	$R_{\theta JB}$	42	46	°C/W
Junction-to-top characterization parameter	Ψ_{JT}	4	12	°C/W
Junction-to-board characterization parameter	Ψ_{JB}	42	46	°C/W

6. Specifications

6.1. Electrical Characteristics: NSI1303M/D0x

(AVDD = 3.0V ~ 5.5V, DVDD = 3.0V ~ 5.5V, INP = -50mV to +50mV, and INN = AGND = 0V, T_A = -40°C to 125°C and sinc³ filter with OSR=256. Unless otherwise noted, Typical values are at AVDD = 5V, DVDD = 3.3V, T_A = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Analog Side Supply Voltage	AVDD	3.0	5.0	5.5	V	
Digital Side Supply Voltage	DVDD	3.0	3.3	5.5	V	
Analog Side Supply Current	IAVDD		11.3	14.8	mA	for M/D01
			11.5	15	mA	for M/D02
Digital Side Supply Current	IDVDD		2.6		mA	for M/D01, C _{LOAD} =15pF
			3.7		mA	for M/D02, C _{LOAD} =15pF
AVDD undervoltage detection threshold voltage	AVDD _{UV}	1.8	2.3	2.7	V	AVDD falling
Analog Input						
Common-mode overvoltage detection level	V _{CMov}	0.9			V	Detection level has a typical hysteresis of 96 mV
Common-mode rejection ratio	CMRR _{dc}		-95		dB	INP = INN, f _{IN} = 0 Hz, V _{CM min} ≤ VIN ≤ V _{CM max}
	CMRR _{ac}		-99		dB	INP = INN, f _{IN} = 10 kHz, V _{CM min} ≤ VIN ≤ V _{CM max}
Input capacitance	C _{IN}		2		pF	INN=AGND
Single-ended input resistance	R _{IN}		4.75		kΩ	INN = AGND
Differential input resistance	R _{IND}		4.9		kΩ	
Input bias current	I _{IB}	-26	-23	-20	μA	T _A = 25°C, INP = INN = AGND, I _{IB} = (I _{IBP} + I _{IBN}) / 2
Input bias current drift	TCI _{IB}		±2		nA/°C	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Common-mode transient immunity	CMTI	100	150		kV/μs	Common-mode transient immunity
Input bandwidth	BW		800		kHz	
DC Accuracy						
Differential nonlinearity	DNL	-0.99		0.99	LSB	
Integral nonlinearity	INL	-4	±1	4	LSB	
Offset error	V _{OS}	-50	±2.5	50	μV	T _A = 25°C, INP = INN = AGND
Offset error thermal drift	TCV _{OS}	-0.5	±0.15	0.5	μV/°C	
Gain error	E _G	-0.2%	±0.005%	0.2%		T _A = 25°C
Gain error thermal drift	TCE _G	-30	±10	30	ppm/°C	
Power supply rejection ratio	PSRR		-100		dB	PSRR vs AVDD, at DC
			-90		dB	PSRR vs AVDD, 100mV and 10kHz ripple
AC Accuracy						
Signal to noise ratio	SNR	81	84		dB	f _{IN} = 1kHz for M/D01
		79	83		dB	f _{IN} = 1kHz for M/D02
Signal to noise and distortion	SINAD	77	82.5		dB	f _{IN} = 1kHz
Total harmonic distortion	THD		-97		dB	f _{IN} = 1kHz
Spurious-free dynamic range	SFDR		96		dB	f _{IN} = 1kHz for M/D01
			97		dB	f _{IN} = 1kHz for M/D02
Digital Input / Output						
Output load capacitance	C _{LOAD}		30		pF	
High-level output voltage	V _{OH}	DVDD-0.1			V	I _{OH} = -20μA
		DVDD-0.4			V	I _{OH} = -4mA
		DVDD-0.8				I _{OH} = -8mA
Low-level output voltage	V _{OL}			0.1	V	I _{OL} = 20μA
				0.4	V	I _{OL} = 4mA
				0.8	V	I _{OL} = 8mA

6.2. Electrical Characteristics: NSI1303M/D2x

(AVDD = 3.0V ~ 5.5V, DVDD = 3.0V ~ 5.5V, INP = -250mV to +250mV, and INN = AGND = 0V, T_A = -40°C to 125°C and sinc³ filter with OSR=256. Unless otherwise noted, Typical values are at AVDD = 5V, DVDD = 3.3V, T_A = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Analog Side Supply Voltage	AVDD	3.0	5.0	5.5	V	
Digital Side Supply Voltage	DVDD	3.0	3.3	5.5	V	
Analog Side Supply Current	IAVDD		11.2	14.3	mA	for M/D21
			11.7	15.1	mA	for M/D22
Digital Side Supply Current	IDVDD		2.6	4.5	mA	for M/D21, CLOAD=15pF
			3.7		mA	for M/D22, CLOAD=15pF
AVDD undervoltage detection threshold voltage	AVDD _{UV}	1.8	2.3	2.7	V	AVDD falling
Analog Input						
Common-mode overvoltage detection level	V _{CMov}	0.9			V	Detection level has a typical hysteresis of 96 mV
Common-mode rejection ratio	CMRR _{dc}		-106		dB	INP = INN, f _{IN} = 0 Hz, V _{CM} min ≤ V _{IN} ≤ V _{CM} max
	CMRR _{ac}		-104		dB	INP = INN, f _{IN} = 10 kHz, V _{CM} min ≤ V _{IN} ≤ V _{CM} max
Input capacitance	C _{IN}		2		pF	INN=AGND
Single-ended input resistance	R _{IN}		19		kΩ	INN = AGND
Differential input resistance	R _{IND}		22		kΩ	
Input bias current	I _{IB}	-24	-18	-12	μA	T _A = 25°C, INP = INN = AGND, I _{IB} = (I _{IBP} + I _{IBN}) / 2
Input bias current drift	TC _{I_{IB}}		±1		nA/°C	
Common-mode transient immunity	CMTI	100	150		kV/μs	Common-mode transient immunity
Input bandwidth	BW		800		kHz	
DC Accuracy						
Differential nonlinearity	DNL	-0.99		0.99	LSB	
Integral nonlinearity	INL	-4	±1	4	LSB	
Offset error	V _{OS}	-100	±2.5	100	μV	T _A = 25°C, INP = INN = AGND
Offset error thermal drift	TCV _{OS}	-1	±0.15	1	μV/°C	
Gain error	E _G	-0.2%	±0.005%	0.2%		T _A = 25°C
Gain error thermal drift	TCE _G	-40	±20	40	ppm/°C	
Power supply rejection ratio	PSRR		-106		dB	PSRR vs AVDD, at DC

Parameters	Symbol	Min	Typ	Max	Unit	Comments
			-95		dB	PSRR vs AVDD, 100mV and 10kHz ripple
AC Accuracy						
Signal to noise ratio	SNR		85		dB	f _{IN} = 1kHz for M/D21
			84.5		dB	f _{IN} = 1kHz for M/D22
Signal to noise and distortion	SINAD		82.5		dB	f _{IN} = 1kHz
Total harmonic distortion	THD		-90	-82	dB	f _{IN} = 1kHz for M/D21
			-95	-82	dB	f _{IN} = 1kHz for M/D22
Spurious-free dynamic range	SFDR		90		dB	f _{IN} = 1kHz for M/D21
			92		dB	f _{IN} = 1kHz for M/D22
Digital Input / Output						
Output load capacitance	C _{LOAD}		30		pF	
High-level output voltage	V _{OH}	DVDD-0.1			V	IOH = -20μA
		DVDD-0.4			V	IOH = -4mA
		DVDD-0.8				IOH = -8mA
Low-level output voltage	V _{OL}			0.1	V	IOL = 20μA
				0.4	V	IOL = 4mA
				0.8	V	IOL = 8mA

6.3. Timing Characteristics

Unless otherwise noted, Typical values are at AVDD = 5V, DVDD = 3.3V, T_A = 25°C. Over operating ambient temperature range (unless otherwise noted)

PARAMETERS	Symbol	MIN	TYP	MAX	Unit	Comments
clock frequency	f _{CLK}	9.6	10	10.4	MHz	For NSI1303xx1
		19.2	20	20.8	MHz	For NSI1303xx2
Duty Cycle	Duty	45%	50%	55%		For NSI1303M/Dx
DOUT rising time	t _R		1.8	3.5	ns	C _{LOAD} = 15pF
DOUT falling time	t _F		1.8	3.5	ns	C _{LOAD} = 15pF
DOUT hold time after rising edge of CLKOUT	t _H	7	10		ns	For NSI1303M/Dx, C _{LOAD} = 15pF
Rising edge of CLKOUT to DOUT valid delay	t _D		11	15	ns	For NSI1303M/Dx, C _{LOAD} = 15pF
Analog setting time	t _{AS}		0.5		ms	AVDD step to 3.0 V with DVDD ≥ 3.0 V, to DOUT valid, 0.1% settling

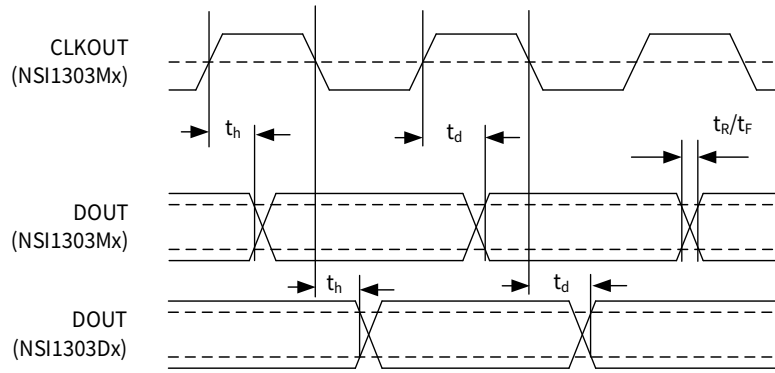


Figure 6.1 NSI1303x digital interface timing

6.4. Typical Performance Characteristics

Unless otherwise noted, test at AVDD = 5V, DVDD = 3.3V, Vin = -250mV to 250mV (NSI1303x2x) or -50mV to 50mV (NSI1303x0x), and sinc³ filter with OSR=256.

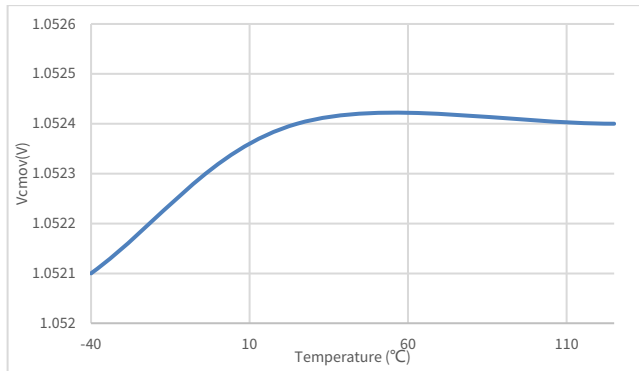


Figure 6.2 Common-Mode Overvoltage Detection Level vs Temperature

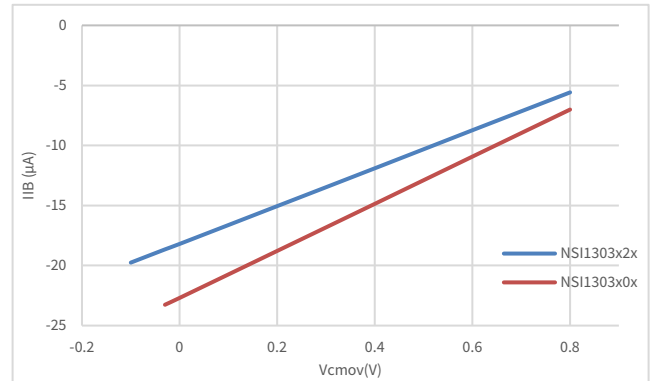


Figure 6.4 Input Bias Current vs Common-Mode voltage

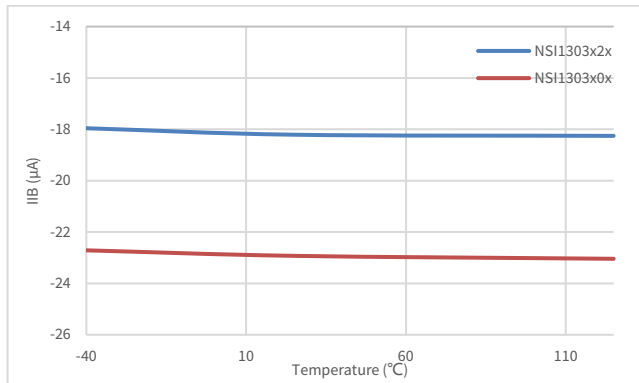


Figure 6.3 Input Bias Current vs Temperature

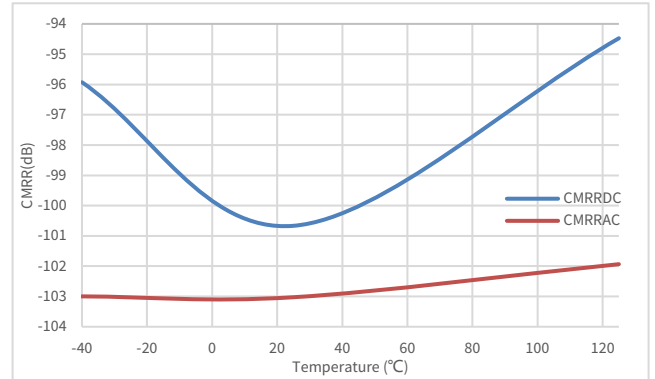


Figure 6.5 Common-Mode Rejection Ratio vs Temperature

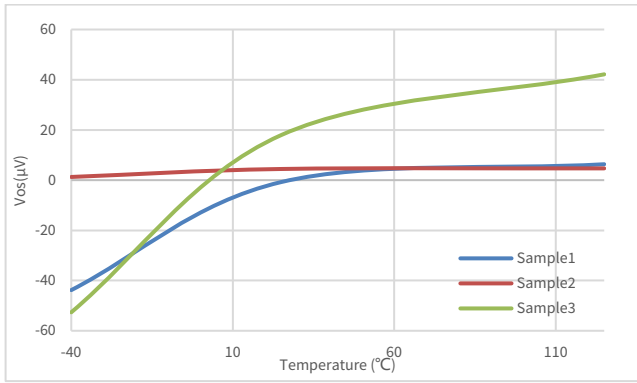


Figure 6.6 Input Offset Voltage vs Temperature

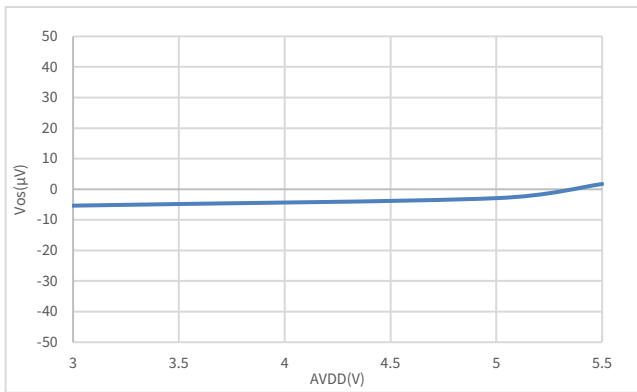


Figure 6.7 Input Offset Voltage vs Analog Side Supply Voltage

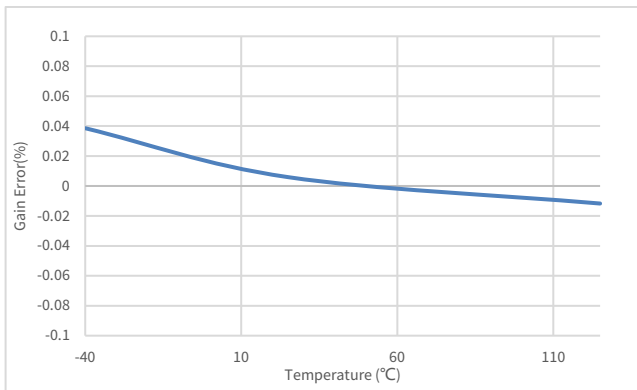


Figure 6.8 Gain Error vs Temperature

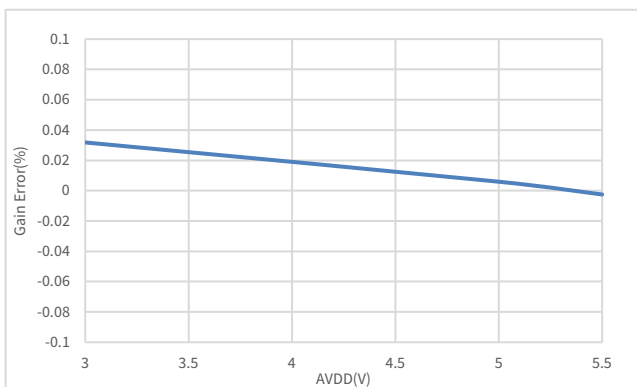


Figure 6.9 Gain Error vs Analog Side Supply Voltage

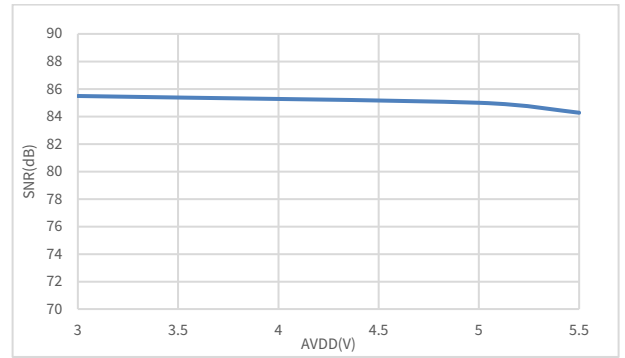


Figure 6.10 Signal-to-Noise Ratio vs Analog Side Supply Voltage

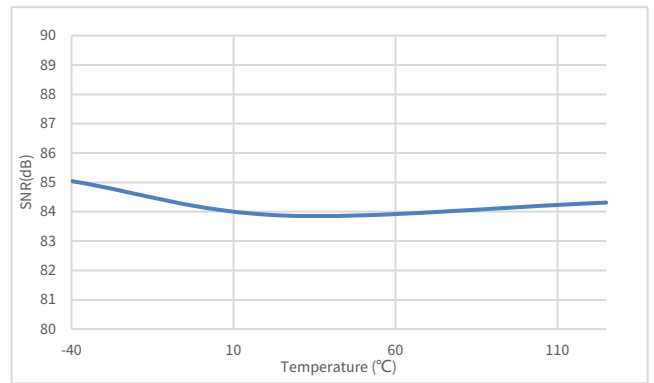


Figure 6.11 Signal-to-Noise Ratio vs Temperature

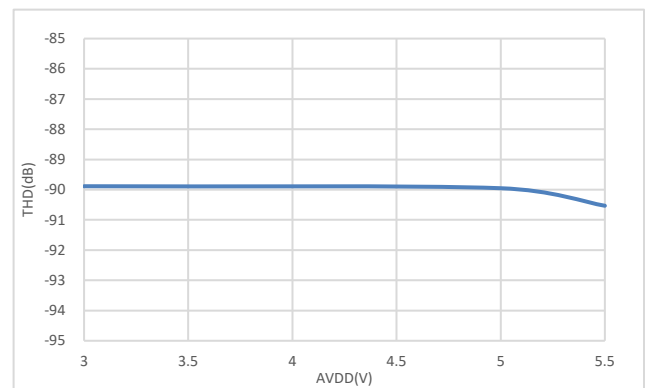


Figure 6.12 Total Harmonic Distortion vs Analog Side Supply Voltage

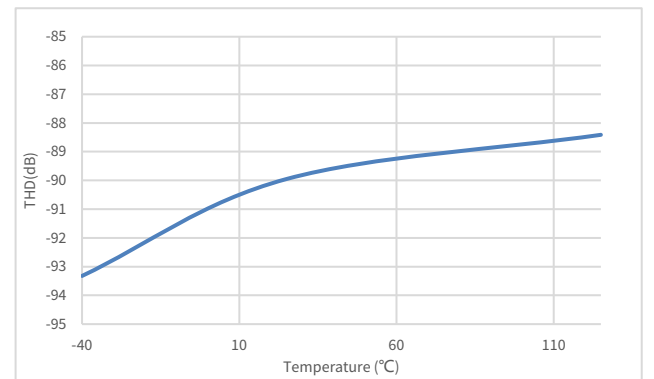


Figure 6.13 Total Harmonic Distortion vs Temperature

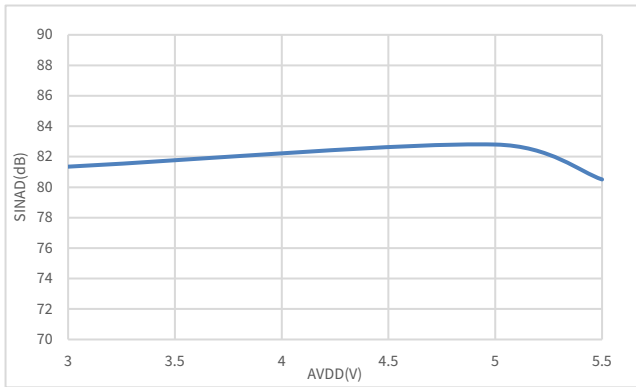


Figure 6.14 Signal-to-Noise + Distortion vs Analog Side Supply Voltage

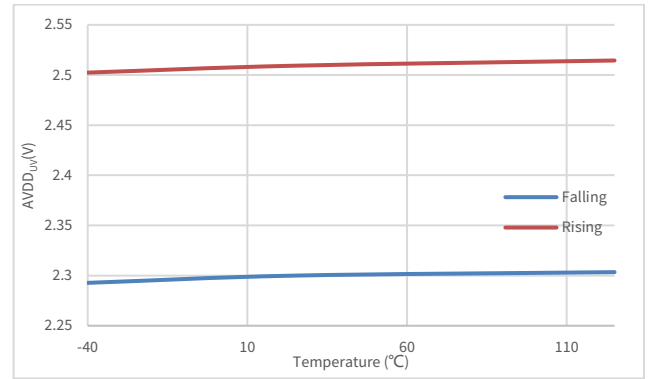


Figure 6.18 Analog Side Under-Voltage Detection Level vs Temperature

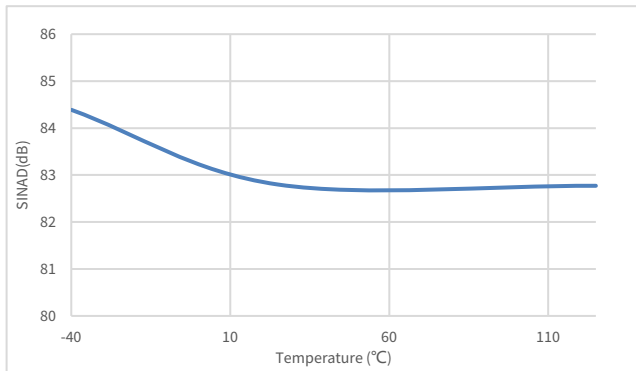


Figure 6.15 Signal-to-Noise + Distortion vs Temperature

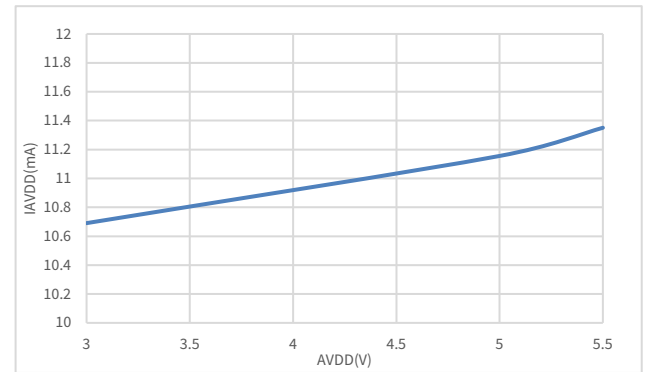


Figure 6.19 Analog Side Supply Current vs Supply Voltage

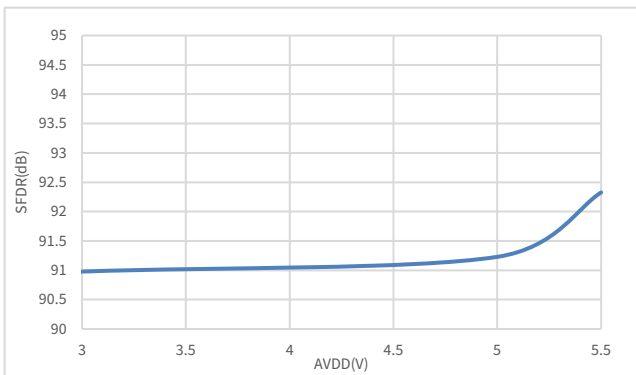


Figure 6.16 Spurious-Free Dynamic Range vs Analog Side Supply Voltage

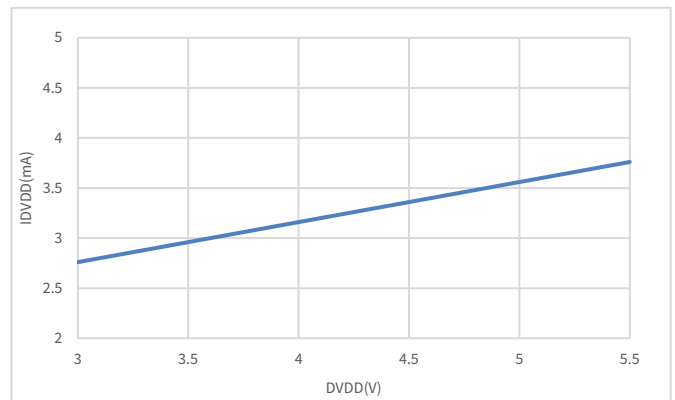


Figure 6.20 Digital Side Supply Current vs Supply Voltage

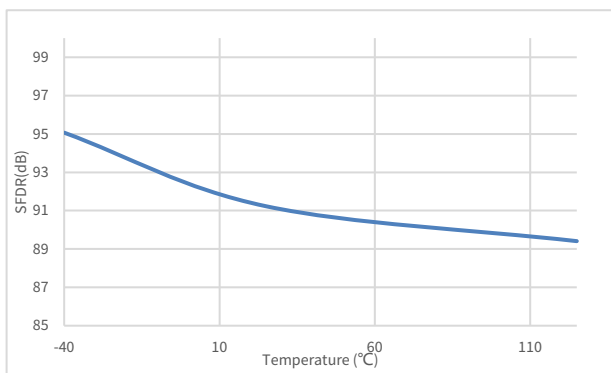


Figure 6.17 Spurious-Free Dynamic Range vs Temperature

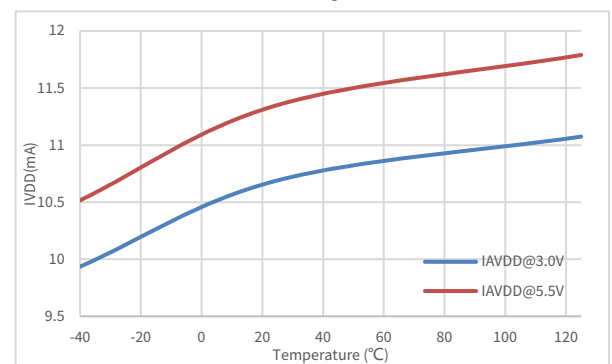


Figure 6.21 Supply Current vs Temperature

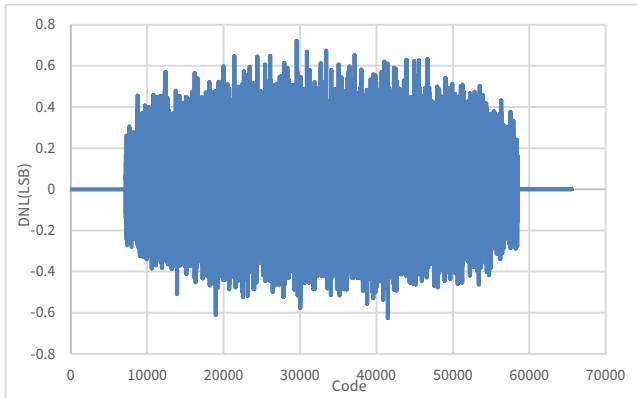


Figure 6.22 Typical Differential Nonlinearity

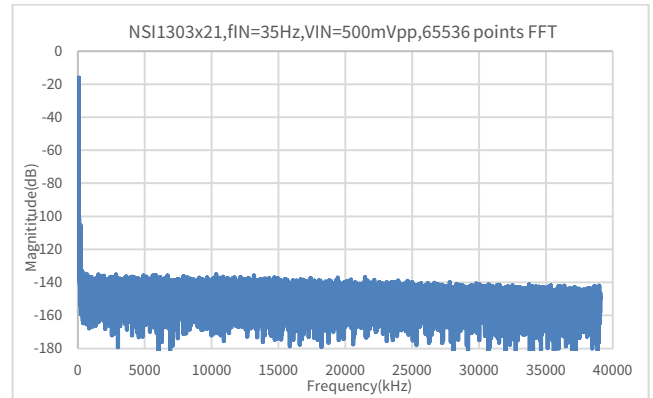


Figure 6.24 Frequency Spectrum

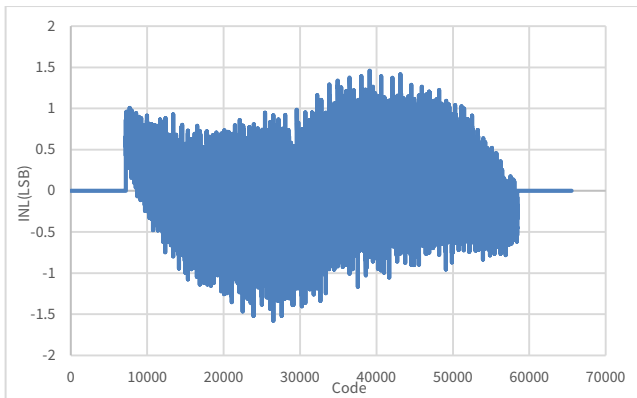


Figure 6.23 Typical Integral Nonlinearity

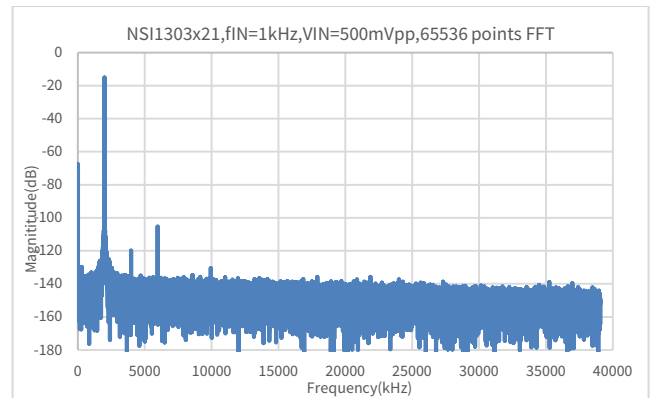


Figure 6.25 Frequency Spectrum

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value	Unit	Comments
Minimum External Air Gap (Clearance)	CLR	8	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	CPG	8	mm	Shortest terminal-to-terminal distance across the package surface
Minimum internal gap	DTI	28	µm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

Description	Test Condition	Value	
		SOP8	SOP16
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	I to IV	I to IV
	For Rated Mains Voltage ≤ 300Vrms	I to IV	I to IV
	For Rated Mains Voltage ≤ 600Vrms	I to IV	I to IV
	For Rated Mains Voltage ≤ 1000Vrms	I to III	I to III
Climatic Classification		40/125/21	
Pollution Degree per DIN VDE 0110		2	

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value		Unit
			SOP8	SOP16	
DIN EN IEC 60747-17 (VDE 0884-17)					
Maximum repetitive isolation voltage		V_{IORM}	2121	2121	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	1500	1500	V_{RMS}
	DC Voltage		2121	2121	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, $t_{ini} = 60\text{ s}$, $V_{pd(m)}=1.2*V_{IORM}$, $t_m=10\text{s}$.	q_{pd}	<5	<5	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, $t_{ini}=60\text{s}$, $V_{pd(m)}=1.6*V_{IORM}$, $t_m=10\text{s}$				pC

Description	Test Condition	Symbol	Value		Unit
			SOP8	SOP16	
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2 \cdot V_{IOTM}$, $t_{ini}=1s$ $V_{pd(m)}=1.875 \cdot V_{IORM}$, $t_m=1s$ (method b1) or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$ (method b2)				pC
Maximum transient isolation voltage	$t = 60sec$	V_{IOTM}	8000	8000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50-us waveform per IEC62368-1	V_{IMP}	6250	6250	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$	V_{IOSM}	10000	10000	V_{PEAK}
Isolation resistance	$V_{IO} = 500V$, $T_A = 25^\circ C$	R_{IO}	$>10^{12}$	$>10^{12}$	Ω
	$V_{IO} = 500V$, $100^\circ C \leq T_A \leq 125^\circ C$	R_{IO}	$>10^{11}$	$>10^{11}$	Ω
	$V_{IO} = 500V$, $T_A = T_s$	R_{IO}	$>10^9$	$>10^9$	Ω
Isolation capacitance	$f = 1MHz$	C_{IO}	0.8	0.8	pF
Safety total power dissipation	$V_I = 5.5V$, $T_J = 150^\circ C$, $T_A = 25^\circ C$	P_s	1430	1524	mW
Safety input, output, or supply current	$\theta_{JA} = 86^\circ C/W$ for SOP8, $V_I = 5.5V$, $T_J = 150^\circ C$, $T_A = 25^\circ C$	I_s	260	/	mA
	$\theta_{JA} = 82^\circ C/W$ for SOP16, $V_I = 5.5V$, $T_J = 150^\circ C$, $T_A = 25^\circ C$		/	277	mA
Maximum safety temperature		T_s	150	150	$^\circ C$
UL1577					
Insulation voltage per UL	$V_{TEST} = V_{ISO}$, $t = 60 s$ (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, $t = 1 s$ (100% production test)	V_{ISO}	5700	5700	V_{RMS}

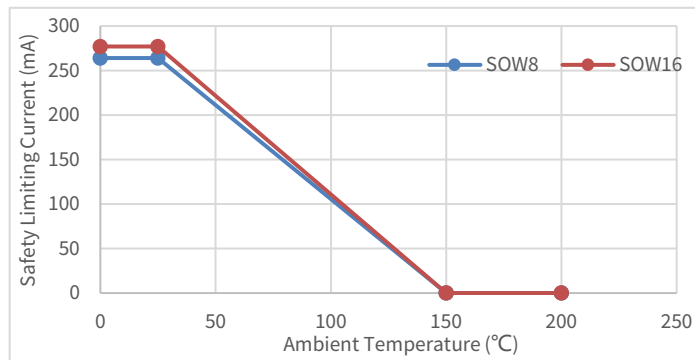


Figure 7.1 NSI1303 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

7.3. Regulatory Information

The NSI1303x-DSWVR are approved or pending approval by the organizations listed in table.

<i>UL</i>		<i>VDE</i>	<i>CQC</i>	<i>TUV</i>
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1
Single Protection, 5700V _{rms} Isolation voltage	Single Protection, 5700V _{rms} Isolation voltage	Reinforce Insulation V _{IORM} =2121V _{peak} V _{IOTM} =8000V _{peak} V _{IOSM} =10000V _{peak}	Reinforced insulation	5000V _{rms} for 1min
E500602	E500602	Certificate No.40052820	CQC20001264938	R50574061

The NSI1303x-DSWR are approved or pending approval by the organizations listed in table.

<i>UL</i>		<i>VDE</i>	<i>CQC</i>	<i>TUV</i>
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1
Single Protection, 5700V _{rms} Isolation voltage	Single Protection, 5700V _{rms} Isolation voltage	Reinforce Insulation V _{IORM} =2121V _{peak} V _{IOTM} =8000V _{peak} V _{IOSM} =10000V _{peak}	Reinforced insulation	5000V _{rms} for 1min
E500602	E500602	Certificate No.40052820	CQC20001264939	R50574061

8. Function Description

8.1. Overview

The NSI1303 is a high performance isolated modulator that accept fully-differential input with internal clock. The fully-differential input is ideally suited to shunt current monitoring in high voltage applications where isolation is required. The analog input is continuously sampled by a second-order Σ - Δ modulator in the device, which is driven by a pre-stage fully-differential amplifier in the device. With the internal voltage reference and clock generator, the modulator convert the analog input signal to a digital bitstream that is synchronous to the internally-generated clock at the CLKOUT pin. The drivers (called TX in the Functional Block Diagram) transfer the output of the modulator across the isolation barrier, as shown in the Functional Block Diagram. The extended clock frequency of 20 MHz on the NSI1303xx2 supports faster control loops and higher performance levels compared to the other solutions available on the market. NSI1303 meets the requirements of different sampling edge in the external digital system, clock rising edge effective for NSI1303Mx and clock falling edge effective for NSI1303Dx.

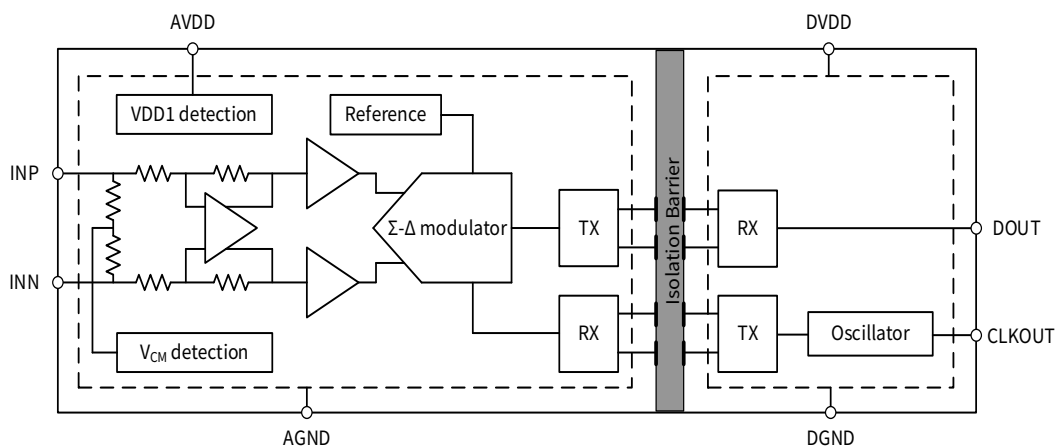


Figure 8.1 Function Block Diagram of NSI1303Mx/NSI1303Dx

8.2. Analog Input

There are two restrictions on the analog input signals (V_{INP} and V_{INN}).

- If the input voltage exceeds the range $AGND - 6\text{ V}$ to $AVDD + 0.5\text{ V}$, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on.
- The linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

8.3. Digital Output

The digital output provides a stream of ones and zeros that can accurately represent the analog input voltage. Within the linear input range, the density of ones in the bitstream is proportional to the input voltage.

Ideally for a 0V input signal, the modulator outputs a bitstream with 50% high time. For a 250mV input signal (for the NSI1303x2x), the modulator outputs a bitstream with 89.06% high time. For a -250mV input signal (for the NSI1303x2x), the modulator outputs a bitstream with 10.94% high time.

If the input signal is greater than or equal to 320mV (64 mV for the NSI1303x0x), the modulator clips with a stream of all ones. If the input signal is less than or equal to -320mV (-64 mV for the NSI1303x0x), the output of the modulator clips with a stream of all zeros. In this case, however, the NSI1303 generates a single 0 (if the input is at positive full-scale) or 1 every 128 clock cycles to indicate proper device function (see section 8.5 for more details).

Figure 8.2 shows the data output vs isolated modulator input voltage.

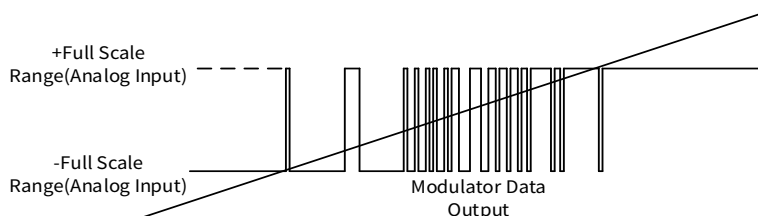


Figure 8.2 data output vs input voltage

Within full-scale input range, Equation 8.1 calculates the ones and zeros density of output bitstream for input voltage:

$$\text{Density} = (V_{IN} + V_{CLIPPING}) / (2 * V_{CLIPPING}) \tag{Equation 8.1}$$

Besides the data output signal at the DOUT pin, the NSI1303M/Dx also provides clock signal at the CLKOUT pin. See the Timing Characteristics in section 5.3 for more details.

8.4. Fail-safe Output

NSI1303 integrates some diagnostic measures and offers a fail-safe output to simplify system-level design. The fail-safe function will be activated in following conditions:

- When the undervoltage of AVDD is detected ($AVDD < AVDD_{UV}$), DOUT pin output a uncoded bitstream of all logic zeros, as shown in Figure 8.3 and Figure 8.4.
- When the overvoltage of common-mode input voltage is detected ($V_{CM} > V_{CMov}$), DOUT pin output a uncode bitstream of all logic ones, as shown in Figure 8.3 and Figure 8.4.

NOTE: If both of the faults above occur at the same time, DOUT pin output a uncode bitstream of all logic zeros. (AVDD missing has a higher priority).

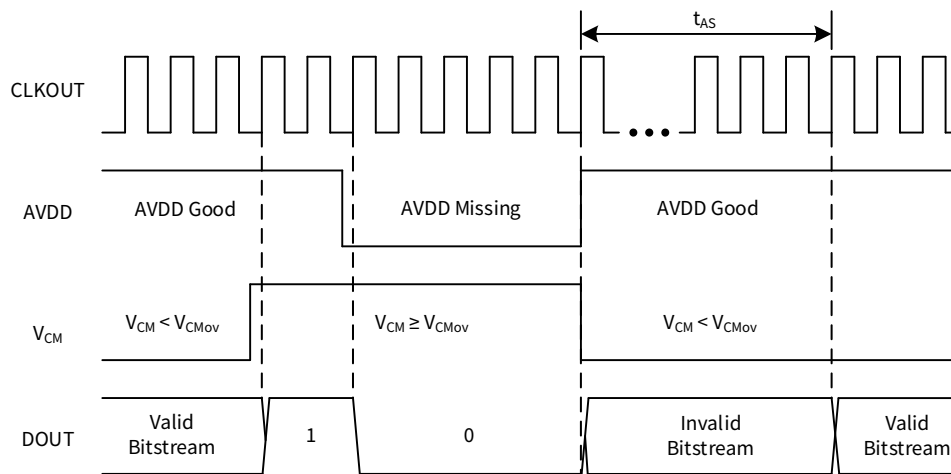


Figure 8.3 Fail-safe Bitstream Output of NSI1303Mx

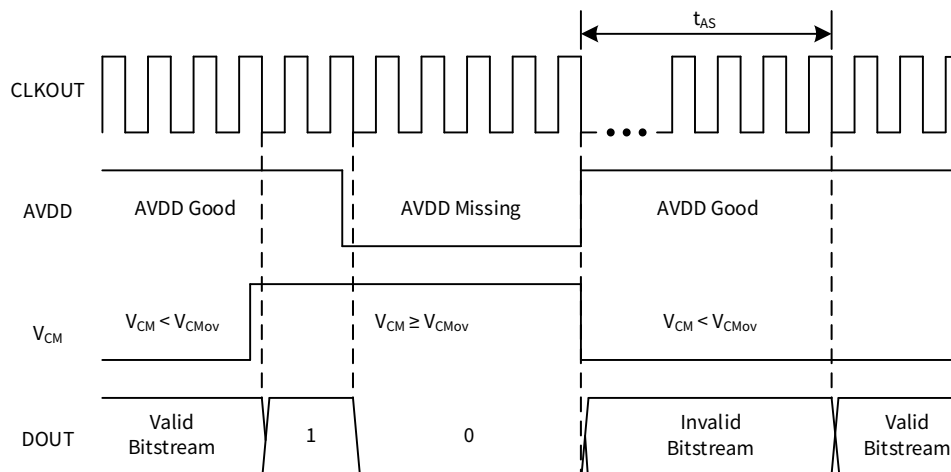


Figure 8.4 Fail-safe Bitstream Output of NSI1303Dx

If an overrange input signal is applied to the NSI1303 ($V_{IN} \geq V_{Clipping}$), the output generates a single 0 or 1 every 128 bits at DOUT, as shown in Figure 8.5 and Figure 8.6.

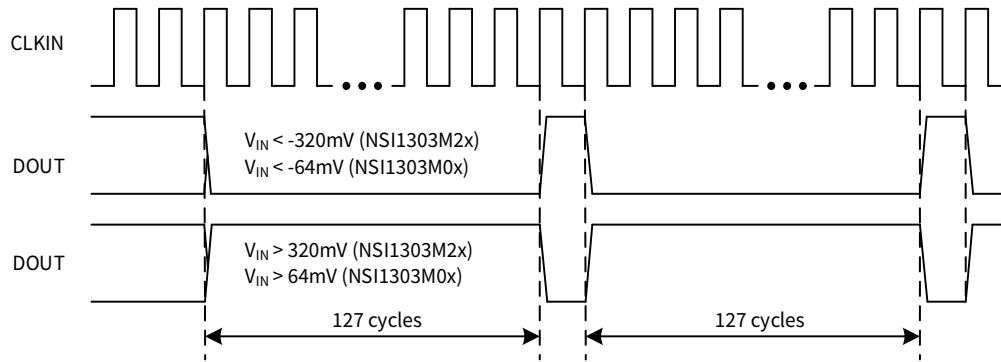


Figure 8.5 Overrange Bitstream Output of NSI1303Mx

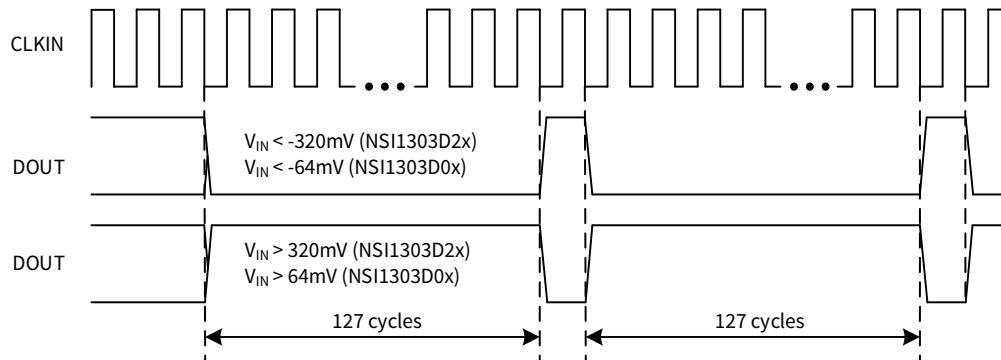


Figure 8.6 Overrange Bitstream Output of NSI1303Dx

9. Application Note

9.1. Typical Application Circuit

NSI1303 is ideally suited to shunt resistor-based current sensing in high voltage applications such as frequency inverters. The typical application circuit is shown in Figure 9.1.

The voltage across the shunt resistor R_{sense} is applied to the differential input of NSI1303 through a RC filter. The internal second-order sigma-delta modulator converts the analog input to a single-bit output stream. The CLKOUT pin outputs the internally generated clock, which is synchronized with the output bit-stream. The external digital system receives the clock signal and provides a digital filter for decimation and quantization noise filtering. NSI1303 is suitable for both rising and falling edge sampling, clock rising edge effective for NSI1303Mx and clock falling edge effective for NSI1303Dx.

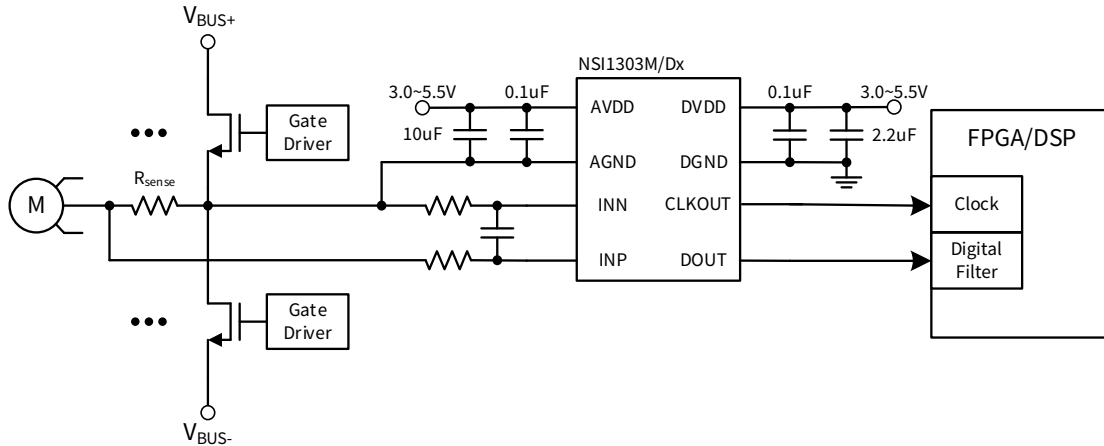


Figure 9.1 Typical application circuit of NSI1303M/Dx in phase current sensing

9.2. Shunt Resistor Selection

Choosing a particular shunt resistor is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller sense resistor decreases power dissipation, while larger sense resistor can improve measure accuracy by utilizing the full input range of isolated amplifier.

There are two other factors should be considered when selecting the shunt resistor:

- The voltage-drop caused by the rated current range must not exceed the recommended linear input voltage range: $V_{SHUNT} \leq FSR$.
- The voltage-drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $V_{SHUNT} \leq V_{Clipping}$.

9.3. Digital Filter

The Σ - Δ modulator has characteristics of noise shaping. Most of the quantization noise is pushed from a low frequency to a higher frequency.

In order to reduce higher-frequency quantization noise, the modulator output is fed to the digital low-pass filter. Subsequently, the signal of interest passes through to the output of the digital filter, while much of the higher-frequency quantization noise is filtered out.

The digital filter serves another function – decimation. It creates a digital output code from the bitstream that the modulator outputs. The ratio of the modulator rate (f_{MOD}) of the delta-sigma modulator to its output data rate (f_{DR}) is the oversampling ratio (OSR). The relationship between f_{DR} and f_{MOD} is:

$$f_{DR} = f_{MOD} / OSR \quad \text{Equation 9.1}$$

A sinc3 filter is recommended since it's simple and requires less hardware resources. Equation 9.2 describes the transfer function of a sinc filter.

$$H(Z) = \left(\frac{1}{DR} \frac{(1-Z^{-DR})}{(1-Z^{-1})} \right)^N \quad \text{Equation 9.2}$$

where:

DR is the decimation rate;

N is the sinc filter order.

The filter can be implemented in an FPGA or DSP. The sinc filter creates a digital output code by taking a multi-order moving average of the modulator output over a certain number of modulator clock periods.

The higher the decimation rate, the higher the conversion accuracy, and the lower the output data rate. So, there is a trade-off between accuracy and data rate. All the characterization in this datasheet is tested with a sinc3 filter with an oversampling ratio (OSR) of 256.

The output data size is expressed in Equation 9.3. The 16 most significant bits are used to return a 16-bit result.

$$Data\ Size = N \times \log_2 DR \quad \text{Equation 9.3}$$

The filter characteristics for a third-order sinc filter are summarized in Table 9.1.

Table 9.1 Sinc3 Filter Characteristics for 20 MHz CLKIN

Decimation Rate (DR)	Data Output Rate (kHz)	Data Size (bits)	Filter Response (kHz)
32	625	15	163.7
64	312.5	18	81.8
128	156.2	21	40.9
256	78.1	24	20.4
512	39.1	27	10.2

9.4. PCB Layout

There are some key guidelines or considerations for optimizing performance in PCB layout:

- NSI1303 requires a 0.1µF bypass capacitor between AVDD and AGND, DVDD and DGND. The capacitor should be placed as close as possible to the VDD pin. If better filtering is required, an additional 1~10µF capacitor may be used.
- Kelvin rules is recommended for the connection between shunt resistor to NSI1303. Because of the Kelvin connection, any voltage drops across the trace and leads should have no impact on the measured voltage.
- Place the shunt resistor close to the INP and INN inputs and keep the layout of both connections symmetrical and run very close to each other to the input of the NSI1303. This minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal.

10. Package Information

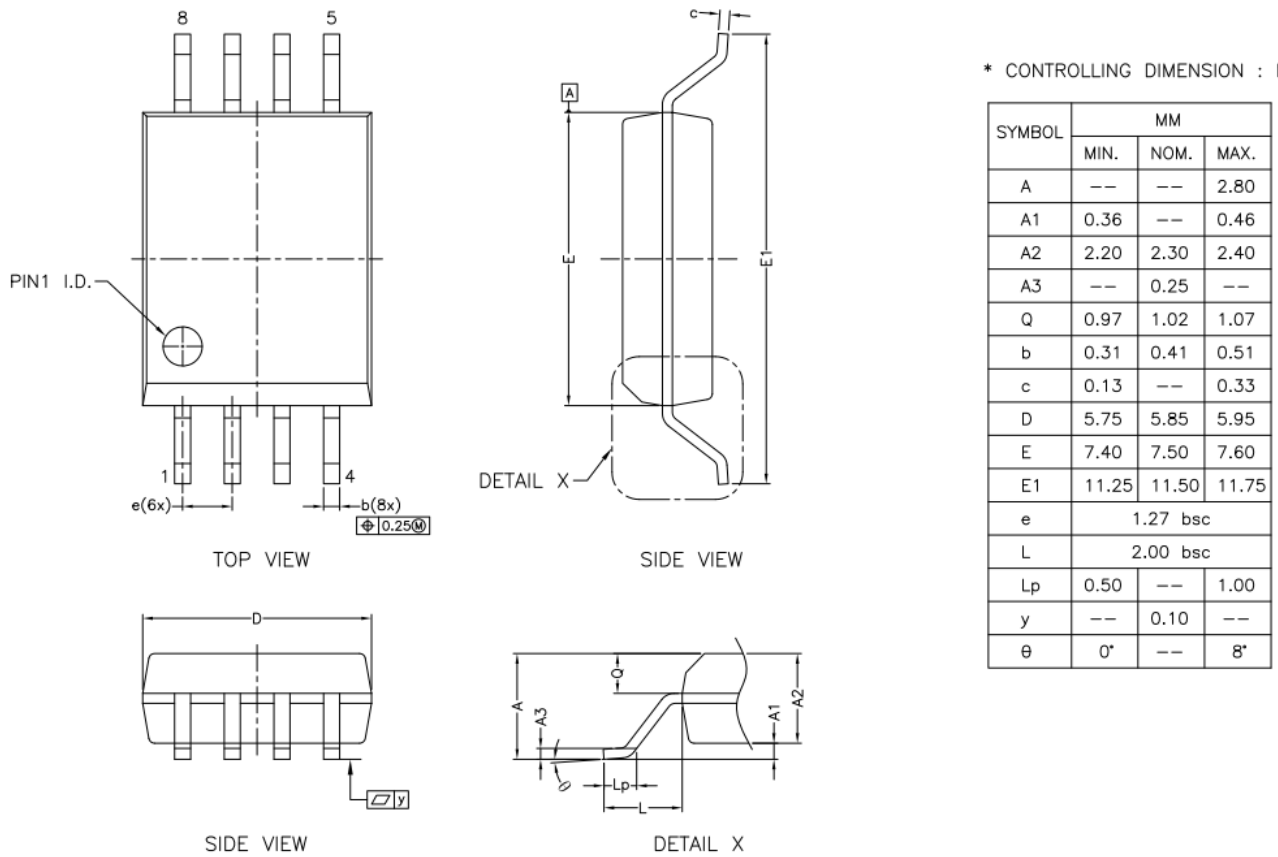
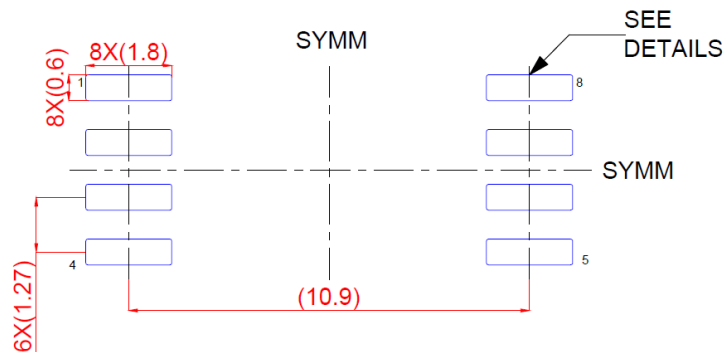


Figure 10.1 SOW8 Package Shape and Dimension in millimeters



LAND PATTERN EXAMPLE(mm)
9.1 mm NOMINAL
CLEARANCE/CREEPAGE



Figure 10.2 SOW8 Package Board Layout Example

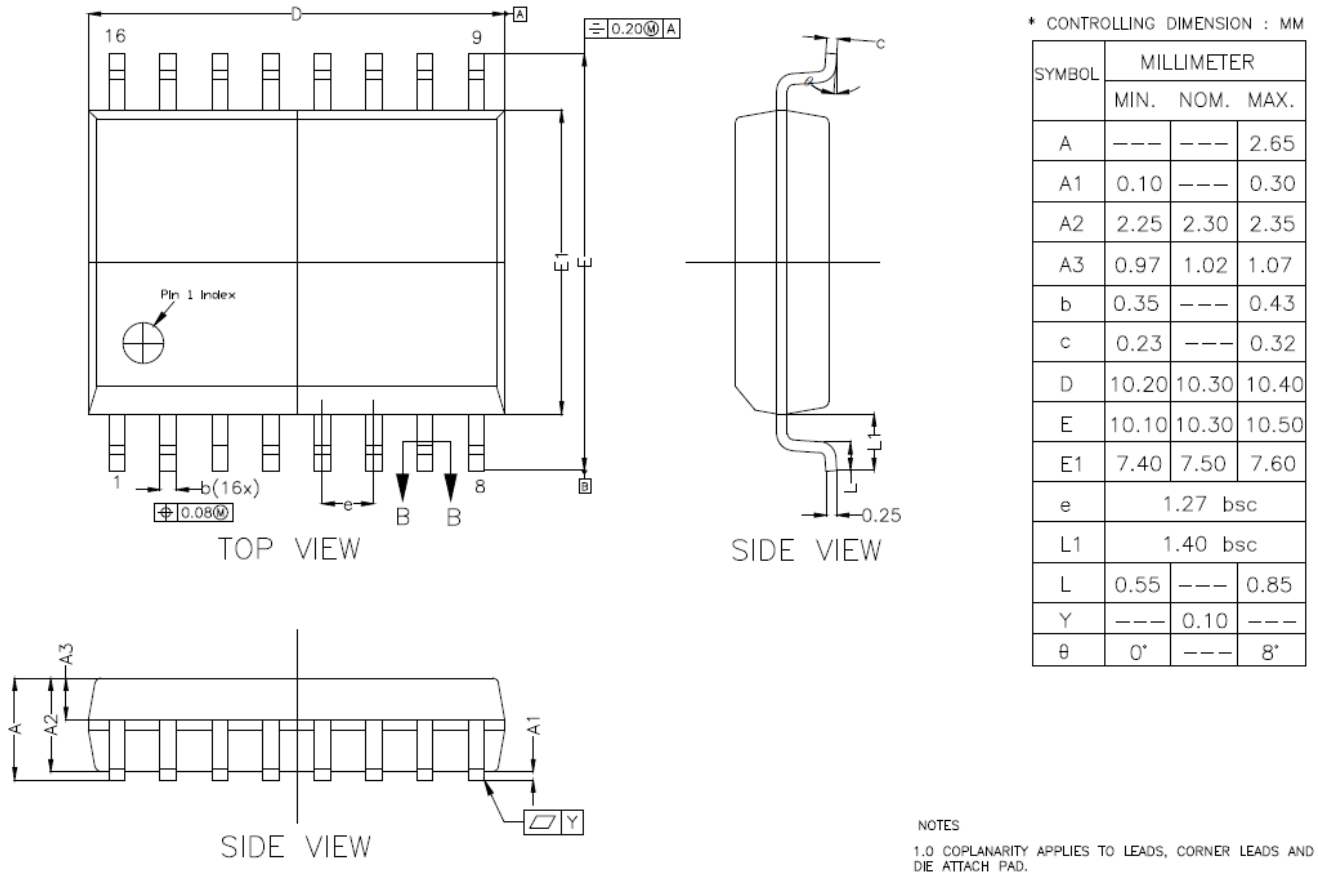


Figure 10.3 SOW16 package shape and dimension in millimeters

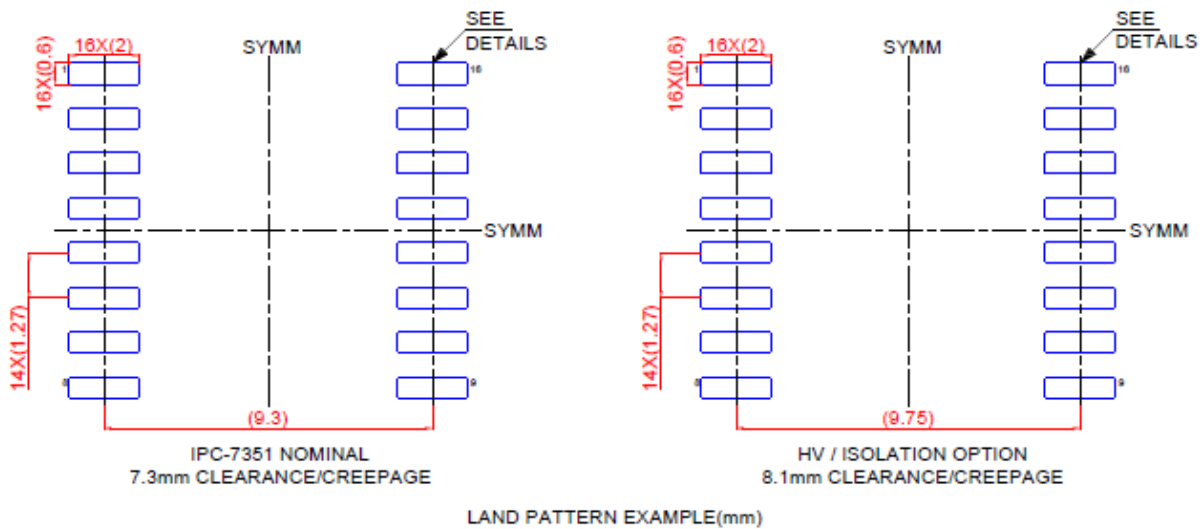


Figure 10.4 SOW16 Package Board Layout Example

11. Ordering Information

Part No.	Isolation Rating(kV)	Linear Input Range(mV)	Moisture Sensitivity Level	Temperature	Automotive	Package Type	Package Drawing	SPQ	Release To Market
NSI1303M01-DSWVR	5	-50 ~ 50	Level-3	-40 to 125°C	No	SOP8 (300mil)	SOW8	1000	No
NSI1303M21-DSWVR	5	-250 ~ 250	Level-3	-40 to 125°C	No	SOP8 (300mil)	SOW8	1000	Yes
NSI1303M02-DSWVR	5	-50 ~ 50	Level-3	-40 to 125°C	No	SOP8 (300mil)	SOW8	1000	Yes
NSI1303M22-DSWVR	5	-250 ~ 250	Level-3	-40 to 125°C	No	SOP8 (300mil)	SOW8	1000	Yes
NSI1303D01-DSWVR	5	-50 ~ 50	Level-3	-40 to 125°C	No	SOP8 (300mil)	SOW8	1000	No
NSI1303D21-DSWVR	5	-250 ~ 250	Level-3	-40 to 125°C	No	SOP8 (300mil)	SOW8	1000	No
NSI1303D02-DSWVR	5	-50 ~ 50	Level-3	-40 to 125°C	No	SOP8 (300mil)	SOW8	1000	No
NSI1303D22-DSWVR	5	-250 ~ 250	Level-3	-40 to 125°C	No	SOP8 (300mil)	SOW8	1000	No
NSI1303M01-DSWR	5	-50 ~ 50	Level-2	-40 to 125°C	No	SOP16 (300mil)	SOW16	1000	No
NSI1303M21-DSWR	5	-250 ~ 250	Level-2	-40 to 125°C	No	SOP16 (300mil)	SOW16	1000	Yes
NSI1303M02-DSWR	5	-50 ~ 50	Level-2	-40 to 125°C	No	SOP16 (300mil)	SOW16	1000	No
NSI1303M22-DSWR	5	-250 ~ 250	Level-2	-40 to 125°C	No	SOP16 (300mil)	SOW16	1000	No
NSI1303D01-DSWR	5	-50 ~ 50	Level-2	-40 to 125°C	No	SOP16 (300mil)	SOW16	1000	No
NSI1303D21-DSWR	5	-250 ~ 250	Level-2	-40 to 125°C	No	SOP16 (300mil)	SOW16	1000	No
NSI1303D02-DSWR	5	-50 ~ 50	Level-2	-40 to 125°C	No	SOP16 (300mil)	SOW16	1000	No
NSI1303D22-DSWR	5	-250 ~ 250	Level-2	-40 to 125°C	No	SOP16 (300mil)	SOW16	1000	No

12. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NSI1303	Click here	Click here	Click here	Click here

13. Tape and Reel Information

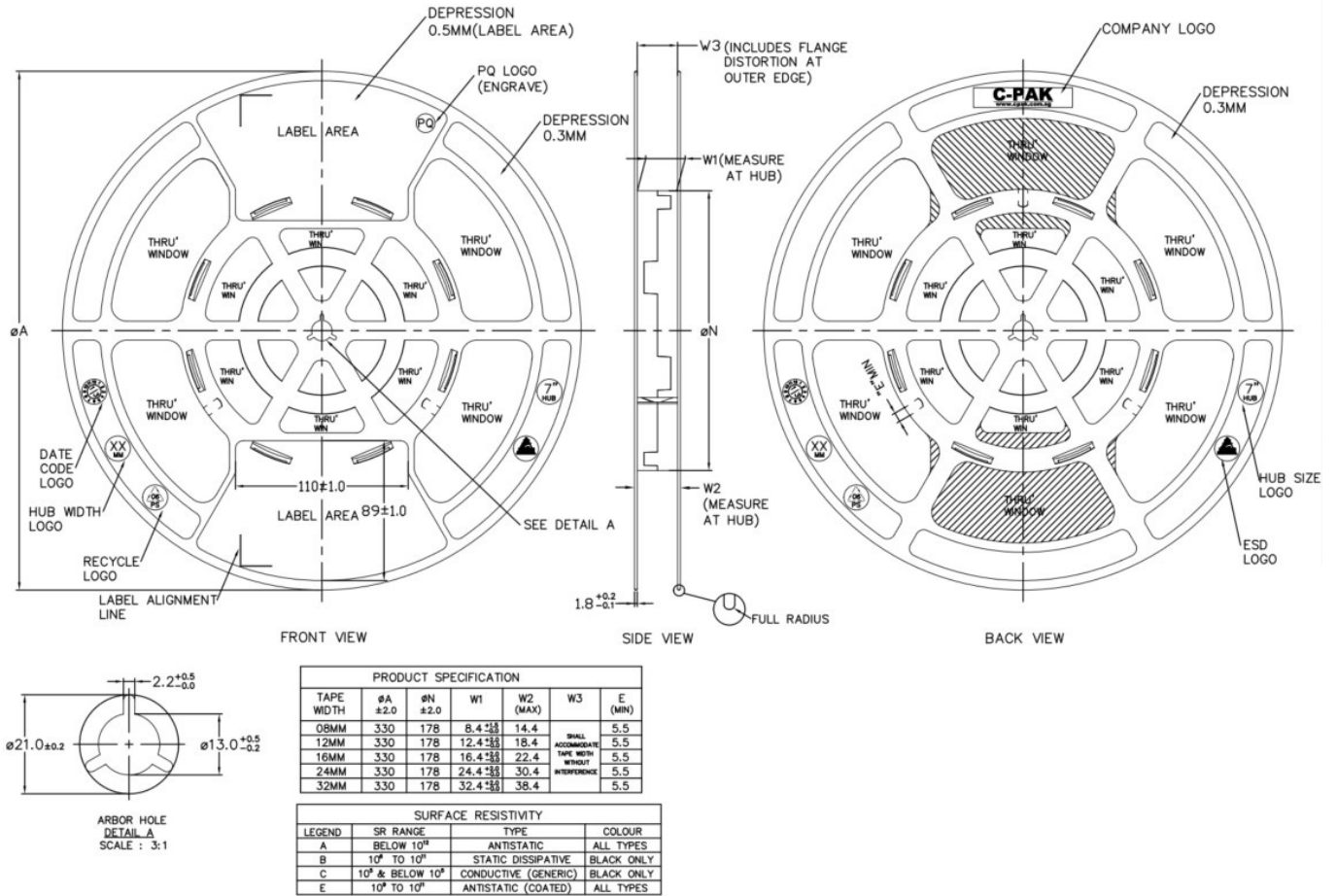


Figure 13.1 Tape Information

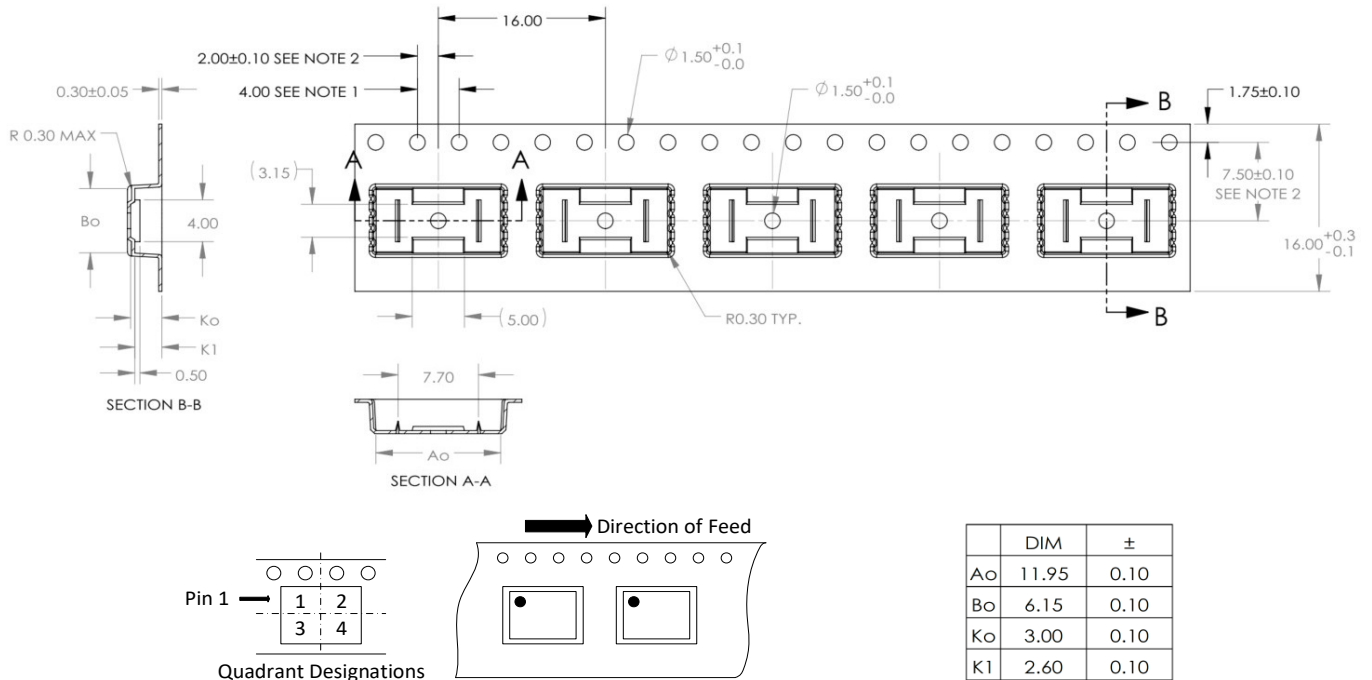
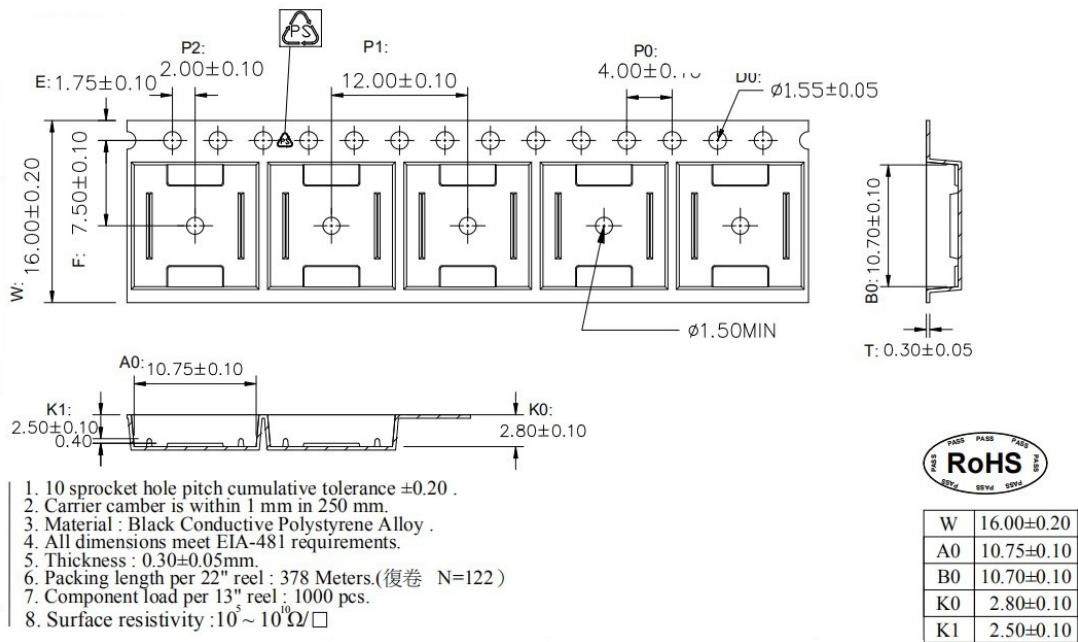


Figure 13.2 Reel Information of SOP8(300mil)



1. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy .
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.30 ± 0.05 mm.
6. Packing length per 22" reel : 378 Meters.(復巻 N=122)
7. Component load per 13" reel : 1000 pcs.
8. Surface resistivity : $10^5 \sim 10^{10} \Omega/\square$

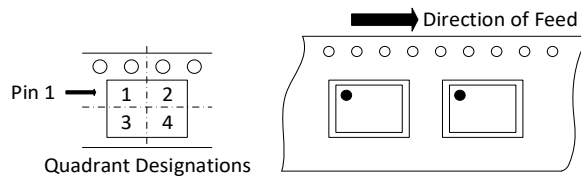


Figure 13.3 Reel Information of SOP16(300mil)

14. Revision History

Revision	Description	Date
1.0	Initial Release	2023/2/9
1.1	<ol style="list-style-type: none">1. Update safety regulatory info2. Update all NSI to NSI.3. Update test temperature condition of IIB, EO and EG4. Update Viso from 5000Vrms to 5700Vrms.	2024/11/29