

Product Overview

NSG65N15K is a high-performance system-in-package integrating a half-bridge gate driver, bootstrap diode and two 650V enhancement mode GaN transistors in symmetrical half-bridge configuration.

The integrated power GaNs have 650V drain-source blocking voltage and R_{DS_ON} of 150 m Ω . The high side of the embedded gate driver can be easily supplied by the integrated bootstrap diode.

The driver operates with a wide supply voltage from 10V to 15V while internal regulator could offer stable driver voltage to keep GaN transistors safe.

The undervoltage lock-out (UVLO) protection feature is provided in low side and high side drivers to prevent the GaN transistors from operating in low efficiency or dangerous conditions

The programmable dead-time control function has been provided.

The device operates in the industrial temperature range, -40°C to 125°C, and is available in a compact 9x9 mm QFN package with exposed pad

Key Features

- 650V integrated half-bridge driver and GaN power transistors
- Typical 150m Ω R_{DS_ON}
- No reverse recovery loss
- UVLO protection on low side and high side
- Stable regulator output for GaN driver
- Short switching delay and mismatch
- programmable Dead-time
- Integrated bootstrap diode

- Operating Temperature: -40~125°C
- RoHS & REACH Compliance
- Lead-free component, suitable for lead-free soldering profile: 260°C

Applications

- High density adapters and Chargers
- Half-bridge, full-bridge, LLC DC-DC converter
- High-Voltage PFC
- Switch-mode power suppliers

Device Information

Part Number	Package	Body Size
NSG65N15K-DQAFR	QFN32	9.0mm x 9.0mm x 0.725mm

Functional Block Diagram

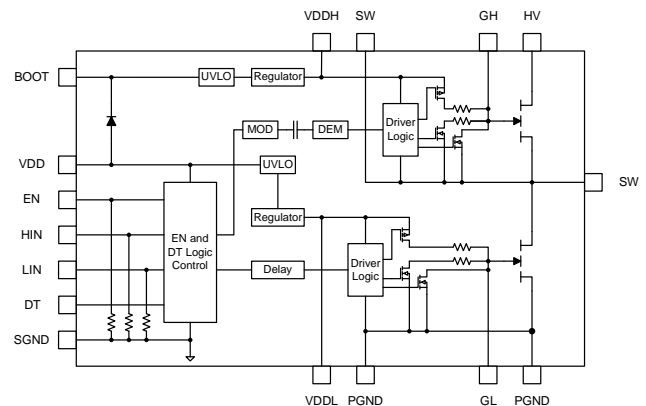


Figure 0.1 NSG65N15K Block Diagram

INDEX

1. PIN CONFIGURATION AND FUNCTIONS3

2. ABSOLUTE MAXIMUM RATINGS4

3. ESD RATINGS4

4. RECOMMENDED OPERATING CONDITIONS4

5. THERMAL INFORMATION4

6. SPECIFICATIONS5

 6.1. DRIVER ELECTRIC CHARACTERISTICS5

 6.2. GAN TRANSISTOR ELECTRIC CHARACTERISTICS6

 6.3. DRIVER DYNAMIC CHARACTERISTICS6

 6.4. GAN TRANSISTOR DYNAMIC CHARACTERISTICS6

 6.5. TYPICAL PERFORMANCE CHARACTERISTICS7

 6.6. PARAMETER MEASUREMENT INFORMATION10

7. FUNCTION DESCRIPTION10

 7.1. UNDER VOLTAGE LOCK OUT (UVLO)10

 7.2. INPUT AND OUTPUT LOGIC11

 7.3. PROGRAMMABLE DEADTIME (DT PIN)11

 7.4. V_{BOOT} UNDER VOLTAGE LOCK OUT (UVLO)12

8. APPLICATION NOTE13

 8.1. TYPICAL APPLICATION CIRCUIT13

 8.2. LAYOUT RECOMMENDATIONS14

9. PACKAGE INFORMATION15

10. ORDERING INFORMATION16

11. TAPE AND REEL INFORMATION17

12. REVISION HISTORY18

1. Pin Configuration and Functions

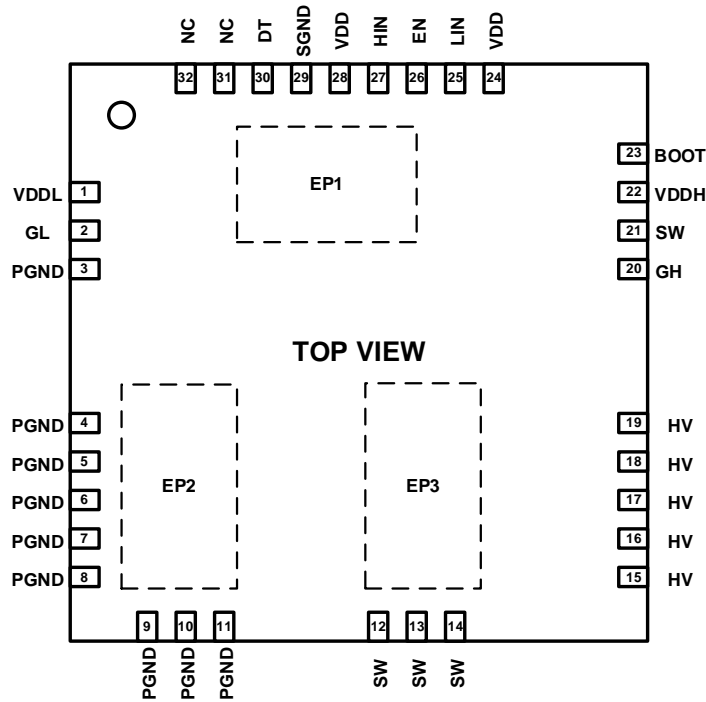


Figure 1.1 Pin Configuration

Table 1.1 Pin Configuration and Description

Pin No.	Symbol	Function
1	VDDL	Low-side voltage regulator output. A ceramic capacitor of not less than 100nF must be connected between Pin1 and Pin3.
2	GL	Low-side GaN gate
3~11, EP2	PGND	Low-side GaN source
12~14,21, EP3	SW	Low-side GaN drain and high-side GaN source
15~19	HV	High-side GaN drain
20	GH	High-side GaN gate
22	VDDH	High-side voltage regulator output. A ceramic capacitor of not less than 100nF must be connected between Pin22 and Pin21.
23	BOOT	High-side gate driver power supply
24, 28	VDD	Half-bridge driver power supply
25	LIN	Low-side driver logic input
26	EN	Half-bridge driver enable logic input
27	HIN	High-side driver logic input
29, EP1	SGND	Logic ground

Pin No.	Symbol	Function
30	DT	Dead-time controller
31, 32	NC	Not connected, be reserved

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
GaN Drain to Source Voltage	V_{DS}	-0.3	650	V
GaN Drain Source Voltage, pulse ¹⁾	$V_{DS, pulse}$	-0.3	750	V
Driver Supply Voltage	VDD to SGND, BOOT to SW	-0.3	24	V
Regulator Output Voltage	VDDL to GND, VDDH to SW	-0.3	7	V
Different Ground Voltage	SGND to PGND	-5	5	V
Input Signal Voltage	HIN, LIN, EN, DT to SGND	-0.3	$V_{VDD}+0.3$	V
	HIN, LIN, EN, DT to SGND, Transient for 50ns	-5	$V_{VDD}+0.3$	V
GaN Gate to Source Voltage ²⁾	GL to PGND, GH to SW	-0.3	$V_{VDDL}+0.3$, $V_{VDDH}+0.3$	V
	GL to PGND, GH to SW, Transient for 50ns	-2	10	V
Continuous current, drain source ³⁾	$I_D @ T_C=25^\circ C$		10.2	A
Pulse Current, drain source ³⁾	$I_D @ T_C=25^\circ C, V_{GS}=6V$ and $t_{Pulse}=10\mu s$		20.5	A
Pulse Current, drain source ³⁾	$I_D @ T_C=125^\circ C, V_{GS}=6V$ and $t_{Pulse}=10\mu s$		10.2	A
Diode Repetitive peak reverse voltage ³⁾	V_{RRM}		750	V
Diode Peak Forward Surge Current 8.3ms single half sine-wave ³⁾	I_{FSM}		12	A
Junction Temperature	T_J	-40	140	$^\circ C$
Storage Temperature	T_{stg}	-55	150	$^\circ C$

1) $V_{DS, pulse}$ is intended for repetitive pulse < 100ns, total time < 1h, $T_J = 125^\circ C$.

2) The minimum V_{GS} is clamped by ESD protection circuit.

3) Range estimated by characterization, not tested in production

3. ESD Ratings

	Ratings	Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD	± 2000	V
	Charged device model (CDM), per AEC-Q100-011-RevB	± 750	V

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
GaN Drain to Source Voltage	V_{DS}	0	600	V
Driver Supply Voltage	VDD to SGND, BOOT to SW	10	15	V
GaN Gate to Source Voltage	GL to PGND, GH to SW	0	V_{VDDL}, V_{VDDH}	V
Input Signal Voltage	HIN, LIN, EN to SGND	0	V_{VDD}	V
Ambient Temperature	T_a	-40	125	$^\circ C$

5. Thermal Information

Parameters	Symbol	Value	Unit
Junction-to-ambient thermal resistance ¹⁾	θ_{JA}	27	$^\circ C/W$

Junction-to-case(top) thermal resistance ¹⁾	$\theta_{JC (top)}$	11.3	°C/W
Junction-to-board thermal resistance ¹⁾	θ_{JB}	5.8	°C/W
Junction-to-top characterization parameter ¹⁾	Ψ_{JT}	2.1	°C/W
Junction-to-board characterization parameter ¹⁾	Ψ_{JB}	4.9	°C/W

1) High Effective Thermal Conductivity Test Board (2s2p) in an environment described in JESD51-2a.

6. Specifications

6.1. Driver Electric Characteristics

VDD = 12V, Ta = -40°C to 125°C. Unless otherwise noted, Typical values are at Tj = 25°C.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Driver Power Supply						
VDD Quiescent Current	I _{VDDQ}		0.42		mA	EN=HIN = LIN = 0V
VDD Operating Current	I _{VDDO}		2.2		mA	EN=5V, HV = SW = 0V, BOOT = 12V, f = 500kHz
BOOT Quiescent Current	I _{BOOTQ}		0.58		mA	EN= HIN = LIN = 0V
BOOT Operating Current	I _{BOOTO}		2.2		mA	EN= 5V, LIN=SW = 0V, BOOT = 12V, f = 500kHz
VDD UVLO Rising Threshold	V _{VDD_ON}	8.0	8.4	8.8	V	
VDD UVLO Falling Threshold	V _{VDD_OFF}	7.5	7.8	8.1	V	
VDD UVLO Hysteresis	V _{VDD_HYS}	0.4	0.6		V	
BOOT UVLO Rising Threshold	V _{BOOT_ON} -V _{SW}	8.0	8.4	8.8	V	
BOOT UVLO Falling Threshold	V _{BOOT_OFF} -V _{SW}	7.5	7.8	8.1	V	
BOOT UVLO Hysteresis	V _{BOOT_HYS}	0.4	0.6		V	
Bootstrap Diode Voltage Drop ¹⁾	V _{DB}		1		V	SW = 0V
Input Logic						
Input Pin Pull-down Resistance	R _{HIN_PD} , R _{LIN_PD}		200		kΩ	HIN = LIN = 3V
Enable Pin Pull-down Resistance	R _{EN_PD}		200		kΩ	EN = 3V
Input Pin High Logic Bias Current	I _{HIN_H} , I _{LIN_H}		20		μA	HIN = LIN = 5V
Enable Pin High Logic Bias Current	I _{EN_H}		20		μA	EN = 5V
Logic High Input Threshold	V _{HIN_H} , V _{LIN_H}	1.7	2.1	2.5	V	
Logic Low Input Threshold	V _{HIN_L} , V _{LIN_L}	0.9	1.2	1.5	V	
Input Hysteresis	V _{HIN_HYS} , V _{LIN_HYS}	0.7	0.9		V	
Enable High Input Threshold	V _{EN_H}	1.7	2.1	2.5	V	
Enable Low Input Threshold	V _{EN_L}	0.9	1.4	1.5	V	
Enable Input Hysteresis	V _{EN_HYS}	0.5	0.7		V	
Driver Output Characteristic						
Regulator Output Voltage	V _{VDDL} , V _{VDDH} -V _{SW}	5.5	6	6.4	V	C _{VDDL} = 100nF, C _{VDDH-SW} = 100nF
Regulator UVLO Rising Threshold	V _{VDDH_ON} , V _{VDDL_ON}	4.1	4.4	4.7	V	

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Regulator UVLO Falling Threshold	$V_{VDDH_OFF}, V_{VDDL_OFF}$	3.8	4.1	4.5	V	
Regulator UVLO Hysteresis	$V_{VDDH_HYS}, V_{VDDL_HYS}$		0.3		V	
Driver Turn-on State Voltage	V_{GH_H}		V_{VDDH}		V	Reference to SW
	V_{GL_H}		V_{VDDL}		V	Reference to PGND
Gate Driver Resistance	R_{GL}, R_{GH}		5.1		Ω	

1) Tested at wafer level.

6.2. GaN Transistor Electric Characteristics

$V_{GS} = 6V$, $T_a = -40^\circ C$ to $125^\circ C$. Unless otherwise noted, Typical values are at $T_j = 25^\circ C$.

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Gate Threshold Voltage ¹⁾	$V_{GS(th)}$		1.7		V	$I_D = 12mA, V_{DS} = V_{GS}$
Drain Source Leakage Current ¹⁾	I_{DSS}		0.45	22	μA	$V_{DS} = 650V, V_{GS} = 0V, T_j = 25^\circ C$
Gate Source Leakage Current ¹⁾	I_{GSS}		60		μA	$V_{DS} = 0V, V_{GS} = 6V$
Drain Source On-state Resistance ¹⁾	$R_{DS(on)}$		150	190	m Ω	$V_{GS} = 6V, I_D = 3.9A, T_j = 25^\circ C$
			300		m Ω	$V_{GS} = 6V, I_D = 3.9A, T_j = 150^\circ C$
Source Drain Reverse Voltage ¹⁾	V_{SD}		2.6		V	$V_{GS} = 0V, I_{SD} = 3.9A$

1) Tested at wafer level.

6.3. Driver Dynamic Characteristics

$V_{DD} = 12V$, $T_a = -40^\circ C$ to $125^\circ C$. Unless otherwise noted, Typical values are at $T_a = 25^\circ C$.

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Minimum Input Pulse Width	t_{PWmin}			20	ns	
Turn-on Delay Time	$t_{D(on)}$		30	60	ns	
Turn-off Delay Time	$t_{D(off)}$		30	60	ns	
VDDL or VDDH Rising Time ¹⁾	t_{VDDL_R}, t_{VDDH_R}		12		μs	$C_{VDDL} = 100nF, C_{VDDH-SW} = 100nF$
Programmed Deadtime	t_{DT_Min}		20		ns	$R_{DT} \leq 14k\Omega$ or $R_{DT} > 620k\Omega, C_{DT} = 1nF$
	t_{DT_Max}		100		ns	$140k\Omega < R_{DT} \leq 200k\Omega, C_{DT} = 1nF$

1) See detail in Figure 7.1.

6.4. GaN Transistor Dynamic Characteristics

$V_{GS} = 6V$, $T_a = -40^\circ C$ to $125^\circ C$. Unless otherwise noted, Typical values are at $T_a = 25^\circ C$.

Parameter	Symbol	Min	Typ	Max	Unit	Comments
VDS Fall Time ¹⁾	t_{G_on}		4		ns	$V_{DS} = 400V, I_D = 8A, L = 318\mu H$
VDS Rise Time ¹⁾	t_{G_off}		4		ns	$V_{DS} = 400V, I_D = 8A, L = 318\mu H$
Total Gate Charge ¹⁾	Q_G		2.0		nC	$V_{GS} = 0$ to $6V, V_{DS} = 400V, I_D = 3.9A, T_j = 25^\circ C$
Output Charge ¹⁾	Q_{OSS}		24.5		nC	$V_{GS} = 0V, V_{DS} = 400V$
Output Capacitance Stored Energy ¹⁾	E_{OSS}		3.5		μJ	$V_{GS} = 0V, V_{DS} = 400V$
Output Capacitance ¹⁾	C_{OSS}		30		pF	$V_{GS} = 0V, V_{DS} = 400V$
Effective Output Capacitance ¹⁾ (Energy related)	C_{O_ER}		43		pF	$V_{GS} = 0V, V_{DS} = 400V$

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Effective Output Capacitance ¹⁾ (Time related)	C _{O_TR}		60		pF	V _{GS} = 0V, V _{DS} = 400V
Source-Drain Reverse Voltage ¹⁾	V _{SD}		2.6		V	V _{GS} = 0 V; I _S = 3.9 A
Reverse Recovery Charge ¹⁾	Q _{rr}		0		nC	I _{SD} =3.9A, V _{DS} = 400V
Reverse Recovery current ¹⁾	I _{rr}		0		A	
Reverse recovery time ¹⁾	t _{rr}		0		ns	

1) Tested at wafer level.

6.5. Typical Performance Characteristics

T_J = 25°C, unless otherwise noted.

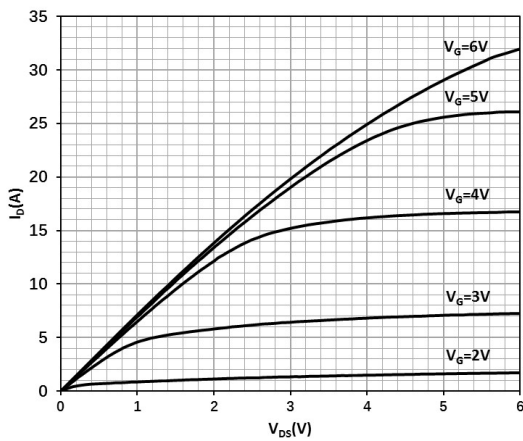


Figure 6.1 I_D vs. V_{DS}, T_J=25°C

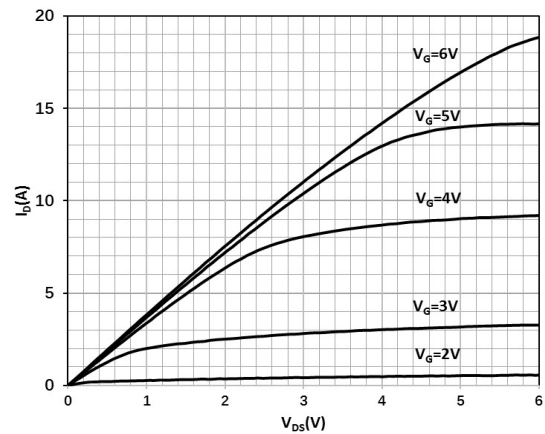


Figure 6.2 I_D vs. V_{DS}, T_J=125°C

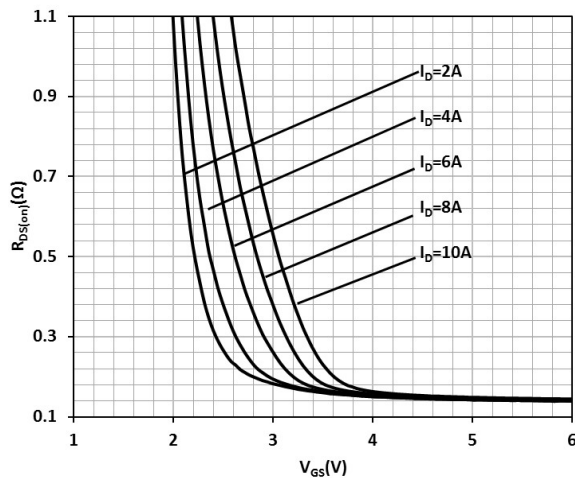


Figure 6.3 R_{DS_on} vs. V_{GS}, T_J=25°C

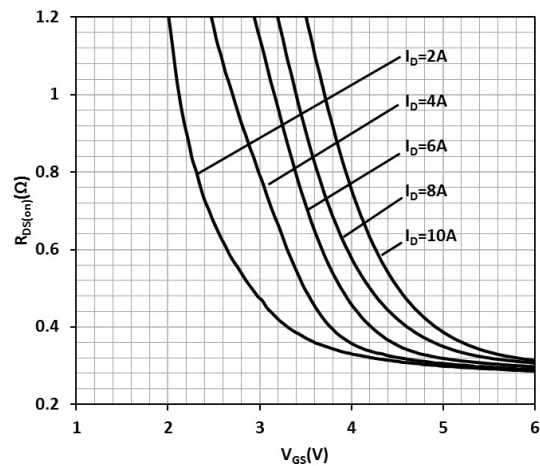


Figure 6.4 R_{DS_on} vs. V_{GS}, T_J=125°C

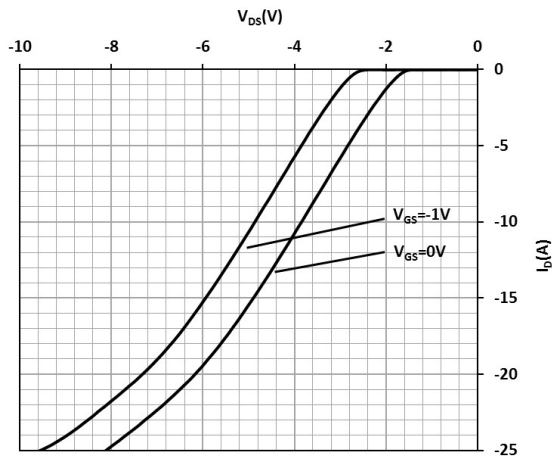


Figure 6.5 I_{SD} vs V_{SD} , $T_J=25^\circ\text{C}$

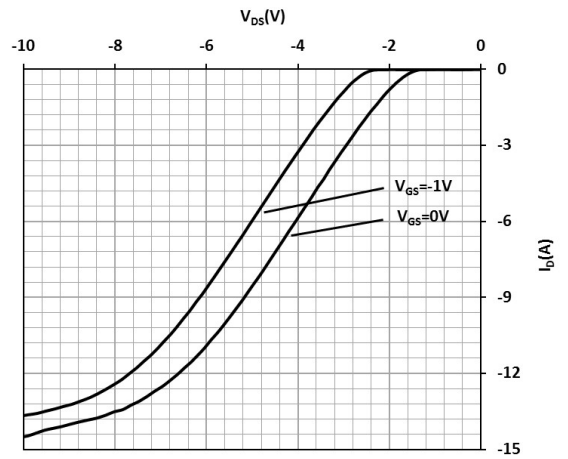


Figure 6.6 I_{SD} vs V_{SD} , $T_J=125^\circ\text{C}$

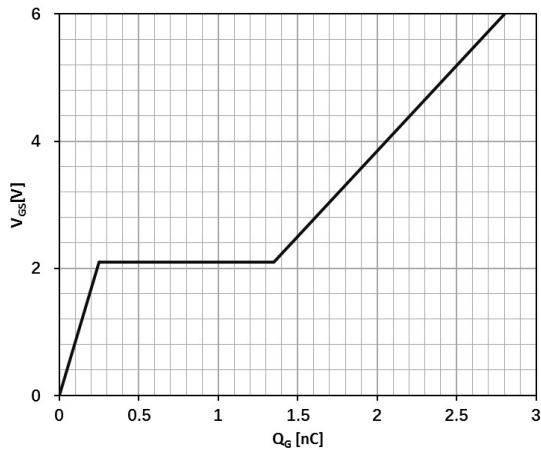


Figure 6.7 Typical Gate Charge, $T_J=25^\circ\text{C}$
 $V_{DC} = 400\text{ V}$; $I_D = 5\text{ A}$

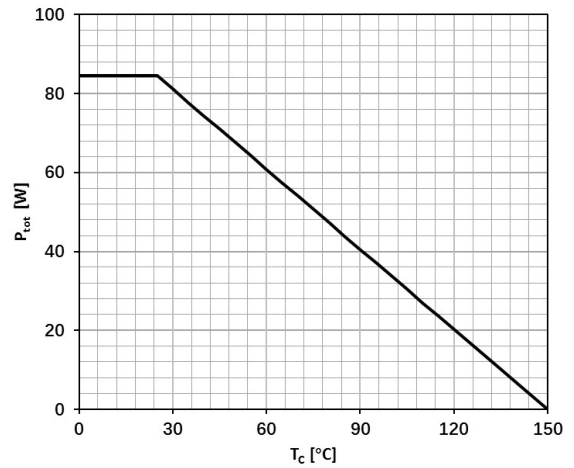


Figure 6.8 Power dissipation

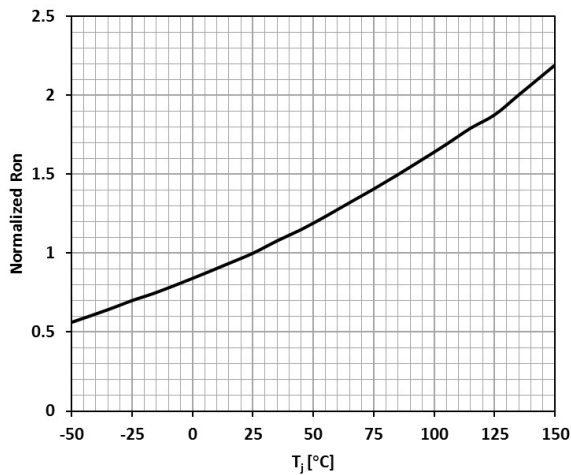


Figure 6.9 Normalized R_{DS_on} , $T_J=25^\circ\text{C}$

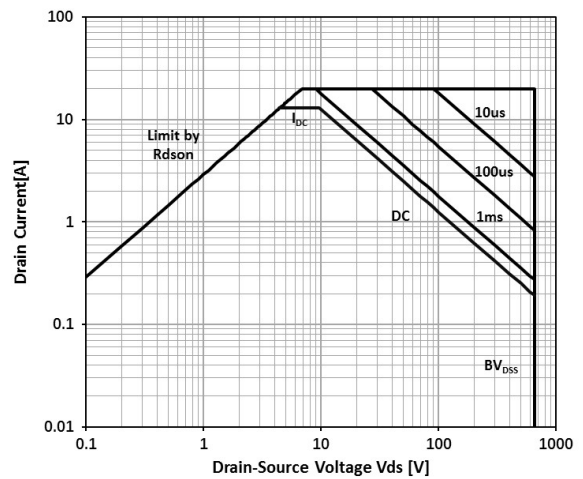


Figure 6.10 Safe operating area, $T_J=25^\circ\text{C}$

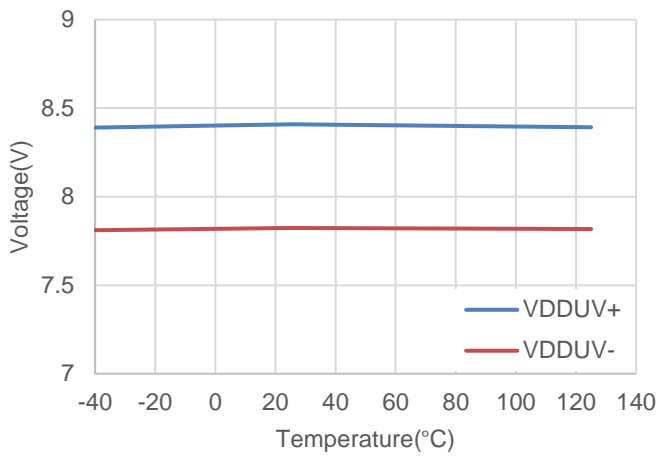


Figure 6.11 VDD UVLO vs. Temperature

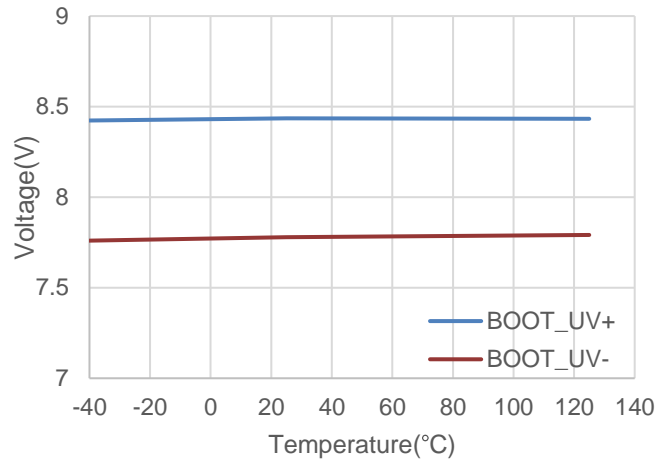


Figure 6.12 BOOT UVLO vs. Temperature

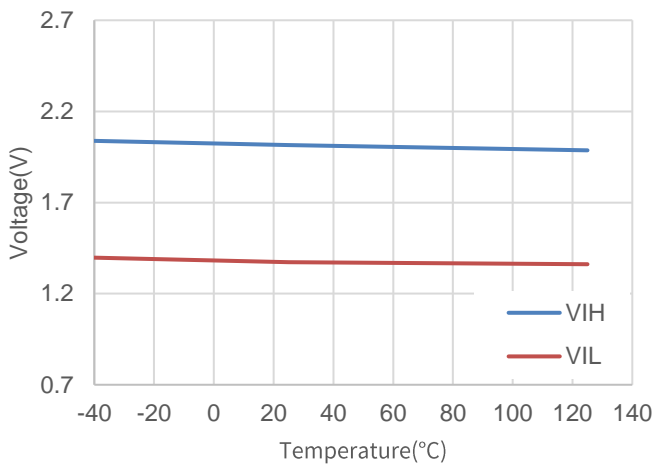


Figure 6.13 Input Logic (EN) Threshold vs. Temperature

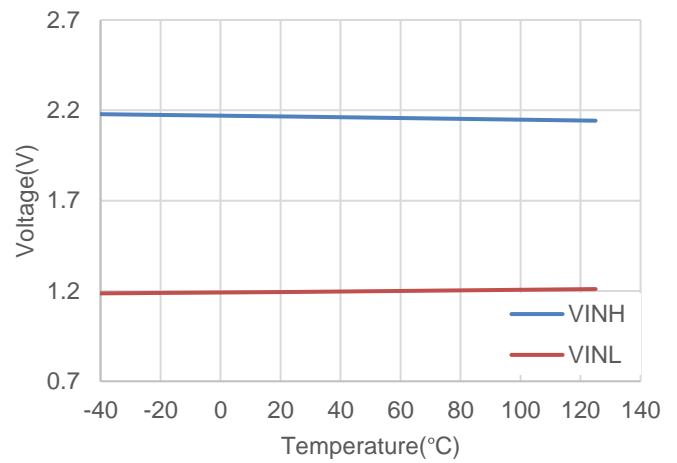


Figure 6.14 Input Logic (HIN, LIN) Threshold vs. Temperature

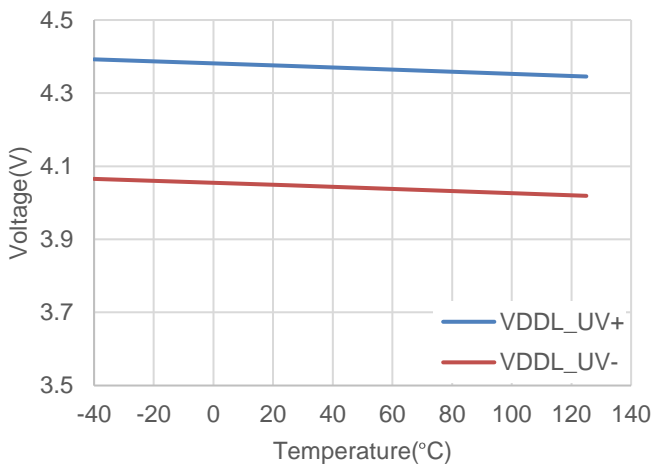


Figure 6.15 VDDL UVLO vs. Temperature

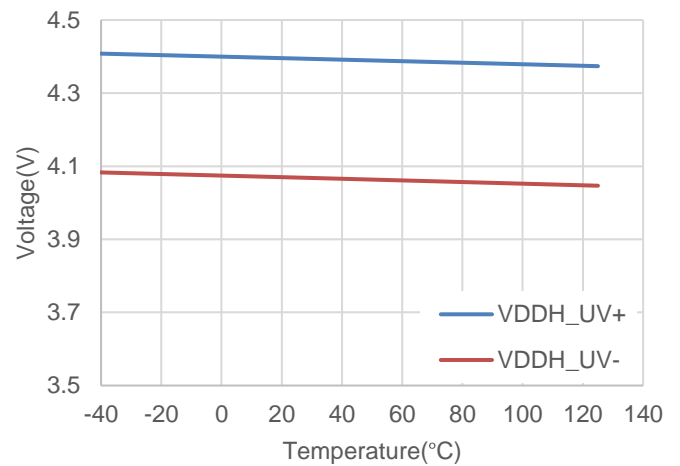


Figure 6.16 VDDH UVLO vs. Temperature

6.6. Parameter Measurement Information

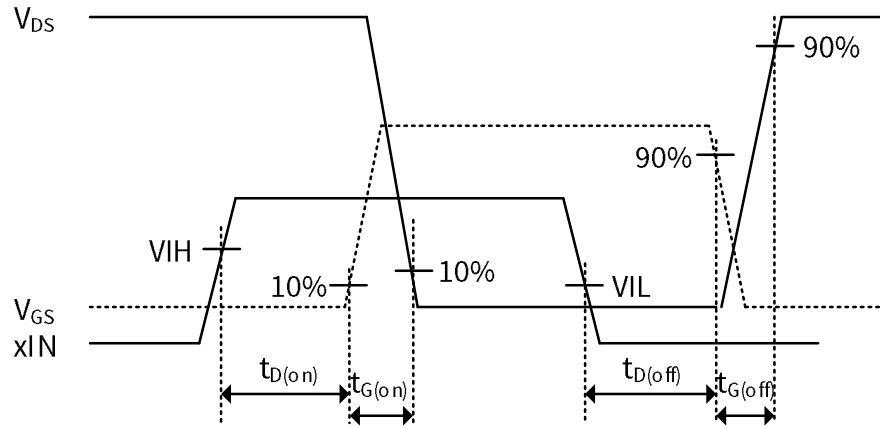


Figure 6.17 Switching Time Waveform

7. Function Description

7.1. Under Voltage Lock Out (UVLO)

The NSG65N15K has internal under voltage lock out (UVLO) protections on low side power supply blocks. The driver output is held low by an active clamp circuit when the supply voltage of VDD is lower than V_{VDD_ON} at power-up status or lower than V_{VDD_OFF} after power-up, regardless of the status of the input pins. Figure 7.1 shows the startup timing sequence.

The 0.6V hysteresis (V_{VDD_HYS}) on VDD ULVO protections are provided to prevent chatter noise from VDD supply and allow small drops in supply power which are usually happened in startup.

A not less than 100nF ceramic capacitor must be used on VDDL to normally operate.

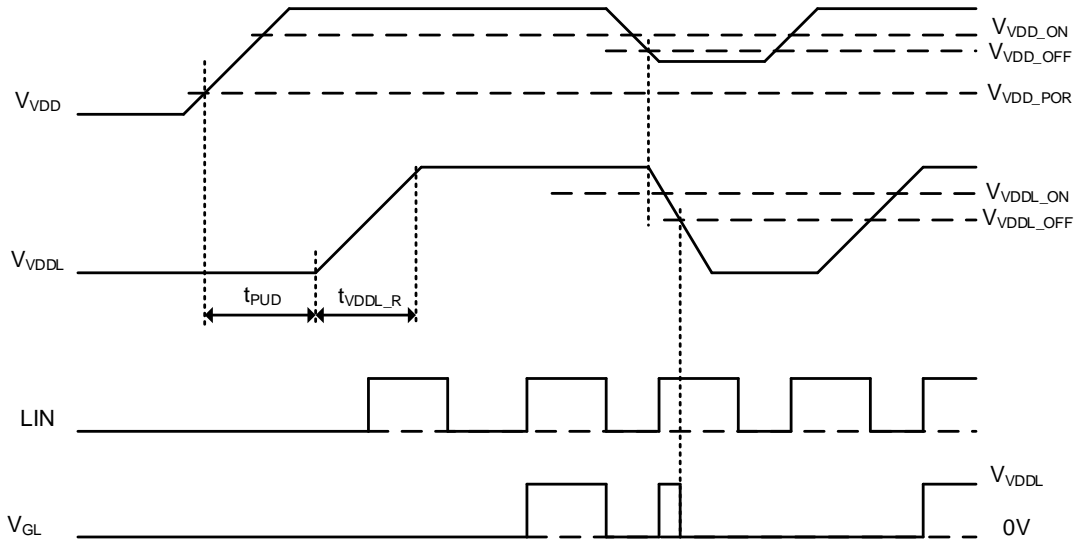


Figure 7.1 VDD UVLO Diagram

7.2. Input and Output Logic

The NSG65N15K is a half-bridge gate driver with dead-time control and integrated two GaN HEMTs and bootstrap diode. The EN pin should be high level to keep the driver operating normally.

Table 7.1 Output status vs. Input and Power status

Input Pins			GaN Transistors		NOTE
EN	HIN	LIN	HS	LS	
L or O	X	X	OFF	OFF	
H	L	L	OFF	OFF	
H	L	H	OFF	ON	GaN transistor turns on after the deadtime expires.
H	H	L	ON	OFF	
H	H	H	OFF	OFF	The input signal is later than VDD power up.

1) H= Logic High; L= Logic Low; O= Left Open; X= Irrelevant.

7.3. Programmable Deadtime (DT pin)

The NSD65N15K has a programmable deadtime control function by placing a resistor R_{DT} between the DT pin and SGND.

- 1) While R_{DT} is lower than 14kΩ or higher than 620kΩ, the deadtime duration (t_{DT}) is set to 20ns.
- 2) While R_{DT} is in range from 140kΩ to 200kΩ, the deadtime duration (t_{DT}) is set to 100ns.

The recommended value of R_{DT} is less 14kΩ or between 140kΩ and 200kΩ. It is also recommended to parallel a ceramic capacitor, for example 1nF, with R_{DT} to achieve better noise immunity.

The programmed deadtime is activated by the input signal's falling edge to prevent shoot-through between high side GaN HEMT and Low side GaN HEMT. The details of input and output logic with deadtime are shown as Figure 7.2

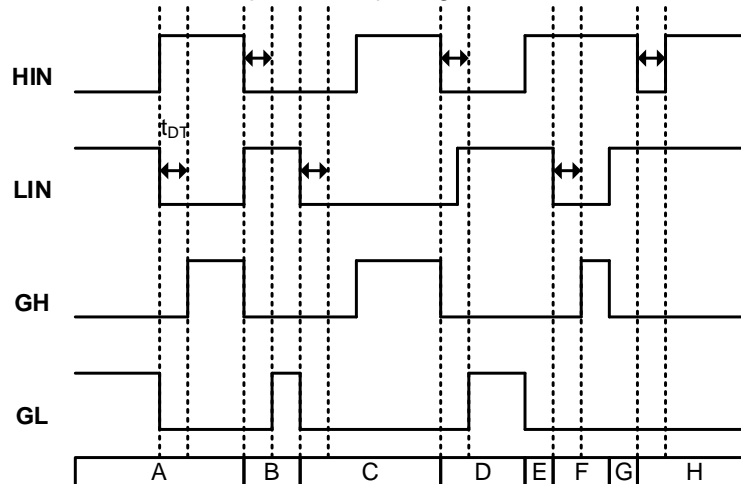


Figure 7.2 Input and Gate Logic with the Programmed Deadtime

Condition	Result
A: HIN goes high, and LIN goes low.	GL goes low immediately, then GH goes high after the programmed deadtime which is assigned at LIN goes low.
B: HIN goes low, and LIN goes high.	GH goes low immediately, then GL goes high after the programmed deadtime which is assigned at HIN goes low.
C: LIN goes low, then HIN goes high after deadtime.	GL goes low immediately, then GH goes high immediately when HIN goes high.

Condition	Result
D: HIN goes low, then LIN goes high before deadtime.	GH goes low immediately, then GL goes high after deadtime
E: HIN goes high, LIN is still high.	GL goes low immediately, and GH keeps low.
F: HIN is still high, LIN goes low.	GH goes high after deadtime while LIN is low, and GL keeps low.
G: HIN is still high, LIN goes high after deadtime	GH goes low immediately, and GL keeps low.
H: HIN goes low then goes high before deadtime while LIN is still high.	GH keeps low and GL keeps low because deadtime control.

7.4. V_{BOOT} Under Voltage Lock Out (UVLO)

The NSG65N15K has internal under voltage lock out (UVLO) protections on high side power supply blocks. The bootstrap diode is integrated to provide the current supply for high side driver. It is possible that an external bootstrap diode was in parallel with the integrated diode. The high side output (GH) is held low by an active clamp circuit when the supply voltage of VDD or BOOT is lower than V_{VDD_ON}/V_{BOOT_ON} at power-up status or lower than V_{VDD_OFF}/V_{BOOT_OFF} after power-up, regardless of the status of the input pins. Figure 7.3 shows the startup timing sequence of BOOT.

The 0.6V hysteresis (V_{BOOT_HYS}) on BOOT ULVO protections is provided to prevent chatter noise from V_{BOOT} supply and allow small drops in supply power which are usually happened in startup.

A not less than 100nF ceramic capacitor must be used between V_{DDH} and SW to normally operate.

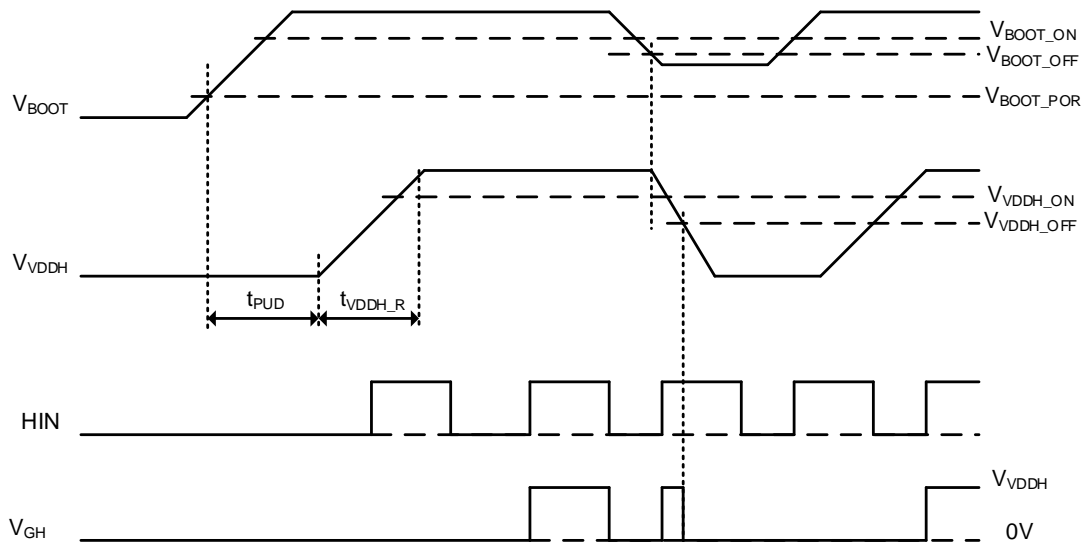


Figure 7.3 V_{BOOT} UVLO Diagram

8. Application Note

8.1. Typical Application Circuit

The circuit shows a typical half-bridge configuration by using the NSG65N15K.

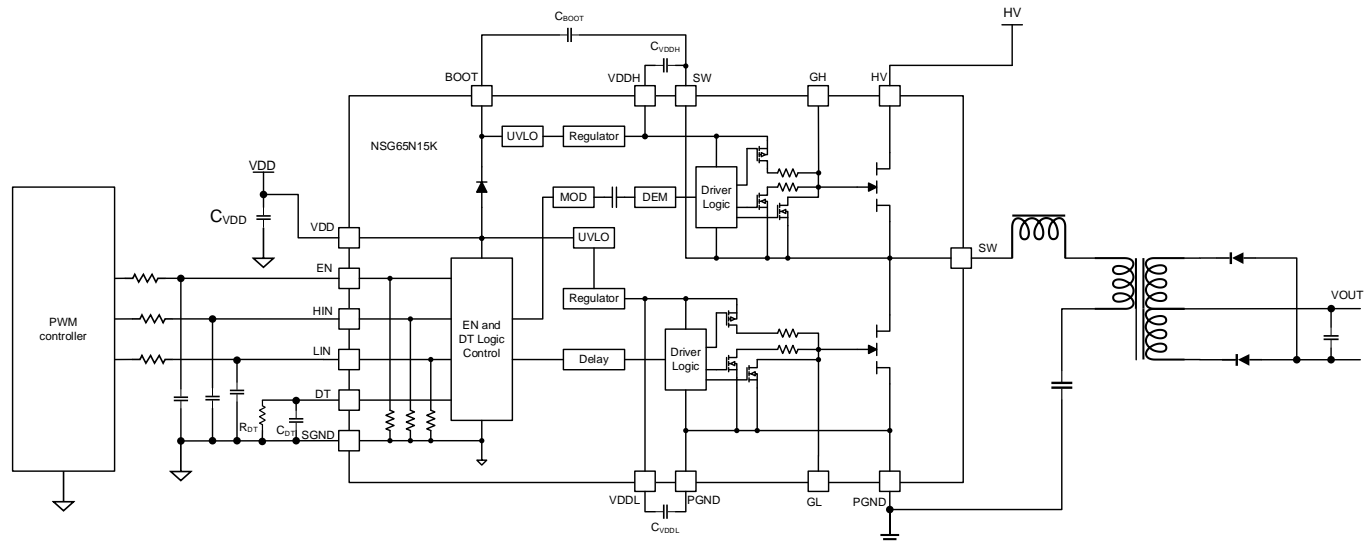


Figure 8.1 Typical Half-Bridge Application Schematic

Supply voltage (VDD): VDD is the low side power supply of NS65N5K. It provides the power for digital inputs, internal logic functions and the internal low-side regulator (VDDL). A single VDD bypass capacitor, C_{VDD} , is required and connected directly between the VDD and SGND pins. The C_{VDD} capacitor should be a ceramic bypass capacitor > 100 nF, located as close as possible to the VDD and SGND pins to properly filter out all glitches while switching.

High-Side Bootstrap Voltage (BOOT): BOOT is the high side gate driver power supply of NSG65N15K. The BOOT voltage is input to an internal regulator which produces the VDDH voltage. The BOOT diode has been integrated in NSG65N15K. The bootstrap capacitor C_{BOOT} connected directly between BOOT and pin21 which is SW. The capacitor C_{BOOT} should be a ceramic capacitor and located as close as possible to the BOOT and SW pins to properly filter out all glitches while switching. The value of C_{BOOT} should be large to provide fully charge for high side normal operation. High side pulses are not produced when the voltage on BOOT pin is less than its UVLO voltage.

Low Side Regulator (VDDL): VDDL is the low side regulator output. The VDDL regulator is fed directly from VDD and directedly provide the drive voltage and current for low side GaN HEMT. The VDDL regulator is referenced to the ground (PGND) pin. Source current for the low-side GaN HEMT is provided from the charge stored in the capacitor C_{VDDL} connected between VDDL and GND. A not less than 100nF ceramic capacitor C_{VDDL} must be connected between VDDL and pin3 which is PGND. The VDDL regulator will not output when VDD voltage is less than its UVLO voltage. When the VDDL voltage is higher than 4.4V which is UVLO turn-on threshold (V_{VDDL_ON}), the output enables; When the VDDL voltage is lower than 4.1V which is UVLO turn-off threshold (V_{VDDL_OFF}), GL outputs low level.

High Side Regulator (VDDH): VDDH is the high side regulator output. The VDDH regulator is fed directly from BOOT and directedly provide the drive voltage and current for high side GaN HEMT. The VDDH regulator is referenced switching node (SW) pin. Source current for the high side GaN HEMT is provided from the charge stored in the capacitor C_{VDDH} connected between VDDH and pin21 which is SW. A not less than 100nF ceramic capacitor C_{VDDH} must be connected between VDDH and SW pins. The VDDH regulator will not output when BOOT voltage is lower than its UVLO voltage. When the VDDH voltage is higher than 4.4V which is its UVLO turn-on threshold (V_{VDDH_ON}), the output enables; When the VDDH voltage is lower than 4.1V which is its UVLO turn-off threshold (V_{VDDH_OFF}), GL outputs low level.

Signal Ground (SGND) and Power Ground (PGND): SGND is the GND for all internal control logic and digital inputs. Internally, the SGND and PGND pins are isolated from each other. PGND is the return reference of the low side gate drive and VDDL. C_{VDDL} should be referenced to the PGND but separate from the power stage ground as shown in Figure 8.1.

The NSG65N15K low side drive circuit is able to withstand -5 V to $+5\text{ V}$ of common mode voltage between SGND and PGND. If the common mode voltage is over the range, NSG65N15K may be damaged. In practical application, SGND and PGND should be connected together with a low impedance resistor or with a short low impedance trace on the PCB.

Switch Node (SW): SW is the return reference of high side gate drive. C_{VDDH} and C_{BST} should be referenced to the SW pin but separate from the power stage switch node as shown in Figure. 8.1 .

Input (LIN, HIN): LIN and HIN are the PWM signal input pins. Both inputs are independent and internally pulled low to SGND such that each output is defaulted to be low. The input is compatible with Transistor-Transistor Logic (TTL).

Enable (EN): Enable (EN) is internally pulled low to SGND so that the driver is defaulted to a disabled output status. EN voltage is above 2.5V , enables the outputs. EN can be controlled by digital signal or connected directly VDD. If EN is pulled low during normal operation, the driver outputs are immediately disabled.

Deadtime (DT): A resistor R_{DT} should be connected between DT and SGND pins in order to configure the deadtime. The recommended value of R_{DT} is less than $14\text{k}\Omega$ or between $140\text{k}\Omega$ and $200\text{k}\Omega$. It is also recommended to parallel a ceramic capacitor, for example 1nF , with R_{DT} to achieve better noise immunity.

High Side Gate Output (GH): GH is the gate of the high side GaN HEMT. If the oscillations happened on GH, a resistor and capacitor series branch can be connected in parallel between GH and SW pin. The value of resistor can be from 0 to 10Ω .

Ligh Side Gate Output (GL): GL is the gate of the low side GaN HEMT. If the oscillations happened on GL, a resistor and capacitor series branch can be connected in parallel between GL and PGND pin. The value of resistor can be from 0 to 10Ω .

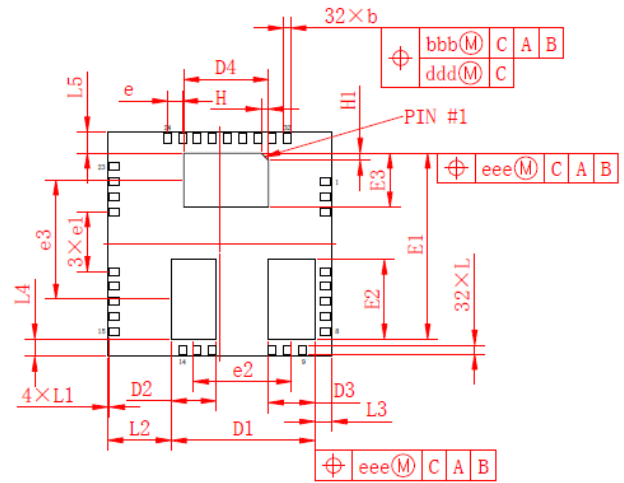
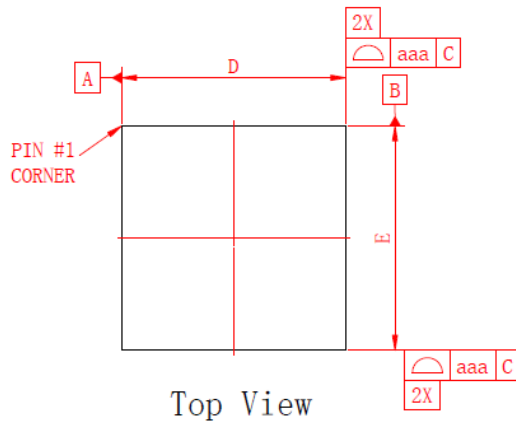
High Voltage (HV): HV is the Drain of the high side GaN HEMT.

8.2. Layout Recommendations

PCB layout is important to get optimal performance. Some of the layout guidelines to be followed are listed below:

- 1) The bypass capacitors connected on VDD, EN, DT and BOOT should be placed as close to their respective pins as possible.
- 2) A not less than 100nF MLCC capacitor should be placed between VDDL and pin3 which is PGND. It should be placed as close to VDDL as possible.
- 3) A not less than 100nF MLCC capacitor should be placed between VDDH and pin21 which is SW. It should be placed as close to VDDH as possible.
- 4) It is able to withstand -5 V to $+5\text{ V}$ of common mode voltage between SGND and PGND. If the common mode voltage is over the range, NSG65N15K may be damaged. In practical application, SGND and PGND must be connected together with a low impedance resistor or with a short low impedance trace on the PCB.

9. Package Information



symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.675	0.725	0.775	0.027	0.029	0.031
c	0.195	0.225	0.255	0.008	0.009	0.010
D	8.900	9.000	9.100	0.350	0.354	0.358
E	8.900	9.000	9.100	0.350	0.354	0.358
D1	5.660	5.760	5.860	0.223	0.227	0.231
E1	7.360	7.460	7.560	0.290	0.294	0.298
D2	1.725	1.800	1.875	0.068	0.071	0.074
D3	1.785	1.860	1.935	0.070	0.073	0.076
D4	3.325	3.400	3.475	0.131	0.134	0.137
E2	3.125	3.200	3.275	0.123	0.126	0.129
E3	2.085	2.160	2.235	0.082	0.085	0.088
H	---	0.300	---	---	0.012	---
H1	---	0.300	---	---	0.012	---
L	0.300	0.375	0.450	0.012	0.015	0.018
L1	0.000	0.075	0.150	0.000	0.003	0.006
L2	2.475	2.550	2.625	0.097	0.100	0.103
L3	0.615	0.690	0.765	0.024	0.027	0.030
L4	0.615	0.690	0.765	0.024	0.027	0.030
L5	0.775	0.850	0.925	0.031	0.033	0.036
e	---	0.600	---	---	0.024	---
e1	---	2.400	---	---	0.094	---
e2	---	3.930	---	---	0.155	---
e3	---	4.780	---	---	0.188	---
b	0.250	0.300	0.350	0.010	0.012	0.014
aaa		0.100			0.004	
bbb		0.150			0.006	
ccc		0.100			0.004	
ddd		0.080			0.003	
eee		0.150			0.006	

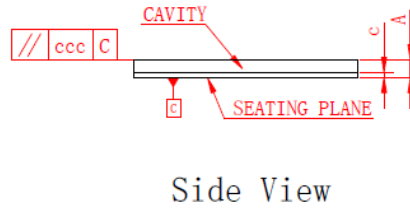


Figure. 9.1 Package Shape and Dimension

10. Ordering Information

Part No.	Temperature	Auto-motive	Package Type	MSL	SPQ
NSG65N15K-DQAFR	-40 to 125°C	NO	QFN	3	1000

11. Tape and Reel Information

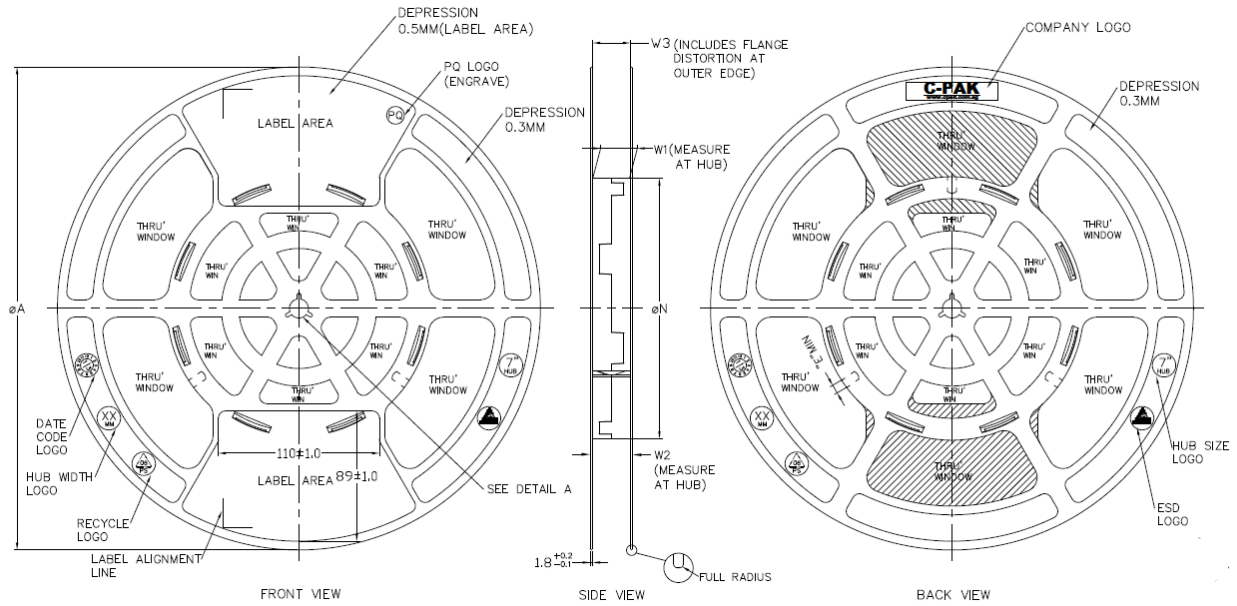


Figure. 11.1 Tape Information

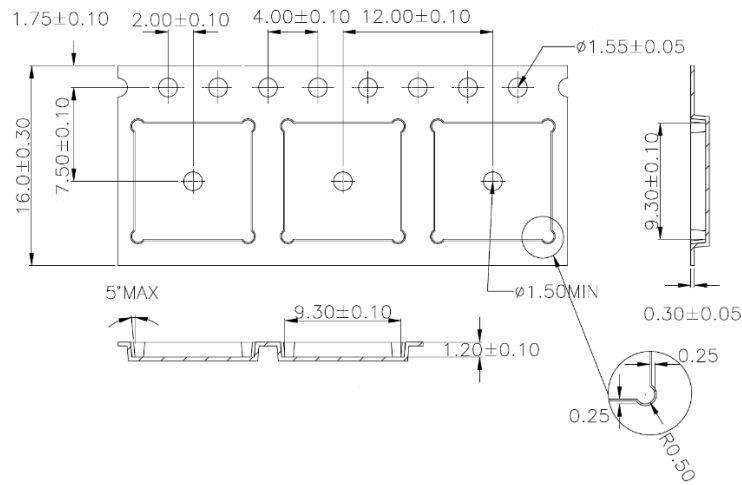


Figure. 11.2 Reel Information

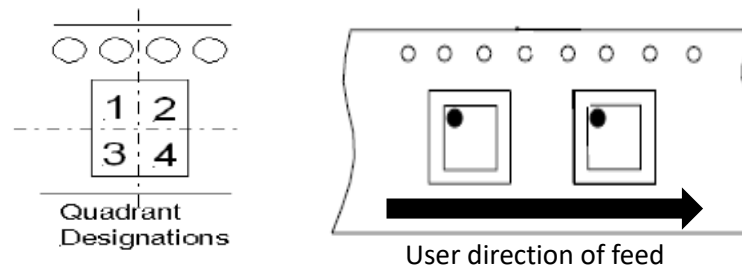


Figure. 11.3 Quadrant Designation for Pin1 Orientation in Tape

12.Revision History

Revision	Description	Date
1.0	Initial internal version	2025/05/29

IMPORTANT NOTICE

The information given in this document (the “Document”) shall in no event be regarded as any warranty or authorization of, express or implied, including but not limited to accuracy, completeness, merchantability, fitness for a particular purpose or infringement of any third party’s intellectual property rights.

Users of this Document shall be solely responsible for the use of NOVOSENSE’s products and applications, and for the safety thereof. Users shall comply with all laws, regulations and requirements related to NOVOSENSE’s products and applications, although information or support related to any application may still be provided by NOVOSENSE.

This Document is provided on an “AS IS” basis, and is intended only for skilled developers designing with NOVOSENSE’s products. NOVOSENSE reserves the rights to make corrections, modifications, enhancements, improvements or other changes to the products and services provided without notice. NOVOSENSE authorizes users to use this Document exclusively for the development of relevant applications or systems designed to integrate NOVOSENSE’s products. No license to any intellectual property rights of NOVOSENSE is granted by implication or otherwise. Using this Document for any other purpose, or any unauthorized reproduction or display of this Document is strictly prohibited. In no event shall NOVOSENSE be liable for any claims, damages, costs, losses or liabilities arising out of or in connection with this Document or the use of this Document.

For further information on applications, products and technologies, please contact NOVOSENSE (www.novosns.com).

Suzhou NOVOSENSE Microelectronics Co., Ltd