NOVOSENSE

NSD7314
Brushed DC Motor Driver Single H-Bridge / Two Half Bridge

Datasheet (EN) 1.0

Product Overview

The device NSD7314 is a brushed-DC motor H-bridge driver for wide range automotive applications including VCU/OBC charger inlet locking, door lock actuator and industrial market like robotics or other small machines application.

Two logic inputs control the H-bridge driver consisted of four N-channel MOSFETs. The device can control motors bidirectionally with up to 6A peak current. The input can be PWM modulated to control motor speed using current chopping method. The device enters sleep mode with low quiescent with nSLEEP input low.

The device is integrated with current chopping regulation, based on an external reference VREF input and the voltage on the IPROBE pin, which is proportional to current flowing through the motor and an external resistor. The current chopping function limits the peak current to a known level especially during motor startup and stall condition.

The device is also fully protected from faults and short circuits, including undervoltage, overcurrent and overtemperature. Also, it provides dedicated nFAULT pin to indicate fault state and alert to the microcontroller.

Applications

- Robotics & Industrial Equipment
- Door Lock actuator
- VCU/OBC charger inlet locking

Device Information

Part Number	Package	Body Size
NSD7314-DHTSPR	HTSSOP16	5mm × 4.4mm
NSD7314-Q1HTSPR	HTSSOP16	5mm × 4.4mm

Key Features

- Single H-Bridge motor driver or two half bridge
- Wide 4.5-V to 36-V operating voltage
- 6A peak / 2.5A continuous current drive
- Flexible driving strategy via configurable control interface pin (INMODE)
  - H-bridge control by IN1&IN2 as two PWM or EN&PH (1x PWM / 1x DIR IO)
  - Independent half bridge control by IN1, IN2
- Integrated current sense with IPROBE output
- Internal current regulation for load with inrush current
- Selectable current limitation mode & OCP action (CLMODE)
  - Cycle by cycle or fixed-off time
  - OCP auto retry or OCP latch off
- Low-Power sleep mode
- Integrated spread spectrum for low EMI
- 16-Pin HTSSOP 5mm X 4.4mm with exposed PAD
- Integrated protection features
  - VM undervoltage lockout (UVLO)
  - Overcurrent protection (OCP)
  - Thermal shutdown (TSD)
  - Fault indicating (nFAULT)
- Industrial grade (NSD7314)
- AEC-Q100 Compliance (NSD7314-Q1)

Functional Block Diagrams

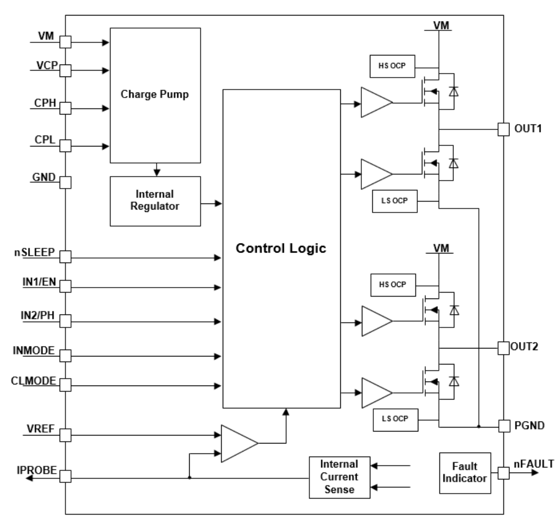


Figure 1. NSD7314 Block Diagram

Index

1. Pin Configuration and Functions

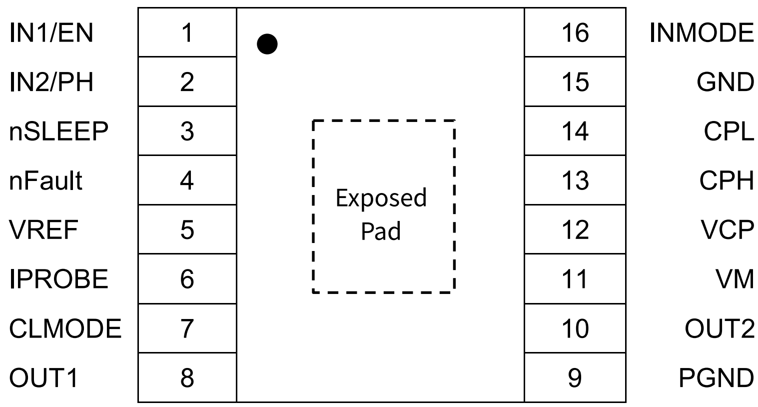


Figure 1.1. NSD7314 Pinout (top view)

Table 1.1 NSD7314 Pin Configuration and Description

Symbol	No	Type	Description
IN1/EN	1	I	Logic inputs 1. Controls the H-bridge output. Has internal pull downs. IN1 can work as PWM input when INMODE is logic low during power up.
IN2/PH	2	I	Logic inputs 2. Controls the H-bridge output. Has internal pull downs. IN2 can work as PHASE DIR input when INMODE is logic low during power up.
nSLEEP	3	I	Driver enable input pin with internal pull down (active HIGH). If nSLEEP input pin is pulled low, all OUTx go to tri-state and device move to low-power sleep state.
nFAULT	4	O	Open-drain output for fault indication. Pull low when fault (OCP, OT, VUVLO) happens. Connect external pull up resistor, typ. 4.7k/10k.
VREF	5	I	Analog input. Apply a voltage between 0.3 to 3.6 V.
IPROBE	6	O	Current feedback output pin, Put external resistor on this pin to ground. See application information section for resistor value selection.
CLMODE(1)	7	I	Current regulation mode selection pin.
OUT1	8	O	H-bridge output1 pin. Connect directly to the motor or other inductive load.
PGND	9	PWR	High-current ground path. Connect PGND directly to board ground.
OUT2	10	O	H-bridge output2 pin. Connect directly to the motor or other inductive load.
VM	11	PWR	5V to 36V power supply. Connect a 0.1-μF bypass capacitor to ground, as well as sufficient bulk capacitor needs to guarantee VM pin voltage in maximum range.
VCP	12	PWR	Charge pump output. Put 100nF X7R capacitor between VCP and VM pins.
CPH	13	PWR	Charge pump high side pin, connect a 22nF X7R capacitor between CPH and CPL pins.

CPL	14	PWR	Charge pump low side pin, connect a 22nF X7R capacitor between CPH and CPL pins.
GND	15	PWR	Logic ground. Connect to board ground
INMODE(1)	16	I	IN1, IN2 operation mode selection pin.
Exposed PAD	—		Exposed pad. Connect to board ground. For good thermal dissipation, use large ground planes on multiple layers, and multiple nearby vias connecting those planes.

(1) The logic status of CLMODE pin & INMODE pin configuration are recognized and latched during device power up or nsleep pin logic low to high.

2. Absolute Maximum Rating

Items	Min	Max	Unit
Power supply voltage (VM)	–0.3	40	V
Charge pump pin (CPH, VCP)	VM – 0.3	VM+7	V
Charge pump pin low side (CPL)	–0.3	7	V
Logic input voltage (IN1/EN, IN2/PH, CLMODE, INMODE, nSLEEP)	–0.3	6	V
VREF input pin (VREF)	–0.3	6	V
Fault output pin (nFAULT)	–0.3	6	V
Current feedback output voltage (IPROBE)	–0.3	6	V
Continuous phase node pin voltage (OUT1, OUT2)	–0.7	VM + 0.7	V
Voltage difference between ground pins (PGND vs. GND)	–0.3	0.3	V

3. ESD Ratings

Symbol	Description	Value	Unit
VESD_HBM	Human Body Model (HBM), VM & OUTx pins per ANSI/ESDA/JEDEC JS-001	±4000	V
	Human Body Model (HBM), other pins per ANSI/ESDA/JEDEC JS-001	±2000	V
VESD_CDM	Charged device model (CDM), Corner pins, per JEDEC specification JS-002	±750	V
	Charged device model (CDM), other pins, per JEDEC specification JS-002	±500	V

4. Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
VM	VM Power supply voltage	4.5		36	V
V_{OD}	nFAULT output voltage range	0		5	V
I_{OD}	nFAULT open drain load current	0		5	mA
VREF	VREF input voltage range	0.3		3.6	V
$V_{IN1/EN, IN2/PH}$	Logic input voltage (IN1/EN, IN2/PH)	0		5	V
fpwm	Logic input PWM frequency (IN1/EN, IN2/PH)	0		100	kHz
Imax	Max output current (1)	0		6	A

(1) When the maximum allowable output load current is considered during application scenario, both power dissipation and thermal condition, including ambient temperature, application board thermal condition etc., shall also be evaluated.

5. Thermal Information

Symbol	Description	Min	Typ	Max	Unit
Ta	Ambient operating ambient temperature	-40		125	°C
Tj	Junction temperature	-40		150	°C
Tstg	Storage temperature	-65		150	°C
Rthjc	Thermal resistance, junction to case bottom		2.7		°C/W
Rthja	Thermal resistance, junction to ambient, on 1S0P PCB based on JEDEC standard		62		°C/W
	Thermal resistance, junction to ambient, on 2S2P (4-layer) PCB based on JEDEC standard		35		°C/W

6. Electrical Characteristics

Valid for industrial version at T_a = 25°C, VM=4.5 to 36V and for automotive version at T_a = -40 to 125°C, VM=4.5 to 36V, unless otherwise specified

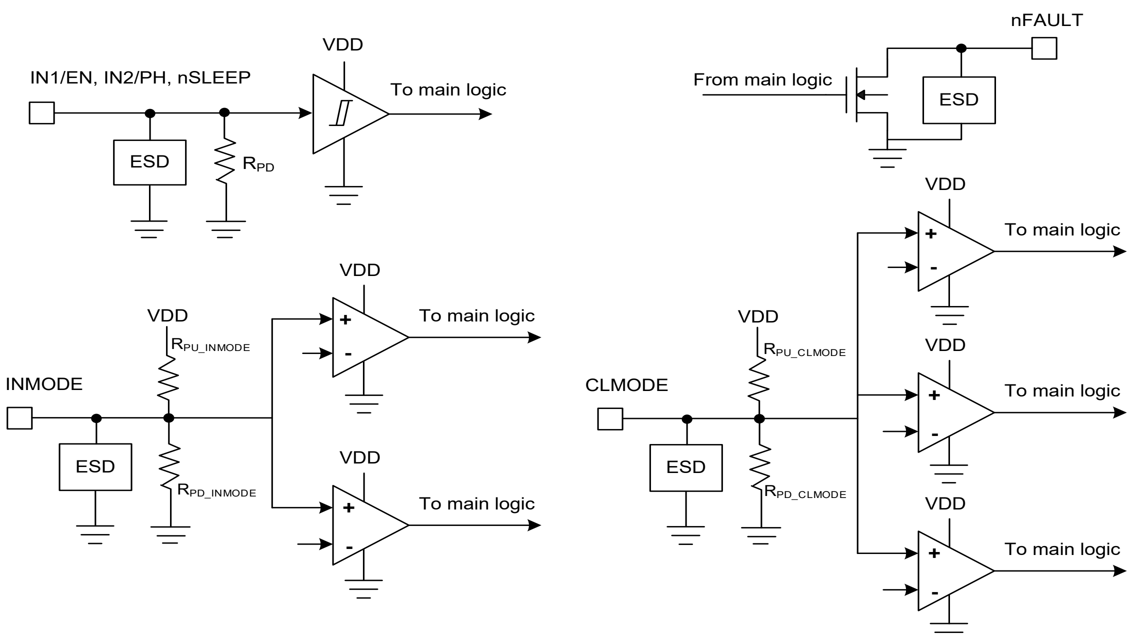
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
POWER SUPPLY (VM)						
VM	VM operating voltage		4.5		36	V
I_{VM}	VM operating supply current	VM = 12 V, nSLEEP = 5V, IN1/EN = IN2/PH = 0V		3	7	mA
I_{VM_SLEEP}	VM sleep current	VM = 12 V, nSLEEP = 0V, T_a = 25°C		1	3	µA
		VM = 12 V, nSLEEP = 0V, T_a = 125°C		3	30	µA
t_{SLEEP}	Turn-off time	nSLEEP = 0V to low power sleep mode			1	ms
t_{WAKE}	Turn-on time	nSLEEP = 5V to active when VM > V_{UVLO}			1	ms
CHARGE PUMP (VCP)						
V_{CP}	Charge pump regulator voltage			5		V
f_{CP}	Charge pump switching frequency			400		kHz
V_{CP_UV}	Charge pump undervoltage			3		V
LOGIC CONTROL INPUT (IN1/EN, IN2/PH, nSLEEP)						
V_{IL}	Input logic low voltage				0.5	V

V_{IH}	Input logic high voltage		1.8			V
V_{HYS}	Input logic hysteresis			0.2		V
I_{IL}	Input logic low current	VIN = 0 V	-5		5	μA
I_{IH}	Input logic high current	VIN = 5 V		50	75	μA
R_{PD}	Pulldown resistance	to GND		100		kΩ
INPUT OPERATION MODE CONTROL PIN (INMODE)						
V_{IL_INMODE}	Tri-level input logic voltage		0		0.65	V
V_{HIZ_INMODE}	Tri-level input Hi-Z voltage		0.9	1.1	1.2	V
V_{IH_INMODE}	Tri-level input logic high		1.5		5.5	V
I_{IL_INMODE}	Input mode low logic current	V_I = 0V	-50	-32		μA
I_{HIZ_INMODE}	Input mode high impedance mode current	V_I = 1.1V	-10		10	μA
I_{IH_INMODE}	Input mode high logic current	V_I = 5V		113	150	μA
R_{PD_INMODE}	Input mode pull down resistance	To GND		44		kΩ
R_{PU_INMODE}	Input mode pull up resistance	To internal generated 5V		156		kΩ
CURRENT LIMITATION MODE CONTROL PIN (CLMODE)						
V_{CLM1}	Input level 1	Voltage to set level 1 (CLMODE pin short to GND)	0		0.45	V
R_{CLM2}	Input level 2	Resistance to GND to set level 2		20		kΩ
R_{CLM3}	Input level 3	Resistance to GND to set level 3		62		kΩ
V_{CLM4}	Input level 4	Voltage to set level 4 (CLMODE pin floating or HIZ)	2.5		5.5	V
R_{PD_CLMODE}	CLMODE pull down resistance	To GND		136		kΩ
R_{PU_CLMODE}	CLMODE pull up resistance	To internal generated 5V		68		kΩ
H-BRIDGE OUTPUTS (OUT1, OUT2)						
$R_{DS(ON)}$	OUT1, OUT2 High-side FET on resistance	VM = 12 V, I = 2 A, Ta= 25°c		120	160	mΩ
		VM = 12 V, I = 2 A, Ta= 125°c		180	240	mΩ

$R_{DS(ON)}$	OUT1, OUT2 Low-side FET on resistance	VM = 12 V, I = 2 A, Ta= 25°c		100	135	mΩ
		VM = 12 V, I = 2 A, Ta= 125°c		150	200	mΩ
t_{RISE}	Output rise timing	VM = 12 V, OUT rising 10% to 90% Automotive version		600		ns
		VM = 12 V, OUT rising 10% to 90% Industrial version		150		ns
t_{FALL}	Output fall timing	VM = 12 V, OUT rising 10% to 90% Automotive version		600		ns
		VM = 12 V, OUT rising 10% to 90% Industrial version		150		ns
t_{DEAD}	Output dead time	Automotive version		750		ns
		Industrial version		150		ns
t_{PD}	Propagation delay	INx to OUTx change, automotive version		1.6		μs
		INx to OUTx change, industrial version		0.5		μs
V_d	Body diode forward voltage	IOUT = 1 A		0.8		V
CURRENT SENSE & REGULATION						
A_{IPROBE}	Current mirror scaling factor			0.45		mA/A
A_{ERR}	Current mirror scaling error	IOUT < 0.4A	-30		30	mA
		0.4A ≤ IOUT < 1A	-7.5		7.5	%
		1A ≤ IOUT < 2A	-6		6	%
		2A ≤ IOUT ≤ 4A	-5.5		5.5	%
t_{DELAY}	Current sense delay timing	Automotive version		6		μs
		Industrial version		3.6		μs
t_{OFF}	PWM off timing			25		μs
t_{BLANK}	PWM blanking time	Automotive version		2.7		μs
		Industrial version		2		μs
t_{DEG}	Current regulation deglitch timing	Automotive version		1.7		μs
		Industrial version		0.6		μs
PROTECTION						
V_{UVLO}		VM falls until UV triggers	4	4.25		V

	VM undervoltage protection	VM rises until operation recovers		4.4	4.7	V
V_{UVLO_HYS}	VM undervoltage hysteresis			150		mV
t_{UVLO}	VM undervoltage deglitch time			10		μs
I_{OCP}	Overcurrent protection threshold		6	10		A
t_{OCP}	Overcurrent deglitch time			3		μs
t_{RETRY}	Overcurrent retry time			2		ms
T_{SD}	Thermal shutdown temperature	Guaranteed by design	150	170	190	°C
T_{HYS}	Thermal shutdown hysteresis			20		°C
nFAULT OPEN DRAIN OUTPUT						
I_{OH}	Output high leakage current	V_{OD} = 5V			1	μA
V_{OL}	Output low voltage	Input current 5mA			0.5	V

7. Logic Input Pins Block Diagram



8. Functional Description

8.1. H-Bridge / Half Bridge Operation

The NSD7314 offers three modes to support a single bidirectional BDC motor, two unidirectional BDC motor, or other output loads with INx pins different control input scenario. The three control modes are determined according by the state of INMODE pin, either logic low, high impedance or logic high as **Table 8.1** shown. It is latched during device powered up and enabled by the nSLEEP pin.

Table 8.1 H-bridge / Half bridge Operation vs. INMODE pin

INMODE Pin Status	Operation Mode
INMODE = floating / High Z	Independent half bridge operation control by IN1, IN2
INMODE = High	H-bridge operation, IN1, IN2 both PWM input
INMODE = Low	H-bridge operation, IN1/EN as PWM input, IN2/PH as direction signal, generic IO input

The two logic input pins, IN1/EN and IN2/PH, are internally pulled down and able to receive up to max 100kHz PWM signal, for controlling the internal integrated output stage to support motor operation in different states (forward drive, reverse drive, slow decay, fast decay) as below **Figure 8.1**

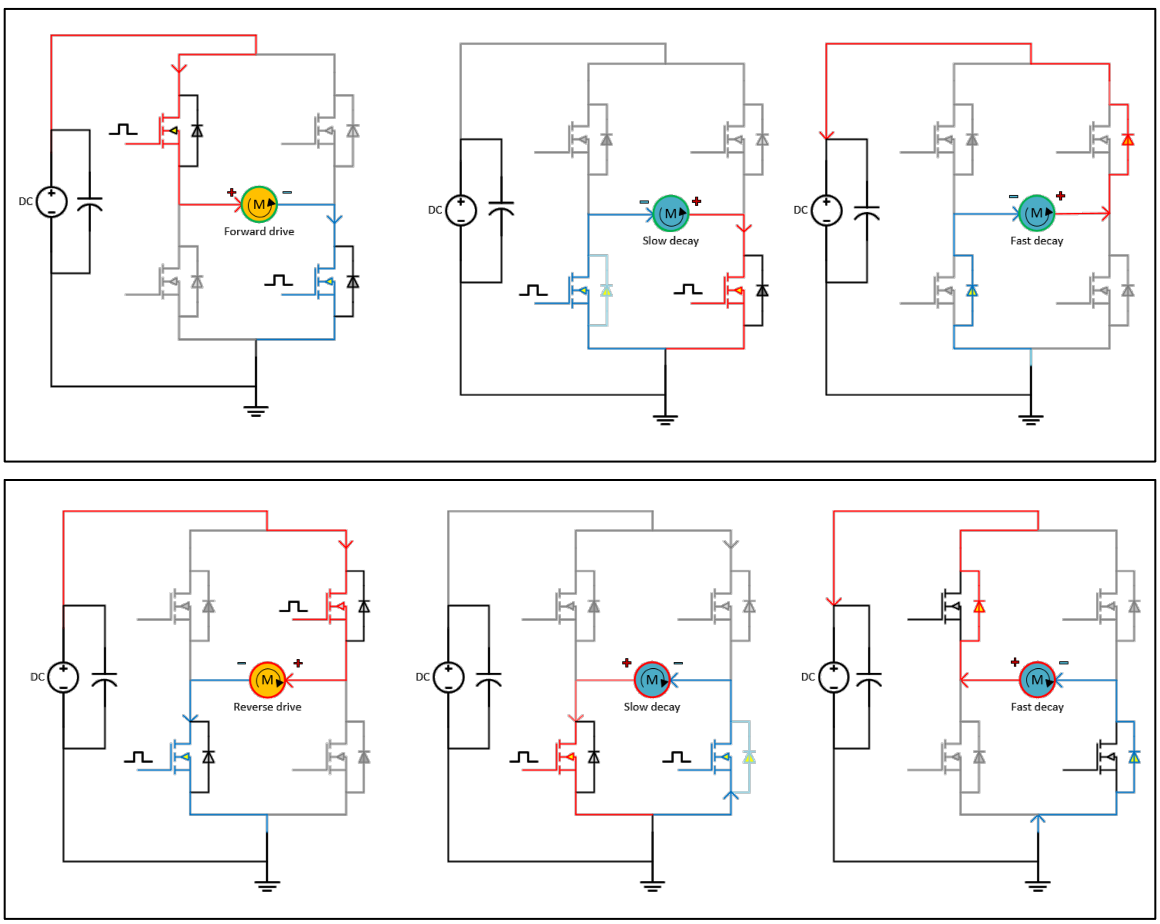


Figure 8.1 High side/low side activation in forward/reverse/slow decay/fast decay

Additionally, an internal dead-time t_{DEAD} is implemented between internal high side and low side switching to avoid cross conduction.

8.1.1. H-Bridge IN1&IN2 PWM Mode (INMODE = High)

When the INMODE pin is logic high and latched after power up, the device works in H-bridge operation, which allows one of input pin (IN1 or IN2) to be used as PWM input, and the other pin always be logic high when we want to drive the moto at a specified speed. The truth table for IN1&IN2 PWM mode is shown in **Table 8.2.**

Table 8.2 IN1&IN2 PWM Control Mode

nSLEEP	IN1	IN2	OUT1	OUT2	Function
0	X	X	High Z	High Z	Sleep
1	0	0	High Z	High Z	Fast decay
1	0	1	L	H	Reverse (OUT2 -> OUT1)
1	1	0	H	L	Forward (OUT1 -> OUT2)
1	1	1	L	L	Low Side slow decay

8.1.2.H-Bridge EN/PH Mode (INMODE = Low)

When the INMODE pin is logic low and latched after power up, the device works in EN/PH mode, which allows IN1/EN to be used as PWM input, IN2/PH as direction signal. It saves one PWM output of microcontroller. The truth table for EN/PH mode is shown in **Table 8.3**.

Table 8.3. EN/PH Control Mode

nSLEEP	IN1/EN	IN2/PH	OUT1	OUT2	Function
0	X	X	High Z	High Z	Sleep
1	0	X	L	L	Low Side Slow Decay
1	1	0	L	H	Reverse (OUT2 -> OUT1)
1	1	1	H	L	Forward (OUT1 -> OUT2)

8.1.3.Independent Half Bridge Mode (INMODE = High Z)

When the INMODE pin is floating and in high impedance after power up, the device works in independent half bridge mode. It allows input pin to control the half bridge output (IN1-> OUT1 or IN2->OUT2) directly. The truth table for independent half bridge mode is shown in **Table 8.4**.

Table 8.4. Independent Half Bridge Control Mode

nSLEEP	INx	OUTx	Function
0	X	High Z	Sleep
1	0	L	OUTx Low Side On
1	1	H	OUTx High Side On

8.2. Current Sense and IPROBE Pin

The IPROBE pin is the scaling output of load current measured by internal current mirror. The shunt-less monitoring technique senses the current flowing through low side drain to source, while the current from source to drain of that channel during slow decay or fast decay is considered as zero.

$$I_{IPROBE} = AIPROBE * (I_{LS1} + I_{LS2})$$

Note:

- If forward / reverse / slow decay in H-bridge IN1/IN2 PWM or EN/PH mode, the current output of the IPROBE pin is proportional to the current with the direction from drain to source in one of the low side mosfet.
- Considering independent half bridge mode, if both low side MOSETs are turning on at the same time, the IPROBE pin shows the sum of the current for low side MOSFET.

The corresponding IPROBE pin voltage V_{IPROBE} can be calculated using I_{IPROBE} and external resistor R_{IPROBE} placed on IPROBE pin to ground.

$$V_{IPROBE} = I_{IPROBE} * R_{IPROBE}$$

The IPROBE pin voltage is generally connected to ADC input of the microcontroller, with the proper external resistor RIPROBE selection, the system can monitor the load current simultaneously. Additionally, NSD7314 integrates an internal clamping circuit on IPROBE pin to limit V_{IPROBE} voltage level and avoid overstressing ADC input of microcontroller, incase external resistor connection is broken, or unexpected high current happens.

Starting from output HIZ to forward or reverse state, the V_{IPROBE} output is delayed from the low-side MOSFET enable command by the sense delay time (t_{DELAY}) as **Figure 8.2** shown. This time is the delay considering low-side MOSFET switch on and the corresponding internal current sensing output being ready. If the device is alternating between drive and slow-decay in H-bridge operation state, then there is one low-side MOSFET sensing the current always on and the sense delay time has no impact to the following IPROBE output. However, changing the direction of driving will cause the current sensing MOSFET switching and the t_{DELAY} re-enable on IPROBE.

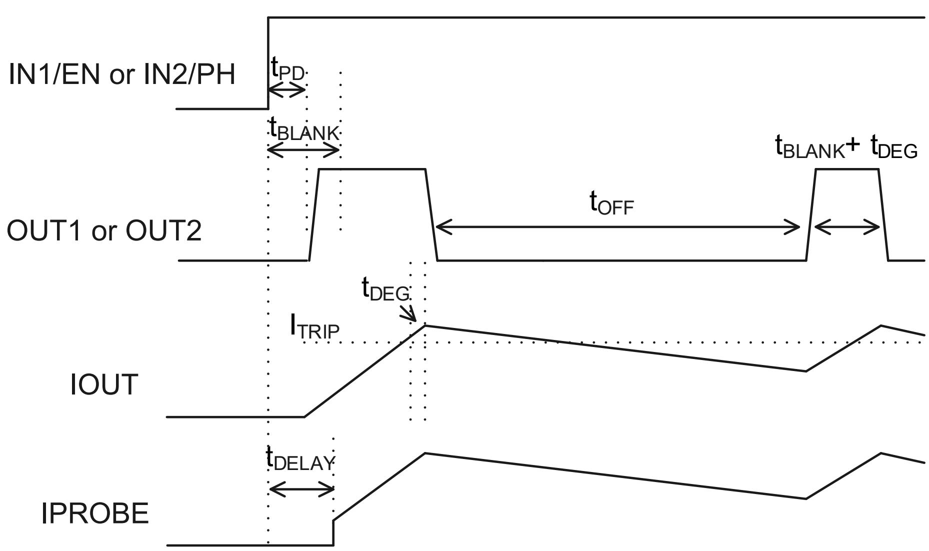


Figure 8.2 Power stage & current sense output timing

If the command on INx pin targets to disable the current sensing low side MOSFET, even the load current may be not zero during MOSFET turn off process, the IPROBE output still turns off immediately along with the input signal.

8.3. Current Regulation/Limitation and VREF, CLMODE Pin

Together with the external VREF input, the current regulation level I_{TRIP} is set according to the external VREF input vs. V_{IPROBE}.

$$I_{TRIP} = \frac{V_{REF}}{AIPROBE * R_{IPROBE}} = \frac{V_{REF}}{0.45mA/A * R_{IPROBE}\ (kohm)}$$

The current regulation function is realized by an internal comparator. When the ITRIP is exceeded (V_{IPROBE} greater than VREF), the comparator output will change and drive OUT1/OUT2 power stage to slow decay operation state for reducing the load current. Additionally, the comparator output will be ignored at the beginning of PWM transition and filtered after ITRIP exceeded; the two timings, t_{BLANK} and t_{DEG}, avoid false sense overcurrent events due to motors or systems capacitance.

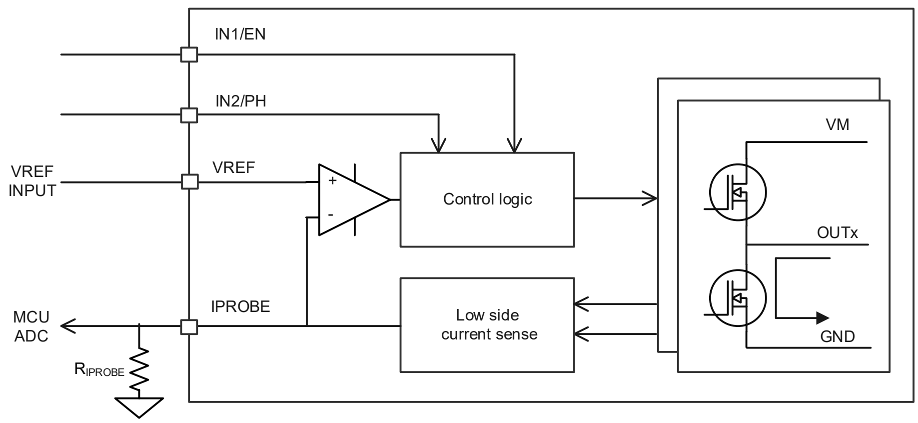


Figure 8.3 Current sense & internal regulation scheme

Regarding the current regulation mode, fixed off-time or cycle-by-cycle, it is selected through CLMODE pin. In application, the CLMODE pin can leave as floating, directly connecting to GND or placing resistor between CLMODE and GND. Similar as INMODE pin, the CLMODE pin status is latched during device enabled by nSLEEP pin. Besides current regulation mode, CLMODE pin also determines the OCP and nFault response. **Table 8.5** shows the summary of function related to CLMODE pin.

Table 8.5 Function Related to CLMODE Pin

CLMODE Pin Status	Current Regulation Mode	Overcurrent response	nFAULT response
CLMODE = floating / High Z	Fixed Off-Time	Latched off	OCP only
CLMODE = 62 kΩ to GND	Cycle-By-Cycle	Latched off	OCP and current regulation
CLMODE = 20 kΩ to GND	Cycle-By-Cycle	Auto retry	OCP and current regulation
CLMODE directly to GND	Fixed Off-Time	Auto retry	OCP only

8.3.1.Fixed Off-Time Current Regulation (CLMODE = GND or Floating)

In fixed off-time current regulation, it supports the control input pins IN1/EN and IN2/PH simple 100% DC high or low, while maintain load current in regulation level at the same time.

When the load current reaches the setting I_{TRIP}, even the input logic remains forward or reverse driving state, the internal regulation controller will automatically move the H-Bridge output to slow decay state by two internal low side MOSFET in ON state for fixed t_{OFF}. After t_{OFF} elapses, the H-bridge will return to driving state according to IN1/EN and IN2/PH pin states.

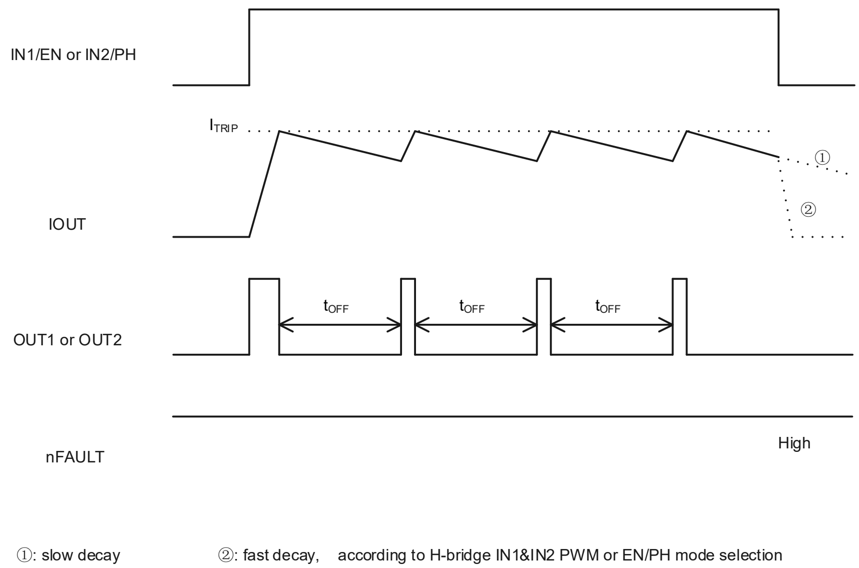


Figure 8.4 Fixed off-time current regulation scheme

8.3.2.Cycle-By-Cycle Current Regulation (CLMODE = 62kΩ or 20kΩ to GND)

In cycle-by-cycle current regulation mode, 100% DC high or low on control input pins is unavailable. Comparing with fixed off-time current regulation, it requires a new control input edge to re-enable the outputs in driving after the low-side slow decay state, so the off-timing in cycle-by-cycle also depends on the input PWM cycle by an external microcontroller, it is not fixed.

The H-bridge also enters low-side slow decay state (both low-side MOSFETs ON) after the load current exceeds I_{TRIP} in cycle-by-cycle mode, and the device additionally pull the nFAULT pin low whenever the H-bridge enters internal current regulation, while fixed off-time current regulation doesn't trigger nFAULT. This can be used to determine when the device outputs are different from the control inputs, or the load current reaches the I_{TRIP} threshold. This is shown in **Figure 8.5** as below. nFAULT will be released when the next control input edge is received.

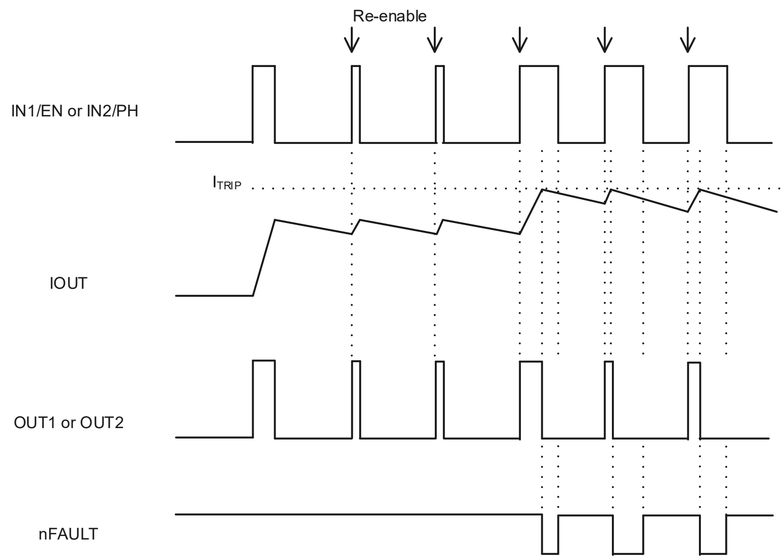


Figure 8.5. Cycle by cycle current regulation scheme

Note:

In half bridge mode, the current regulation function is disabled, neither fixed off-time nor cycle by cycle.

8.4. Low Power Sleep Mode & nSLEEP Pin

Low power sleep mode in NSD7314 is active when both nSLEEP keeps for low after 1ms (typ.) tsleep. It disables most internal circuits, including charge pump and control logic blocks etc., and reduces device current consumption.

When nSLEEP pins state moves to high and remains at least 100us, the device will start to exit from low power sleep mode. After 1ms (typ.) t_{WAKE} delay timing, OUT1 and OUT2 can be active in normal driving reverse / forward according to IN1/EN and IN2/PH inputs. Two mode control pin logic state, INMODE & CLMODE, are latched after t_{WAKE} timing finished. Any logical change of INMODE & CLMODE pins in normal working state is ignored.

8.5. Protection Function

8.5.1.VM Undervoltage Protection

When VM power supply pin voltage falls below the undervoltage low threshold (V_{UVLO}) over 10us typ. undervoltage deglitch time, OUT1 and OUT2 internal power stage MOSFETs are disabled and nFAULT pin are pulled LOW. When VM rise above the V_{UVLO}(HIGH), the device automatically resumes normal operation according to IN1/EN & IN2/PH pin status.

8.5.2.Charge Pump Undervoltage Protection

If the charge pump voltage on the VCP pin falls below the undervoltage threshold voltage (VCP_UV), all MOSFETs in output stage will be disabled and the nFAULT pin pulled low. Normal operation will be resumed when the VCP undervoltage condition disappears and VCP rises above the VCP_UV threshold.

8.5.3.Overcurrent Protection

The device integrates internal current monitor to against output load short, OUT1 / OUT2 pin short to battery or GND.

If one of these faults happens and internal sensed current > OCP threshold I_{OCP} for longer than t_{OCP}, all output MOSFET will be disabled for H-bridge working mode (INMODE = HIGH or LOW).

In the meantime, device provides two overcurrent protection recovery mechanism, auto-retry or fault latch, selected by CLMODE pin. For auto-retry, after H-bridge output MOSFET disabled for the duration t_{RETRY}, the device automatically re-enables and works according to the state of IN1/EN and IN2/PH pins. While OCP fault is still present, the protection and auto retry repeats; otherwise, the device moves to normal operation state. For OCP fault latch off, the H-bridge output keeps disable until device internal logic reset by nSLEEP LOW or power down / up on VM supply.

Note:

- In independent half bridge mode (INMODE=HIZ), one channel OCP fault only disables the corresponding output and drives nFAULT low, the other output continues normal operation.
- In independent half bridge mode (INMODE=HIZ) and auto-retry selected, if an overcurrent event occurs first in one half bridge, then later the other half bridge happens OCP during the first one t_{RETRY}, the retry timer of the first half bridge will be reset to t_{RETRY} and then both two half bridges are enabled again together after retry timer expires.

8.5.4. Overtemperature

If the device internal junction temperature over T_{SD} threshold, the internal MOSFET also will automatically be disabled. Normal operation will be resumed when internal junction temperature drops below T_{SD}-T_{HYS}

8.5.5. Fault Protection Summary

Fault	Condition	Output stage	nFAULT	Recovery procedure
VM undervoltage	VM < $V_{UVLO (LOW)}$	Disabled, HIZ	LOW	VM > $V_{UV (HIGH)}$
VCP undervoltage	VCP < V_{CP_UV}	Disabled, HIZ	LOW	VCP > V_{CP_UV}
OCP	I > I_{OCP}	Disabled, HIZ	LOW	Auto-retry with t_{RETRY} interval or latched off
Over temperature	T_J > T_{SD}	Disabled, HIZ	LOW	T_J < T_{SD} - T_{HYS}
Overload	I > I_{TRIP} in cycle by cycle	Slow decay, low side ON	LOW	Control Input New Edge

9. Application Information

9.1. Application Diagram

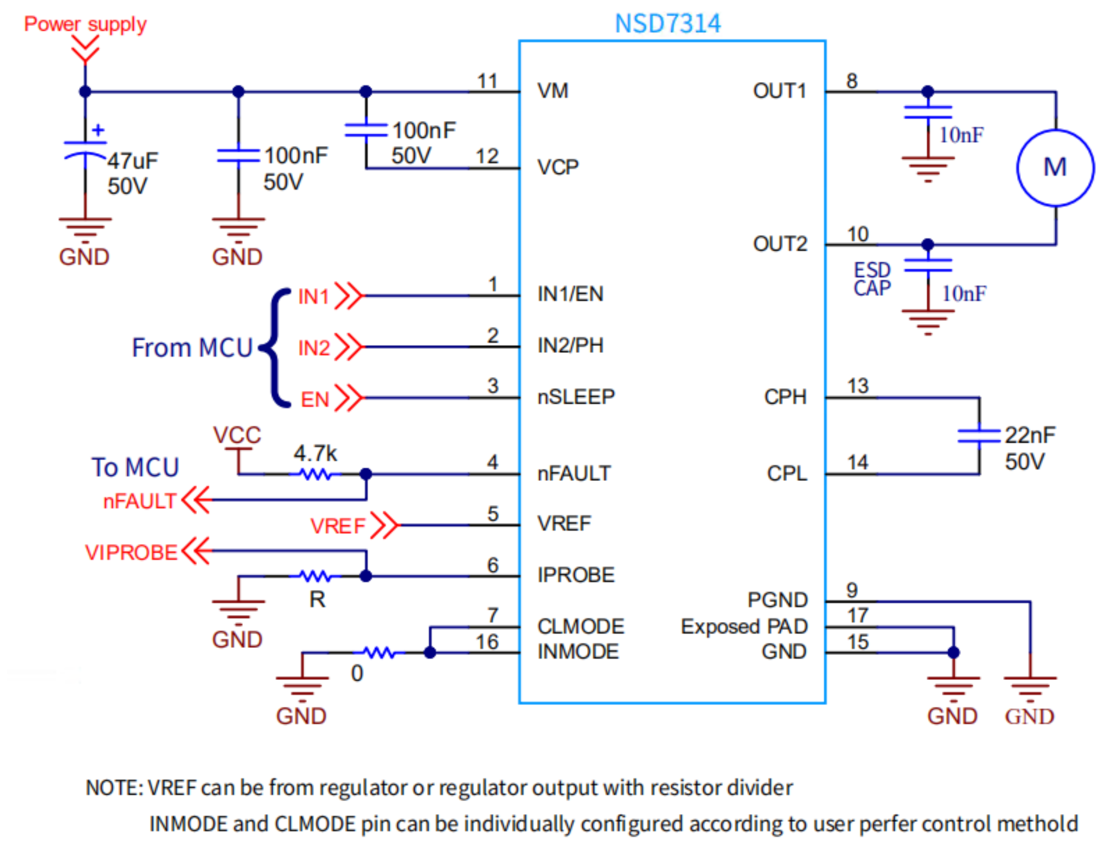


Figure 9.1 Typical application connection

9.2. IPROBE Pin and External Resistor Selection

An external resistor, R_{IPROBE}, should be put on IPROBE pin in order to generate the proportional voltage V_{IPROBE} with refer to load current. MCU can use ADC to measure the V_{IPROBE} and monitor the load current.

Additional, NSD7314 integrates an internal clamp which limits IPROBE pin max voltage up to VREF input plus one diode. In case of unexpected high load current or R_{IPROBE} loss, the clamp circuit protects both IPROBE pin and MCU ADC pin and easy the external application circuit.

Hence, the resistor value is suggested to be calculated based on AIPROBE scaling factor and maxim load current in the application.

$$R_{IPROBE} \leq \frac{V_{REF}}{A_{IPROBE} * I_{TRIP}}$$

For example, I_{TRIP} = 2.5A, VREF=2.5V and A_{IPROBE} = 0.45mA/A, then R_{IPROBE} should be chosen below 2.2 kohm with 1% accuracy / SMT 0603 or 0402 size.

In case the current regulation function is not required in application, R_{IPROBE} shall be used as 0ohm and VREF > 0.5v.

9.3. Device Power Dissipation and Continuous Driving Current

Total device power dissipation (P_{TOT}) is consisted of three parts: VM supply current and related dissipation (P_{VM}), H-bridge switching loss (P_{SW}) and H-bridge MOSFET ON static power dissipation (P_{ON}).

$$P_{TOT} = P_{VM} + P_{SW} + P_{ON}$$

$$P_{TOT} = VM * I_{VM} + I_{LOAD} * V_M * \left(t_{rise} + t_{fall}\right) * f_{PWM} + I_{LOAD}^2 * (R_{DS(ON)_{HS}} + R_{DS(ON)_{LS}})$$

If the input PWM frequency is used below 20kHz, the switching loss P_{SW} is insignificant comparing with P_{ON}, therefore, the power loss of NSD7314 under this condition can be quickly estimated by the formula

$$P_{TOT} \approx I_{RMS}^2 \times (R_{DS(ON)_{HS}} + R_{DS(ON)_{LS}})$$

The device junction temperature calculation is defined as $T_J = T_{amb} + (R_{thja} * P_{TOT})$, for continuous driving, the device internal temperature must be less than Tj max (150°c) for system operating.

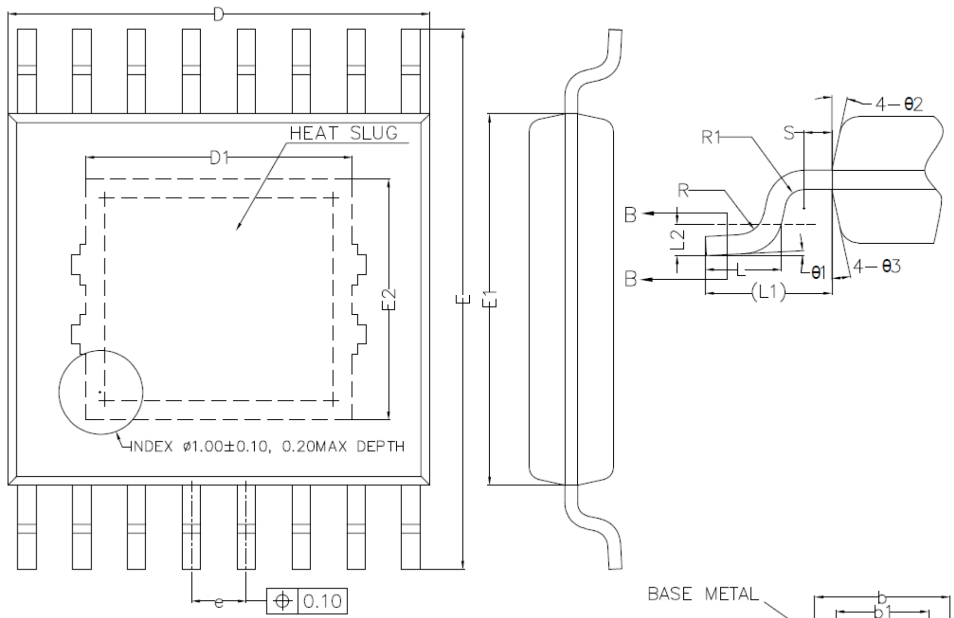
9.4. Layout Tips

For optimized thermal performance, the NSD7314 exposed pad must be directly soldered to the PCB surface, also multiple vias should be used to transfer the heat to other PCB layers. In the meanwhile, the PCB is recommended to have higher copper coverage and thick ground plane.

For robust and reliable electrical usage, the power supply pin VM should be decoupled with a bulk capacitor (47uF or 100uF) and one low value ceramic capacitor (100nF typical). The placement of two capacitors suggests close to VM pin as much as possible.

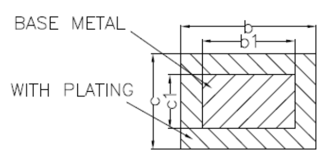
10. Package Information

10.1. HTSSOP16 Package Information

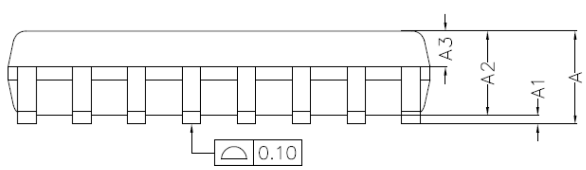


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.32	0.42	0.52
b	0.20	—	0.29
b1	0.19	0.22	0.25
c	0.15	—	0.20
c1	0.14	0.15	0.16
D	4.90	5.00	5.10
D1	3.16REF		
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	2.86REF		
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R	0.09	—	—
R1	0.09	—	—
S	0.20	—	—
θ1	0°	—	8°
θ2	10°	12°	14°
θ3	10°	12°	14°

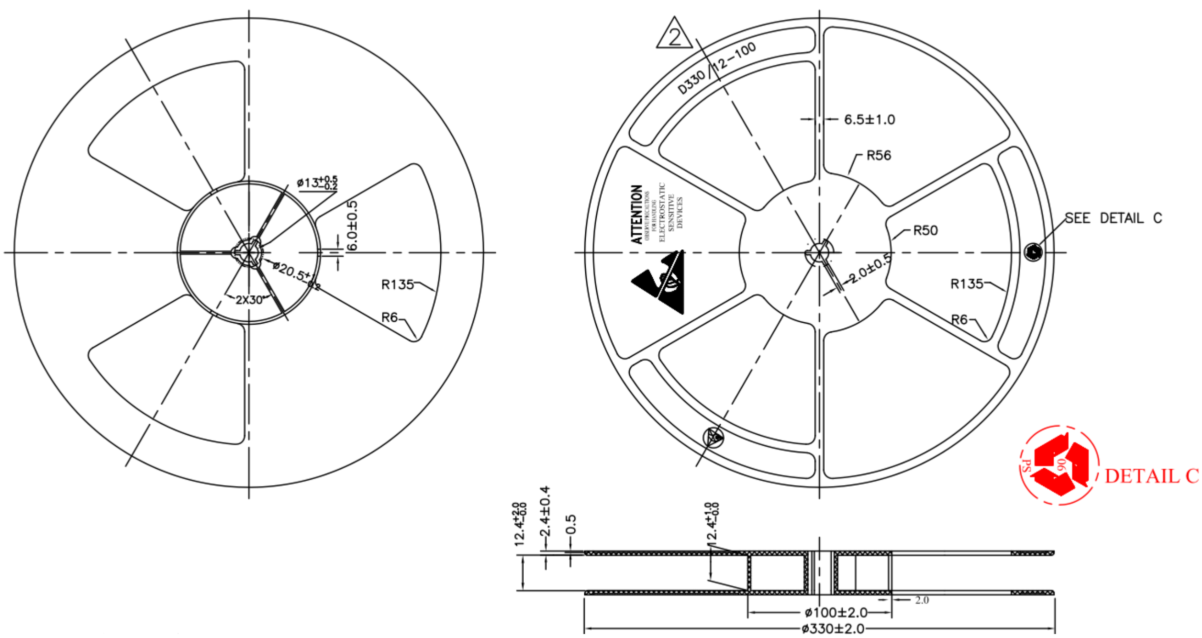


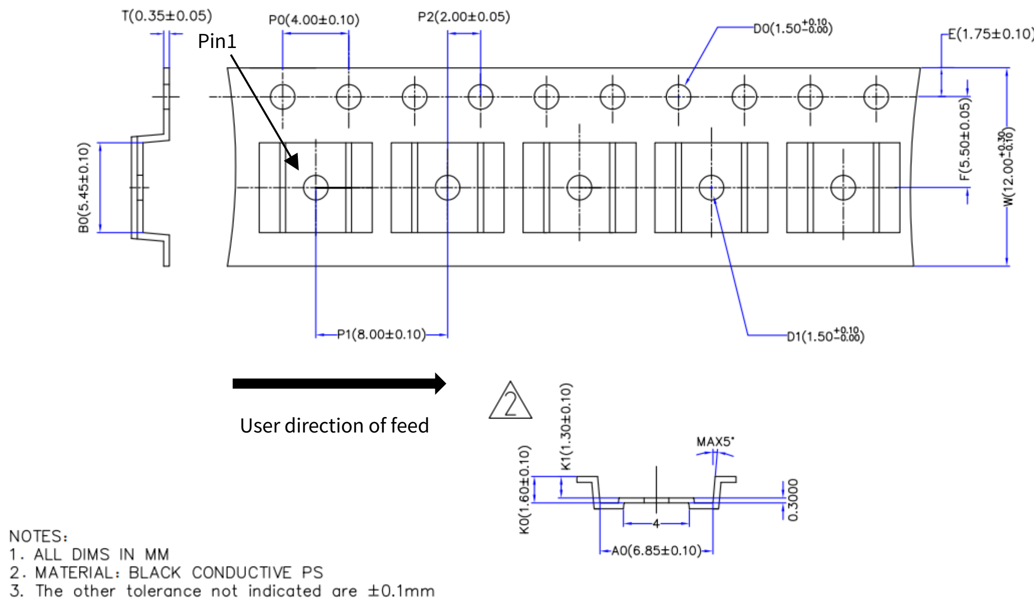
SECTION B−B



NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO−153 ABT
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

10.2. HTSSOP16 Packaging Information





11. Ordering Information

Part Number	Automotive / Industrial	Package Type	MSL	SPQ
NSD7314-DHTSPR	Industrial	HTSSOP16	MSL3	4000
NSD7314-Q1HTSPR	Automotive	HTSSOP16	MSL3	4000
Note: All packages are RoHS compliant with peak reflow temperature of 260°C according to the JEDEC industry standard classifications and peak solder temperature.				

12. Revision History

Revision	Description	Date
0.1	Initial version	2022/11/5
0.2	Revised current sense & regulation figures and parameter value	2023/3/5
0.3	Update AEC-Q100 compliance	2024/6/20
1.0	Revise electrical parameters & function description, and release to 1.0	2025/4/8

IMPORTANT NOTICE

The information given in this document (the “Document”) shall in no event be regarded as any warranty or authorization of, express or implied, including but not limited to accuracy, completeness, merchantability, fitness for a particular purpose or infringement of any third party’s intellectual property rights.

Users of this Document shall be solely responsible for the use of NOVOSENSE’s products and applications, and for the safety thereof. Users shall comply with all laws, regulations and requirements related to NOVOSENSE’s products and applications, although information or support related to any application may still be provided by NOVOSENSE.

This Document is provided on an “AS IS” basis, and is intended only for skilled developers designing with NOVOSENSE’s products. NOVOSENSE reserves the rights to make corrections, modifications, enhancements, improvements or other changes to the products and services provided without notice. NOVOSENSE authorizes users to use this Document exclusively for the development of relevant applications or systems designed to integrate NOVOSENSE’s products. No license to any intellectual property rights of NOVOSENSE is granted by implication or otherwise. Using this Document for any other purpose, or any unauthorized reproduction or display of this Document is strictly prohibited. In no event shall NOVOSENSE be liable for any claims, damages, costs, losses or liabilities arising out of or in connection with this Document or the use of this Document.

For further information on applications, products and technologies, please contact NOVOSENSE (www.novosns.com).

Suzhou NOVOSENSE Microelectronics Co., Ltd