NSD2622N
700V Half Bridge Gate Driver for GaN
Datasheet (EN) 1.0

Product Overview

The NSD2622N is a high voltage half bridge driver designed to drive enhancement-mode GaN HEMT. The NSD2622N has separated gate outputs allowing independent adjustment of the switching-on and switching-off capability by changing impedance for gate loop. The positive bias is maintained by an internal voltage regulator, with adjustable output from 5V to 6.5V. To avoid GaN HEMT falsely turn on due to cross-talk in high voltage or high-power conditions, this device also integrates negative bias of -2.5V, thus eliminating the need for an external negative bias circuit. In addition，the NSD2622N offers a 5V linear regulator, as the power supply to external circuit, e.g., digital isolators.

The driver features undervoltage lockout (UVLO)and over-temperature protection (OTP) to ensure the systems work properly. It is a fixed 20ns dead-time to prevent cross-conduction.

The device operates in the industrial temperature range, -40°C to 125°C, and is available in a compact 5.0 x 7.0mm QFN package.

Key Features

- 5V to 6.5V adjustable positive output voltage
- -2.5V integrated negative bias
- Compatible with high side bootstrap supply
- Independent 2A source and 4A sink current
- 5V LDO output for external circuit, e.g., digital isolators.
- 10ns typical minimum input pulse width
- 38ns typical propagation delay
- 5ns typical pulse distortion
- 6.5ns typical rise time (1nF load)
- 6.5ns typical fall time (1nF load)
- 20ns typical deadtime
- High immunity to common-mode voltage transition (±200V/ns) for robust operation during fast switching
- UVLO and over-temperature protection
- Operation temperature: -40°C ~125°C
- RoHS-compliant packages: Pb-Free, Halogen-Free

Applications

- DC-to-DC Converter
- AC to DC Converters
- Switching-Mode Power Supplies
- Solar Power and UPS

Device Information

Part Number	Package	Body Size
NSD2622N-DQAER	QFN30	5.0mm*7.0mm*0.85mm

Application Block Diagram

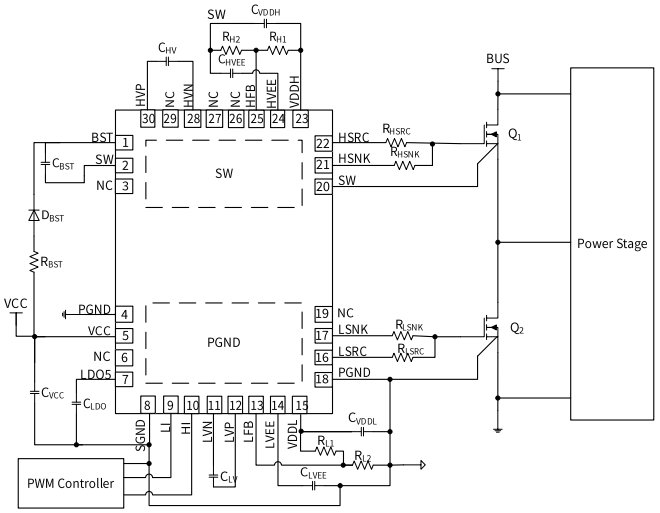

Figure 0.1 NSD2622N Block Diagram

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1. Pin Configuration and Functions

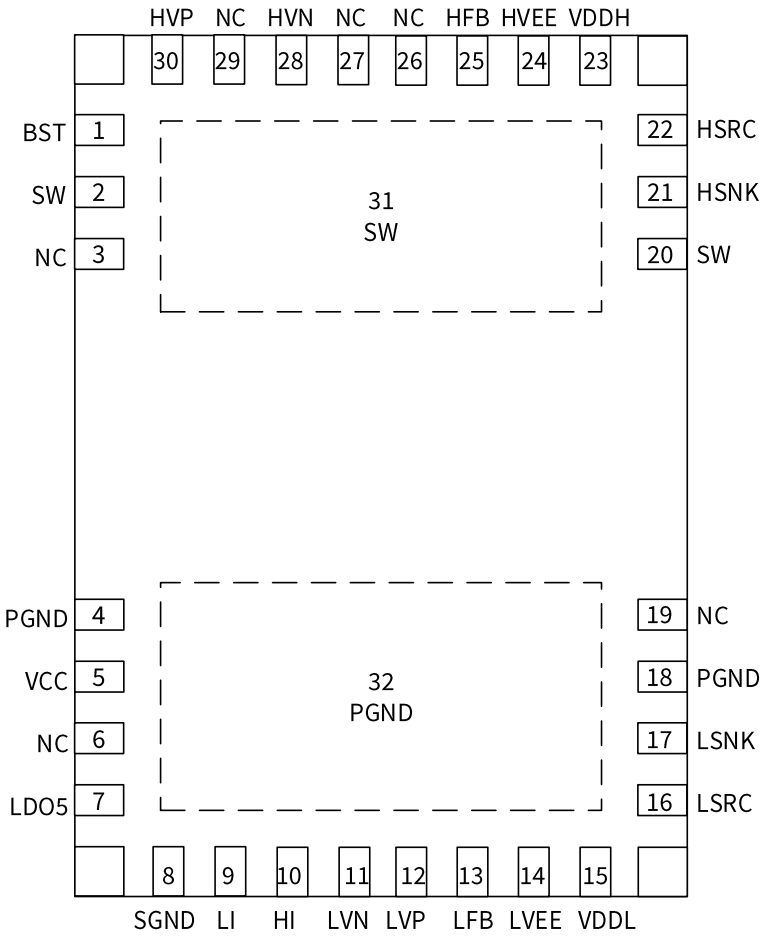


Figure 1.1 NSD2622N Top View

Table 1.1 NSD2622N Pin Configuration and Description

Pin	*Name*	*Function*
1	BST	Power supply for high-side regulator.
2, 20, 31	SW	High-side driver reference (switching node).
3, 6, 19, 26, 27, 29	NC	Not Connected.
4, 18, 32	PGND	Low side driver reference (Power ground).
5	VCC	Power supply for logic and low-side regulator.
7	LDO5	Low side 5V internal regulated voltage output refer to SGND. The total value of capacitor should be more than 100nF and lower than 1uF.
8	SGND	Low-side signal and logic ground.

Pin	Name	Function
9	LI	Low side driver logic input.
10	HI	High side driver logic input.
11	LVN	Negative terminal of low-side charge pump.
12	LVP	Positive terminal of low-side charge pump.
13	LFB	Feedback voltage for VDDL adjustment.
14	LVEE	Low side negative rail voltage for the turn-off. The typical output voltage is -2.5V.
15	VDDL	Low side voltage regulator output. Connect a resistance between this pin and LFB to set the driver output voltage. The detailed information refers to Figure 7.3.
16	LSRC	Low side driver sourcing output.
17	LSNK	Low side driver sinking output.
21	HSNK	High side driver sinking output.
22	HSRC	High side driver sourcing output.
23	VDDH	High side voltage regulator output. Connect a resistance between this pin and HFB to set the driver output voltage. The detailed information refers to Figure 7.3.
24	HVEE	High side negative rail voltage for the turn-off. The typical output voltage is -2.5V.
25	HFB	Feedback voltage for VDDH adjustment.
28	HVN	Negative terminal of high-side charge pump.
30	HVP	Positive terminal of high-side charge pump.

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
SW to PGND Voltage, pulse	Vsw to PGND	-700	700	V
Driver Supply Voltage	VCC to SGND, BST to SW	-0.3	18	V
	VCC to PGND	-0.3	18	V
	VCC to LVEE, BST to HVEE	-0.3	18	V
	VCC to SGND, BST to SW for <100ns	-0.3	20	V
	VCC to PGND, for <100ns	-0.3	20	V
	VCC to LVEE, BST to HVEE, for <100ns	-0.3	20	V
Regulator Output Voltage	VDDL to PGND, VDDH to SW	-0.3	9	V

Parameters	Symbol	Min	Max	Unit
Different Ground Voltage	SGND to PGND	-3	3	V
Negative Regulator Output Voltage	LVEE to PGND, HVEE to SW	-5	0	V
	LVEE to SGND	-5	0	V
	VDDL to LVEE，VDDH to HVEE	-0.3	9	V
Input Signal Voltage	HI, LI to SGND	-10	18	V
Low side driver Output voltage	LSRC, LSNK	LVEE-0.3	VDDL+0.3	V
	LSRC, LSNK，for < 100ns	LVEE-2.0	VDDL+0.3	V
High side driver Output voltage	HSRC, HSNK	HVEE-0.3	VDDH+0.3	V
	HSRC, HSNK, for < 100ns	LVEE-2.0	VDDL+0.3	V
Regulator output voltage	LDO5 to SGND	-0.3	5.5	V
Charge pump negative voltage	LVN to PGND, HVN to SW	-5	1.5	V
Charge pump positive voltage	LVP to PGND, HVP to SW	-0.3	5	V
Feedback voltage	LFB to PGND, HFB to SW	-0.3	5	V
Storage temperature	T_{stg}	-55	150	°C
Operation junction temperature	T_J	-40	150	°C
Allowable offset voltage slew rate	dV_{sw}/dt	-	200	V/ns

3. ESD Ratings

Ratings		Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC Q100-002	±2000	V
	Charged device model (CDM), per AEC Q100-011	±500	V

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
SW to PGND	V_{SW} to PGND	-700	700	V
SGND to PGND	SGND to PGND	-2.5	2.5	V
Driver Supply Voltage	VCC to SGND, BST to SW	5	15	V
Low side Gate to Source Voltage	LSRC, LSNK	LVEE	VDDL	V
High side Gate to Source Voltage	HSRC, HSNK	HVEE	VDDH	V
Input Signal Voltage	HI, LI to SGND	-5	VCC	V
Regulator output voltage	VDDL to PGND, VDDH to SW	5	6.5	V
Ambient Temperature	Ta	-40	125	°C

5. Thermal Information

Parameters	Symbol	QFN	Unit
Junction-to-ambient thermal resistance[1)]	R_{JA}	36	°C/W
Junction-to-case(top) thermal resistance[1)]	$R_{JC\ (top)}$	27	°C/W
Junction-to-top characterization parameter[2)]	Ψ_{JT}	3.8	°C/W
Junction-to-board characterization parameter[2)]	Ψ_{JB}	7.7	°C/W

1) Standard JESD51-7 High Effective Thermal Conductivity Test Board (2s2p) in an environment described in JESD51-2a.

2) Obtained by Simulating in an environment described in JESD51-2a.

6. Specifications

6.1. Electrical Characteristics

VCC=12V, For typical values, Ta= 25°C. For min/max values, Ta = -40°C to 125°C, unless otherwise noted.

Parameters	Symbol	Min	Norm	Max	Unit	Comments
Bias Current						
VCC Quiescent Current With charge pump	I_{VCC_Q}		3.0		mA	LI=HI=0V, VDDL=6V, C_{LVEE}=680nF
BST Quiescent Current With charge pump	I_{BST_Q}		3.0		mA	LI=HI=0V, VDDH=6V, C_{HVEE}=680nF
VCC Operating Current With charge pump	I_{VCC_O}		14.1		mA	LI=500kHz, VDDL=6V, HI=500kHz, 1nF load, C_{LVEE}=680nF
BST Operating Current With charge pump	I_{BST_O}		13.2		mA	LI=500kHz, VDDH=6V, HI=500kHz, 1nF load, C_{HVEE}=680nF
Under Voltage Lockout (UVLO)						
VCC UVLO Rising Threshold	V_{VCC_ON}	4.2	4.5	4.8	V	
VCC UVLO Falling Threshold	V_{VCC_OFF}		4		V	
VCC UVLO Hysteresis	V_{VCC_HYS}		0.5		V	
BST UVLO Rising Threshold	V_{BST_ON}	4.2	4.5	4.8	V	
BST UVLO Falling Threshold	V_{BST_OFF}		4		V	
BST UVLO Hysteresis	V_{BST_HYS}		0.5		V	
Regulator Supply Characteristic						
LDO5 output voltage	V_{LDO5}	4.7	5	5.3	V	
LDO5 output current	I_{LDO5}			50	mA	Cap>=100nF
Driver output voltage						
UVLO Positive Threshold on VDDx	V_{VDDL_UV+}, V_{VDDH_UV+}	4.2	4.5	4.8	V	
UVLO Negative Threshold on VDDx	V_{VDDL_UV-}, V_{VDDH_UV-}		4.25		V	
VDDx UVLO hysteresis	V_{VDDx_UVH}		0.25		V	
Reference voltage	V_{LFB}, V_{HFB}	0.97	1	1.03	V	
Negative charge pump						
Negative output voltage	V_{VEEL} V_{VEEH}	-3	-2.5	-2	V	
Input Pin Characteristics						
LI, HI input putdown current	I_{LI}, I_{HI}		28		uA	Input=5V
Logic High Input Threshold	V_{HI_H}, V_{LI_H}	1.7	2.0	2.2	V	
Logic Low Input Threshold	V_{HI_L}, V_{LI_L}	0.9	1.1	1.3	V	
Logic Hysteresis	V_{LI_HYS}, V_{HI_HYS}		0.9		V	
Output Pin Characteristics						
Low-level output Voltage, V_{LSNK}-V_{LVEE} or V_{HSNK}-V_{HVEE}	V_{OL}		5		mV	I_xSNK=10mA
High-level output Voltage, V_{VDDL}-V_{LSRC}, or V_{VDDH}-V_{HSRC}	V_{OH}		14		mV	I_xSRC=10mA

Peak source current[1)]	I_{LSRC} , I_{HSRC}		2		A	VDDx=6V
Peak sink current[1)]	I_{LSNK} , I_{HSNK}		4		A	VDDx=6V
Dead time						
Dead time	T_{DT}		20		ns	
Thermal Shutdown						
Thermal Shutdown Temperature[1)]	T_{SD}		165		°C	
Thermal Shutdown Hysteresis[1)]	T_{SH}		20		°C	
Operation Frequency						
Maximum Operation Frequency[1)]	F_{sw_max}			4	MHz	

1) Not test covered. Guaranteed by design.

6.2. Switching Characteristics

VCC=12V, For typical values, Ta= 25°C. For min/max values, Ta = -40°C to 125°C, unless otherwise noted

Parameters	*Symbol*	*Min.*	*Norm.*	*Max.*	*Unit*	*Comments*
Turn off propagation delay time	T_{lphl}, T_{hphl}		38	55	ns	No load
Turn on propagation delay time	T_{lplh}, T_{hplh}		38	55	ns	No load
Pulse width distortion	t_{PWD}		5	10	ns	No load
Delay matching	t_{MD}		4		ns	No load
Rise time	T_r		6.5		ns	Load=1nF, VDDx=6V
Fall time	T_f		6.5		ns	Load=1nF, VDDx=6V
Minimal input pulse	t_{PWM_MIN}		10	20	ns	

6.3. Typical Performance Characteristics

VCC=12V, Ta=25°C，unless otherwise notes.

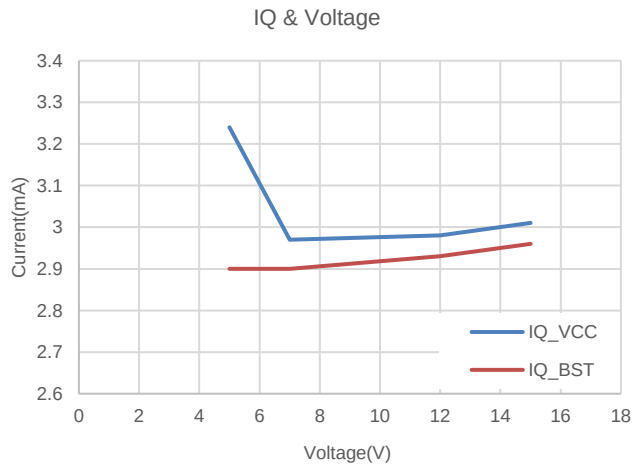


Figure 6.1 Quiescent current vs Voltage

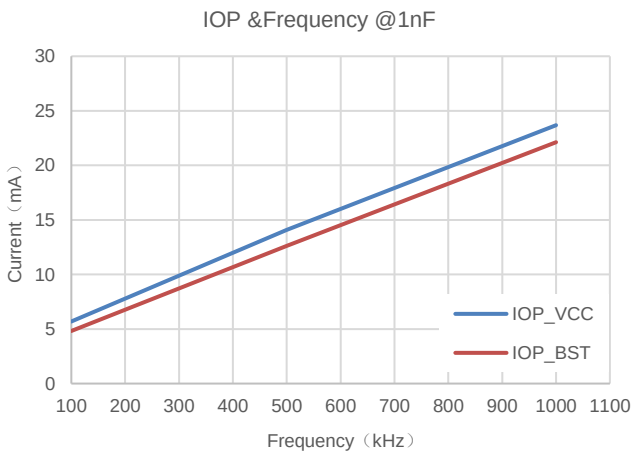


Figure 6.2 Operation current vs frequency

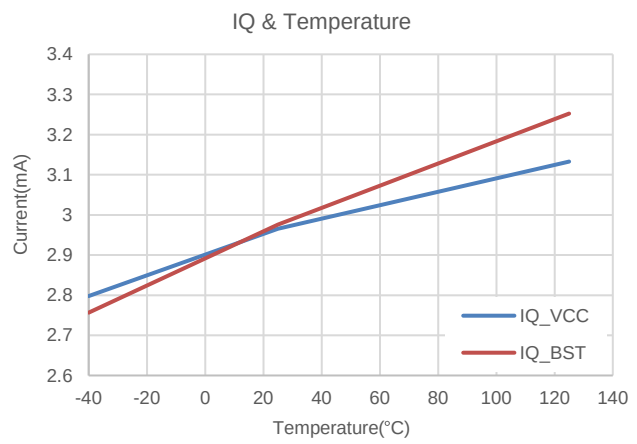


Figure 6.3 Quiescent current vs Temperature

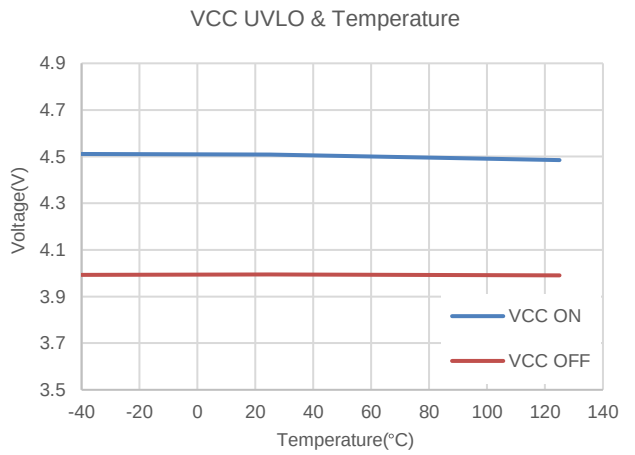


Figure 6.4 VCC UVLO vs Temperature

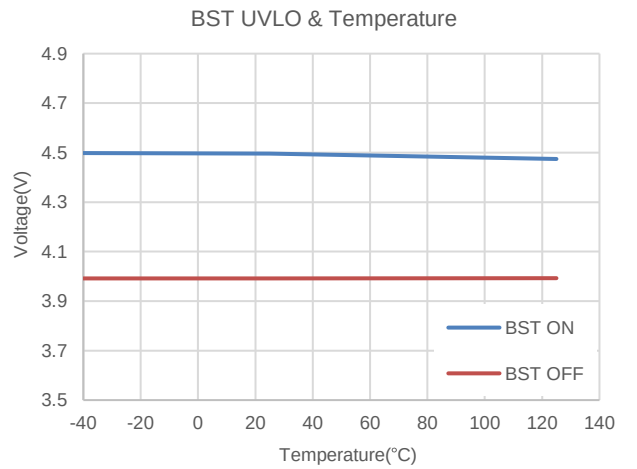


Figure 6.5 BST UVLO vs Temperature

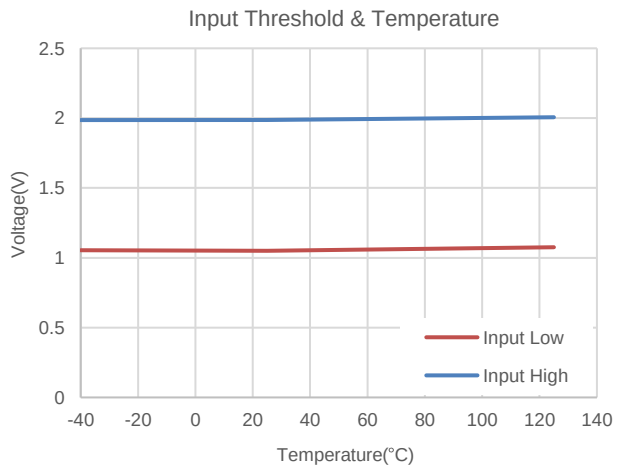


Figure 6.6 Input logic threshold vs Temperature

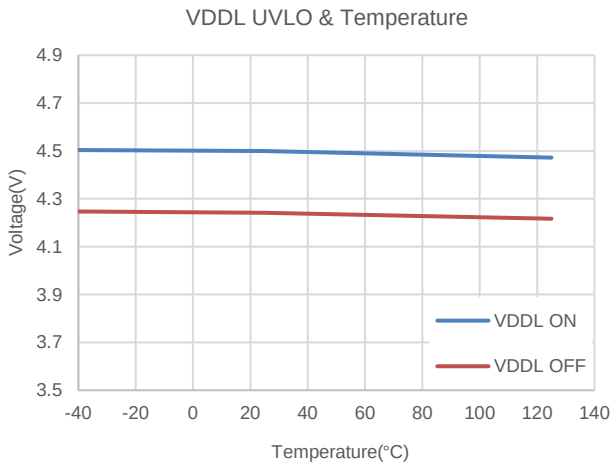


Figure 6.7 VDDL UVLO vs Temperature

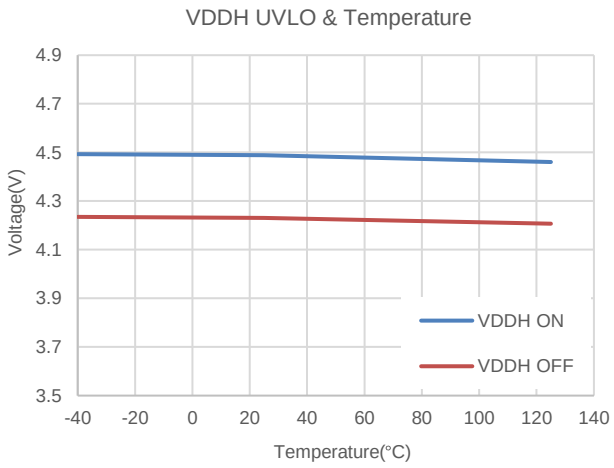


Figure 6.8 VDDH UVLO vs Temperature

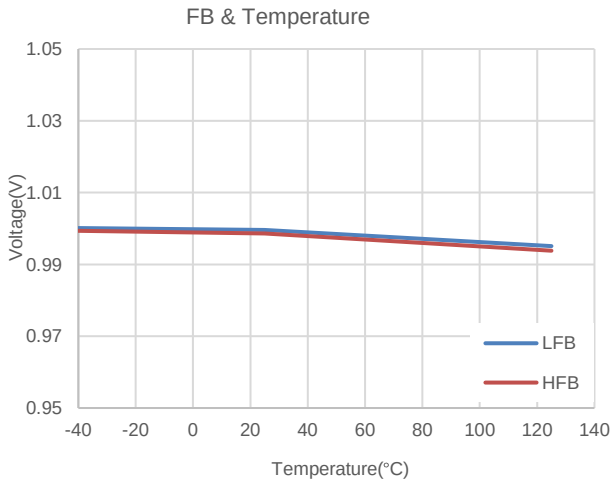


Figure 6.9 FB Vs Temperature

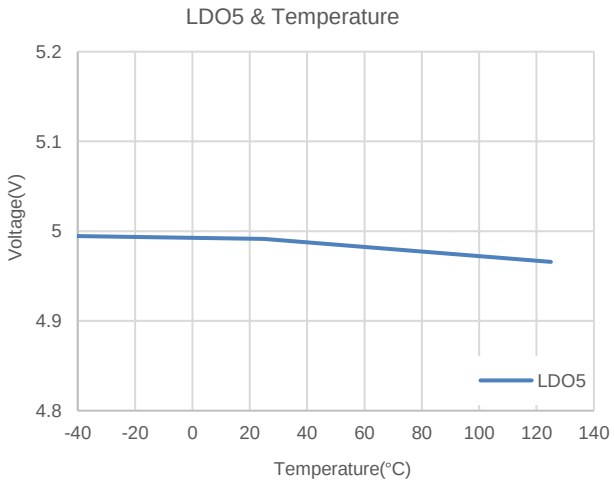


Figure 6.10 LDO5 output voltage & Temperature

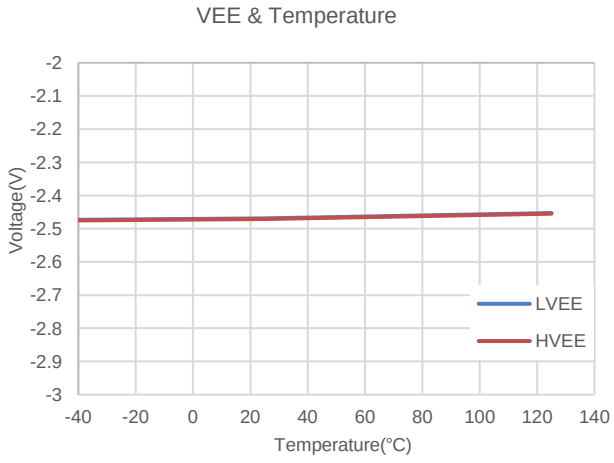


Figure 6.11 Negative output voltage & Temperature

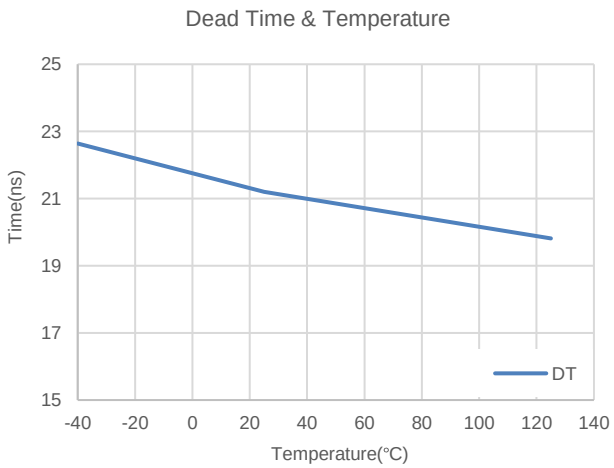


Figure 6.12 Dead Time & Temperature

6.4. Parameter Measurement Information

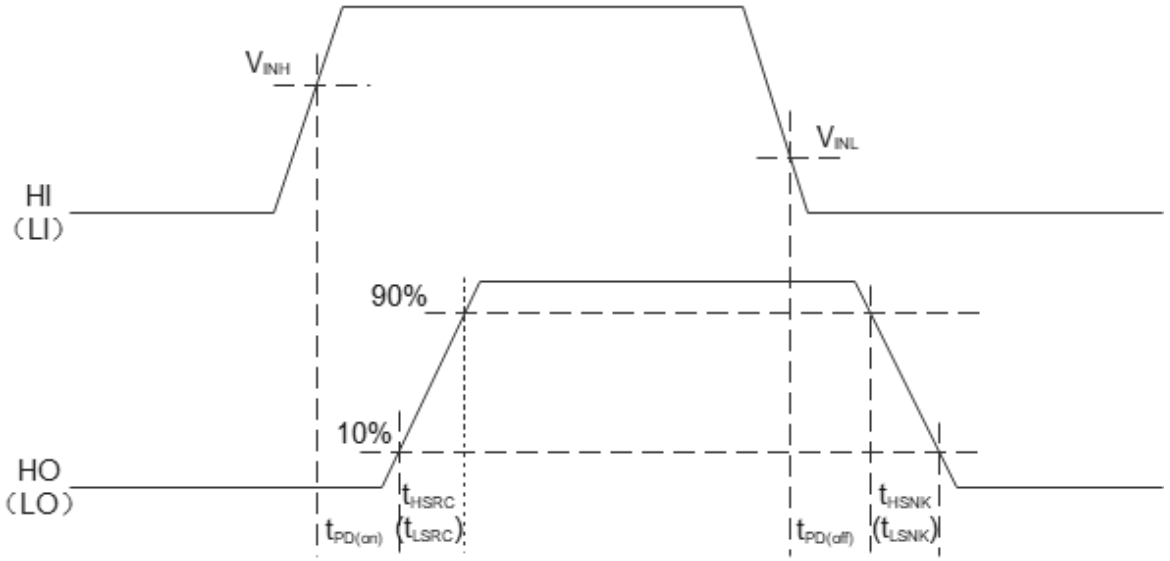


Figure 6.13 Propagation Delay, Rise and Fall time

7. Function Description

7.1. Overview

The NSD2622N is a high voltage half bridge driver designed to drive the enhancement-mode GaN HEMT. The NSD2622N has separated gate outputs allowing independent adjustment of the switching-on and switching-off capability by changing impedance for gate loop. The NSD2622N provides the negative switching off function to improve the GaN HEMT community. The NSD2622N provides the positive voltage turn-on regulator which can be adjusted the output voltage through the external resistor. In addition, the NSD2622N offers a 5V LDO output and OTP function. It has a fixed 20ns deadtime.

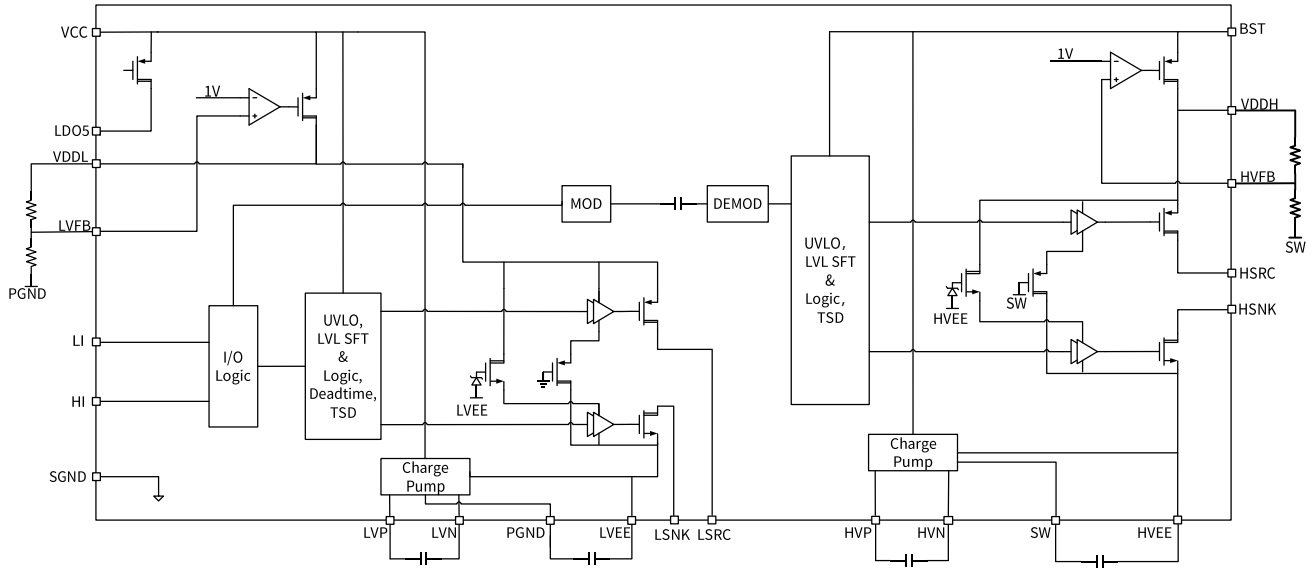


Figure 7.1 NSD2622N Functional Block Diagram

7.2. Under Voltage Lock Out (UVLO)

The NSD2622N has internal under voltage lock out (UVLO) protections on low side and high side power supply blocks. The driver output is held low by an active clamp circuit when the supply voltage of VCC or BST is lower than V_{VCC_ON} / V_{BST_ON} at power-up status or lower than V_{VCC_OFF} / V_{BST_OFF} during power-down, regardless of the status of the input pins.

The 0.5V UVLO hysteresis on VCC (or BST) is provided prevent chatter noise from VCC (or BST) and allow small drops in power supply which usually happens during startup. When the voltage of VCC (or BST) is more than V_{VCC_POR} (or V_{BST_POR}) which is approximate 2V, the positive regulator and the charge pump begin to operate and the negative voltage LVEE (or HVEE) and the positive voltage VDDL (or VDDH) begins to setup. In order to reduce the rush current during the startup, the negative charge current is limited to only about 3mA from the negative regulator LVEE (or HVEE) output. When the voltage of VDDL (or VDDH) rises to be more than its UVLO threshold voltage, the negative voltage will quickly fall down to -2.5V. In Figure 7.2, t_{PUD} is the power up delay time which is about 65us based on the parameters in Table 8.1. It should be noted that t_{PUD} was related to the capacitor at VDDL (or VDDH).

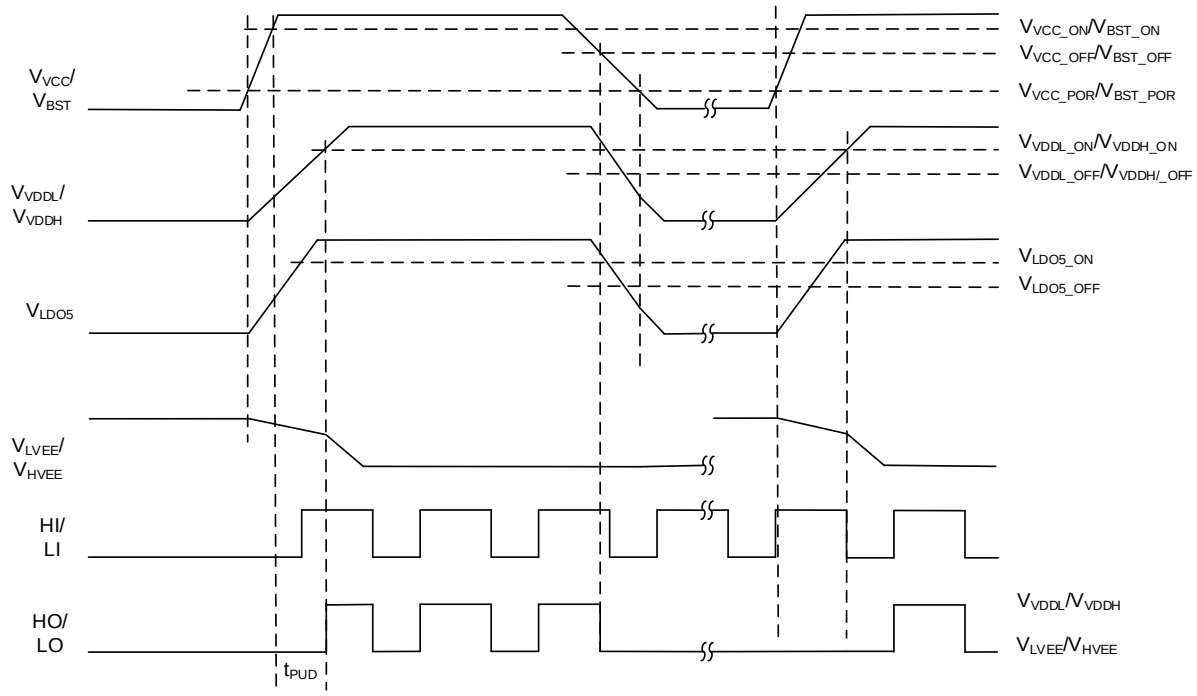


Figure 7.2 UVLO Diagram

7.3. Regulator 5V Output (LDO5)

The NSD2622N integrated a 5V linear regulator in the low side. It can be used to provide the power for the digital insulator or other devices. Its maximum output current is 50mA. In order to keep the output voltage stable, a capacitor should be placed between LDO5 and SGND pin. The capacitance can be from 100nF to 1uF. It should be noted that the bigger capacitance, the longer 5V regulator set up.

7.4. Feedback Voltage (LFB/HFB) and Positive Regulator Output (VDDL/VDDH)

The NSD2622N respectively integrated a positive linear regulator in the low side and the high side. LFB is the positive input to the internal error amplifier and used to control the VDDL output voltage. HFB is the positive input to the internal error amplifier and used to control the VDDH output voltage. The output voltage can be calculated following the below equation (1). The recommended range of resistor R2 is from 1kΩ to 20kΩ. In order to keep the output voltage on VDDL (or VDDH) stable, a capacitor should be placed between VDDL (or VDDH) and PGND (or SW). The value of capacitor C1 can be from 470nF to 1uF. The bigger value of capacitor C1, the longer power delay up. The VDDL (or VDDH) begins to build up if VCC

(or BST) voltage is more than V_{VCC_POR} (or V_{BST_POR}) which is appropriated 2V. The acceptable output voltage range is from 5V to 6.5V. If the output voltage is more than 6.5V, the device maybe damaged.

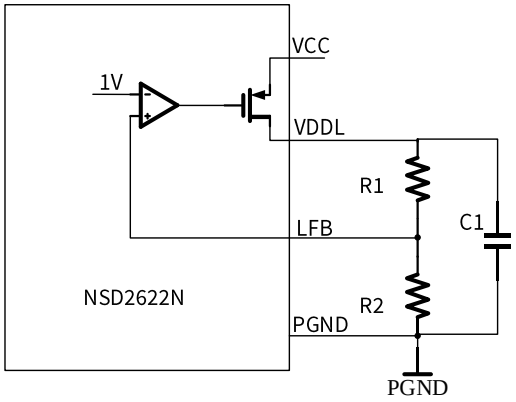


Figure 7.3 Positive Regulator Diagram

$$V_{VDDL} = \frac{R_1+R_2}{R_2} \times 1V \quad (1)$$

7.5. Negative Voltage (LVEE/HVEE) and Charge Pump (LVP/LVN, HVP/HVN)

The NSD2622N respectively integrated a negative voltage in the low side and the high side to return the sink current. The negative voltage generation is based on the charge pump technology. When VCC (or BST) voltage is more than their V_{VCC_POR} (or V_{BST_POR}) voltage, the negative voltage begins to build up. The typical negative output voltage is -2.5V and its tolerance is ±0.5V. In order to keep the negative output voltage stable, a capacitor should be placed between LVEE (or HVEE) and PGND (or SW). The capacitance range is from 680nF to 1uF. It should be noted that the bigger capacitance, the longer power set up.

LVP and LVN is respectively the positive pin and the negative pin of charge pump circuit in the low side. One capacitor should be placed between LVP and LVN to normal operate. A 100nF capacitor is recommended.

HVP and HVN is respectively the positive pin and the negative pin of charge pump circuit in the high side. One capacitor should be placed between HVP and HVN to normal operate. A 100nF capacitor is recommended.

7.6. Input and Output Logic Table

LI and HI are the PWM signal input pins. Both inputs are independent and internally pulled down to SGND such that each output is defaulted to be low. When the voltage on VCC or VDDL is less than their UVLO, the low side output is low level. When the voltage on BST or VDDH is less than their UVLO, the high side output is low level. When all the voltage on VCC, BST, VDDL and VDDH are more than their UVLO, the user can refer Table 7.1 to get the output status.

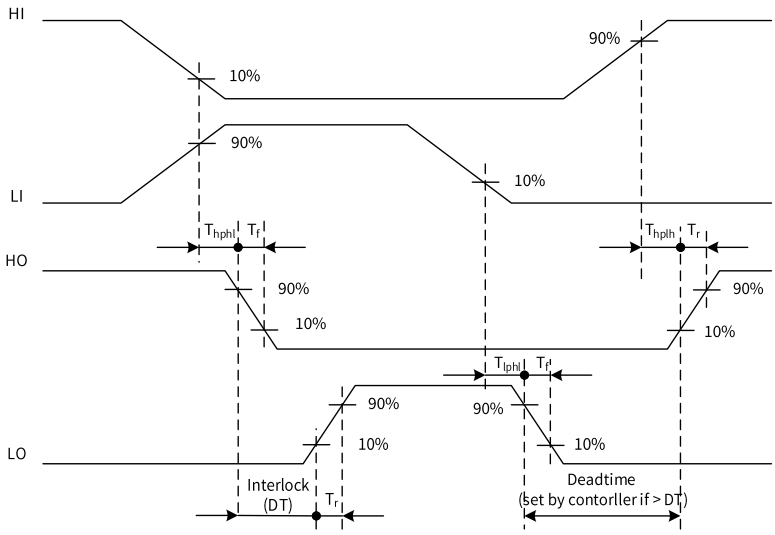


Figure 7.4 Deadtime switching Parameters

Table 7.1 NSD2622N Output status vs. Input status

Input Pins		Output Pins		Output Pins		NOTE
HI	LI	HSRC	HSNK	LSRC	LSNK	
L	L	Open	L	Open	L	
L	H	Open	L	H	Open	Driver's outputs turn on after the deadtime expires.
H	L	H	Open	Open	L	
H	H	Open	L	Open	L	The input signal is later than VDD power up.

7.7. Output Stage (LSRC/LSNK, HSRC/HSNK)

The NSD2622N provides 2A source and 4A sink peak current output capability. The user can select the different resistor to adjust the turn-on and turn-off slew of GaN HEMT to optimize the system performance. The output LSNK (or HSNK) is actively pulled down to LVEE (or HVEE) in undervoltage condition which guarantee the gate voltage of GaN HEMT lower than its threshold voltage. In order to reduce the ringing caused by parasitic inductance on PCB, the device should be located nearly the gate of GaN HEMT and the circuit loop should be as short as possible. To prevent the gate voltage overshoot of GaN HEMT, it is suggested that the gate turn-on driver resistor was more than $2\sqrt{\frac{L_G}{C_{GS}}}$ and the turn-off resistor was more than 1Ω. L_G is the drive loop inductance and C_{GS} is the GaN HEMT input capacitance.

7.8. Interlock function

The NSD2622N provides the interlock function for two channels to prevent the upper and lower GaN HEMT shoot through. The internal typical interlock time is 20ns. The user can refer Figure 7.4 to get the deadtime switching information.

7.9. Overtemperature Protection (OTP)

The NSD2622N provides the OTP function. When its junction temperature is more than 165℃ which is the typical value, LSRC(or HSRC) will be open and LSNK(or HSNK) be pull-down. Then the junction temperature begins to decrease. When the junction temperature drops below some value, the device starts to operate again. The typical value of OTP hysteresis is 20℃.

8. Application Note

8.1. Typical Application Circuit

Figure 8.1 shows a typical half-bridge configuration by using the NSD2622N.

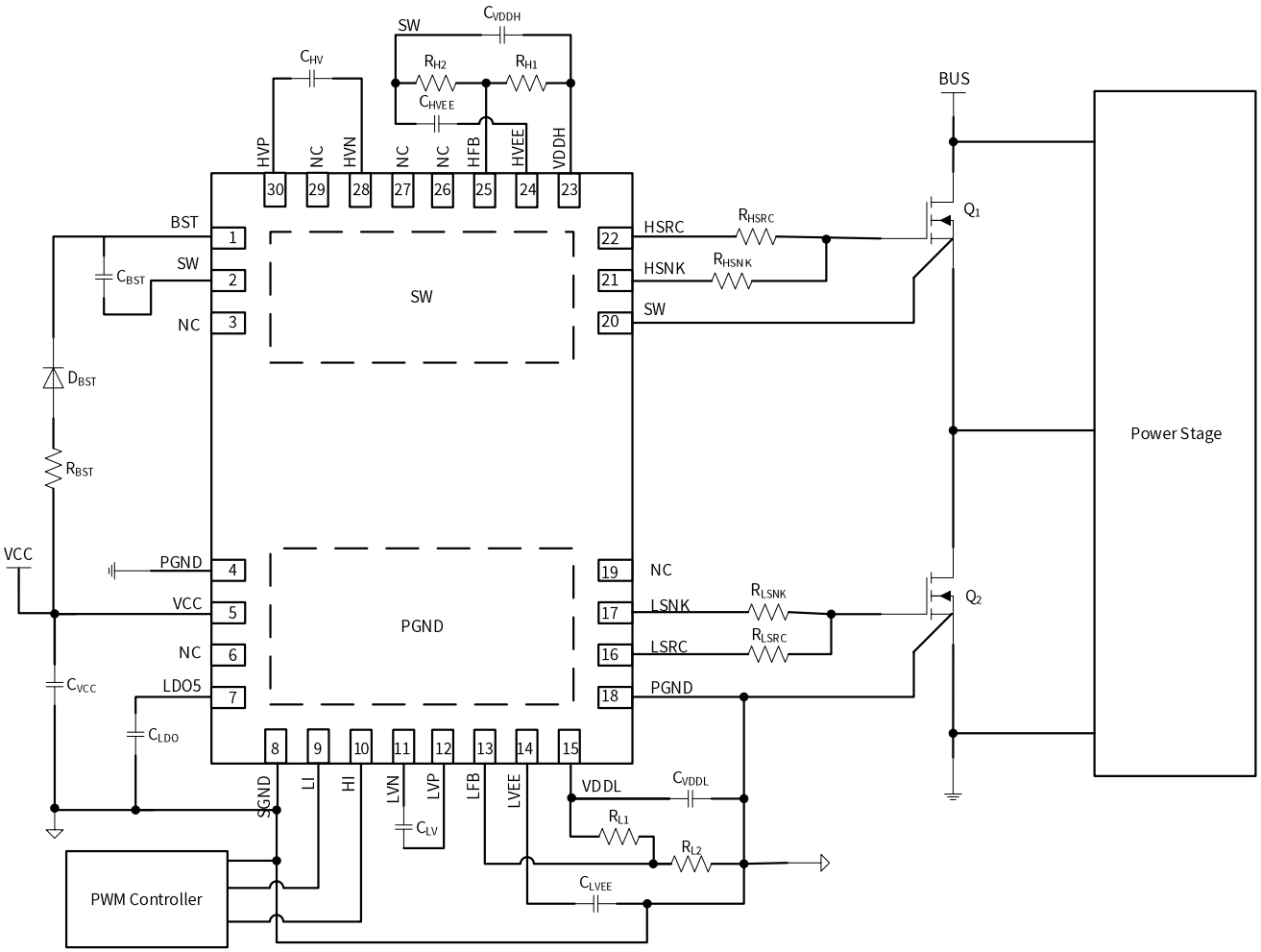


Figure 8.1 Typical Simplified Application Schematic

Supply voltage (VCC): VCC is the low side power supply of NSD2622N. When the VCC voltage is lower than its UVLO, the LSRC will be open and LSNK be pulled down. A bypass capacitor, C_{VCC}, which is more than 1uF is required and should be located as close as possible to VCC and SGND. A low ESR and low ESL capacitor is recommended to use. It should be noted that an inrush current of about 200mA occurs during the startup which the duration is tens of microseconds

High-Side Bootstrap Voltage (BST): BST is the high side power supply of NSD2622N. The bootstrap capacitor C_{BST} should be a ceramic capacitor and located as close as possible to BST and SW to properly filter out all glitches while switching. The capacitance value of C_{BST} should be large enough to provide fully charge for high side normal operation. No high side pulses are output when the BST voltage is less than its UVLO. In general, a 1uF capacitor is recommended to use.

The bootstrap diode D_{BST} should be fast recovery diodes or SiC Schottky diode with a low forward voltage drop and low junction capacitance. Its rated voltage must be greater than BUS voltage.

The purpose of the bootstrap resistor R_{BST} is to limit peak charging current of C_{BST}, especially during the startup. A too small resistor may not limit the peak current enough, resulting in excessive ringing which can cause jitter in the high side gate

drive or EMI problems. A large resistor will dissipate more power and create a longer RC time constant causing a longer start up time. A bootstrap resistor in the range of 1Ω < R_{BST} < 10Ω is usually sufficient.

5V Regulator (LDO5): It can output provide the power for the digital isolator. Its maximum output current is 50mA.If LDO5 is not used, a capacitor C_{LDO} should be connected directly between LDO5 and SGND. The recommended capacitance is from 100nF to 1uF.

Signal Ground (SGND) and Power Ground (PGND): SGND is the reference ground for all internal control logic and digital inputs. PGND is the return reference of VDDL and LVEE. For GaN HEMT Q2 included a source Kelvin return, a direct connection should be made from PGND to its Kelvin return. The NSD2622N is able to withstand −3 V to +3 V of common mode voltage between SGND and PGND. It may be damaged if the common mode voltage is over the range. It is recommended that SGND and PGND were directly short or connected with a low impedance resistor.

Switch Node (SW): SW is the return reference of the high side gate driver. For GaN HEMT Q1 included a source Kelvin return, a direct connection should be made from SW to its Kelvin return.

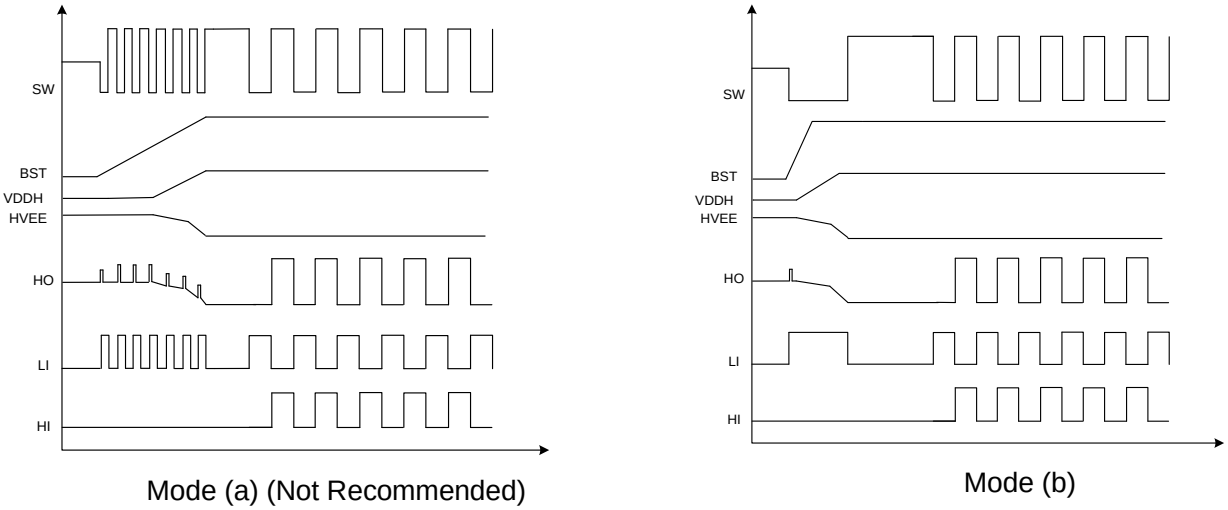
The BOM in Table 8.1 was used in the lab to verify the performance of NSD2622N.

Table 8.1 Bill of Materials for the reference

Designator	Qty	Value	Description	Part number	Manufacturer
C_{VDDH}, C_{VDDL}	2	470nF	Cap, CERM, 470nF,10V, +/-10%, X7R	GRM155R71A474KE01	MuRata
C_{LVEE}, C_{HVEE}	2	680nF	Cap, CERM, 680nF,10V, +/-10%, X7S	GCM155C71A684KE38	MuRata
C_{LV}, C_{HV}, C_{LDO}	3	100nF	Cap, CERM, 0.1uF, 25V, +/-10%, X7R,	GRM155R71E104KE14	MuRata
C_{VCC}, C_{BST}	2	1uF	Cap, CERM, 1uF, 50V, +/-10%, X7T	GRM188D71H105KE01	MuRata
D_{BST}	1	600V	Diode, Super-fast, 600V， 1A, SOD123F	SF1JWF-7	Diodes Inc.
R_{BST}, R_{LSNK}, R_{HSNK}	3	2	RES, 2， 1%, 0603	0603WAF200KT5E	Uni-Royal
R_{L2}, R_{H2}	2	10k	RES, 10k， 1%, 0402	0402WGF1002TCE	Uni-Royal
R_{L1}, R_{H1}	2	49.9k	RES, 49.9k， 1%, 0402	0402WGF4992TCE	Uni-Royal

8.2. Startup Timing Sequence of High Side Driver

BST is the high side power supply of NSD2622N. If the bootstrap diode is used to provide the voltage for BST, the startup time sequence of mode (b) is recommended.



Mode (a) (Not Recommended)　　Mode (b)

Figure 8.2 Startup Timing Sequence

Before starting up, the voltage of BST and the voltage of the negative voltage HVEE of the high side driver were not established. When the startup timing sequence of mode a) is adopted, the rise speed of BST voltage is slow and the established time of the negative voltage HVEE will be long and the gate of the high side GaN HEMT cannot be pulled down to HVEE during the HVEE voltage setup. When the low side GaN HEMT is repeatedly switched on and off during BST setup, the gate of the high side GaN HEMT will be rushed to a certain positive voltage affected by its Miller capacitor. It is very dangerous when this value exceeds its threshold voltage.

Before the startup, the voltage of SW node is one half of bus voltage. When using the startup timing sequence of mode b), the first pulse of the input LI signal is enough wide, both BST voltage and the negative bias HVEE of the high side driver can be effectively established. Then the gate of the high side GaN HEMT is strongly pulled down to the HVEE through the sink resistor R_{HSNK}. When the low side GaN HMET is turned on again, the gate voltage of the high side GaN HEMT is not charged to more than its threshold due to the existence of the negative voltage of the HVEE，which ensure the system to reliably operate. The first input pulse width of LI signal should be enough wide to make sure the voltage of HVEE completely setup. It should be noted that the established time of the negative bias HVEE was related to the capacitor C_{HVEE}. The larger the capacitance of C_{HVEE}, the longer the established time of the negative bias HVEE.

8.3. Power Dissipation Calculation

The gate of GaN HEMT will be pulled up to VDDL (or VDDH) through the drive resistor during turn-on and pulled down to LVEE (or HVEE) through the drive resistor during turn-off. To prevent the gate voltage overshoot of GaN HEMT, it is recommended that the gate turn-on driver resistor is more than $2\sqrt{\frac{L_G}{C_{GS}}}$ and turn-off resistor is more than 1Ω. L_G is the drive loop inductance and C_{GS} is the gate capacitance of GaN HEMT. When the GaN HEMT Q1 and Q2 are same, the power loss of driver resistor can be calculated with equation (2) and (3) and the power loss of NSD2622N can refer to equation (4).

$$P_{RLSRC} \approx 0.5 \times Q_G \times \left(V_{DDL} + V_{LVEE}\right) \times f_{SW} \times \frac{R_{LSRC}}{R_{OH}+R_{LSRC}} \quad (2)$$

$$P_{RLSNK} \approx 0.5 \times Q_G \times \left(V_{DDL} + V_{LVEE}\right) \times f_{SW} \times \frac{R_{LSNK}}{R_{OL}+R_{LSNK}} \quad (3)$$

$$P_{IC} \approx V_{CC} \times (2 \times Q_G \times f_{SW} + I_{VCC_Q} + I_{LDO5} + \frac{1}{R_{L2}}) + V_{BST} \times (2 \times Q_G \times f_{SW} + I_{BST_Q} + \frac{1}{R_{H2}}) - 2 \times (P_{RLSRC} + P_{RLSNK}) \quad (4)$$

P_{RLSRC}: the power dissipation of turn-on resistor
P_{RLSNK}: the power dissipation of turn-off resistor
P_{IC}: the total power dissipation of NSD2622N
Q_G: the gate charge of GaN HEMT
V_{DDL}: the voltage of VDDL
V_{DDH}: the voltage of VDDH
f_{sw}: the switching frequency
R_{LSRC}: the turn-on resistor
R_{LSNK}: the turn-off resistor
R_{OH}: the output pull-up resistor of NSD2622N. The typical value is 0.5Ω
R_{OL}: the output pull-down resistor of NSD2622N. The typical value is 1.4Ω
V_{CC}: the voltage of VCC
I_{VCC_Q}: the quiescent current of VCC
V_{BST}: the voltage of BST
I_{BST_Q}: the quiescent current of BST
I_{LDO5}: the load current of LDO5
R_{L2}: the resistor between LFB and PGND
R_{H2}: the resistor between HFB and SW

8.4. PCB Layout

PCB layout is important to get optimal performance. Some of the layout guidelines to be followed are listed below:

1) The bypass capacitors connected on VCC, LDO5, LVEE, VDDL, BST, HVEE, VDDH should be placed as close to their respective pins as possible. Their ESR and ESL should be low.
2) A low ESR and low ESL capacitor should be placed between LVP and LVN. It should be placed as close to LVP and LVN as possible.
3) A low ESR and low ESL capacitor should be placed between HVP and HVN. It should be placed as close to HVP and HVN as possible.
4) The trace impedance between SGND and PGND should be low.
5) The driver should be placed close to the GaN HEMTs. PGND and SW should be connected with the GaN HEMTs Kelvin return. The source and sink gate drive resistors should be placed as close to the GaN HEMTs as possible. The lengths of gate drive loop should be short to minimum the parasitic inductance.

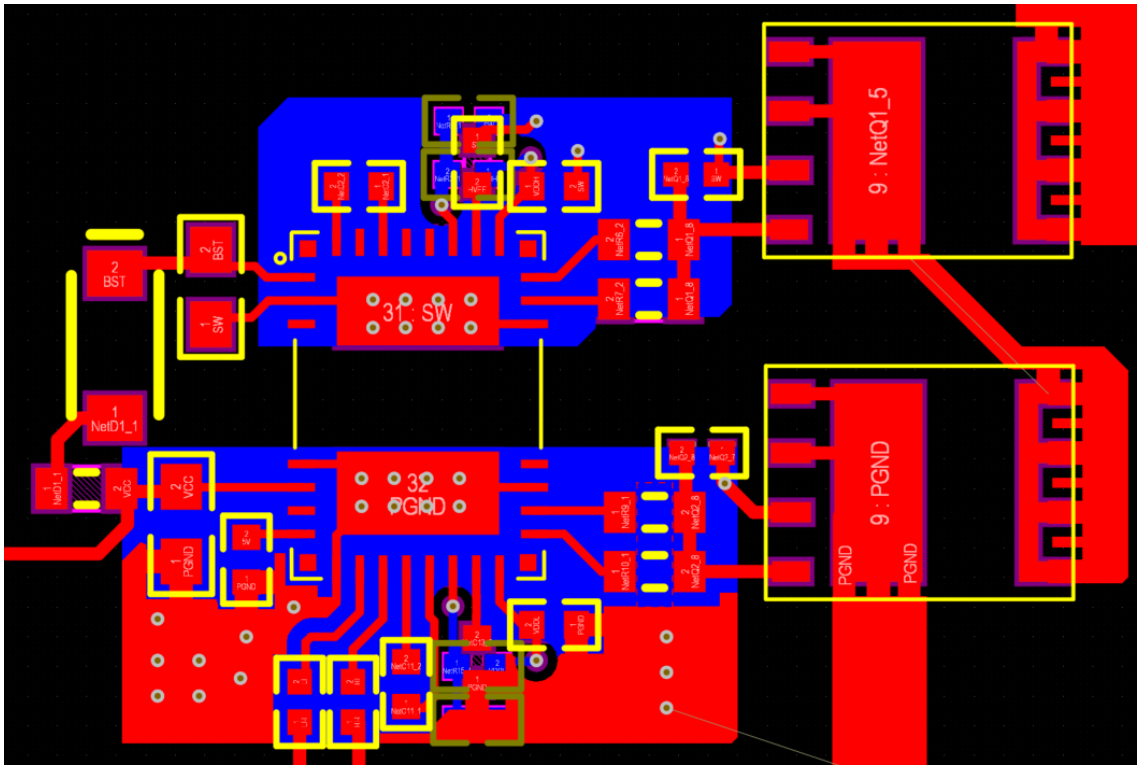
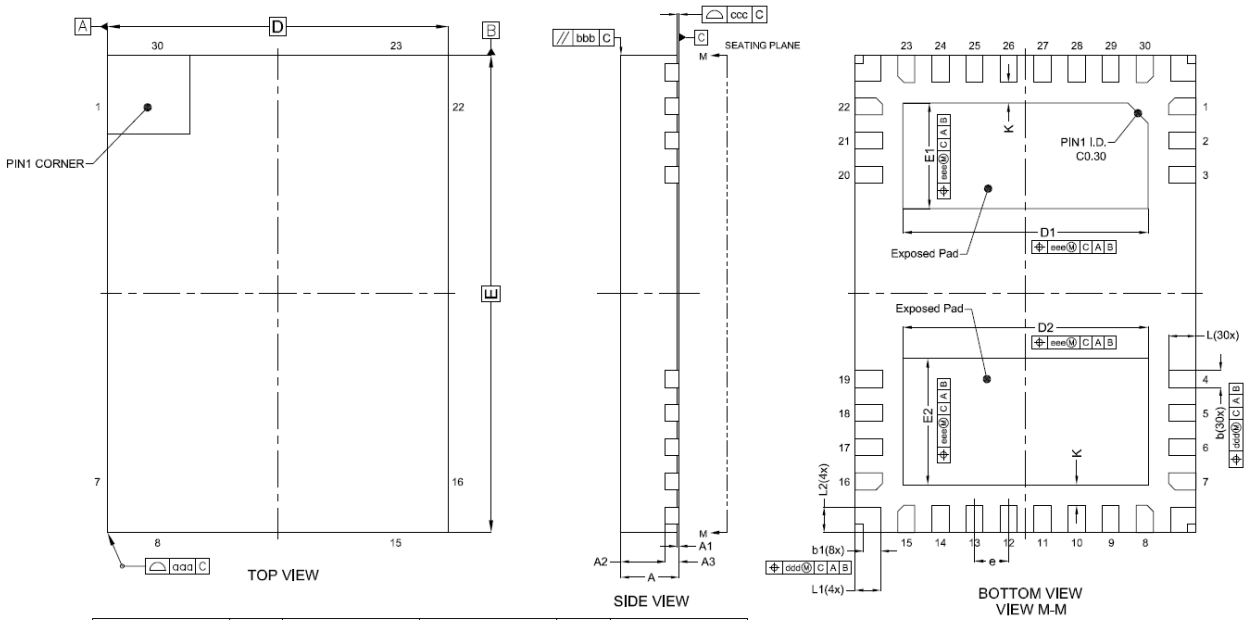


Figure 8.3 PCB Layout Example

9. Package information



DESCRIPTION		SYMBOL	MILLIMETER		
			MIN	NOM	MAX
TOTAL THICKNESS		A	0.80	0.85	0.90
STAND OFF		A1	0.00	---	0.05
MOLD THICKNESS		A2	0.60	0.65	0.70
L/F THICKNESS		A3	0.203 REF		
BODY SIZE	X	D	4.90	5.00	5.10
	Y	E	6.90	7.00	7.10
LEAD PITCH		e	0.50 BSC		
LEAD WIDTH		b	0.20	0.25	0.30
		b1	0.20	0.25	0.30
LEAD LENGTH		L	0.35	0.40	0.45
		L1	0.325	0.375	0.425
		L2	0.325	0.375	0.425

DESCRIPTION		SYMBOL	MILLIMETER		
			MIN	NOM	MAX
EP SIZE	X	D1	3.55	3.60	3.65
	Y	E1	1.50	1.55	1.60
	X	D2	3.55	3.60	3.65
	Y	E2	1.80	1.85	1.90
LEAD EDGD TO EP EDGE		K	0.30 REF		
TOLERANCE OF FORM AND POSITION					
GEOMETRIC TOLERANCE		aaa	0.10		
MOLD FLATNESS		bbb	0.10		
LEAD COPLANARITY		ccc	0.08		
LEAD POSITION OFFSET		ddd	0.10		
EXPOSED PAD OFFSET		eee	0.10		

NOTES

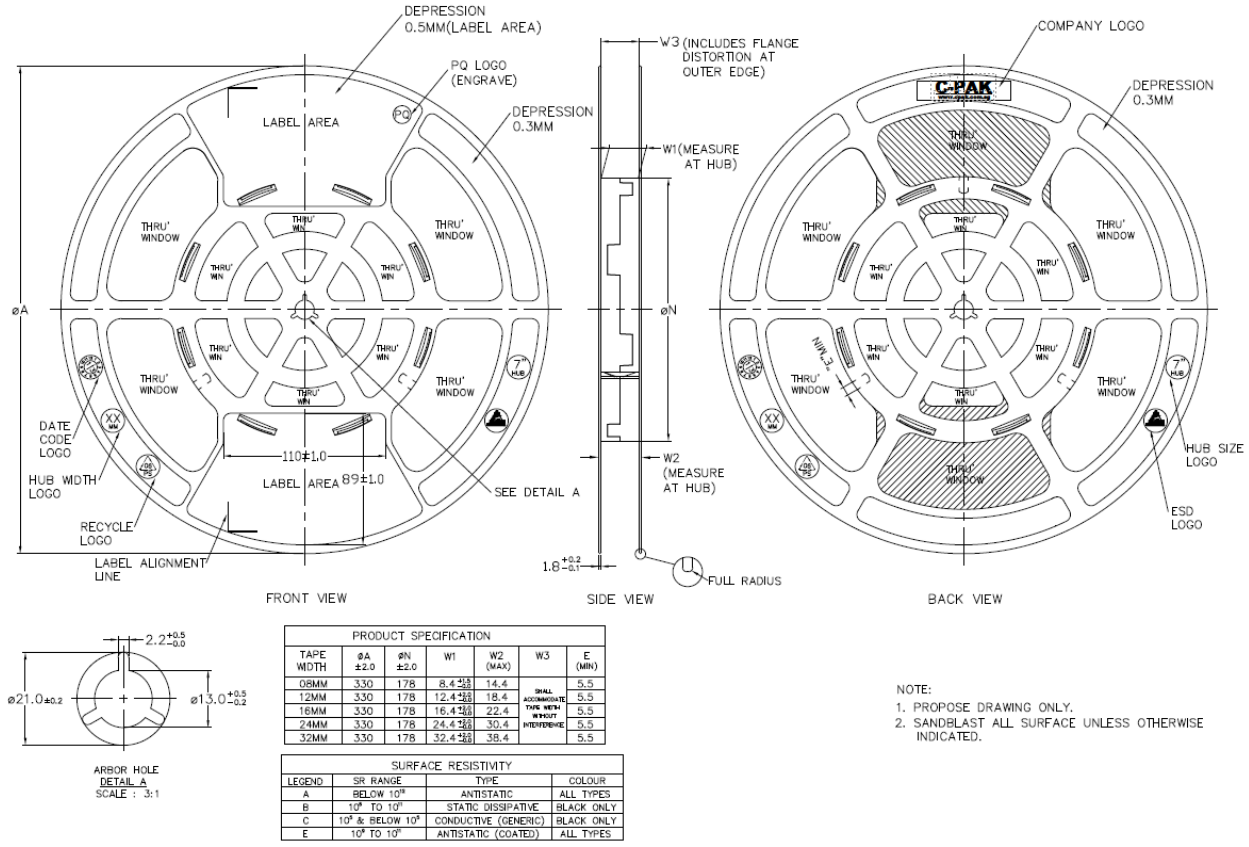
1,0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 9.1 QFN30 Package Shape and Dimension

10.Ordering Information

Part No.	*Driver-side UVLO TYP.*	*Temperature*	*Auto-motive*	*Package Type*	*MSL*	*SPQ*
NSD2622N-DQAER	4.5V	-40 to 125℃	No	QFN30	3	3000
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.						

11.Tape and Reel Information



PRODUCT SPECIFICATION

TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4	18.4		5.5
16MM	330	178	16.4	22.4		5.5
24MM	330	178	24.4	30.4		5.5
32MM	330	178	32.4	38.4		5.5

SURFACE RESISTIVITY

LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{5}	ANTISTATIC	ALL TYPES
B	10^{5} TO 10^{8}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{9}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES

Figure 11.1 Reel information of QFN30

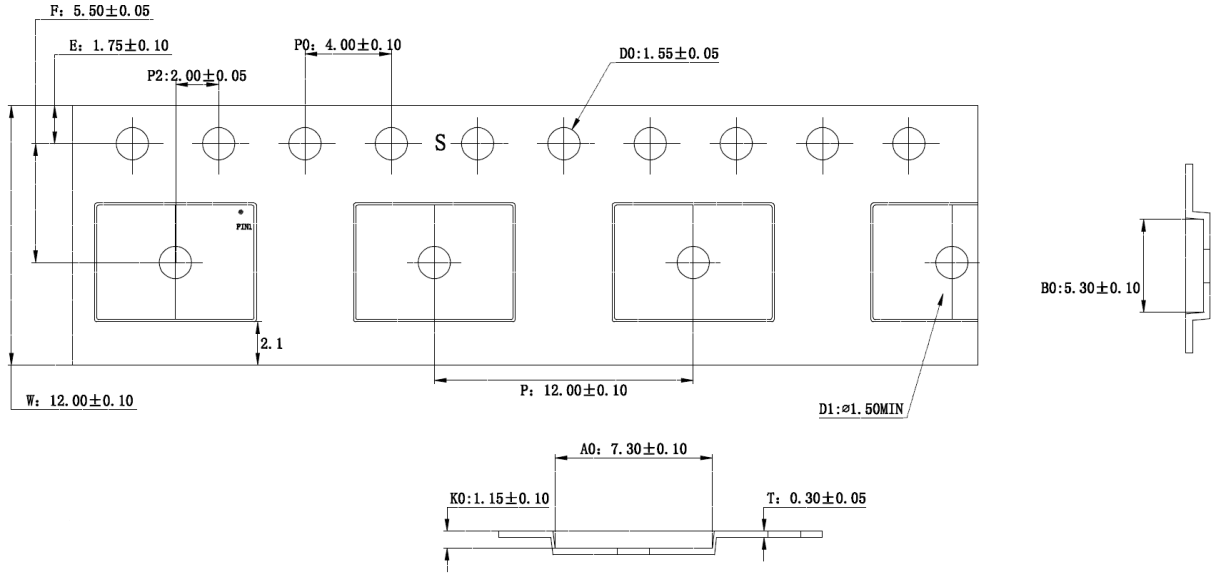


Figure 11.2 Tape information of QFN30

12.Revision History

Revision	Description	Date
1.0	Initialization	2025/02/14

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