NOVOSENSE

NSD2012N
Single Channel Gate Driver for GaN
Datasheet (EN) 1.0

Product Overview

The NSD2012N is a single channel driver designed to drive enhancement-mode GaN HEMT. The NSD2012N has separated gate outputs allowing independent adjustment of the switching-on and switching-off capability by changing impedance for gate loop. The positive bias is maintained by an internal voltage regulator, with adjustable output from 5V to 6.5V. This device also integrates negative bias, with adjustable output from -0.5V to -2.5V, thus avoid GaN HEMT falsely turn on due to cross-talk in high voltage or high -power conditions.

In addition, the NSD2012N also offers a fixed 5V linear regulator, as the power supply to external circuit, e.g., digital isolators.

The driver features undervoltage lockout (UVLO)and over-temperature protection (OTP) to ensure the systems work properly.

The device operates in the industrial temperature range, -40°C to 125°C, and is available in a compact 3.0 x 3.0mm QFN package.

Key Features

- 5V to 6.5V adjustable positive output voltage
- -0.5V to -2.5V adjustable negative bias
- Independent 2A source and 4A sink current
- 5V LDO output for external circuit, e.g., digital isolators.
- 6.5ns typical rise time (1nF load)
- 6.5ns typical fall time (1nF load)
- 5ns typical minimum input pulse width
- 23ns typical propagation delay
- 5ns typical pulse distortion
- UVLO and over-temperature protection
- Operation temperature: -40℃~125℃
- RoHS-compliant packages: Pb-Free, Halogen-Free

Applications

- DC-to-DC Converter
- AC to DC Converter
- Switching-Mode Power Supplies
- Solar Power and UPS

Device Information

Part Number	Package	Body Size
NSD2012N-DQAFR	QFN12	3.0mm*3.0mm*0.65mm

Functional Block Diagram

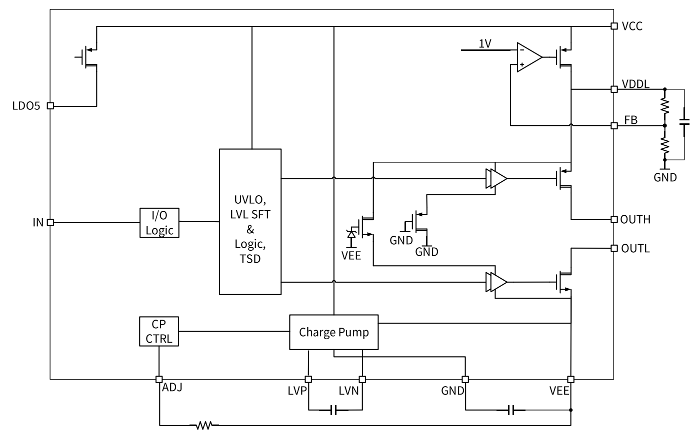

Figure 0.1 NSD2012N Block Diagram

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1. Pin Configuration and Functions

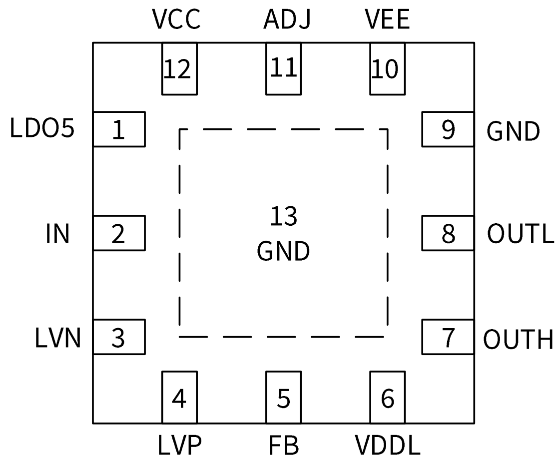


Figure 1.1 NSD2012N Top View

Table 1.1 NSD2012N Pin Configuration and Description

Pin	Name	Function
1	LDO5	Internal linear regulated 5V voltage output.
2	IN	PWM logic signal Input.
3	LVN	Negative terminal of charge pump.
4	LVP	Positive terminal of charge pump.
5	FB	Feedback voltage for VDDL adjustment
6	VDDL	Linear regulator voltage output. Connect a resistor between this pin and VFB to set the driver output voltage. The detailed information refers to Figure 7.3
7	OUTH	Driver sourcing output
8	OUTL	Driver sinking output
9,13	GND	Reference ground.
10	VEE	Negative rail voltage for the turn-off. The typical output voltage is -2.5V when ADJ was floating.
11	ADJ	VEE output voltage adjustment pin. The detailed information refers to Table 7.1
12	VCC	Power supply for logic and regulator.

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
Driver Supply Voltage	VCC to GND	-0.3	18	V
	VCC to VEE	-0.3	18	V
	VCC to GND for <100ns	-0.3	20	V
	VCC to VEE for <100ns	-0.3	20	V
Regulator Output Voltage	VDDL to GND	-0.3	9	V
Negative Regulator Output Voltage	VEE to GND	-5	0	V
Negative Regulator Output Voltage	VDDL to VEE	-0.3	9	V
Input Signal Voltage	IN to GND	-10	18	V
Driver Output voltage	OUTH, OUTL	VEE-0.3	VDDL+0.3	V
Adjustable voltage	ADJ to GND	0.3	5	V
Regulator output voltage	LDO5 to GND	-0.3	5.5	V
Charge pump negative voltage	LVN to GND	-5	1.5	V
Charge pump positive voltage	LVP to GND	-0.3	5	V
Feedback voltage	FB to GND	-0.3	5	V
Storage temperature	T_{stg}	-55	150	°C
Operation junction temperature	T_J	-40	150	°C

3. ESD Ratings

	Ratings	Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC Q100-002	±2000	V
	Charged device model (CDM), per AEC Q100-011	±500	V

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
Driver Supply Voltage	VCC to GND	5	15	V
Gate to Source Voltage	OUTH, OUTL	VEE	VDDL	V
Input Signal Voltage	IN to GND	-5	VCC	V
Regulator output voltage	VDDL to GND	5	6.5	V
Ambient Temperature	Ta	-40	125	°C

5. Thermal Information

Parameters	*Symbol*	*QFN*	*Unit*
Junction-to-ambient thermal resistance[1)]	R_{JA}	70.1	°C/W
Junction-to-case(top) thermal resistance[1)]	$R_{JC\ (top)}$	67.3	°C/W
Junction-to-top characterization parameter[2)]	Ψ_{JT}	10.1	°C/W
Junction-to-board characterization parameter[2)]	Ψ_{JB}	22.3	°C/W

1) Standard JESD51-7 High Effective Thermal Conductivity Test Board (2s2p) in an environment described in JESD51-2a.
2) Obtained by Simulating in an environment described in JESD51-2a.

6. Specifications

6.1. Electrical Characteristics

VCC=12V, For typical values, Ta= 25°C. For min/max values, Ta = -40°C to 125°C, unless otherwise noted.

Parameters	*Symbol*	*Min*	*Norm*	*Max*	*Unit*	*Comments*
Bias Current						
VCC Quiescent Current With charge pump	I_{VCC_Q}		2.5		mA	IN= 0V , VDDL=6V, C_{VEE}=680nF
VCC Operating Current With charge pump	I_{VCC_O}		13.2		mA	IN=500kHz, VDDL=6V, 1nF load C_{VEE}=680nF
Under Voltage Lockout (UVLO)						
VCC UVLO Rising Threshold	V_{VCC_ON}	4.2	4.5	4.8	V	
VCC UVLO Falling Threshold	V_{VCC_OFF}		4		V	
VCC UVLO Hysteresis	V_{VCC_HYS}		0.5		V	
Regulator Supply Characteristic						
LDO5 output voltage	V_{LDO5}	4.75	5	5.25	V	
LDO5 output current				50	mA	Cap>=100nF
Driver output voltage						
UVLO Positive Threshold on VDDL	V_{VDDL_UV+}	4.2	4.5	4.8	V	
UVLO Negative Threshold on VDDL	V_{VDDL_UV-}		4.25		V	
VDDL UVLO hysteresis	V_{VDDL_UVH}		0.25		V	
Reference voltage	V_{FB}	0.97	1	1.03	V	
Negative charge pump						
Negative output voltage	V_{VEE}	-3	-2.5	-2	V	ADJ is floating
Input Pin Characteristics						
Input putdown current	I_{IN}		30		uA	Input=5V
Logic High Input Threshold	V_{IN_H}	1.7	2.0	2.2	V	
Logic Low Input Threshold	V_{IN_L}	0.9	1.1	1.3	V	
Logic Hysteresis	V_{IN_HYS}		0.9		V	
Output Pin Characteristics						
Low-level output Voltage, V_{OUTL}-V_{VEE}	V_{OL}		5		mV	I_OUTL=10mA
High-level output Voltage, V_{VDDL}-V_{OUTH}	V_{OH}		14		mV	I_OUTH=10mA
Peak source current[1)]	I_{OUTH}		2		A	VDDL=6V
Peak sink current[1)]	I_{OUTL}		4		A	VDDL=6V
Thermal Shutdown						
Thermal Shutdown Temperature[1)]	T_{SD}		165		°C	
Thermal Shutdown Hysteresis[1)]	T_{SH}		20		°C	
Operation Frequency						
Maximum Operation Frequency[1)]	F_{sw_max}			4	MHz	

1) Not test covered. Guaranteed by design.

6.2. Switching Characteristics

VCC=12V, For typical values, Ta= 25°C. For min/max values, Ta = -40°C to 125°C, unless otherwise noted

Parameters	*Symbol*	*Min.*	*Norm.*	*Max.*	*Unit*	*Comments*
Turn off propagation delay time	T_{phl}		23		ns	No load
Turn on propagation delay time	T_{plh}		23		ns	No load
Pulse width distortion	t_{PWD}		5	10	ns	No load
Rise time	T_r		6.5		ns	Load=1nF, VDDL=6V
Fall time	T_f		6.5		ns	Load=1nF, VDDL=6V
Minimal input PWM pulse	t_{PWM_MIN}		5	10	ns	

6.3. Typical Performance Characteristics

VCC=12V, Ta=25°C，unless otherwise notes.

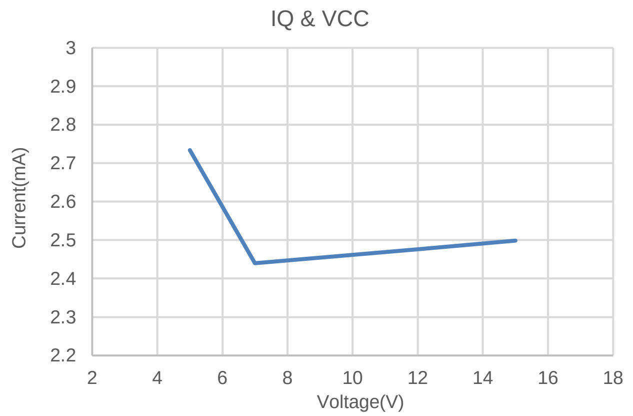


Figure 6.1 Quiescent current vs Voltage

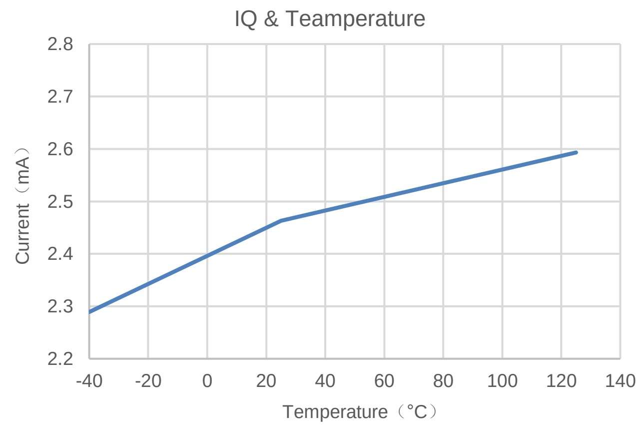


Figure 6.2 Quiescent current vs Temperature

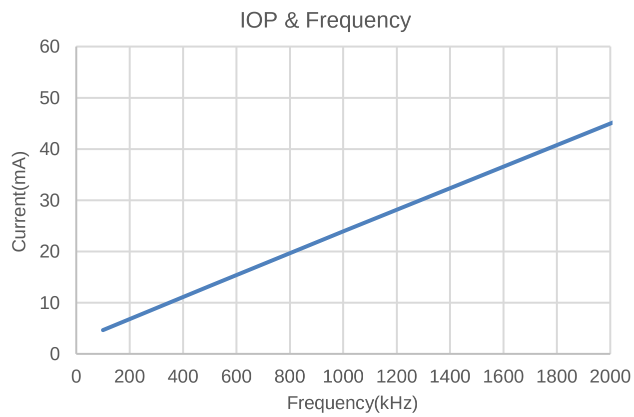


Figure 6.3 Operation current vs Frequency @1nF load

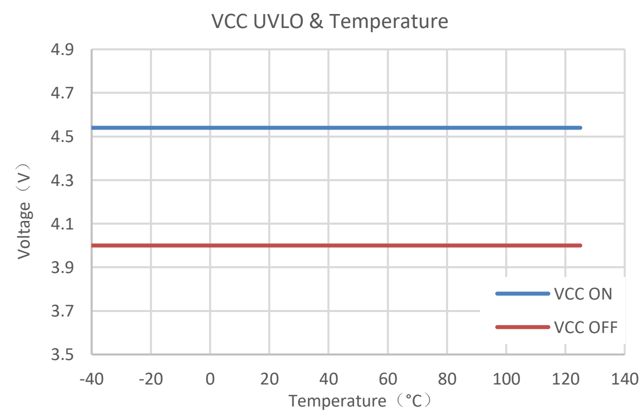


Figure 6.4 VCC UVLO vs Temperature

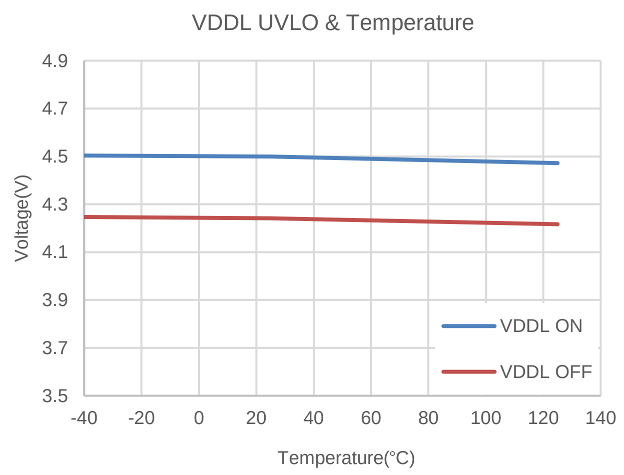


Figure 6.5 VDDL UVLO vs Temperature

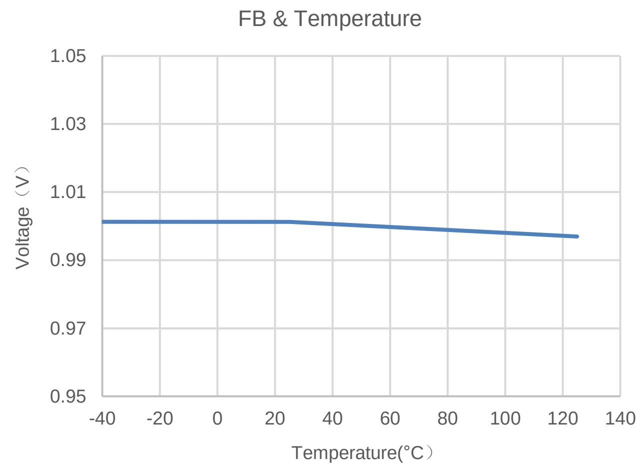


Figure 6.6 FB Vs Temperature

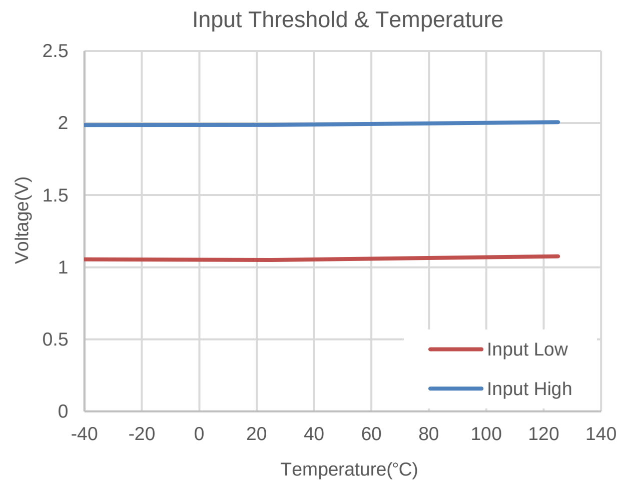


Figure 6.7 Input logic threshold vs Temperature

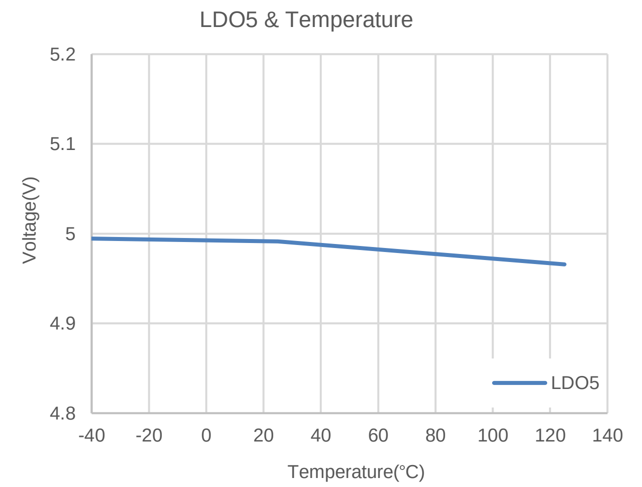


Figure 6.8 LDO5 output voltage & Temperature

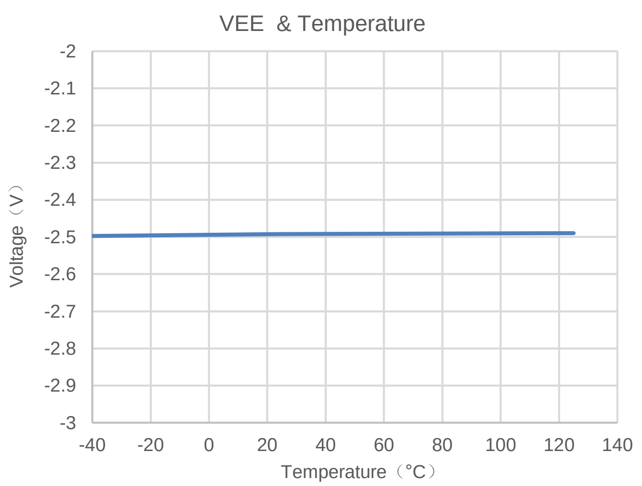


Figure 6.9 VEE output voltage & Temperature

6.4. Parameter Measurement Information

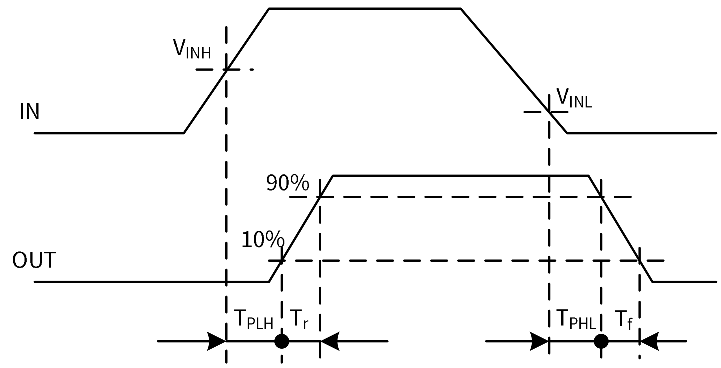


Figure 6.10 Propagation Delay, Rise and Fall time

7. Function Description

7.1. Overview

The NSD2012N is a single channel driver designed to drive enhancement-mode GaN HEMT. The NSD2012N has separated gate outputs allowing independent adjustment of the switching-on and switching-off capability by changing impedance for gate loop. It provides the negative switching off function to improve the GaN HEMT community. Its negative output voltage can be adjusted through the external resistor. It provides the positive voltage turn-on regulator which can be adjusted the output voltage through the external resistor. In addition, it offers a 5V LDO output and OTP function.

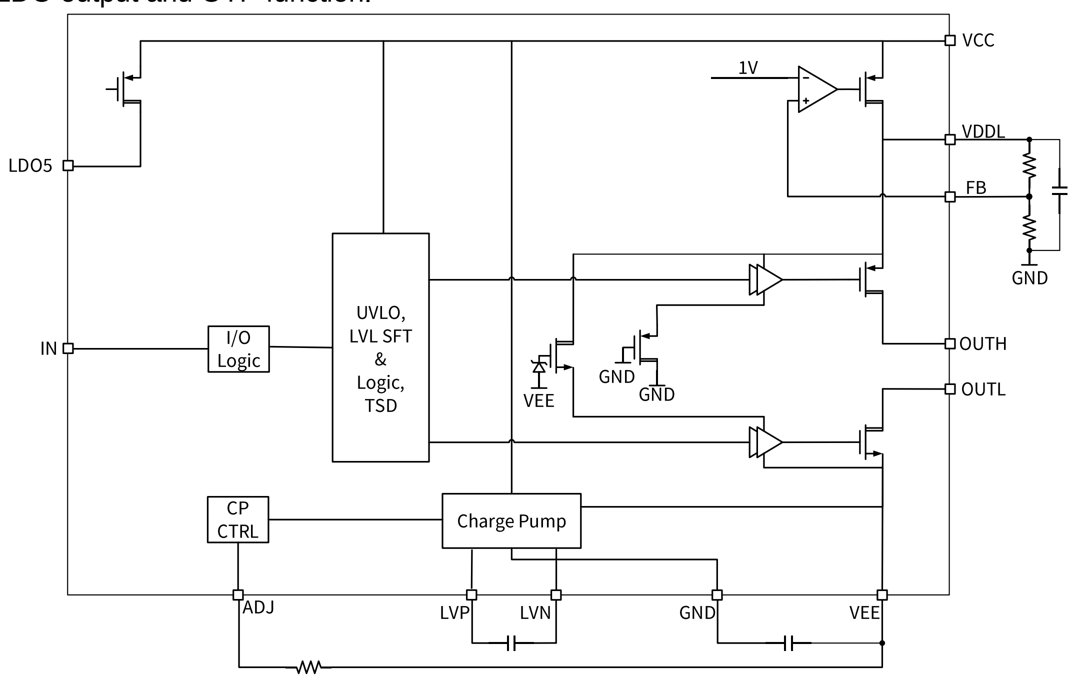


Figure 7.1 NSD2012N Functional Block Diagram

7.2. Under Voltage Lock Out (UVLO)

The NSD2012N has internal under voltage lock out (UVLO) protections. The driver output is held low by an active clamp circuit when the supply voltage of VCC is lower than V_{VCC_ON} at power-up status or lower than V_{VCC_OFF} after power-up, regardless of the status of the input pins.

The 0.5V UVLO hysteresis on VCC is provided prevent chatter noise from VCC and allow small drops in power supply which usually happens during startup. When the voltage of VCC is more than V_{VCC_POR} which is approximate 2V, the positive regulator and the charge pump begin to operate and the negative voltage VEE and the positive voltage VDDL begins to setup. In order to reduce the rush current during the startup, the negative charge current is limited to only about 3mA from the negative regulator VEE output. When the voltage of VDDL rises to be more than its UVLO threshold voltage, the negative voltage will quickly fall down to -2.5V if ADJ floats. In Figure 7.2, t_{PUD} is the power up delay time which is about 60us based on the parameters in Table 8.1. It should be noted that t_{PUD} was related to the capacitor at VDDL.

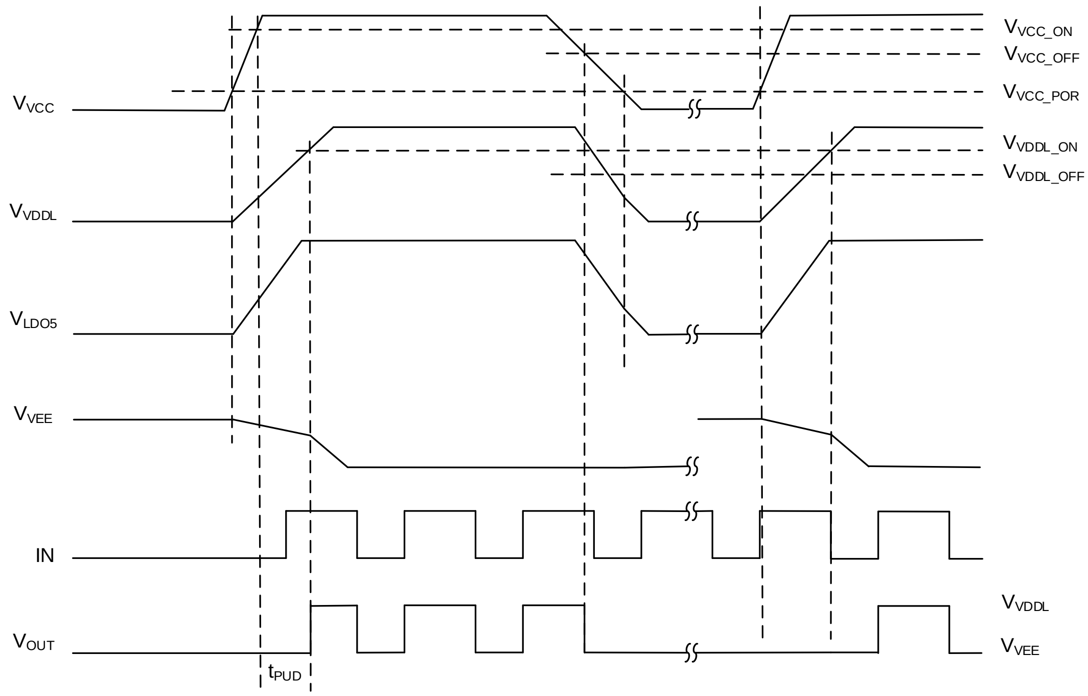


Figure 7.2 UVLO Diagram

7.3. Regulator 5V Output (LDO5)

The NSD2012N integrated a 5V linear regulator. It can be used to provide the power for the digital insulator or other device and its maximum of output current is 50mA. In order to keep the output voltage stable, a capacitor should be placed between LDO5 and GND pin. The capacitance can be from 100nF to 1uF. It should be noted that the bigger capacitance, the longer 5V regulator set up.

7.4. Feedback Voltage (FB) and Positive Regulator Output (VDDL)

The NSD2012N integrated a positive linear regulator. FB is the positive input to the internal error amplifier and used to control the VDDL output voltage. The output voltage can be calculated following the below equation (1). The recommended range of resistor R2 is from 1kΩ to 20kΩ.In order to keep the output voltage on VDDL stable, a capacitor should be placed between VDDL and GND pin. The value of capacitor C1 can be from 470nF to 1uF. The bigger value of capacitor C1, the longer power delay up. The VDDL begins to build up if VCC voltage is more than V_{VCC_POR} which is appropriated 2V. The acceptable output voltage range is from 5V to 6.5V. If the output voltage is more than 6.5V, the device may be damaged.

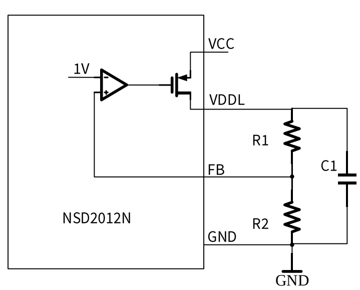


Figure 7.3 Positive Regulator Diagram

$$V_{VDDL} = \frac{R_1+R_2}{R_2} \times 1V \quad (1)$$

7.5. Adjustable Negative (ADJ/VEE) And Charge Pump (LVP/LVN)

The NSD2012N integrated a negative voltage to return the sink current. The negative voltage generation is based on the charge pump technology. When VCC voltage is more than V_{VCC_POR} voltage, the negative voltage begins to build up. When the ADJ floats, the typical negative output voltage is -2.5V and its tolerance is ±0.5V. In order to keep the output voltage on VEE stable, a capacitor should be placed between VEE and GND pin. The capacitance range is from 680nF to 1uF. It should be noted that the bigger capacitance, the longer power delay up. The different negative voltage can be achieved by adjusting the resistor between ADJ and VEE. The corresponding relationship between the negative voltage and the resistance is shown in Table 7.1.

Table 7.1 Resistance value connected to VEE

R_{ADJ}	Unit	Negative voltage（VEE）	Unit
47	KΩ	-0.5	V
110	KΩ	-1.0	V
232	KΩ	-1.5	V
Floating	KΩ	-2.5	V

LVP and LVN is respectively the positive pin and the negative pin of charge pump circuit. One capacitor should be placed between LVP and LVN to normal operate. A 100nF capacitor is recommended.

7.6. Input and Output Logic Table

When the voltage on VCC is less than its UVLO, the output is low level. When the voltage on VCC and VDDL are more than their UVLO, the user can refer to Table 7.2.

Table 7.2 NSD2012N Output status vs. Input status

Input Pin	Output Pins		NOTE
IN	OUTH	OUTL	
L	Open	L	
H	H	Open	
Floating	Open	L	

7.7. Output Stage (OUTH/OUTL)

The NSD2012N provides 2A source and 4A sink peak current output capability. The user can select the different resistance to adjust the turn-on and turn-off slew of GaN HEMT to optimize the system performance. The output OUTL is active pulled down in undervoltage condition which guarantee the gate voltage of GaN HEMT lower than its threshold voltage. In order to reduce the ringing caused by parasitic inductance on PCB, the NSD2012N should be located near the gate of GaN HEMT and the circuit loop should be as short as possible. To prevent the gate voltage overshoot of GaN HEMT, it is suggested that the gate turn-on driver resistor was more than $2\sqrt{\frac{L_G}{C_{GS}}}$ and the turn-off resistor was more than 1Ω. L_G is the drive loop inductance and C_{GS} is the GaN HEMT input capacitance.

7.8. Overtemperature Protection (OTP)

The NSD2012N provides the OTP function. When the junction temperature of NSD2012N is arrived 165℃, OUTH will be open and OUTL be pull-down. Then the junction temperature begins to decrease. When the junction temperature drops below some value, the device starts to operate again. The typical value of OTP hysteresis is 20℃.

8. Application Note

8.1. Typical Application Circuit

Figure 8.1 shows a typical half-bridge configuration by using the NSD2012N.

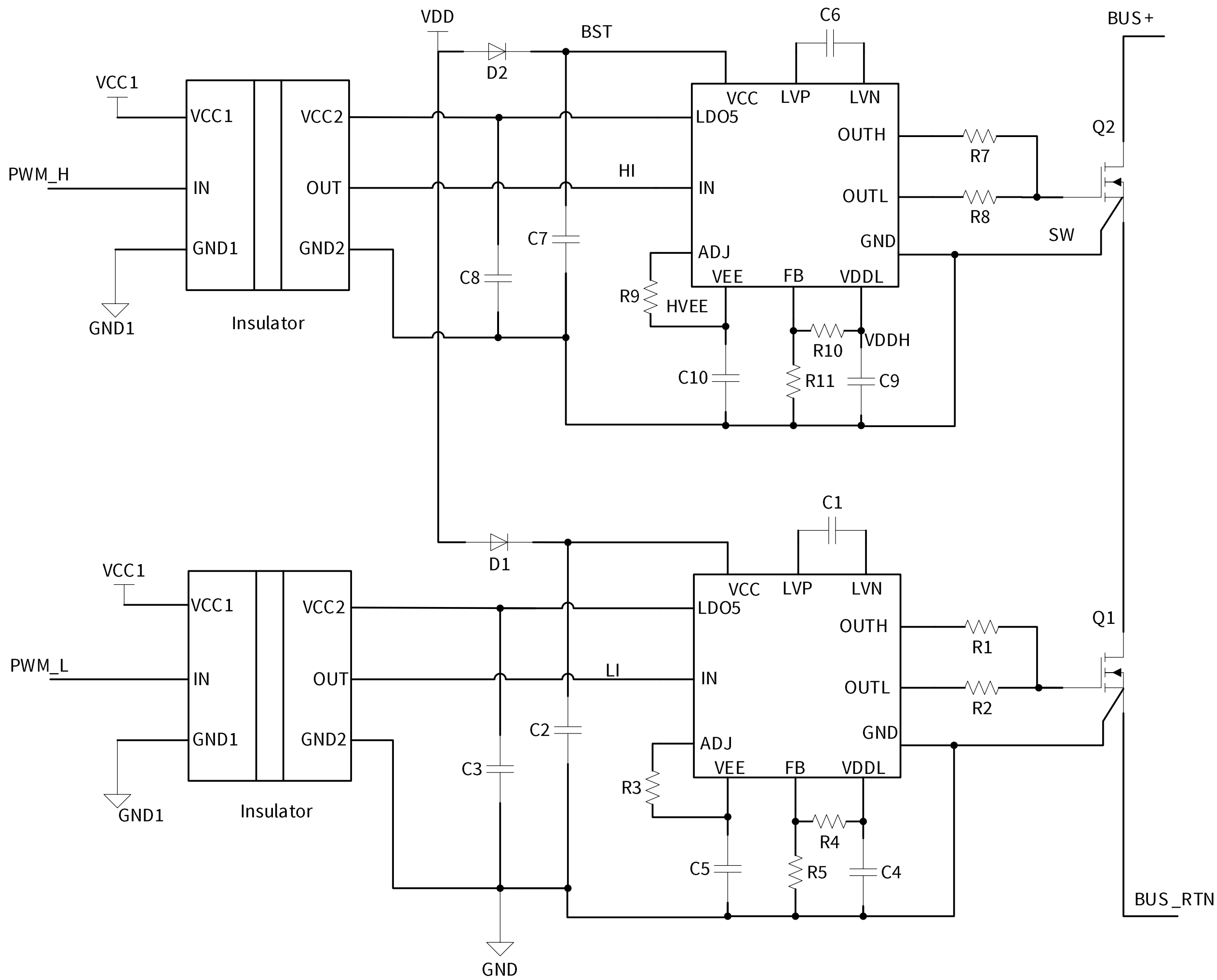


Figure 8.1 Typical Simplified Application Schematic

Supply voltage (VCC): VCC is the power supply of NSD2012N. When the VCC voltage is lower than its UVLO, the OUTH will be open and OUTL be pulled down. A bypass capacitor, C_2, which is more than 1uF is required and should be located as close as possible to VCC and GND. A low ESR and low ESL capacitor is recommended to use. It should be noted that an inrush current of about 200mA occurs during the startup which the duration is tens of microseconds.

5V Regulator (LDO5): It can output provide the power for the digital isolator. Its maximum output current is 50mA.If LDO5 is not used, a capacitor C_3 should be connected directly between LDO5 and GND. The recommended capacitance is from 100nF to 1uF.

Driver Output (OUTH and OUTL): OUTH controls turn-on of the GaN HEMT and OUTL controls turn-off of the GaN HEMT. The gate of GaN HEMT will be pull up to VDDL through OUTH during turn-on and pull down to VEE through OUTL during turn-off.

Ground (GND): GND is the reference ground. For GaN HEMT included a source Kelvin return, a direct connection should be made from GND to the GaN HEMT Kelvin return.

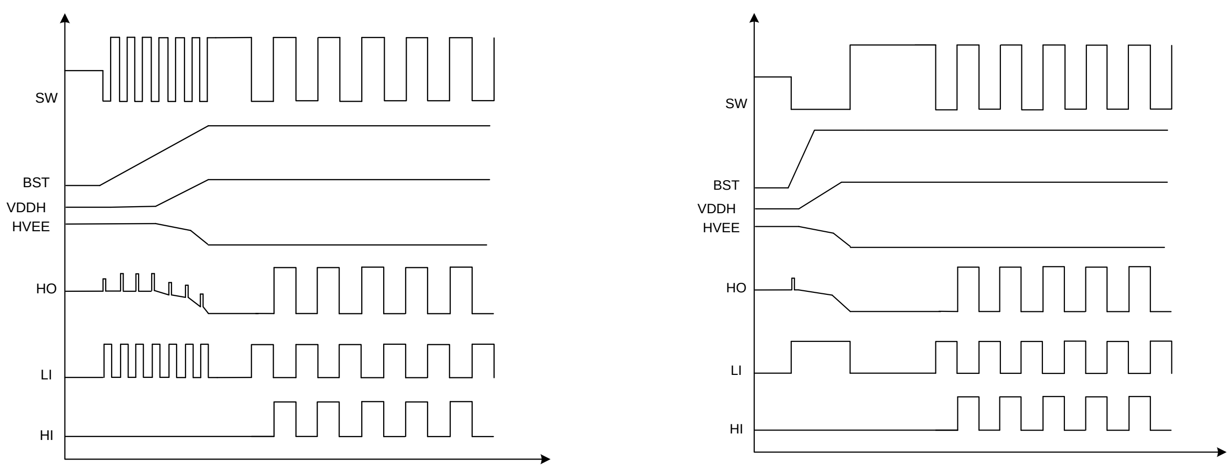
The BOM in Table 8.1 was used in the lab to verify the performance of NSD2012N.

Table 8.1 Bill of Materials for the reference

Designator	Qty	Value	Description	Part number	Manufacturer
C_4, C_9	2	470nF	Cap, CERM, 470nF,10V, +/-10%, X7R	GRM155R71A474KE01	MuRata
C_5、C_{10}	2	680nF	Cap, CERM, 680nF,10V, +/-10%, X7S	GCM155C71A684KE38	MuRata
C_1, C_3, C_6	3	100nF	Cap, CERM, 0.1uF, 25V, +/-10%, X7R,	GRM155R71E104KE14	MuRata
C_2, C_7	2	1uF	Cap, CERM, 1uF, 50V, +/-10%, X7T	GRM188D71H105KE01	MuRata
D_2	1	600V	Diode, Super-fast, 600V，1A, SOD123F	SF1JWF-7	Diodes Inc.
R_2, R_8	2	2	RES, 2，1%, 0603	0603WAF200KT5E	Uni-Royal
R_5, R_{11}	2	10k	RES, 10k，1%, 0402	0402WGF1002TCE	Uni-Royal
R_4, R_{10}	2	49.9k	RES, 49.9k，1%, 0402	0402WGF4992TCE	Uni-Royal

8.2. Startup Timing Sequence of High Side Driver for Half Bridge

If the bootstrap diode is used to provide the voltage for high side driver in Figure 8.1, the startup time sequence of mode (b) is recommended.



Mode (a) (Not Recommended)

Mode (b)

Figure 8.2 Startup Timing Sequence

Before starting up, the voltage of BST and the voltage of the negative voltage HVEE of the high side driver were not established. When the startup timing sequence of mode a) is adopted, the rise speed of BST voltage is slow and the established time of the negative voltage HVEE will be long and the gate of the high side GaN HEMT cannot be pulled down to HVEE during the HVEE voltage setup. When the low side GaN HEMT is repeatedly switched on and off during BST setup, the gate of the high side GaN HEMT will be rushed to a certain positive voltage affected by its Miller capacitor. It is very dangerous when this value exceeds its threshold voltage.

Before the startup, the voltage of SW node is one half of bus voltage. When using the startup timing sequence of mode b), the first pulse of the low side input signal is enough wide, both BST voltage and the negative bias HVEE of the high side driver can be effectively established. Then the gate of the high side GaN HEMT is strongly pulled down to the HVEE through the sink resistor R_8. When the low side GaN HEMT is turned on again, the gate voltage of the high side GaN HEMT is not charged to more than its threshold due to the existence of the negative voltage of the HVEE，which ensure the system to reliably operate. The first input pulse width of LI signal should be enough wide to make sure the voltage of HVEE completely setup. It should be noted that the established time of the negative bias HVEE was related to the capacitor C_{10}. The larger the capacitance of C_{10}, the longer the established time of the negative bias HVEE.

8.3. Power Dissipation Calculation

The gate of GaN HEMT will be pulled up to VDDL through the drive resistor during turn-on and pulled down to VEE through the drive resistor during turn-off. To prevent the gate voltage overshoot of GaN HEMT, it is recommended that the gate turn-on driver resistor is more than $2\sqrt{\frac{L_G}{C_{GS}}}$ and turn-off resistor is more than 1Ω. L_G is the drive loop inductance and C_{GS} is the gate capacitance of GaN HEMT. The power loss of driver resistor in Figure 8.1 can be calculated with equation (2) and (3) and the power loss of NSD2012N can refer to equation (4).

$$P_{R1} \approx 0.5 \times Q_G \times (V_{VDDL} + V_{VEE}) \times f_{SW} \times \frac{R_1}{R_{OH}+R_1} \quad (2)$$

$$P_{R2} \approx 0.5 \times Q_G \times (V_{VDDL} + V_{VEE}) \times f_{SW} \times \frac{R_2}{R_{OL}+R_2} \quad (3)$$

$$P_{IC} \approx V_{CC} \times (2 \times Q_G \times f_{SW} + I_{VCC_Q} + I_{LDO5} + \frac{1}{R_5}) - (P_{R1} + P_{R2}) \quad (4)$$

P_{R1}: the power dissipation of turn-on resistor
P_{R2}: the power dissipation of turn-off resistor
P_{IC}: the total power dissipation of NSD2012N
Q_G: the gate charge of GaN HEMT
V_{DDL}: the voltage of VDDL
f_{sw}: the switching frequency
R_1: the turn-on resistor
R_2: the turn-off resistor
R_{OH}: the output pull-up resistor of NSD2012N. The typical value is 0.5Ω
R_{OL}: the output pull-down resistor of NSD2012N. The typical value is 1.4Ω
V_{CC}: the voltage of VCC
I_{VCC_Q}: the quiescent current of VCC
I_{LDO5}: the load current of LDO5
R_5: the resistor between FB and GND

8.4. PCB Layout

PCB layout is important to get optimal performance. Some of the layout guidelines to be followed are listed below:

1) The bypass capacitors connected on VCC, LDO5, VEE, VDDL should be placed as close to their respective pins as possible. Their ESR and ESL should be low.
2) A low ESR and low ESL capacitor should be placed between LVP and LVN. It should be placed as close to LVP and LVN as possible.
3) The driver should be placed close to the GaN HEMT. GND should be connected with the GaN HEMT Kelvin return. The source and sink gate drive resistors should be placed as close to the GaN HEMT as possible. The lengths of gate drive loop should be short to minimum the parasitic inductance.

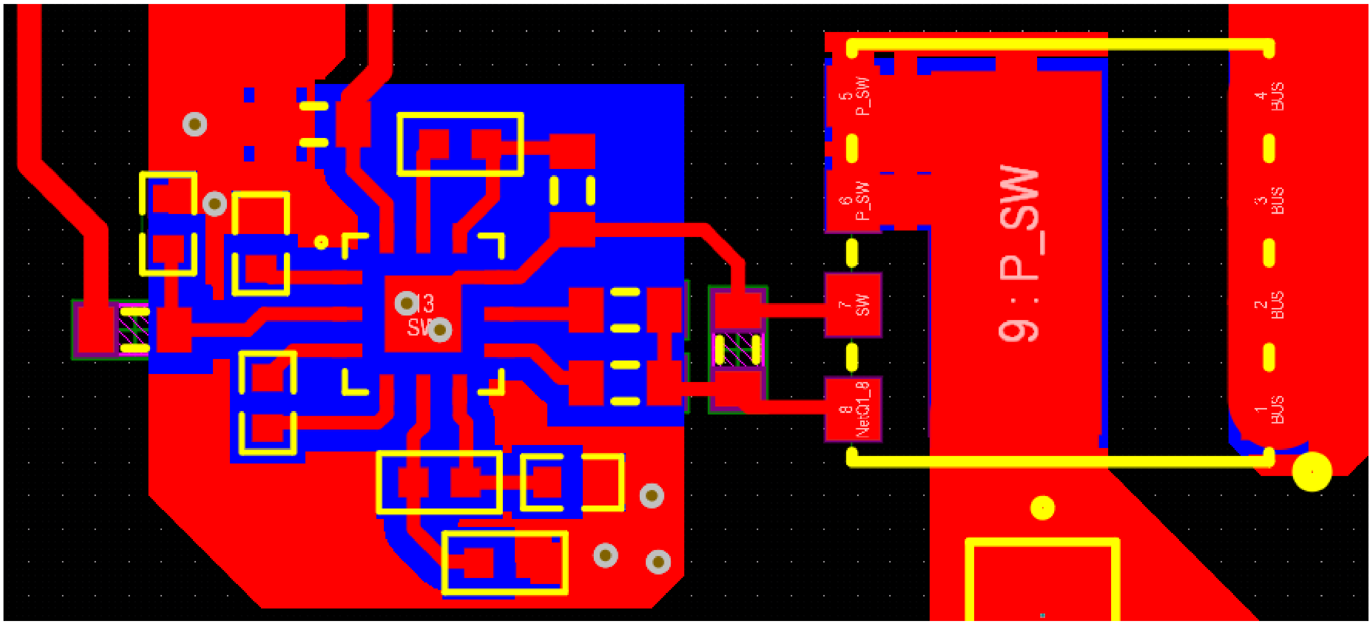
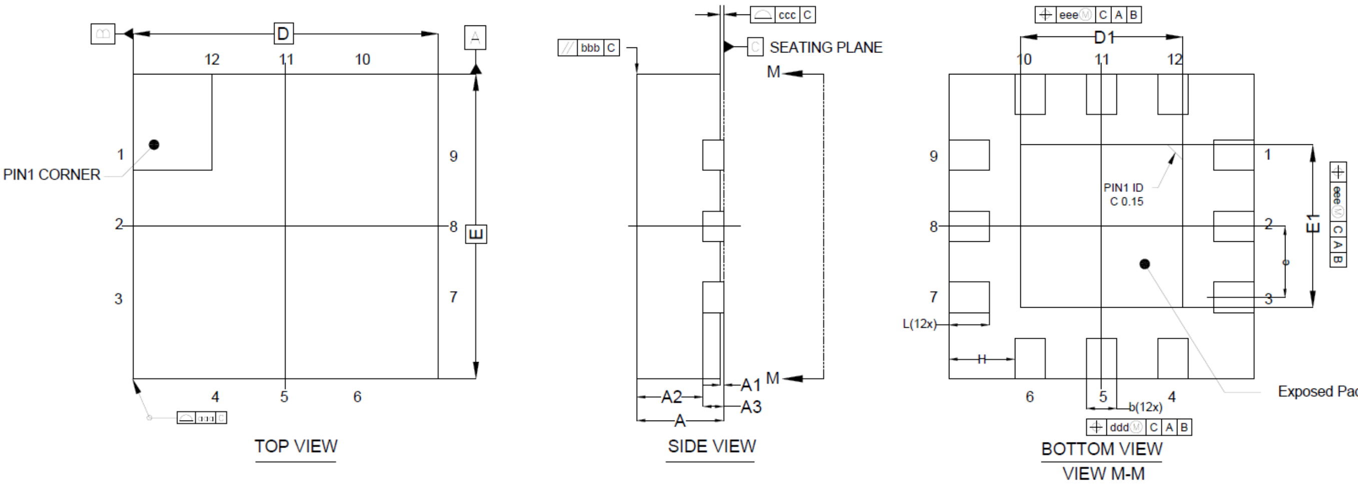


Figure 8.3 PCB Layout Example

9. Package Information



DESCRIPTION		SYMBOL	MILLIMETER		
			MIN	NOM	MAX
TOTAL THICKNESS		A	0.80	0.85	0.90
STAND OFF		A1	0.00	---	0.05
MOLD THICKNESS		A2	0.60	0.65	0.70
L/F THICKNESS		A3	0.203 REF		
BODY SIZE	X	D	2.95	3.00	3.05
	Y	E	2.95	3.00	3.05
LEAD PITCH		e	0.70 BSC		
LEAD WIDTH		b	0.25	0.30	0.35
LEAD LENGTH		L	0.35	0.40	0.45
EP SIZE	X	D1	1.55	1.60	1.65
	Y	E1	1.55	1.60	1.65
LEAD EDGD TO PKG EDGE		H	0.650 REF		
TOLERANCE OF FORM AND POSITION					
GEOMETRIC TOLERANCE		aaa	0.05		
MOLD FLATNESS		bbb	0.10		
LEAD COPLANARITY		ccc	0.08		
LEAD POSITION OFFSET		ddd	0.10		
EXPOSED PAD OFFSET		eee	0.10		

NOTES

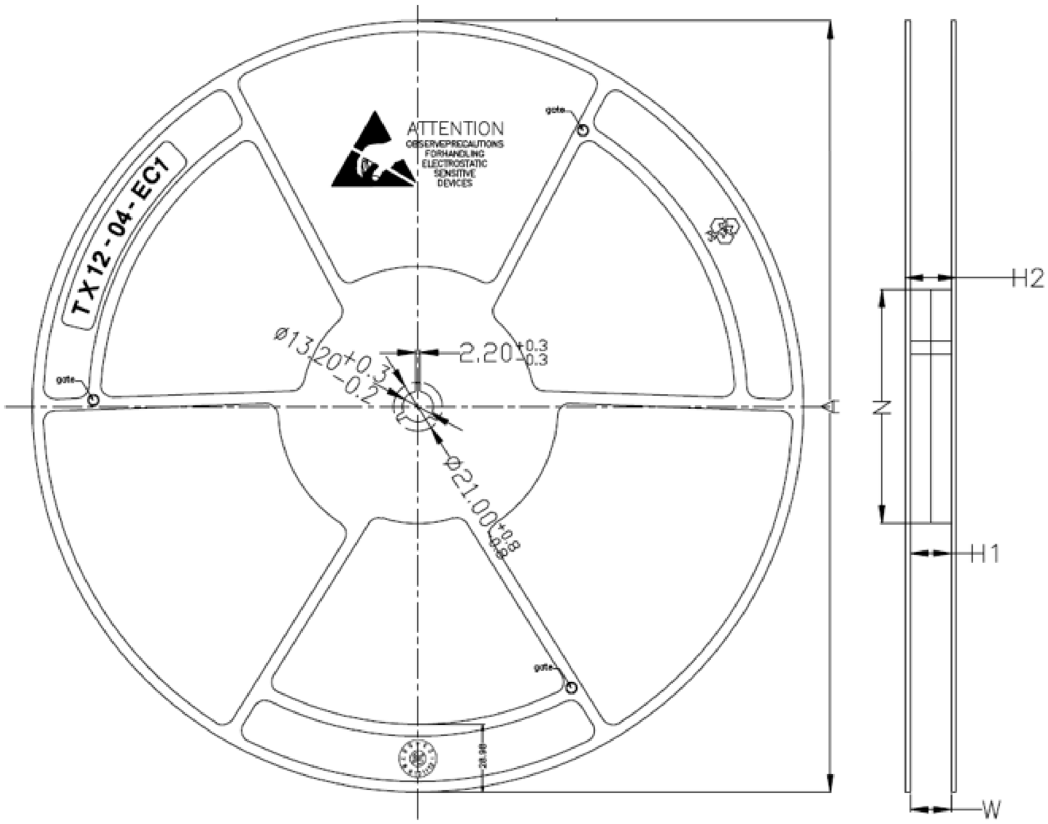
1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 9.1 QFN12 Package Shape and Dimension

10.Ordering Information

Part No.	*UVLO TYP.*	*Temperature*	*Auto-motive*	*Package Type*	*MSL*	*SPQ*
NSD2012N-DQAFR	4.5V	-40 to 125℃	No	QFN12	2	5000

11. Tape and Reel Information



NOTES:
1.MATERIAL:DISSIPATIVE(BLACK)
2.FLANGE WARPAGE:3 MM MAXIMUM 5
3.ALL DIMENSIONS ARE IN MM
4.ESD - SURFACE RESISTIVITY-10 TO 10 OHMS/SQ
5.GENERAL TOLERANCE: ±0.25 MM

PRODUCT SPECIFICATIONS					
TAPE WIDTH	ØA $^{+2}_{-2}$	ØN $^{+2}_{-2}$	H1 $^{+2}_{-0}$	H2 $^{+1}_{-1}$	W $^{+3.5}_{-0.2}$
12MM	330	100	12.4	16.6	12.4

Figure 11.1 Tape information

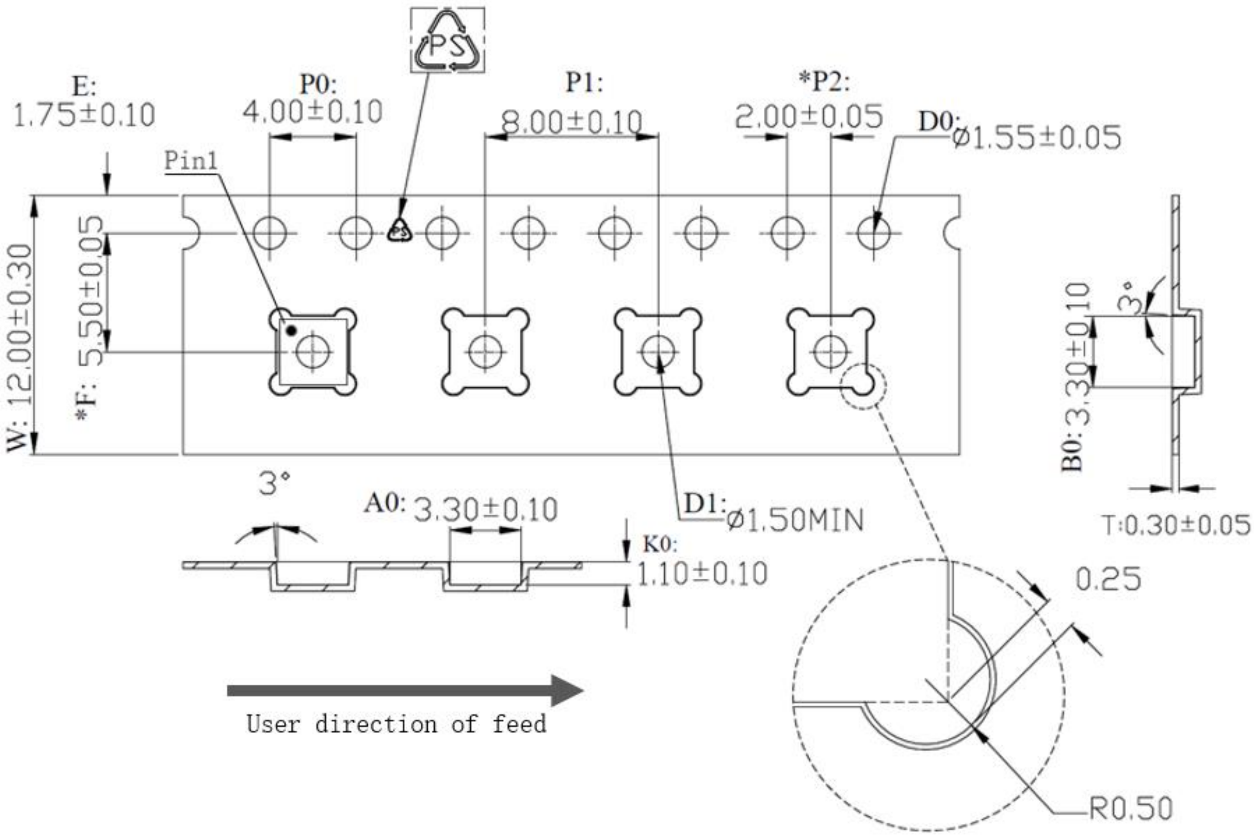


Figure 11.2 Reel information

12. Revision History

Revision	Description	Date
1.0	Initialization	2025/07/14

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