

Product Overview

The NSCSA240-Q1 is a high-precise, bidirectional current sense amplifier that can measure voltage drops across shunt resistors over a wide common mode range from -4 V to 80 V, independent of the supply voltage. The high-precision current measurement is achieved through a combination of low offset voltage ($\pm 5 \mu\text{V}$ typical), small gain error (0.05%, typical) and a high DC CMRR (135 dB, typical). The NSCSA240-Q1 is designed for high voltage, bidirectional measurements in switching systems that see large common-mode voltage transients at the device's inputs. The enhanced PWM rejection circuitry inside the NSCSA240-Q1 ensures minimal signal disturbance at the output due to the common-mode voltage transitions at the input.

The NSCSA240-Q1 operates from a single 2.7 V to 5.5 V supply, drawing 2.6 mA of supply current. The NSCSA240-Q1 is available in four gain options: 20V/V, 50V/V, 100V/V, and 200V/V. Multiple gain options allow for optimization between available shunt resistor values and wide output dynamic range requirements.

Key Features

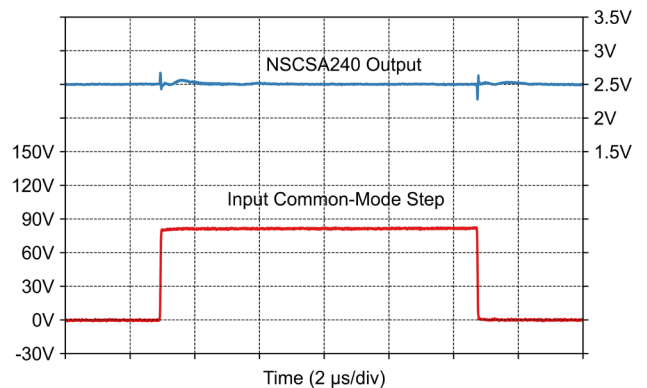
- AEC-Q100 Grade 1 Qualified for Automotive Applications
- Operating Temperature Range: -40°C to $+125^{\circ}\text{C}$
- Enhanced PWM Rejection
- Wide Common-Mode Range: -4 V to 80 V
- Excellent CMRR:
 - 135-dB DC CMRR (Typical)
 - 90-dB AC CMRR at 50 kHz
- Accuracy:
 - Gain Error: 0.05% (Typical)
 - Offset Voltage: $\pm 5\mu\text{V}$ (Typical)
- Gain Options:
 - NSCSA240A1: 20 V/V
 - NSCSA240A2: 50 V/V
 - NSCSA240A3: 100 V/V
 - NSCSA240A4: 200 V/V
- ROHS&REACH Compliance

Device Information

Part Number	Package	Body Size
NSCSA240-Q1	TSSOP (8)	3.00 mm × 4.40 mm
	SOIC (8)	4.90 mm × 3.91 mm

Typical Application

- Electronic Power Steering
- Stability and Traction Control
- Motor and Actuator Control
- Solenoid and Valve Control



Enhanced PWM Rejection

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1.Pin Configuration and Function

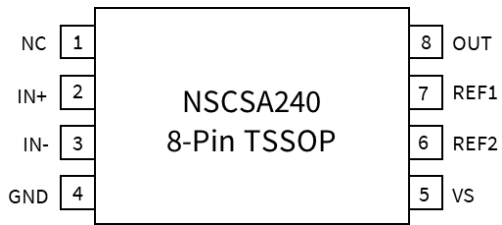


Figure 1-1 8-Pin TSSOP Package Top View

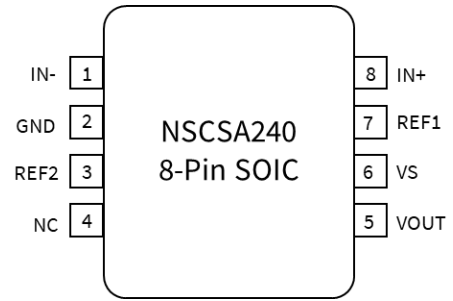


Figure 1-2 8-Pin SOIC Package Top View

Table 1-1 Pin Functions

SYMBOL	TSSOP	SOIC	FUNCTION
GND	4	2	Ground
IN-	3	1	Current-sense amplifier negative input
IN+	2	8	Current-sense amplifier positive input
NC	1	4	Connect to ground
OUT	8	5	Output voltage
REF1	7	7	Reference1 voltage. Connect to 0 V to V_s
REF2	6	3	Reference2 voltage. Connect to 0 V to V_s
V_s	5	6	Power supply

2. Specifications

2.1. Absolute Maximum Ratings¹

Parameters	Symbol	Min	Max	Unit
Supply voltage	V_S	-0.3	6	V
Differential, +IN to -IN inputs			± 80	V
Common-Mode, +IN, -IN to GND		-5	85	V
REF1, REF2, NC inputs		GND - 0.3	$V_S + 0.3$	V
Output		-0.3	$V_S + 0.3$	V
Junction temperature	T_J		150	°C
Storage temperature	T_{stg}	-55	150	°C

2.2. ESD Ratings

Ratings		Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC Q100-002 • All pins	± 2000	V
	Charged device model (CDM), per AEC Q100-011 • All pins	± 2000	V

2.3. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
Common-mode input voltage	V_{CM}	-4	80	V
Operating supply voltage	V_S	2.7	5.5	V
Operating free-air temperature	T_A	-40	125	°C

2.4. Thermal Information

Parameters	Symbol	TSSOP	SOIC	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	149.1	113.5	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC(TOP)}$	33.2	51.9	°C/W
Junction-to-board thermal resistance	θ_{JB}	78.4	57.8	°C/W

¹ Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability

3. Electrical Characteristics

$T_A = 25\text{ }^\circ\text{C}$, $V_S = 5\text{ V}$, $V_{SENSE} = V_{IN+} - V_{IN-}$, $V_{SENSE} = 0\text{ mV}$, $V_{CM} = 12\text{ V}$, and $V_{REF1} = V_{REF2} = V_S / 2$ (unless otherwise noted)

Parameters	Symbol	Condition	Min	Typ	Max	Unit
INPUT						
Common-mode input range	V_{CM}	$V_{IN+} = -4\text{V to } 80\text{V}$, $V_{SENSE} = 0\text{ mV}$ $T_A = -40\text{ }^\circ\text{C to } 125\text{ }^\circ\text{C}$	-4		80	V
Common-mode rejection ratio	CMRR	$V_{IN+} = -4\text{V to } 80\text{V}$, $V_{SENSE} = 0\text{ mV}$ $T_A = -40\text{ }^\circ\text{C to } 125\text{ }^\circ\text{C}$	12 5	135		dB
		$T_A = -40\text{ }^\circ\text{C to } 125\text{ }^\circ\text{C}$	110			
		$f = 50\text{ kHz}$		90		
Offset voltage, input-referred	V_{OS}	$V_{SENSE} = 0$		± 5	± 25	μV
Offset voltage Drift	dV_{OS}/dT	$V_{SENSE} = 0$, $T_A = -40\text{ }^\circ\text{C to } 125\text{ }^\circ\text{C}^{(1)}$		± 0.06	± 0.25	$\mu\text{V}/^\circ\text{C}$
Power-supply rejection ratio	PSRR	$V_S = 2.7\text{ V to } 5.5\text{ V}$ $V_{SENSE} = 0$, $T_A = -40\text{ }^\circ\text{C to } 125\text{ }^\circ\text{C}$		± 5	± 15	$\mu\text{V}/\text{V}$
Input bias current	I_B	I_{B+} , I_{B-} , $V_{SENSE} = 0$, $V_{CM} = 12\text{ V}$		92		μA
		I_{B+} , I_{B-} , $V_{SENSE} = 0$, $V_{CM} = 80\text{ V}$		225		
Reference input range			GN D		V_S	
OUTPUT						
Gain	G	NSCSA240A1		20		V/V
		NSCSA240A2		50		
		NSCSA240A3		100		
		NSCSA240A4		200		
Gain error	GE	$\text{GND} + 50\text{ mV} \leq V_{OUT} \leq V_S - 0.1\text{V}$		$\pm 0.05\%$	$\pm 0.1\%$	
Gain drift		$T_A = -40\text{ }^\circ\text{C to } 125\text{ }^\circ\text{C}^{(1)}$		± 2	± 3	ppm/ $^\circ\text{C}$
Non-linearity error		$\text{GND} + 0.1\text{V} \leq V_{OUT} \leq V_S - 0.1\text{V}$		$\pm 0.01\%$		
Reference divider accuracy		$V_{OUT} = (V_{REF1} - V_{REF2}) / 2$, A1(Gain=20), A2(Gain=50), A4(Gain=200)		0.02%	0.1%	
Reference divider accuracy		A3(Gain=100)		0.02%	0.15%	
Reference voltage rejection ratio (input-referred)	RVRR	$V_{REF1} = V_{REF2} = \text{GND} + 0.1\text{V} \leq V_{OUT} \leq V_S - 0.1\text{V}$ $T_A = -40\text{ }^\circ\text{C to } +125\text{ }^\circ\text{C}$		± 3	± 15	$\mu\text{V}/\text{V}$
VOLTAGE OUTPUT						
Swing to V_S		$R_L = 10\text{ k}\Omega$ to GND $T_A = -40\text{ }^\circ\text{C to } 125\text{ }^\circ\text{C}$		V_S -0.02	V_S -0.05	V
Swing to GND		$R_L = 10\text{ k}\Omega$ to GND $T_A = -40\text{ }^\circ\text{C to } 125\text{ }^\circ\text{C}$		0.005	0.01	V

⁽¹⁾ Temperature drift-related limits are guaranteed by characterization results

Electrical Characteristics (continued)

$T_A = 25\text{ }^\circ\text{C}$, $V_S = 5\text{ V}$, $V_{SENSE} = V_{IN+} - V_{IN-}$, $V_{SENSE} = 0\text{ mV}$, $V_{CM} = 12\text{ V}$, and $V_{REF1} = V_{REF2} = V_S / 2$ (unless otherwise noted)

FREQUENCY RESPONSE				
-3dB bandwidth	BW	NSCSA240A1, G = 20	600	KHz
		NSCSA240A2, G = 50	550	
		NSCSA240A3, G = 100	500	
		NSCSA240A4, G = 200	450	
Settling time	T_s	Output settles to 0.1%	10	μs
Slew rate	SR		4	$\text{V}/\mu\text{s}$
NOISE (INPUT REFERRED)				
Voltage noise density		Input referred	40	$\text{nV}/\sqrt{\text{Hz}}$
0.1-Hz to 10-Hz Voltage Noise		Input referred	0.8	μVpp
POWER SUPPLY				
Operating voltage range	V_S		2.7	5.5
Quiescent current	I_Q		2.6	2.9
		$T_A = -40^\circ\text{C}$ to 125°C	3	
TEMPERATURE RANGE				
Specified Range	T_A		-40	125
				$^\circ\text{C}$

4. Typical Performance Characteristics

$T_A = 25\text{ }^\circ\text{C}$, $V_S = 5\text{ V}$, $V_{\text{SENSE}} = V_{\text{IN}+} - V_{\text{IN}-}$, $V_{\text{SENSE}} = 0\text{ mV}$, $V_{\text{CM}} = 12\text{ V}$, and $V_{\text{REF}1} = V_{\text{REF}2} = V_S / 2$ (unless otherwise noted)

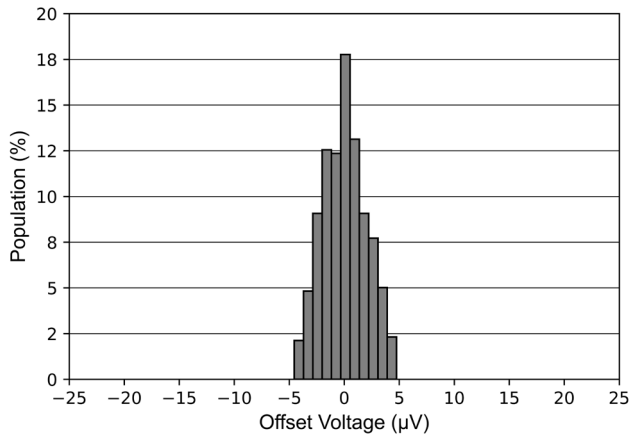


Figure 4-1 Input Offset Voltage Distribution

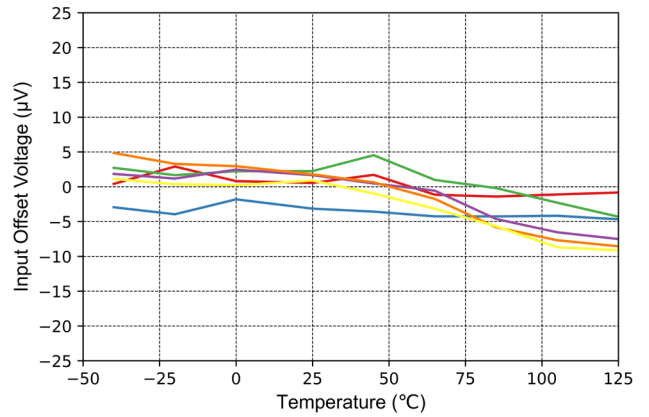


Figure 4-2 Input Offset Voltage vs Temperature

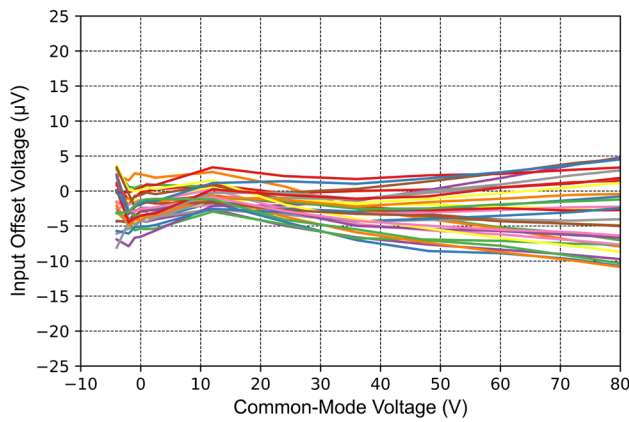


Figure 4-3 Input Offset Voltage vs Common-Mode Voltage

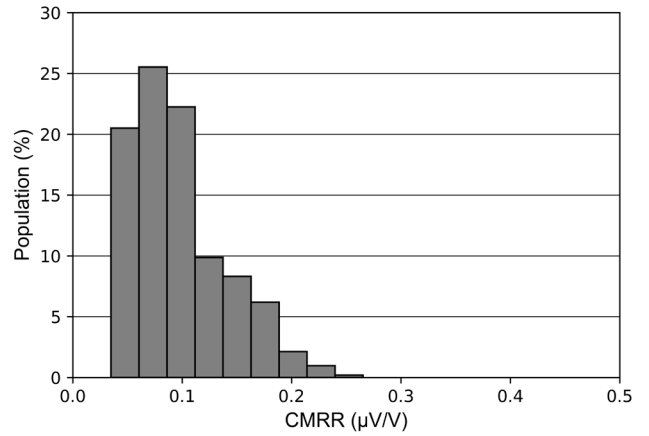


Figure 4-4 Common-Mode Rejection Ratio Distribution

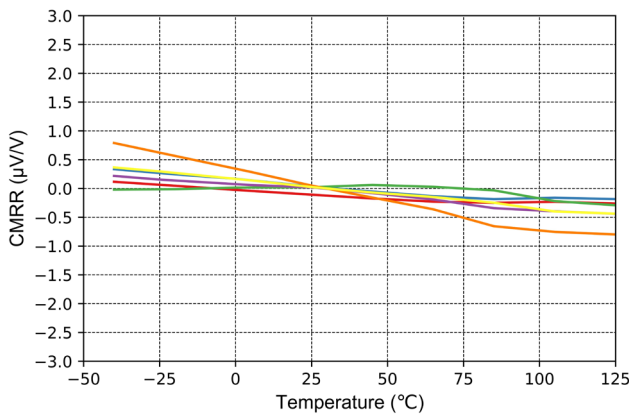


Figure 4-5 Common-Mode Rejection Ratio vs Temperature

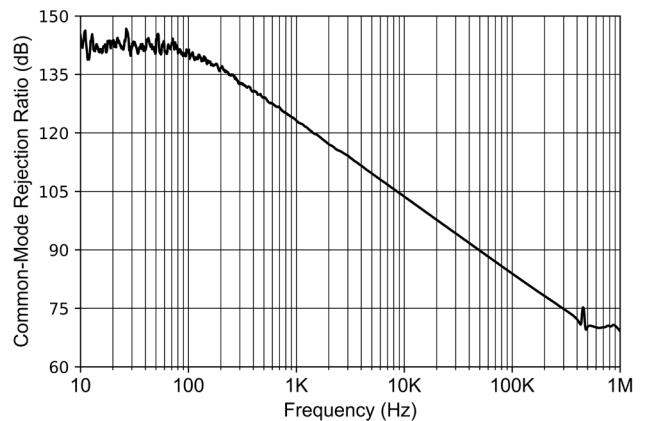


Figure 4-6 Common-Mode Rejection Ratio vs Frequency

Typical Performance Characteristics (continued)

$T_A = 25\text{ }^\circ\text{C}$, $V_S = 5\text{ V}$, $V_{\text{SENSE}} = V_{\text{IN}+} - V_{\text{IN}-}$, $V_{\text{SENSE}} = 0\text{ mV}$, $V_{\text{CM}} = 12\text{ V}$, and $V_{\text{REF1}} = V_{\text{REF2}} = V_S / 2$ (unless otherwise noted)

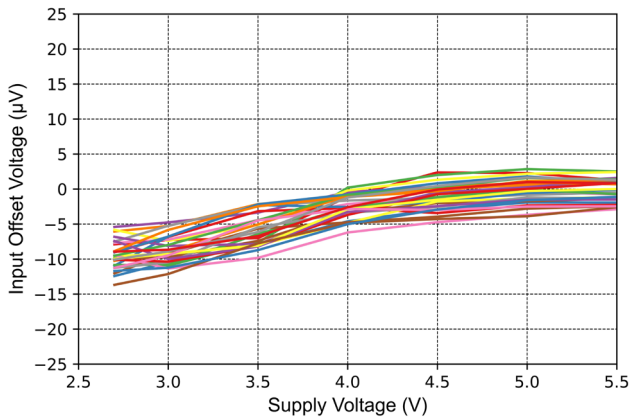


Figure 4-7 Input Offset Voltage vs Supply Voltage

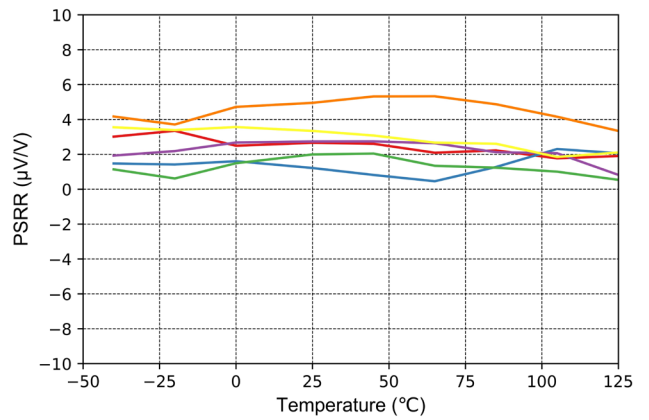


Figure 4-8 Power-Supply Rejection vs Temperature

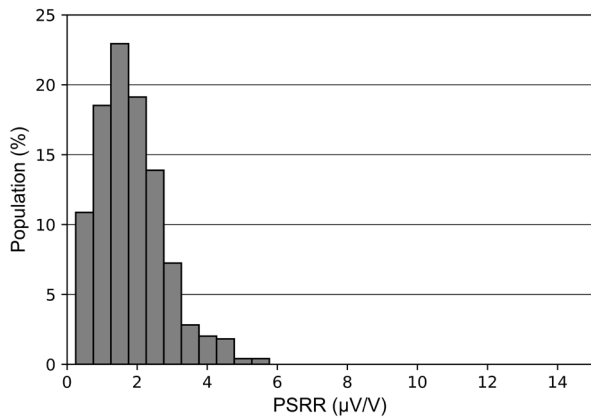


Figure 4-9 Power-Supply Rejection Ratio Distribution

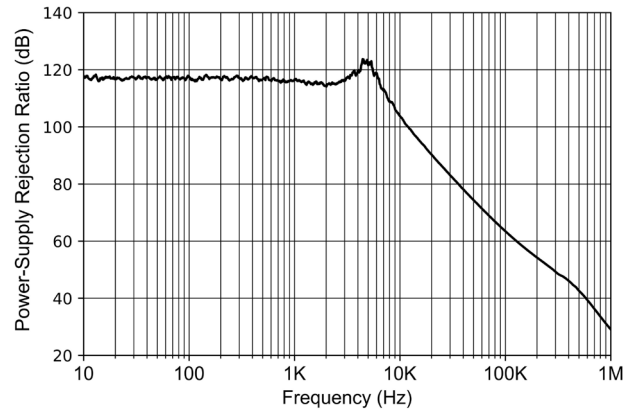


Figure 4-10 Power-Supply Rejection Ratio vs Frequency

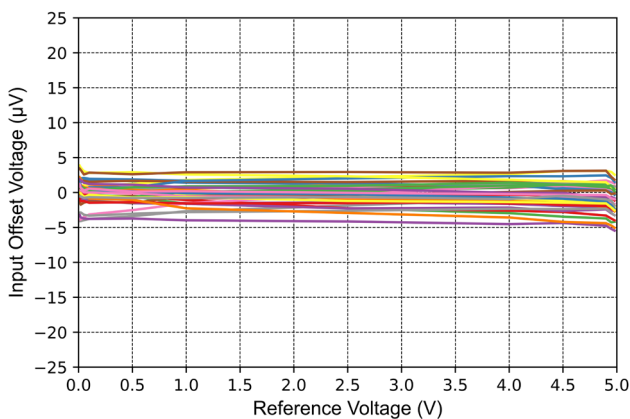


Figure 4-11 Input Offset Voltage vs Reference Voltage

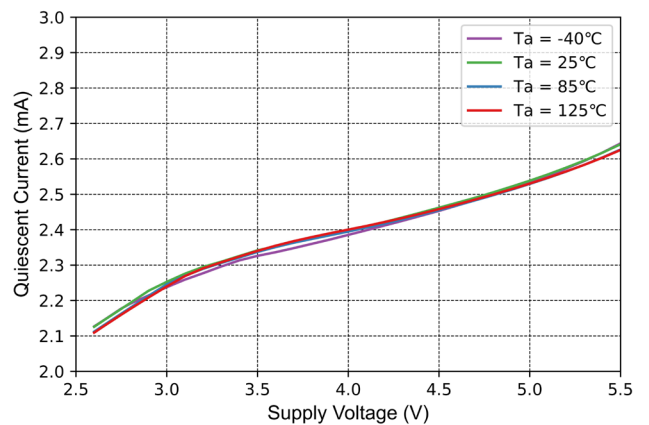


Figure 4-12 Quiescent Current vs Supply Voltage

Typical Performance Characteristics (continued)

$T_A = 25\text{ }^\circ\text{C}$, $V_S = 5\text{ V}$, $V_{SENSE} = V_{IN+} - V_{IN-}$, $V_{SENSE} = 0\text{ mV}$, $V_{CM} = 12\text{ V}$, and $V_{REF1} = V_{REF2} = V_S / 2$ (unless otherwise noted)

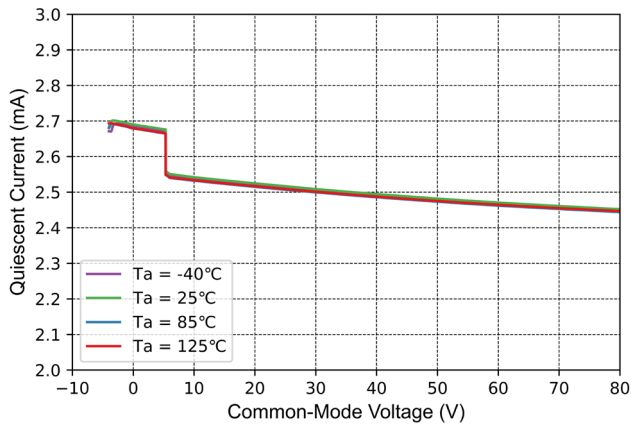


Figure 4-13 Quiescent Current vs Common-Mode Voltage

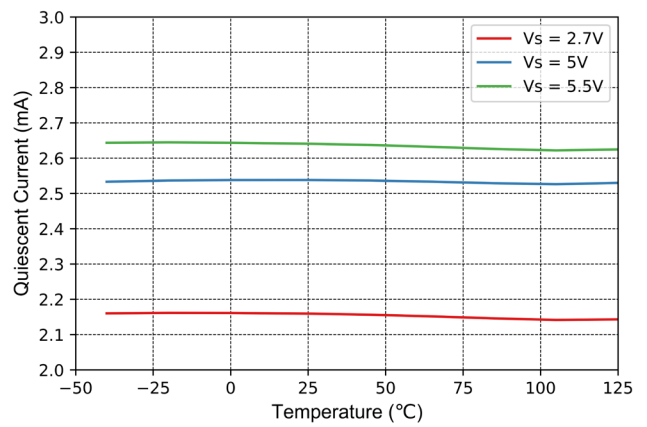


Figure 4-14 Quiescent Current vs Temperature

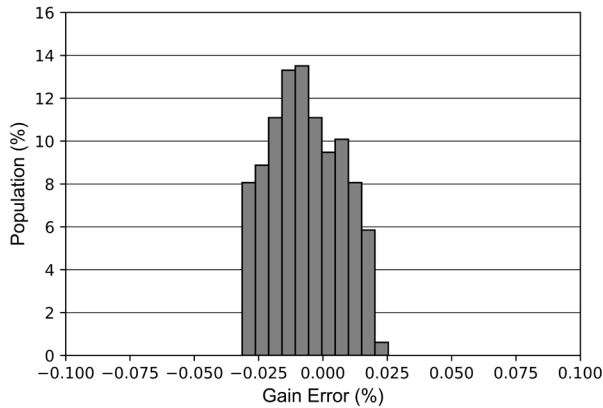


Figure 4-15 Gain Error Production Distribution

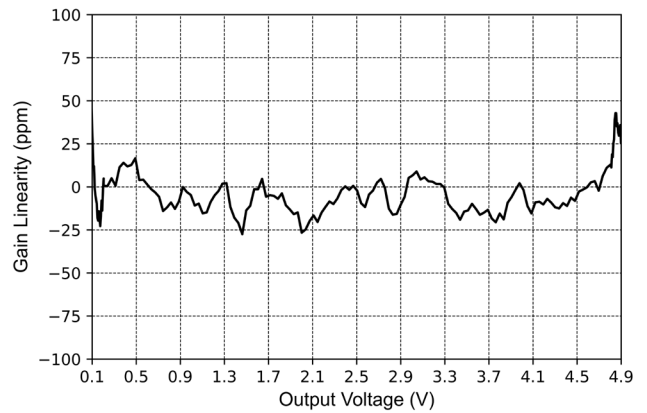


Figure 4-16 Gain Nonlinearity vs. vs Output Voltage

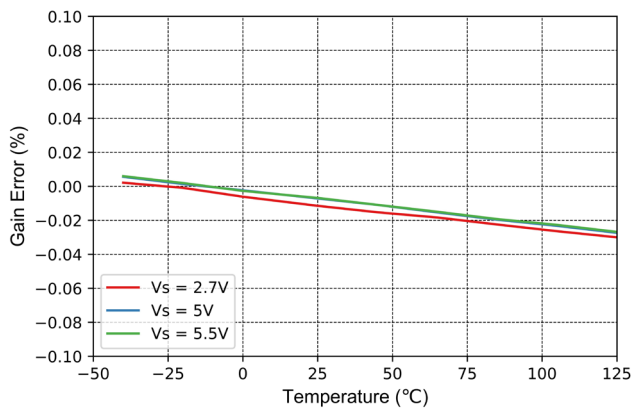


Figure 4-17 Gain Error vs Temperature

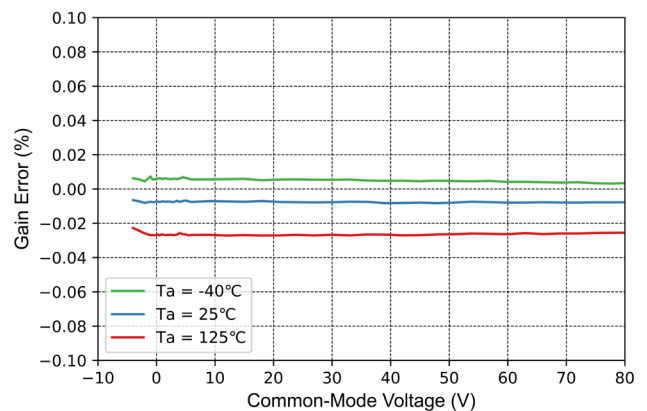


Figure 4-18 Gain Error vs Common-Mode Voltage

Typical Performance Characteristics (continued)

$T_A = 25\text{ }^\circ\text{C}$, $V_S = 5\text{ V}$, $V_{SENSE} = V_{IN+} - V_{IN-}$, $V_{SENSE} = 0\text{ mV}$, $V_{CM} = 12\text{ V}$, and $V_{REF1} = V_{REF2} = V_S / 2$ (unless otherwise noted)

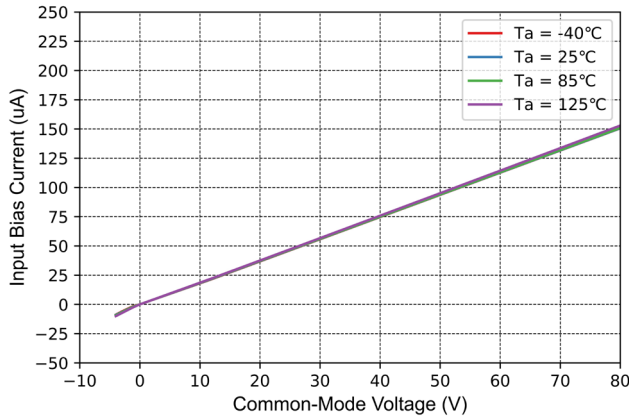


Figure 4-19 Input Bias Current vs Common-Mode Voltage $V_S = 0$

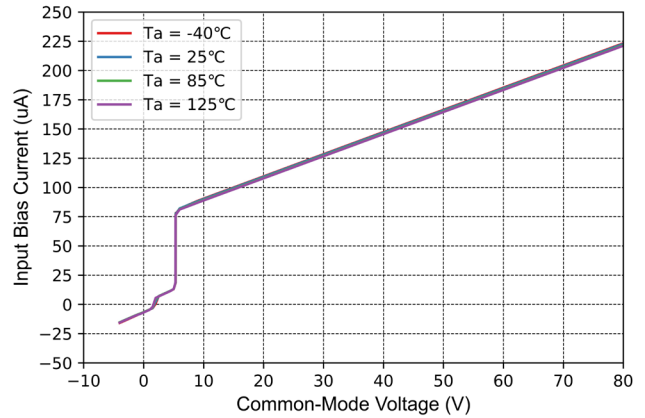


Figure 4-20 Input Bias Current vs Common-Mode Voltage $V_S = 5\text{ V}$

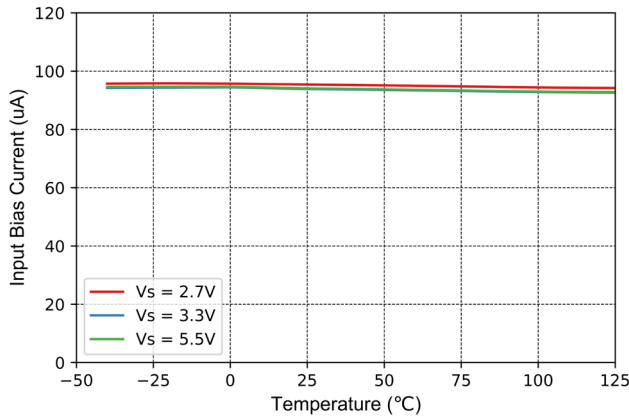


Figure 4-21 Input Bias Current vs Temperature

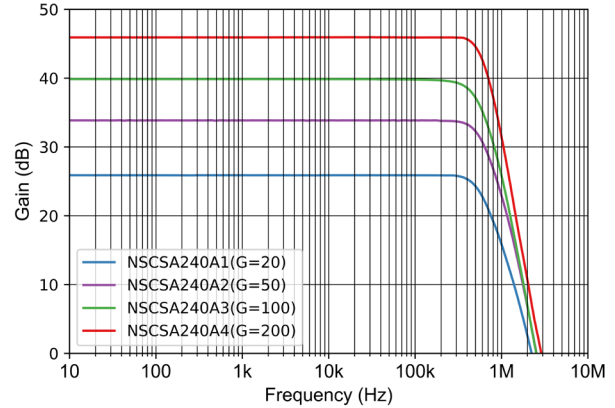


Figure 4-22 Gain vs Frequency

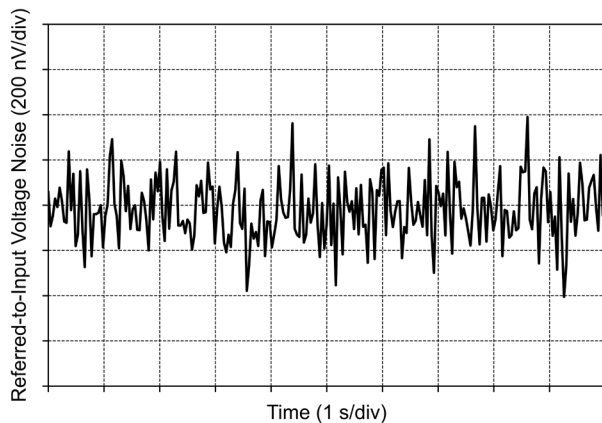


Figure 4-23 0.1-Hz to 10-Hz Voltage Noise

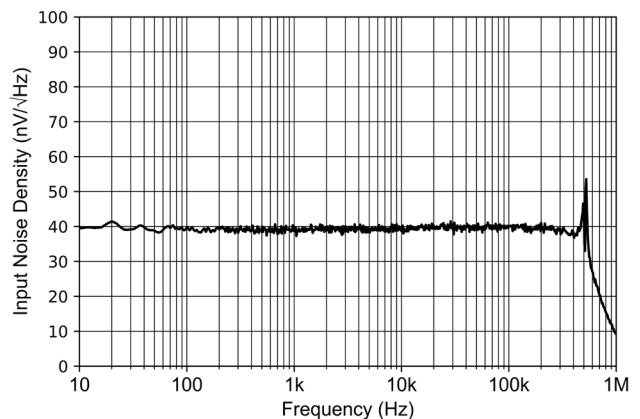


Figure 4-24 Input-Referred Voltage Noise vs Frequency

Typical Performance Characteristics (continued)

$T_A = 25\text{ }^\circ\text{C}$, $V_S = 5\text{ V}$, $V_{SENSE} = V_{IN+} - V_{IN-}$, $V_{SENSE} = 0\text{ mV}$, $V_{CM} = 12\text{ V}$, and $V_{REF1} = V_{REF2} = V_S / 2$ (unless otherwise noted)

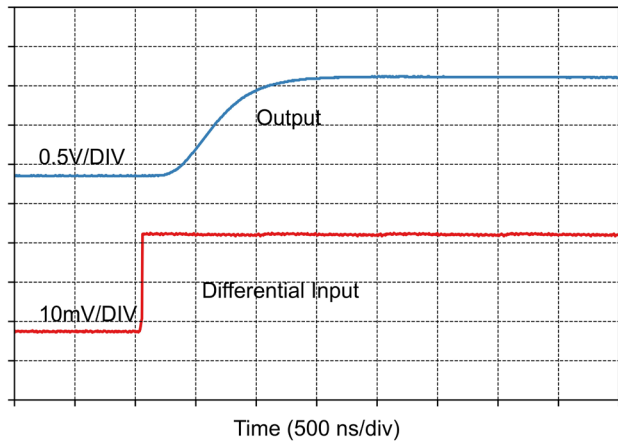


Figure 4-25 Small Signal Response, Raising

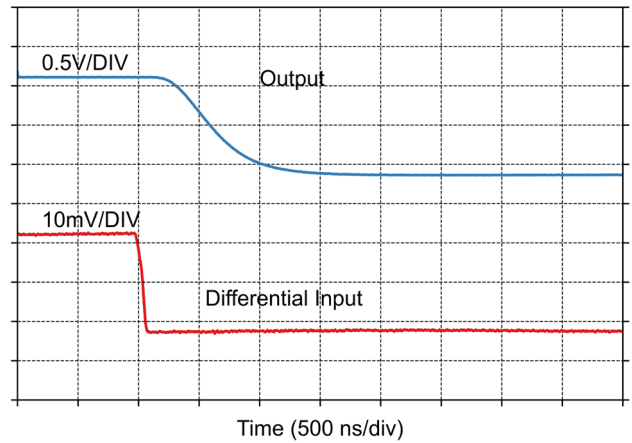


Figure 4-26 Small Signal Response, Falling

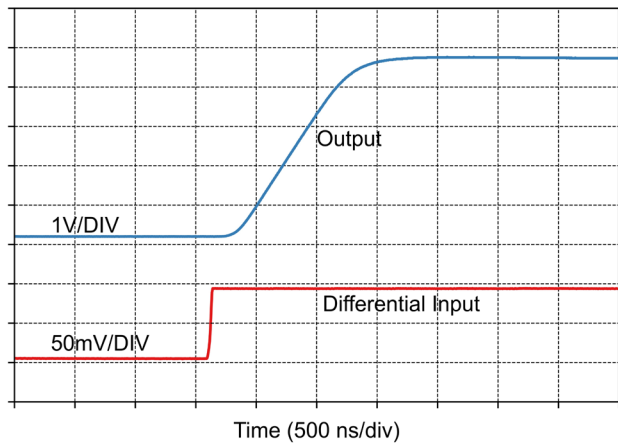


Figure 4-27 Large Signal Response, Raising

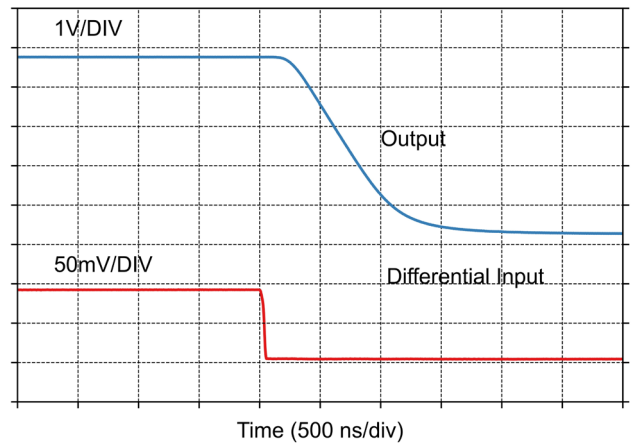


Figure 4-28 Large Signal Response, Falling

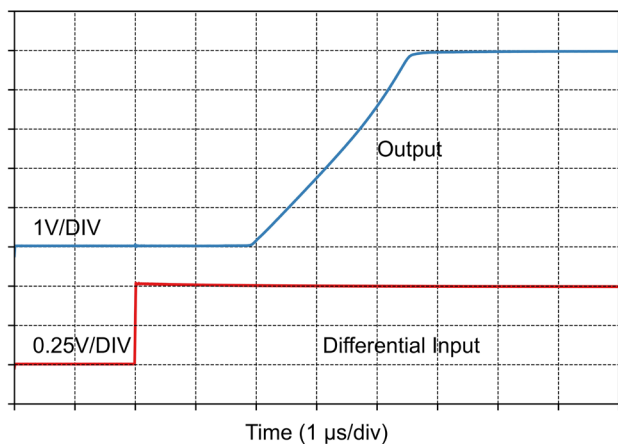


Figure 4-29 Differential Overload Recovery, Rising

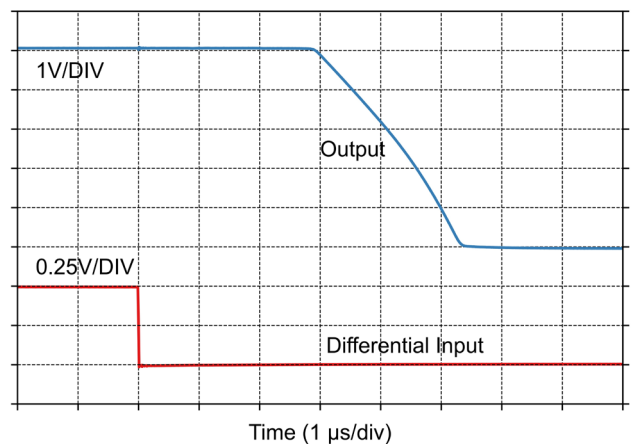


Figure 4-30 Differential Overload Recovery, Falling

Typical Performance Characteristics (continued)

$T_A = 25\text{ }^\circ\text{C}$, $V_S = 5\text{ V}$, $V_{\text{SENSE}} = V_{\text{IN}+} - V_{\text{IN}-}$, $V_{\text{SENSE}} = 0\text{ mV}$, $V_{\text{CM}} = 12\text{ V}$, and $V_{\text{REF1}} = V_{\text{REF2}} = V_S / 2$ (unless otherwise noted)

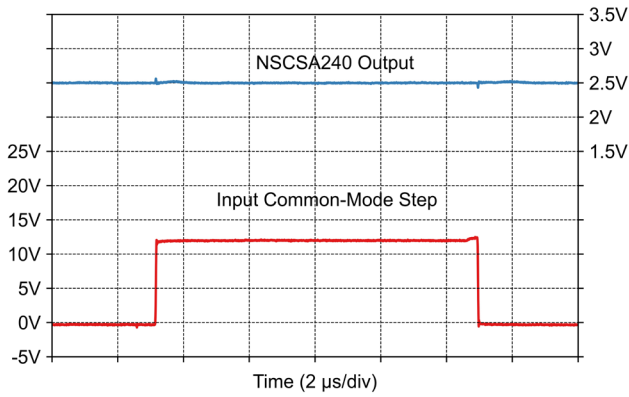


Figure 4-31 12V Common-Mode Voltage Transient Response

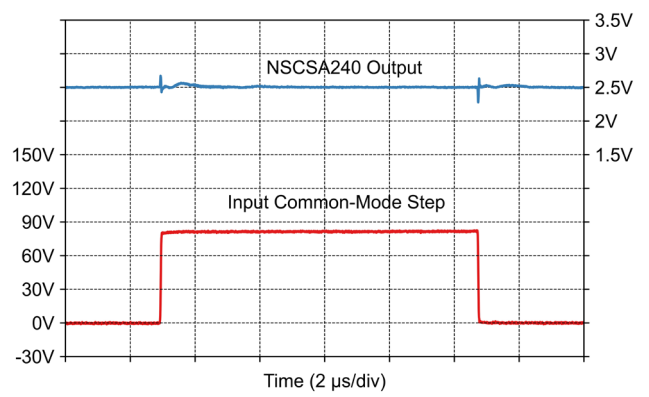


Figure 4-32 80V Common-Mode Voltage Transient Response

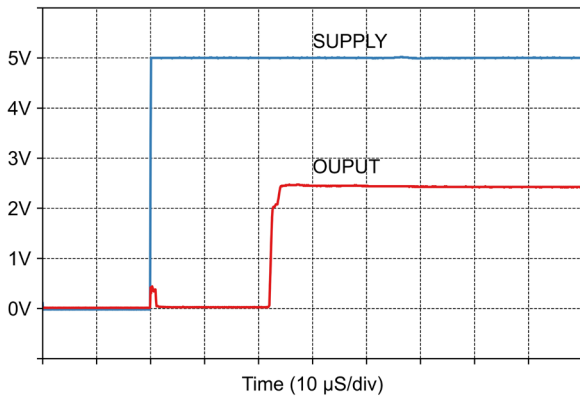


Figure 4-33 Start-Up Response

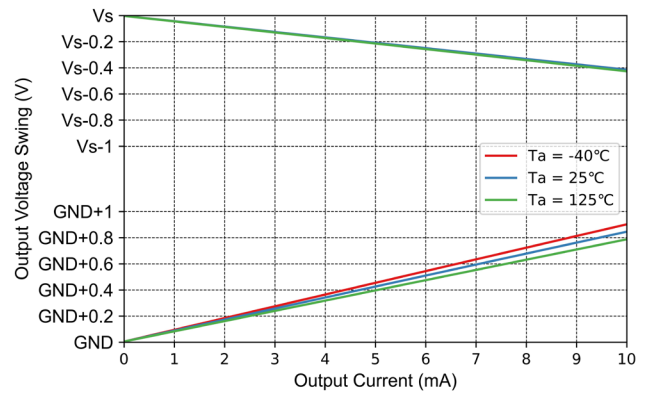


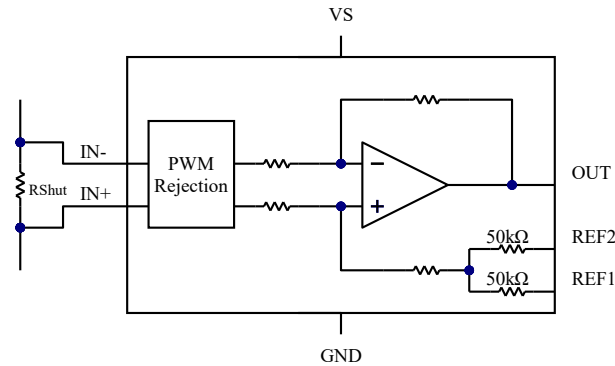
Figure 4-34 Output Voltage Swing vs Output Current

5. Detailed Description

5.1. Overview

NSCSA240-Q1 is a current-sense amplifier that offers a wide common-mode range, precision, zero-drift topology, excellent common-mode rejection ratio (CMRR), and features enhanced pulse width modulation (PWM) rejection. Enhanced PWM rejection reduces the effect of common-mode transients on the output signal that are associated with PWM signals. Multiple gain versions are available to allow for the optimization of the desired full-scale output voltage based on the target current range expected in the application.

5.2. Functional Block Diagram



5.3. Feature Description

5.3.1. Amplifier Input Signal

The NSCSA240-Q1 is designed to handle large common-mode transients over a wide voltage range. Input signals from current measurement applications for linear and PWM applications can be connected to the amplifier to provide a highly accurate output, with minimal common-mode transient artifacts.

5.3.2. Enhanced PWM Rejection Operation

The enhanced PWM rejection feature of the NSCSA240-Q1 provides increased attenuation of large common-mode $\Delta V/\Delta t$ transients. Large $\Delta V/\Delta t$ common-mode transients associated with PWM signals are employed in applications such as motor or solenoid drive and switching power supplies. Traditionally, large $\Delta V/\Delta t$ common mode transitions are handled strictly by increasing the amplifier signal bandwidth, which can increase chip size, complexity and ultimately cost. The NSCSA240-Q1 is designed with high common-mode rejection techniques to reduce large $\Delta V/\Delta t$ transients before the system is disturbed as a result of these large signals. The high AC CMRR, in conjunction with signal bandwidth, allows the NSCSA240-Q1 to provide minimal output transients and ringing compared with standard circuit approaches.

5.3.3. Input Signal Bandwidth

The NSCSA240-Q1 input signal, which represents the current being measured, is accurately measured with minimal disturbance from large $\Delta V/\Delta t$ common-mode transients as previously described. For PWM signals typically associated with motors, solenoids, and other switching applications, the current being monitored varies at a significantly slower rate than the faster PWM frequency. The NSCSA240-Q1 bandwidth is defined by the -3 dB bandwidth of the current-sense amplifier inside the device; see the Electrical Characteristics table. The device bandwidth provides fast throughput and fast response required for the rapid detection and processing of overcurrent events. Without the higher bandwidth, protection circuitry may not have adequate response time and damage may occur to the monitored application or circuit.

5.3.4. Selecting the Sense Resistor (RSENSE)

The NSCSA240-Q1 determines the current magnitude from measuring the differential voltage developed across a resistor. This resistor is referred to as a current-sensing resistor or a current-shunt resistor. The flexible design of the device allows a wide input signal range across this current-sensing resistor.

The current-sensing resistor is ideally chosen solely based on the full-scale current to be measured, the full-scale input range of the circuitry following the device, and the device gain selected. The minimum current sensing resistor is a design-based decision in order to maximize the input range of the signal chain circuitry. Full-scale output signals that are not

maximized to the full input range of the system circuitry limit the ability of the system to exercise the full dynamic range of system control.

Two important factors to consider when finalizing the current-sensing resistor value are: the required current measurement accuracy and the maximum power dissipation across the resistor. A larger resistor voltage provides for a more accurate measurement, but increases the power dissipation in the resistor. The increased power dissipation generates heat, which reduces the sense resistor accuracy because of the temperature coefficient. The voltage signal measurement uncertainty is reduced when the input signal gets larger because any fixed errors become a smaller percentage of the measured signal. The design trade-off to improve measurement accuracy increases the current-sensing resistor value. The increased resistance value results in an increased power dissipation in the system which can additionally decrease the overall system accuracy. Based on these relationships, the measurement accuracy is inversely proportional to both the resistance value and power dissipation contributed by the current-shunt selection.

By increasing the current-shunt resistor, the differential voltage is increased across the resistor. Larger input differential voltages require a smaller amplifier gain to achieve a full-scale amplifier output voltage. Smaller current-shunt resistors are desired but require large amplifier gain settings. The larger gain settings often have increased error and noise parameters, which are not attractive for precision designs. Historically, the design goals for high-performance measurements forced designers to accept selecting larger current-sense resistors and the lower gain amplifier settings. The NSCSA240-Q1 provides 100-V/V and 200-V/V gain options that offer the high-gain setting and maintains high-performance levels with offset values below 25 μ V. These devices allow for the use of lower shunt resistor values to achieve lower power dissipation and still meet high system performance specifications.

6. Layout

6.1. Layout Guidelines

6.1.1. High-Precision Applications

For high-precision applications, verify accuracy and stability of the amplifier by:

- Providing a precision reference connected to REF1 and REF2
- Optimizing the layout of the power and sensing path of the sense resistor (see the Layout section)
- Providing adequate bypass capacitance on the supply pin.

6.1.2. Kelvin Connection from the Current-Sense Resistor

To provide accurate current measurements, verify the routing between the current-sense resistor and the amplifier uses a Kelvin connection. Use the information provided in Figure 6-1 and Figure 6-2.

6.2. Layout Example

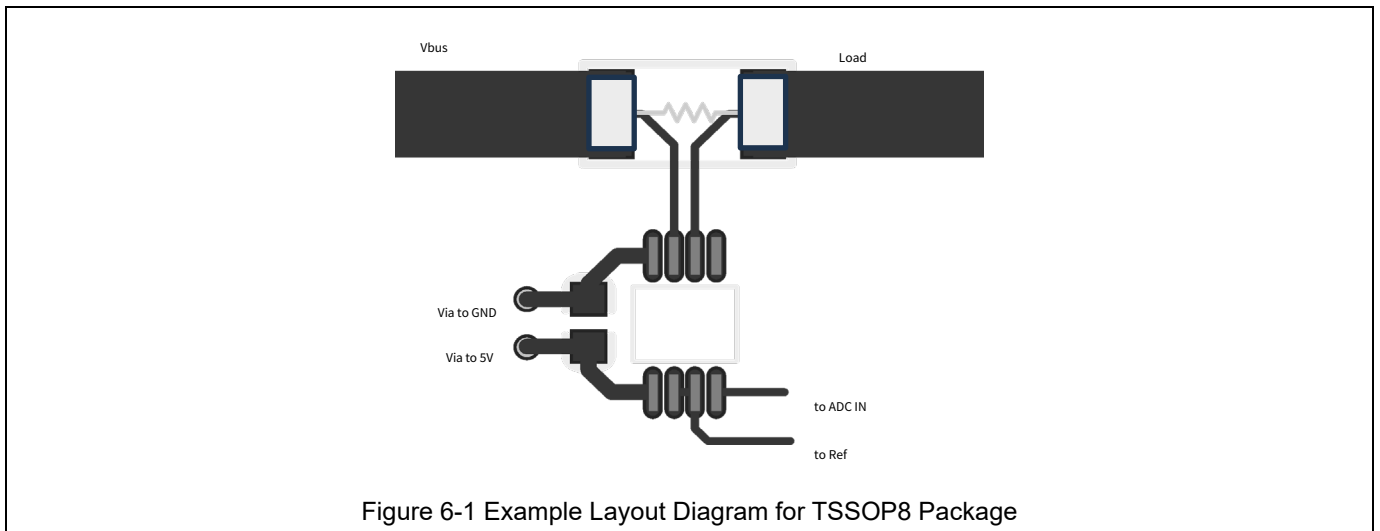


Figure 6-1 Example Layout Diagram for TSSOP8 Package

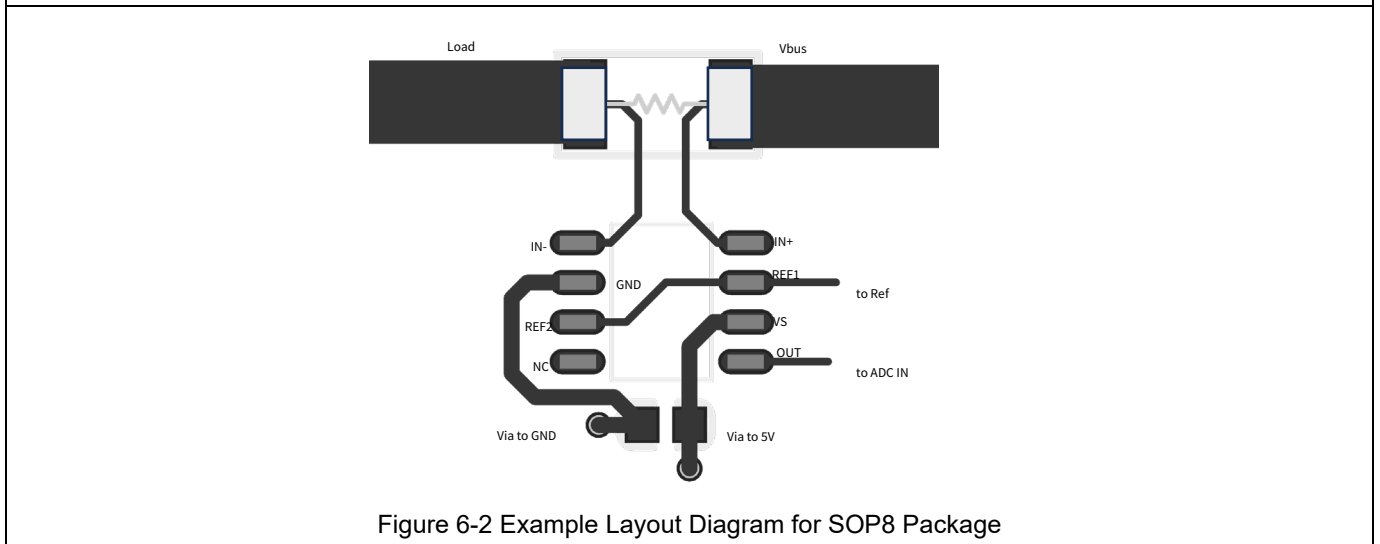
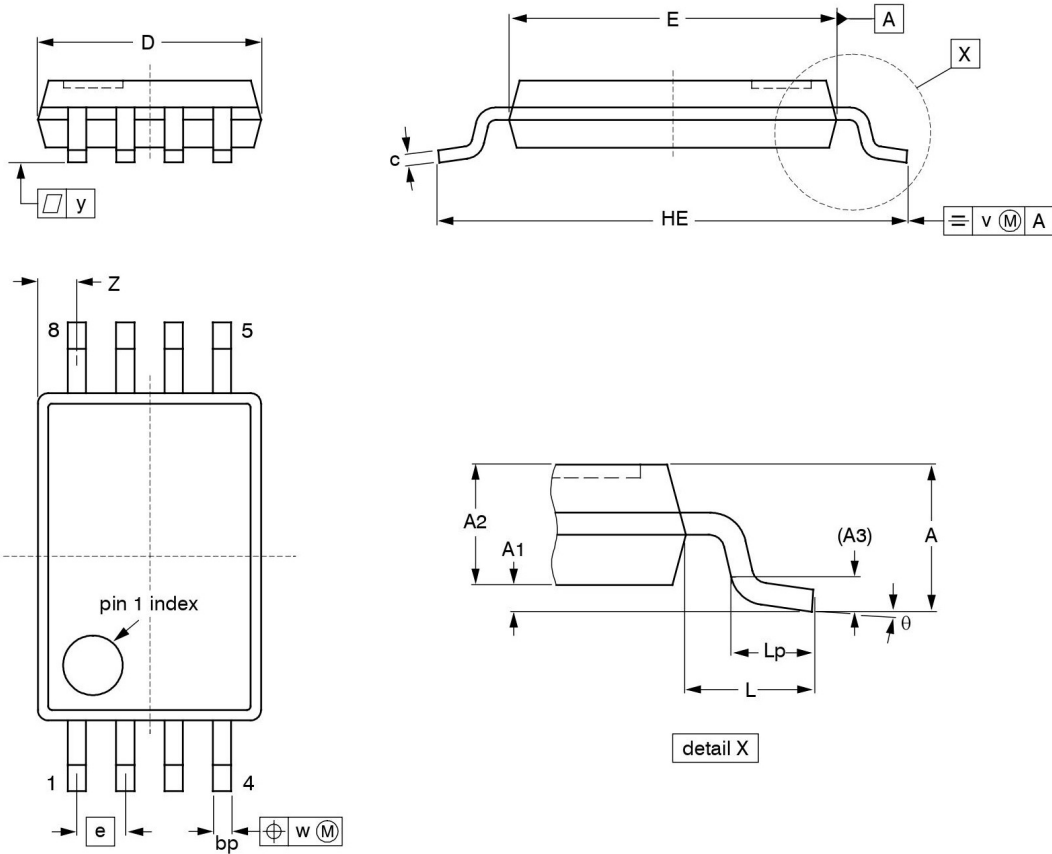


Figure 6-2 Example Layout Diagram for SOP8 Package

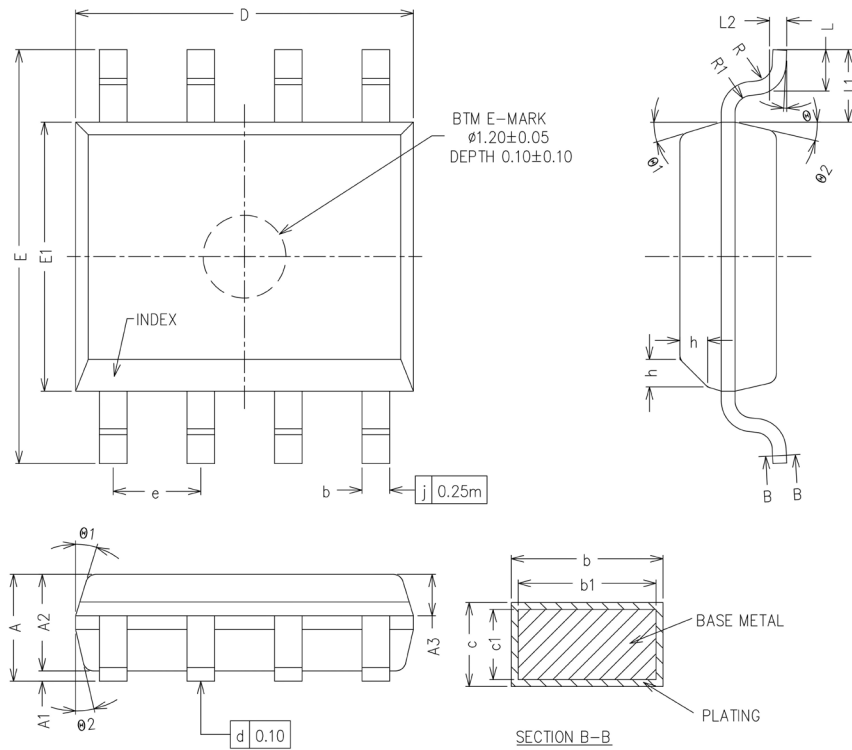
7. Package Information

7.1. TSSOP (8)



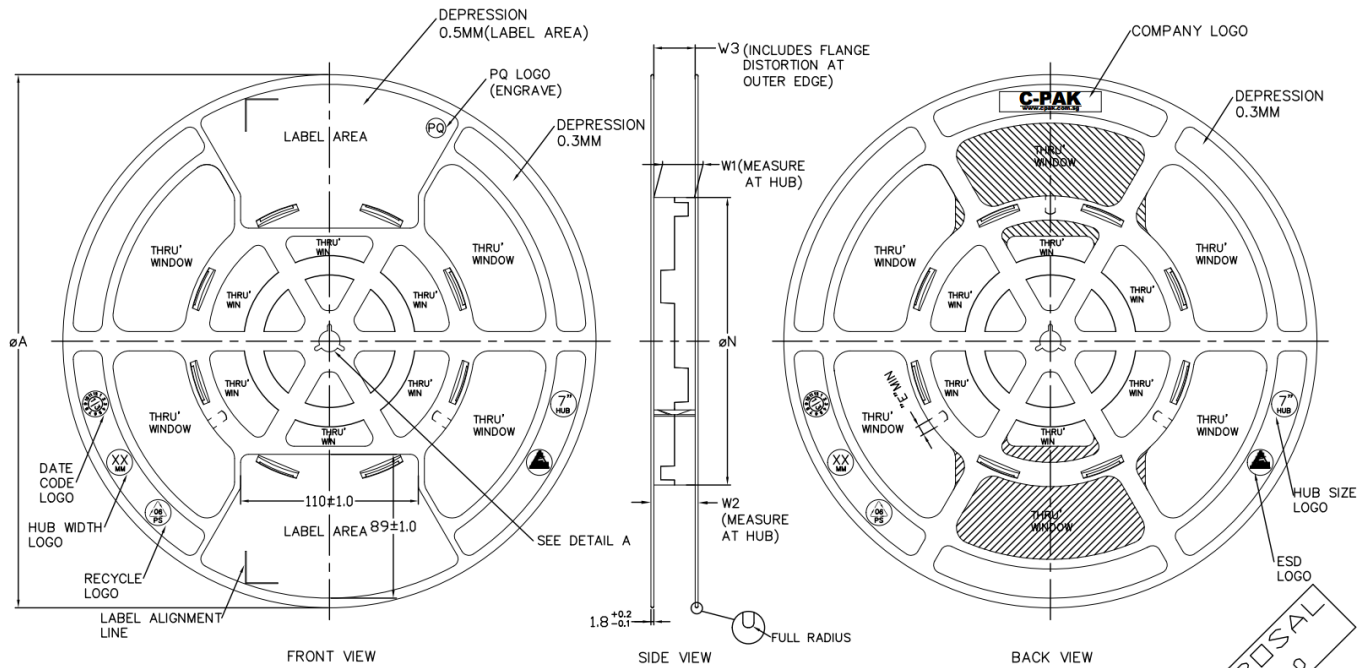
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	--	1.1	--	0.04331
A1	0.05	0.15	0.00197	0.00591
A2	0.85	0.95	0.03346	0.03740
A3	0.25 REF		0.00984 REF	
bp	0.19	0.3	0.00748	0.01181
D	2.90	3.10	0.11417	0.12205
E	4.30	4.50	0.16929	0.17717
e	0.65 BSC		0.02559 BSC	
HE	6.3	6.5	0.24803	0.25591
L	0.94 REF		0.03701 REF	
Lp	0.5	0.7	0.01969	0.02756
v	0.1		0.00394	
w	0.1		0.00394	
y	0.1		0.00394	
θ	0°	8°	0°	8°

7.2. SOIC (8)

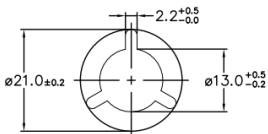


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.05315	0.06890
A1	0.05	0.25	0.00197	0.00984
A2	1.30	1.50	0.05118	0.05906
A3	0.50	0.70	0.01969	0.02756
b	0.38	0.47	0.01496	0.01850
b1	0.37	0.43	0.01457	0.01693
c	0.17	0.25	0.00669	0.00984
c1	0.17	0.23	0.00669	0.00906
D	4.80	5.00	0.18898	0.19685
E	5.80	6.20	0.22835	0.24409
E1	3.80	4.00	0.14961	0.15748
e	1.17	1.37	0.04606	0.05394
L	0.45	0.80	0.01772	0.03150
L1	1.04 REF		0.04094 REF	
L2	0.25 BSC		0.00984 BSC	
R	0.07	—	0.00276	—
R1	0.07	—	0.00276	—
h	0.30	0.50	0.01181	0.01969
θ	0°	8°	0°	8°
θ1	15°	19°	15°	19°
θ2	11°	15°	11°	15°

8.Tape And Reel Information



PROPOSAL
REV 0



ARBOR HOLE
DETAIL A
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	ϕA ± 2.0	ϕN ± 2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 ^{±0.1}	14.4		5.5
12MM	330	178	12.4 ^{±0.1}	18.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
16MM	330	178	16.4 ^{±0.1}	22.4		5.5
24MM	330	178	24.4 ^{±0.1}	30.4		5.5
32MM	330	178	32.4 ^{±0.1}	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOR
A	BELOW 10 ⁹	ANTISTATIC	ALL TYPES
B	10 ⁹ TO 10 ¹⁰	STATIC DISSIPATIVE	BLACK ONLY
C	10 ⁸ & BELOW 10 ⁹	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10 ⁹ TO 10 ¹⁰	ANTISTATIC (COATED)	ALL TYPES

- NOTE:
1. PROPOSE DRAWING ONLY.
2. SANDBLAST ALL SURFACE UNLESS OTHERWISE INDICATED.

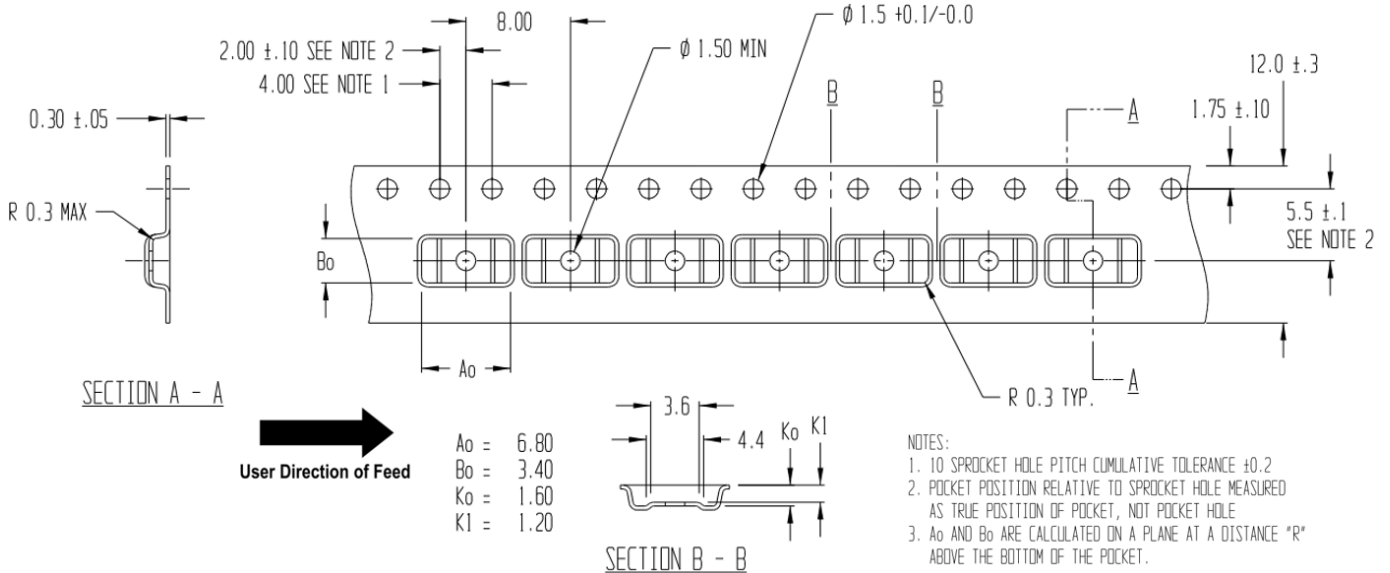
TITLE : 13X7 LATCH REEL LW			
S.R : REFER TO TABLE	TOOL NO :	CPAK XXXX	PDI :
SCALE : NTS	SHRINKAGE :	0.45%	TOLERANCE :
REV : 000001	MATERIAL :	PS	X.X ±0.25
UNIT : MM	WARPAGE :	---	X.XX ±0.13
SHT : 1/1	NAME :	DATE :	ANGLE :
DRAWN : LZ TAM	030614	X	±30°
CHECK : KC LEE	030614	X.X	±15°

DWG-REF.	REV.
EMB02-14	0

7 TAM030614	0	REV	03/06/2014	DESCRIPTION
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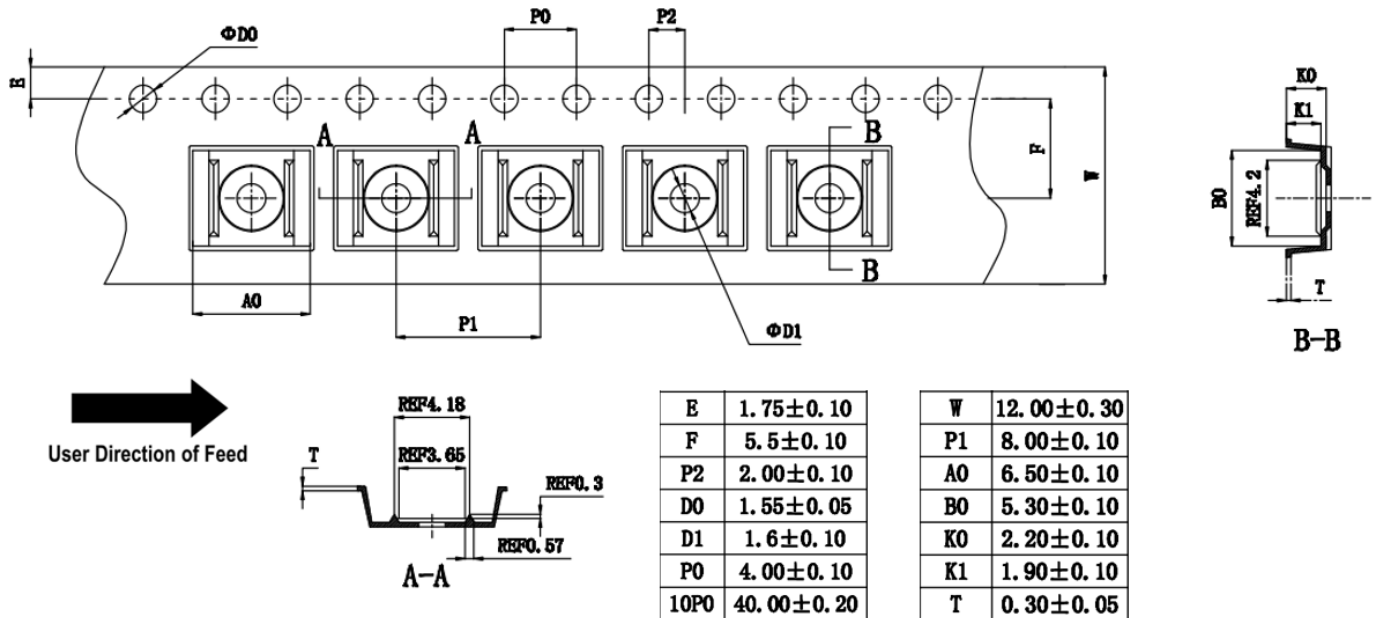


8.1. TSSOP (8)

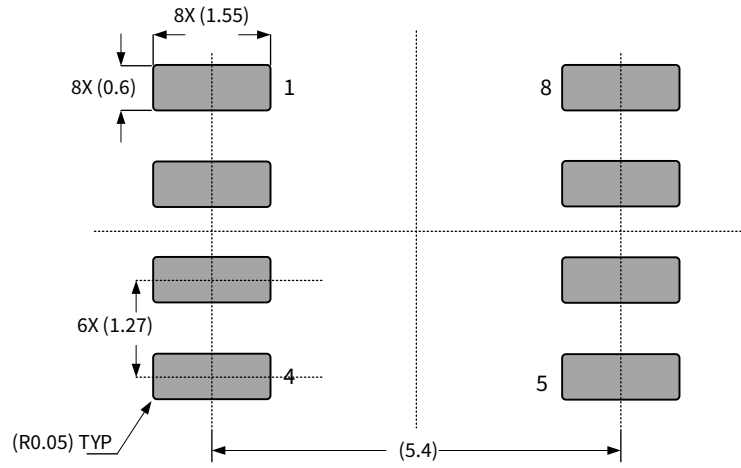


Note: 3000ea/reel.

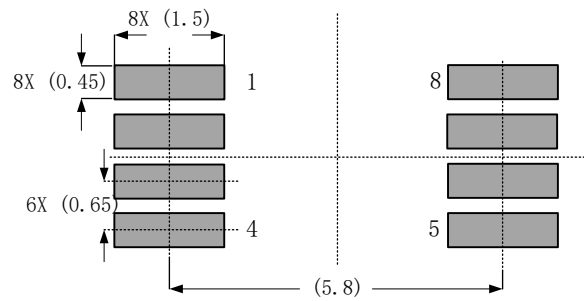
8.2. SOIC (8)



9.Example of Solder Pads Dimensions



Example of solder pads dimensions of SOIC (8)



Example of solder pads dimensions of TSSOP (8)

10. Order Information

<i>Part Number</i>	<i>Package</i>	<i>Gain</i>	<i>MSL Level</i>	<i>Op Temp (°C)</i>	<i>SPQ</i>
NSCSA240A1-Q1TSPR	TSSOP (8)	20	1	-40~+125	3000
NSCSA240A2-Q1TSPR	TSSOP (8)	50	1	-40~+125	3000
NSCSA240A3-Q1TSPR	TSSOP (8)	100	1	-40~+125	3000
NSCSA240A4-Q1TSPR	TSSOP (8)	200	1	-40~+125	3000
NSCSA240A1-Q1SPR	SOIC (8)	20	3	-40~+125	2500
NSCSA240A2-Q1SPR	SOIC (8)	50	3	-40~+125	2500
NSCSA240A3-Q1SPR	SOIC (8)	100	3	-40~+125	2500
NSCSA240A4-Q1SPR	SOIC (8)	200	3	-40~+125	2500

11.Revision History

Revision	Description	Date
1.0	Initial Release version	2026/02

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