

Product Overview

The NSC6362 is a digital amplifier with PDM output for MEMS Microphone. The NSC6362 has integrated low noise bias circuit for MEMS microphone, high performance analog amplifier deliver the genuine sound quality and an Σ - Δ modulator based A/D converter. Both of the bias voltage and the gain can be adjusted by the internal OTP, so the NSC6362 can support different MEMS transducers with different parameters, which also improves the yield and provide better consistency of sensitivity. The NSC6362 is a 8-pin chip includes a SEL pin for selecting data asserting clock edge. The programming of the NSC6362 can be done using the one-wire-interface shared by the SEL pin. The NSC6362 supports dynamic current biasing based on the input clock frequency thus it can be used in different power modes.

Key Features

- Operation Voltage: 1.62V~3.6V
- Work Mode: Sleep mode, Low power mode and Normal mode
- Current Consumption: 330uA@768 kHz, 770uA@2.4MHz
- Input Equivalent Noise: 3 μ Vrms (-110dBV, a-weight)
- Gain Trimming: 0~23dB
- Bias Voltage: 7V~18V
- Data Selection: Rising edge and falling edge
- Operating Temperature: -40°C ~ 85°C
- Package: Chip (Wafer)
- RoHS Compliance

Applications

Audio digital amplifier for MEMS microphones for cellphone, laptop, wearable devices, smart home devices, TV, remote controllers and IoT.

Block Diagram

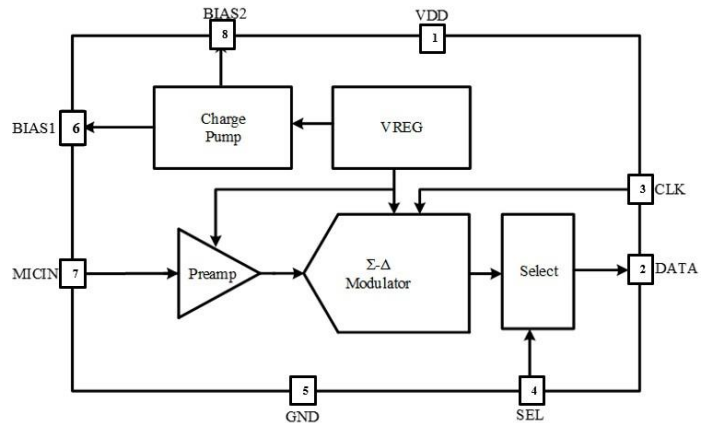


Figure 1. NSC6362 Block Diagram

INDEX

1. PAD CONFIGURATION AND FUNCTIONS.....	3
2. ABSOLUTE MAXIMUM RATINGS	3
3. ESD RATINGS	4
4. RECOMMENDED OPERATING CONDITIONS.....	4
5. SPECIFICATIONS.....	4
5.1. ELECTRICAL CHARACTERISTICS.....	4
5.2. INTERFACE TIMING SPECIFICATIONS	6
6. APPLICATION NOTE	6
6.1. SYSTEM CONNECTION.....	6
7. ORDERING INFORMATION	7
8. REVISION HISTORY	7

1. Pad Configuration and Functions

Die Size: 680umx856um

Pad Size: 60umx60um

Scribe Line: 60um

Pad Thickness: 0.9um

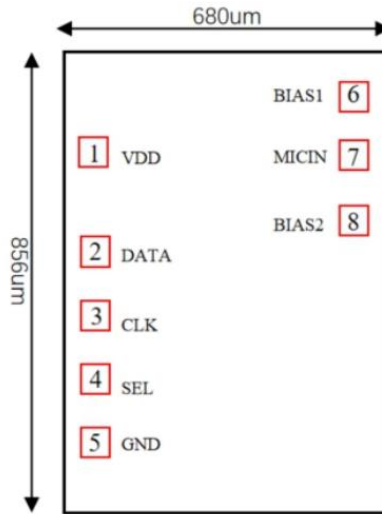


Figure 1.1 NSC6362 Pad Configuration Diagram

Table 1.1 NSC6362 Pad Configuration and Description

NSC6362 PIN No.	Symbol	Function	Pad Coordinates (X,Y)[um]	
1	VDD	Supply Voltage	-290.4	137.8
2	DATA	PDM Output	-290.4	-32.9
3	CLK	Clock Input	-290.4	-141.2
4	SEL	L/R Selection, internally pulled low	-290.4	-236.2
5	GND	Ground	-290.4	-331.2
6	BIAS1	Bias Voltage Output	290.4	217.3
7	MICIN	MEMS Input	287.1	126.9
8	BIAS2	Bias Voltage Output	290.4	14.6

Note: The center of the chip is the origin.

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD	-0.3		6.5	V	
Maximum Input Voltage	VIN	-0.4		+0.4	V	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Operating Temperature	Top	-40		85	°C	
Storage Temperature	Tstg	-40		125	°C	

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the devices at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3. ESD Ratings

Ratings		Value	Unit
Electrostatic Discharge	Human body model (HBM), JESD22-A114 ● VDD, DATA, CLK, SEL	±2.0	kV
	Charged device model (CDM), JESD22-C101 ● VDD, DATA, CLK, SEL	±500	V

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Voltage	V _{DD}	1.62	1.8	3.6	V	
Logic Input High	V _{IH}	0.65* VDD		VDD+0.3	V	
Logic Input Low	V _{IL}	-0.3		0.35* VDD	V	
Logic Output High	V _{OH}	VDD-0.45			V	
Logic Output Low	V _{OL}			0.45	V	
Clock Duty Cycle ¹		40		60	%	

1) 50% duty cycle for optimal performance.

5. Specifications

5.1. Electrical Characteristics

Typical test conditions are V_{DD} =1.8V, Clock=2.4MHz, T=25±2°C, 55±20% R.H., ASIC only test with a 0.1uF decoupling capacitor across VDD and GND, unless otherwise specified.

Parameters	Symbol	Min	Typ	Max	Unit	Comments
General Specifications						
Supply Voltage	V _{DD}	1.62	1.8	3.6	V	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
General Specifications						
Polarity		Increasing density of 1's				Increasing sound pressure
Data Format		1/2 cycle PDM				
Gain	V_G	0		23	dB	Changes with MEMS capacitance
Bias Voltage	V_{bias}	7		18	V	Refer to trimming instructions
Short Output Current	I_{sc}	1		20	mA	DATA PIN Short to GND
Output Load	C_{load}			100	pF	
Fall Asleep Time	T_{slp}			20	us	Time to Reset which means Data is High-Z after VDD has been off for more than 2ms, while Clock always on.
Start Up Time	T_{start}			20	ms	Time to start up which means Sens reaches $\pm 0.5dBFS$ after VDD has been on, while Clock always on.
Mode Change Time	T_{mc}			20	ms	Time to mode change which means Sens reaches $\pm 0.5dBFS$ after Clock frequency change, while VDD always on.
Total Harmonic Distortion	THD		1		%	500mVpp input, default Gain
			10		%	730mVpp input, default Gain
Normal Mode Specifications						
Clock Frequency	F_{clk}	1.3		4.8	MHz	
Supply Current	I_{DD}		770		uA	
Input Referred Noise	V_n		3		uV	
Power Supply Rejection Ratio	PSRR		60		dBFS	200mVpp 1KHz Sine wave, Gain= default value
Low Power Mode Specifications ($F_{clk}=768kHz$)						
Clock Frequency	F_{clk}	150		900	kHz	
Supply Current	I_{DD}		330		uA	
Input Referred Noise	V_n		4.5		uV	
Sleep Mode Specifications ($F_{clk}<10kHz$)						
Clock Frequency	F_{clk}	0		10	kHz	
Sleep Current	I_{sleep}		3		uA	$F_{clk} = 0Hz, VDD=1.8V$

5.2. Interface Timing Specifications

Typical test conditions are $V_{DD} = 1.8V$, Clock=2.4MHz, $T = 25 \pm 2^\circ C$, 55±20% 6R.H., ASIC only test with a 0.1uF decoupling capacitor across VDD and GND, unless otherwise specified.

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Clock Rising Time	T_R			15	ns	
Clock Falling Time	T_F			15	ns	
DATA into Hi Z time	T_{DZ}	5		20	ns	
DATA Valid Time	T_{DV}	40		100	ns	RL=100KΩ, CL=100pF
Delay Time for Data Driven	T_{DD}	25		50	ns	
Clock Duty Cycle		40	50	60	%	

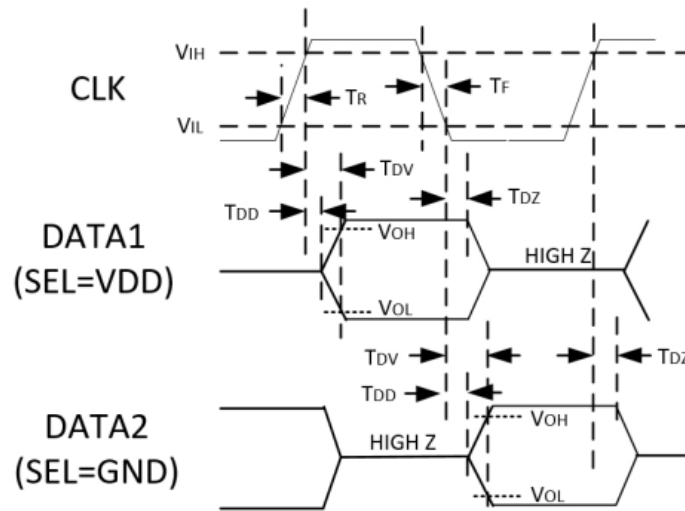


Figure 5.1 Timing Diagram of CLK and DATA1/DATA2 Terminals

6. Application Note

6.1. System Connection

NSC6362 can be used individually or in parallel.

The SEL pin can be flexibility connected to GND or VDD for different application scenarios, such as mono or stereo.

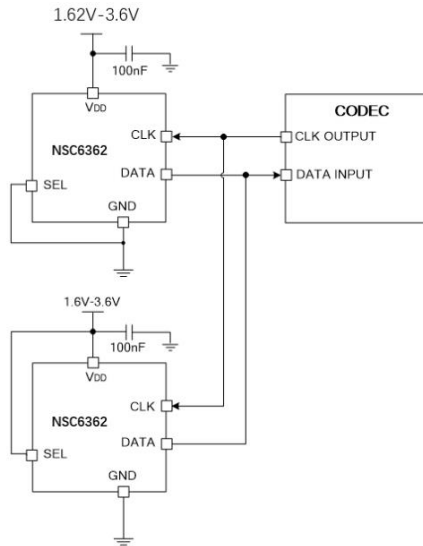


Figure 6.1 System Connection

Note:

1. Place 100nF decoupling capacitor between VDD and GND, and place this capacitor as near to ASIC’s VDD PIN as possible.
2. Connect SEL PIN to VDD PIN or GND PIN as near as possible. Keep SEL PIN away from DATA PIN.
3. Keep DATA PIN’s route away from ASIC’s MICIN PIN and BIAS PIN. Shield DATA route from ASIC’s substrate if it’s under ASIC’s substrate.

7. Ordering Information

Part Number	Package	Wafer Size	Minimum Ordering Quantity(MOQ)
NSC6362-L075P12D	Whole Wafer	8 inches	1pcs wafer

8. Revision History

Revision	Description	Date
1.0	Initial Version	2021/4/25
1.1	Update fig4.1 description	2021/4/27
1.2	Update chip view	2021/5/31
1.3	Update spec description	2021/7/2
1.4	Update spec4.1 description	2022/7/11
1.5	Update timing specification	2022/7/19
1.6	Update the template, ordering Information	2024/1/19

IMPORTANT NOTICE

The information given in this document (the “Document”) shall in no event be regarded as any warranty or authorization of, express or implied, including but not limited to accuracy, completeness, merchantability, fitness for a particular purpose or infringement of any third party’s intellectual property rights.

Users of this Document shall be solely responsible for the use of NOVOSENSE’s products and applications, and for the safety thereof. Users shall comply with all laws, regulations and requirements related to NOVOSENSE’s products and applications, although information or support related to any application may still be provided by NOVOSENSE.

This Document is provided on an “AS IS” basis, and is intended only for skilled developers designing with NOVOSENSE’ products. NOVOSENSE reserves the rights to make corrections, modifications, enhancements, improvements or other changes to the products and services provided without notice. NOVOSENSE authorizes users to use this Document exclusively for the development of relevant applications or systems designed to integrate NOVOSENSE’s products. No license to any intellectual property rights of NOVOSENSE is granted by implication or otherwise. Using this Document for any other purpose, or any unauthorized reproduction or display of this Document is strictly prohibited. In no event shall NOVOSENSE be liable for any claims, damages, costs, losses or liabilities arising out of or in connection with this Document or the use of this Document.

For further information on applications, products and technologies, please contact NOVOSENSE (www.novosns.com).

Suzhou NOVOSENSE Microelectronics Co., Ltd