NSC6360: MEMS Microphone Preamp

Datasheet (EN) 1.4

Product Overview

The NSC6360 is adigitalpre-amplifier with PDM output for MEMS Microphone.The NSC6360 has integrated low noise bias circuit for MEMSmicrophone, high performance analog pre-amplifier deliver thegenuine sound qualityand an ∑-Δ modulator based A/D converter. Both of the bias voltage and thegain can be adjusted by the internal OTP, so the NSC6360 can support different MEMS transducers with different parameters, which also improves the yield and provide better consistency of sensitivity.The NSC6360 is a 7-pin chip includes a SEL pin for selecting data asserting clock edge. The programming of the NSC6360 can be done using the one-wire-interface shared by the SEL Fpin. The NSC6360 supports dynamic current biasing based on the input clock frequency thus it can be used in different power modes.

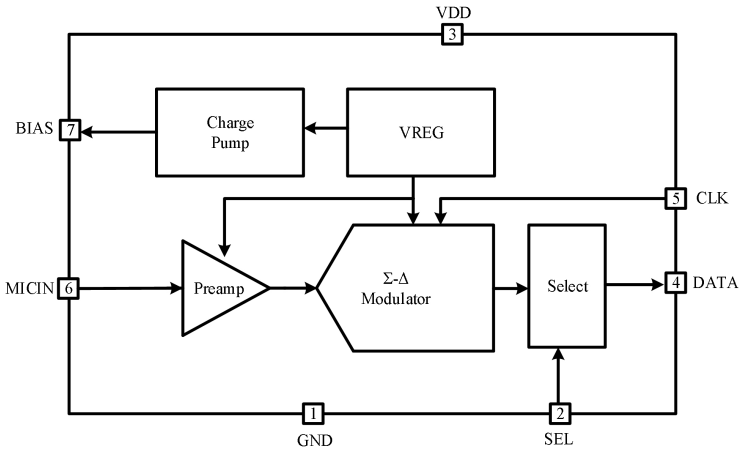
Key Features

Operating Voltage	1.6V~3.6V
Work Mode	Sleep Mode, Low power mode and Normal Mode
Current Consumption	300 uA@768 kHz, 800 uA@2.4MHz.
Input equivalent noise	4.5μVrms (-107dBV, a-weight)
Gain (OTP trimming)	9~17dBFS/dBVrms with 0.6dB/Step
Bias Voltage	7.6V~15.9V with 1.18V/Step
Data selection	Rising edge and falling edge
Operating temperature	-40ºC ~ 85ºC
Package	Chip (Wafer)

Applications

- PDM output MEMS Microphone

Block Diagram



Index

1.0 ABSOLUTE MAXIMUM RATINGS

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power Supply Voltage	VDD	-0.3		6.5	V	
Maximum Input Voltage	VIN	-0.4		+0.4	V	
Operating Temperature	Top	-40		85	℃	
StorageTemperature	Tstg	-40		125	℃	
ESD Tolerance	HBM	±2			kV	
	CDM	±500			V	

2.0 ELECTRICAL CHARACTERISTICS

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
General Specifications (TA = 25°C VDD = 1.8 V, SEL = GND)						
Supply Voltage	VDD	1.6	1.8	3.6		
DC Output			0		%FS	+-100
Polarity		Increasing density of 1's				Increasing sound pressure
Data Format		1/2 cycle PDM				
Gain	V_G	9	13	17	dBFS/dBVp	OTP Trimming, 0.6dB/Step
Bias Voltage	V_{bias}	7.6	7.6	15.9	V	OTP Trimming setup, 1.18V/Step
Variation of Vbais	Varvb	-10	0	-10	%	
Short Output Current	Isc	1		20	mA	DATA PIN Short to GND
Output Load	Cload			140	pF	
Fall Asleep Time	Tslp			20	us	Fclk< 250kHz
Wake-up Time	Twk			20	ms	Fclk> 350 kHz
Power Up Time	Tpu			20	ms	
Mode Change Time	Tmc			20	us	
Total Harmonic Distortion	THD			1	%	32mVpp input, Gain= 13dBFS/dBVp
				3	%	56mVpp input, Gain= 13dBFS/dBVp
NormalMode Specifications(25°C VDD = 1.6 V~3.6V, SEL = GND, Fclk = 2.4MHz, no load, unless otherwise indicated						
Clock Frequency	Fclk	1		4.8	MHz	

Supply Current	Idd		800	1000	uA	
Input referred noise	Vn		3.5		uV	
Power Supply Rejection Ratio	PSRR		50		dBFS	200mVpp 1KHzSinewave, Gain= 13 dBFS/dBVp
Power Supply Rejection	PSR		-80		dBFS	100mVpp 217Hz Square wave, Gain= 13 dBFS/dBVp
Low Power Mode Specifications(25°C VDD = 1.8~3.6 V, SEL = GND, Fclk=768kHz, no load, unless otherwise indicated						
Clock Frequency	Fclk	350		800	kHz	
Supply Current	Idd		300	400	uA	
Input referred noise	Vn		6		uV	
Sleep Mode Specifications(25°C VDD = 1.8 V, SEL = GND, Fclk< 250kHz, no load, unless otherwise indicated						
Clock Frequency	Fclk	0		250	kHz	
Sleep Current	Isleep		32			Fclk = 0Hz, VDD =1.8V
			42			Fclk =0Hz, VDD = 3.6V
Interface Specifications						
Logic input High	Vih	0.65*VDD		VDD+0.3	V	
Logic input Low	Vil	-0.3		0.35*VDD	V	
Logic Output High	Voh	VDD-0.45			V	
Logic Output Low	Vol			0.45	V	
Clock Duty Cycle		40		60	%	

3.0 FUNCTION DESCRIPTION

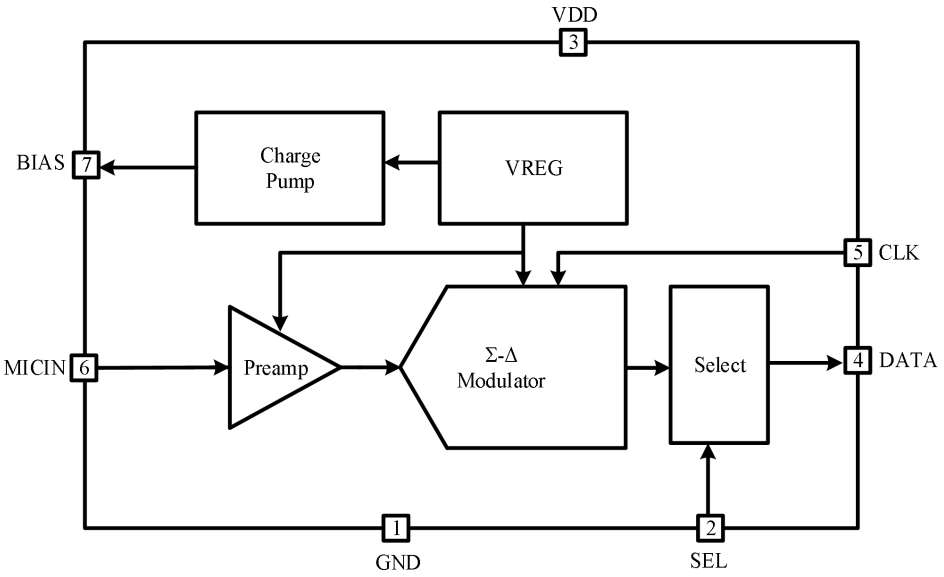
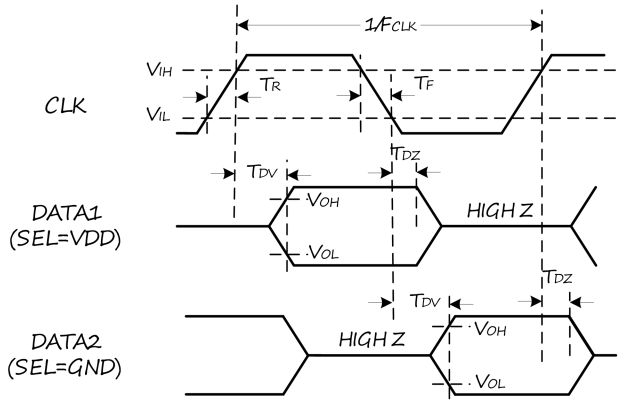


Figure 3.1 Block Diagram of NSC6360

3.1. I/O TIMING

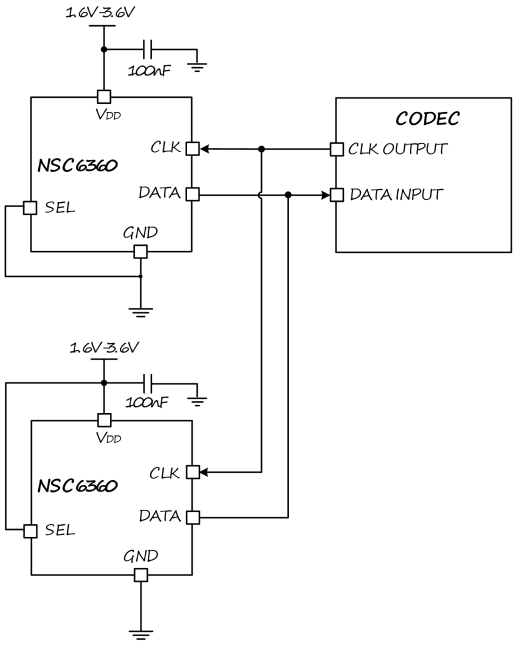


Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Clock Rising Time	T_R			15	ns	RL=1MΩ, CL=12pF
Clock Falling Time	T_F			15	ns	RL=1MΩ, CL=12pF
DATA into Hi Z time	T_{DZ}	0		20	ns	RL=1MΩ, CL=12pF
DATA Valid time	T_{DV}	24	36	48	ns	RL=1MΩ, CL=12pF
Clock Jitter				0.5	ns	Period jitter in RMS
Clock Duty Cycle		40	50	60	%	
Clock Frequency		350	2400	4800	KHz	

Figure 3.2 Timing Diagram of CLK and DATA1/DATA2 Terminals

3.2. TYPICAL APPLICATION CIRCUITS

The SEL pin can be flexibility connected to GND or VDD for different application scenarios, such as mono or stereo.



SEL Pad Connection	*Channel Selected*
VDD	DATA1
GND	DATA2

Figure 3.3 Typical Application Circuit of NSC6360

4.0 CHIP OUTLINE

Chip Size: 0.905mm x 0.779mm
ChipThickness: >200µm
Pad Size: 60µm x 60µm
Pad Thickness: 0.8375µm

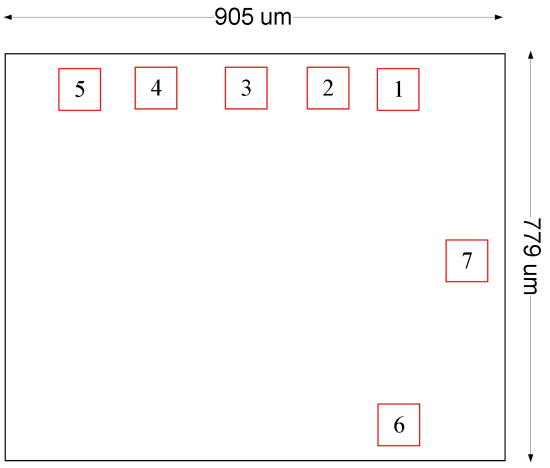
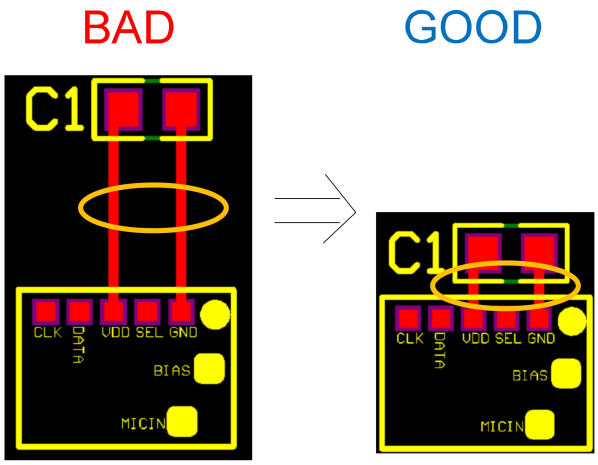


Figure 4.1 Chip view

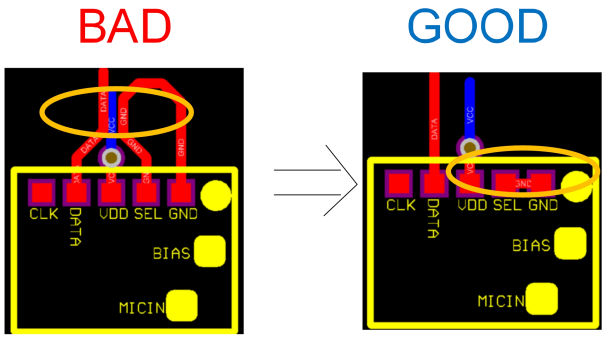
PIN NO.	SYMBOL	FUNCTION	X	UNIT	Y	UNIT
1	GND	Ground	706.205	μm	721.32	μm
2	SEL	L/R Selection, internally pulled low	480.47	μm	721.32	μm
3	VDD	Supply voltage	349.2	μm	720.8	μm
4	DATA	PDM output	218.07	μm	721.3	μm
5	CLK	Clock input	90.07	μm	721.32	μm
6	MICIN	MEMS input	698.21	μm	48.01	μm
7	BIAS	Bias Voltage Output	854.31	μm	435.83	μm

5.0 LAYOUT NOTE

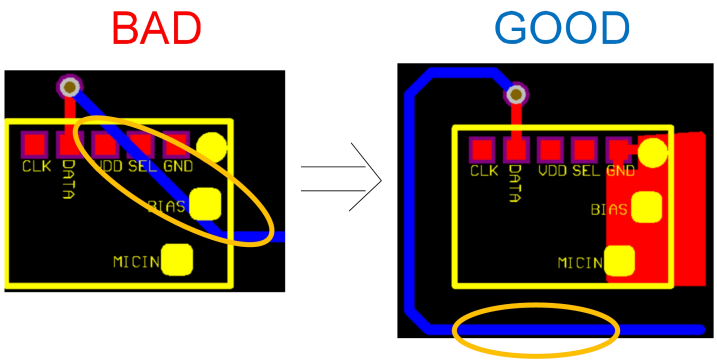
1. Place 100nF decoupling capacitor between VDD and GND, and place this capacitor as near to ASIC's VDD PIN as possible.



2. Connect SEL PIN to VDD PIN or GND PIN as near as possible. Keep SEL PIN away from DATA PIN.



3. Keep DATA PIN's route away from ASIC's MICIN PIN and BIAS PIN. Shield DATA route from ASIC's substrate if it's under ASIC's substrate.



6.0 ORDER INFORMATION

Please refer to "NSC6360_Part_Selection_Guide.xlsx".

7.0 REVISION HISTORY

Revision	Description	Date
0.0	Initial Version	2016/9/28
0.1	1. Update pin definition 2. Update Chip Outline Section	
0.2	1. Update Gain definition 2. Update Fall Asleep Time, Wake-up Time, Power Up Time, Mode Change Time 3. Update PSRR, PSR 4. Add propagation delay parameter	2019/4/26
1.0	1.Update some layout detail	2019/5/23
1.2	1.Add application note	2019/6/12
1.3	1.Add order information	2020/6/2
1.4	Update vbias variation, 2.4MHz/768kHz IDDmax	2021/3/2