NSC2860

General sensor conditioning converter

Datasheet (EN) 1.0

Product Overview

NSC2860 is a highly integrated signal conditioning chip for capacitive sensors. The NSC2860 uses a C/V converter and a 24-bit ADC to form the main signal measurement channel, and a 24-bit ADC to form the auxiliary temperature measurement channel. Through the built-in MCU, the NSC2860 supports the 2nd order temperature drift calibration of the sensor's zero, sensitivity and the highest 3rd order nonlinear calibration. The calibration coefficient is stored in a 64 bytes multi-programmable EEPROM. The NSC2860 integrates a regulator with an external JFET, and can support a variety of output modes such as digital interface output, analog voltage output, 4-20mA transmission output, SPI/I²C/PWM/PDM digital output. The high integration and clever interface scheme enable the NSC2860 to calibrate and transmit capacitive sensor transmitter modules with minimal external components.

Key Features

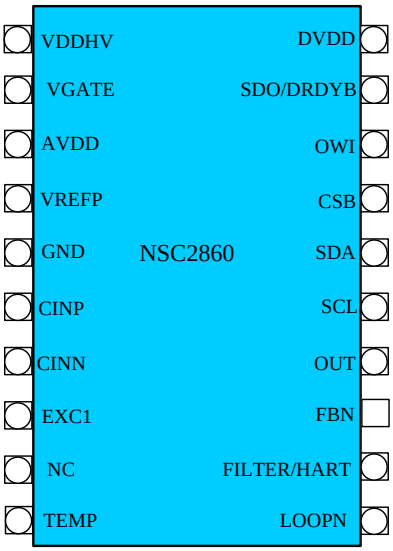
- Low drift voltage reference
- C/V converter, supports max differential capacitance input up to ±16pF
- 24-bit ADC for primary signal measurement
- 24-bit ADC for temperature measurement
- Internal and external temperature sensor supported
- 16-bit DAC
- 1X~8X digital gain
- Multiple filter settings, 50/60Hz power frequency suppression
- Sensor calibration algorithm embedded in a built-in MCU
- 64 bytes EEPROM
- 4~20mA current loop
- Ratiometric or absolute voltage output
- SPI/I²C
- PWM/PDM
- High voltage regulator with external JFET or Bipolar
- TSSOP20 Package
- Operation temperature: -40℃~125℃
- RoHS & REACH compliance

Applications

- Capacitive pressure sensors and transmitters
- Capacitive level transmitter

Device Information

Part Number	*Package*	*Body Size*
NSC2860_TSSOP	TSSOP20	6.4mm × 6.5mm



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1. Pin Configuration and Functions

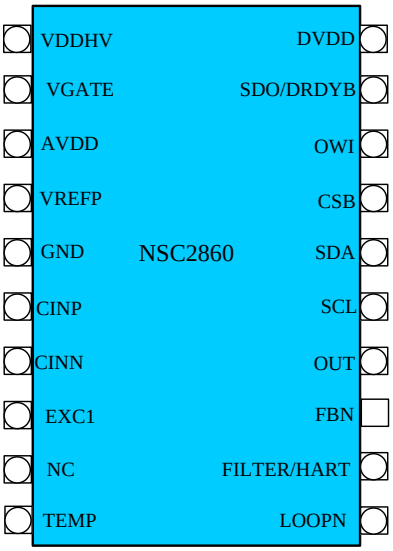


Figure1.1 TSSOP20 package pin configuration

Table 1.1 TSSOP20 package pin description

PIN.No.	*Pin Name*	*Type*	*Description*
1	VDDHV	Supply	Supply with overvoltage/reverse voltage protection
2	VGATE	Analog Output	JFET Regulation Output
3	AVDD	Supply	Power Supply
4	VREFP	Analog	Reference Voltage Output/Input
5	GND	Supply	Ground
6	CINP	Analog	Analog input positive
7	CINN	Analog	Analog input negative
8	EXC	Analog	Capacitive excitation signal pin
9	NC	Analog	Keep float
10	TEMP	Analog	External temperature sensor input (ODR_T ≠ 4'b1111) External Negative Reference Voltage input (ODR_T = 4'b1111)
11	LOOPN	Analog	Loop negative port
12	FILTER/HART	Analog	DAC output filter/HART
13	FBN	Analog	Output drive feedback
14	OUT	Analog	Driver output pin
15	SCL	Digital Input	I^2C/SPI clock signal
16	SDA	Digital I/O	I^2C data signal (SDA) or SPI data signal (SDIO)
17	CSB	Digital Input	I^2C/SPI mode selection pin, SPI chip selection

18	OWI	Digital Input	One-wire interface
19	SDO/DRDYB	Digital Input	4-wire SPI date output/data ready interruption
20	DVDD	Analog	1.8V DVDD digital LDO output

2. Absolute Maximum Ratings

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
VDDHV	$VDDHV_{max}$	-24		28	V	70℃, 1 hour
AVDD	$AVDD_{max}$	-0.3		6.5	V	
Analog Pin Voltage		-0.3		AVDD+0.3	V	
VGATE Pin Voltage	$VGATE_{max}$	-0.3		7.5	V	
LOOPN Pin Voltage	$LOOPN_{max}$	-1.2		0.3	V	
Analog Output Current Limit				25	mA	
Digital Pin Voltage		-0.3		AVDD+0.3	V	25℃
Maximum Junction Temperature	T_j			155	℃	
Storage Temperature		-60		150	℃	
Operation Temperature	T_{A_EXT}	-40		125	℃	Normal temperature range
	T_{A_ADV}	-40		85	℃	Best Performance Temp range
	T_{A_BST}	125		150	℃	Extended temperature range, for 500h max over life time

3. ESD Ratings

Ratings		*Value*	*Unit*
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002 Rev E ● All other pins to AVDD/DVDD ● All other pins to GND ● IO pins to IO pins	±2	kV
	Charged device model (CDM), per JESD22-C101F ● All pins	±500	V

4. Electrical Characteristics

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply and Regulation						
Supply Voltage Range	AVDD	3	5	5.5	V	Supply on AVDD Pin
JFET Regulator Output	AVDDJ	4.9	5	5.1	V	JFET_LVL=0
		3.23	3.3	3.37	V	JFET_LVL=1
	PSRRAVDDJ	100			dB	@DC
		40			dB	@20kHz
DVDD Output	DVDD	1.75	1.8	1.85	V	
Power on Reset	VPOR_AVDD		2.5		V	POR threshold during power-up
	VPOR_HYS		0.1		V	POR threshold hysteresis
Current (Sensor Not Included)	I_{avdd1}		1.5		mA	4~20mA Transmitter mode (OUT_MODE = 01xb)
	I_{avdd2}		1.65		mA	0~5V voltage output (OUT_MODE = 00xb)
	I_{avdd5}		1.35		mA	Digital output only (OUT_MODE = 111b)
	I_{cmd}		45		µA	COMMAND MODE, SPI/I^2C, JFET_DIS = 1
Capacitance Measurement Channel						
Capacitance input range	C_{RANGE}		±16		pF	CV_RANGE<1:0>=0'b00
			±12		pF	CV_RANGE<1:0>=0'b01
			±8		pF	CV_RANGE<1:0>=0'b10
			±4		pF	CV_RANGE<1:0>=0'b11
Common-mode capacitor input range	C_{CM_RANGE}		192/VREF		pF	CV_RANGE<1:0>=0'b00
			144/VREF		pF	CV_RANGE<1:0>=0'b01
			96/VREF		pF	CV_RANGE<1:0>=0'b10
			96/VREF		pF	CV_RANGE<1:0>=0'b11
CAPDAC Range		0		63.5	pF	0.5pF/LSB
ADC resolution	RES_{RAW}		24		Bits	
ADC output data rate	ODR_P	2.5		2400	Hz	
ENOB	ENOB_P	Refer to Table6.1			Bits	Depend on ODR_P

Ss	**Exciting Source**					
Excitation frequency	CV_FREQ		38.4		kHz	CV_RANGE<1:0>=0'b00/01
			76.8		kHz	CV_RANGE<1:0>=0'b10/11
Excitation voltage amplitude	VAC		VREF/2		V	
Driving ability	DRV		50		pF	Allow capacitance to ground
Reference Voltage and Current Source						
Internal Bandgap Reference	VBG	1.119	1.2	1.201	V	Cannot measure directly, proportional with AVDDJ and VREF
VBG TC	VBG_TC		5	20	ppm/℃	-40°C~105℃
VREF (VREFP-VREFN)	VREF		4 or 2.5		V	VREF_DIS=0
Temperature Measurement Channel (Internal and External Temperature Sensor)						
TADC Resolution	RES_T		24		Bit	
TADC Gain	GAIN_T	1		4		1,2,4
TADC Output Data Rate	ODR_T	2.5		2400	Hz	
TADC ENOB	ENOB_T	Refer to Table 6.2, 6.3				
Built-in temperature sensor error			±1.5	±3	℃	-40 to 125℃
TEMP input impedance			1		Gohm	
DAC and Output Buffer						
DAC Resolution			16		Bit	
DAC Full Scale	VFSDAC	5V, 3.3V, 1.2V or AVDD				Depend on DAC_REF<1:0>
DNL of DAC	DNL			1	LSB	
INL of DAC	INL			10	LSB	
DAC Output RMS Noise	V_{rms}		0.5		mV	
Output Load Resistance	R_{load}	1			kOhm	0~5V Absolute Voltage Output Mode
Output Load Capacitance	C_{load}			150	nF	Voltage Output Mode
Output Shorted Current Limit	I_{short_lmt}	12		25	mA	Voltage Output Mode
Clamp High Level	V_{clamph}	0.5		1	VFSDAC	Output Short to VDD or GND
Clamp Low Level	V_{clampl}	0		0.5	VFSDAC	Set by CLAMP_HIGH<7:0>

4~20mA Current Loop						
Loop Reference Resistor	R_{loop}		50		Ohm	
Loop Current Noise	I_{rms}		0.2		μA	0.1Hz~10Hz
Downscale Alarm Current	I_{faulth}		3.375		mA	
Upscale Alarm Current	I_{faultl}		21.75		mA	
Diagnostic and Alarm						
Fault Alarm High	FAULT_HIGH	98%			VDD	
Fault Alarm Low	FAULT_LOW			2%	VDD	
OSC						
ADC Clock	FOSC_MOD		614.4		kHz	
Clock Rate Error	FOSC_ERR	-1%		1%		-40~125℃
PDM/PWM						
PDM Modulation Frequency	FPDM	19.2		153.6	kHz	
PWM Frequency	FPWM		300		Hz	
PWM Resolution	RPWM		12		bit	
EEPROM						
Programming Temperature	T_{EEP}	-40		105	℃	
Programming Supply Voltage	V_{EEP}	4.5		5.5	V	
Time for EEPROM Programming	T_{EEP}		0.8		s	
Endurance			10		k	
Date Retention		10			A	@150℃
Serial Interface						
Communication Data Rate	F_{sclk}			10	MHz	SPI Interface
				400	kHz	I^2C Interface
				50	kHz	OWI Interface

5. Register Description

The register map of the NSC2860 includes two parts, normal registers and EEPROM registers. The normal registers include data registers and some control registers, while the EEPROM registers are mainly configuration registers and calibration coefficients. All EEPROM registers should be written by external interface on command mode (register 'CMD' = '0x00').

5.1. Normal Registers

IF_CTRL (R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0x00	7, 0	SDO_ACTIVE	1'b1 1'b1	Set either of these two bits to: 0: SPI3-wire; 1: SPI4-wire (SDO as serial output)
	6, 1	LSB_FIRST	1'b0 1'b0	Set either of these two bits to: 0: SPI MSB first; 1: SPI LSB first
	5, 2	SOFTRESET	1'b0 1'b0	Set either of these two bits to 1 to reset the chip. Return to 0 after reset.

STATUS (Read Only)

Address	*Bit*	*Register Name*	*Default*	*Description*
0x02	7 – 3	ERROR_CODE<4:0>	5'b00000	Bit6=1: VIP open or short to VREF; Bit5=1: VIP short to GND; Bit4=1: VIN open or short to VREF; Bit3=1: VIN short to GND.
	2	CRC_ERR	1'b0	1: CRC error detected during EEPROM loading; When CRC error is asserted, EEPROM register bits 'OWI_DIS', 'OWI_AC_EN', 'OWI_WINDOW', 'JFET_DIS', 'VREF_DIS', 'EEPROM_LOCK' are forced to 0.
	1	LOADING_END	1'b0	1: EEPROM loading end flag
	0	DRDY	1'b0	1: Set after a new data updated and automatically cleared after a register reading to PDATA/TDATA or before the next data's coming.

PDATA (Read Only, Primary Channel Data Register)

Address	*Bit*	*Register Name*	*Default*	*Description*
0x06	7 – 0	PDATA<23:16>	0x00	Signed, 2's complement: When 'RAW_P' = 1, store the ADC output of primary channel; When 'RAW_P' = 0, store the calibrated primary channel data.
0x07	7 – 0	PDATA<15:8>	0x00	
0x08	7 – 0	PDATA<7:0>	0x00	

TDATA (Read Only, Temperature Channel Data Register)

Address	Bit	Register Name	Default	Description
0x09	7 – 0	TDATA<23:16>	0x00	Signed, 2's complement: When 'RAW_T' = 1, store the ADC output of temperature channel; When 'RAW_T' = 0, store the calibrated temperature data, LSB = 1/2^16℃. Real Temperature = TDATA/2^16+25 ℃
0x0A	7 – 0	TDATA<15:8>	0x00	
0x0B	7 – 0	TDATA<7:0>	0x00	

DAC_DATA (R/W, DAC Input Data Register)

Address	Bit	Register Name	Default	Description
0x12	7 – 0	DAC_DATA<15:8>	0x00	DAC input data, unsigned; When 'RAW_P' = 0, set by the internal calibration logic, read only, When 'DAC_BLANK'= 1 and 'RAW_P'= 1, set externally through serial interface.
0x13	7 – 0	DAC_DATA<7:0>	0x00	
0x14	0	DAC_BLANK	1'b0	Blank DAC input update when 'RAW_P' = 1, should be set before writing DAC_MSB and DAC_LSB and cleared after the writing is finished.

COMMAND (R/W, Command Register)

Address	Bit	Register Name	Default	Description
0x30	7 – 0	CMD<7:0>	0x03	0x00: Command mode, all EEPROM can be written only in command mode; 0x01/0x02: Reserved; 0x03: Active mode; 0x33: Enter EEPROM Program Mode

QUIT_OWI (Write Only)

Address	Bit	Register Name	Default	Description
0x61	7 – 0	QUIT_OWI<7:0>	0x00	Write '0x5D' to this register to quit OWI communication. If 'QUIT_OWI_CNT' = 0x00, quit OWI communication permanently; If 'QUIT_OWI_CNT' is not 0x00, quit OWI mode temporarily for some certain time and then get back to OWI mode.

QUIT_OWI_CNT (R/W)

Address	Bit	Register Name	Default	Description
0x62	7 – 0	QUIT_OWI_CNT<7:0>	0x00	Time for temporarily quit OWI communication Mode. 0x00: Quit forever, 0x01: 50ms, 0x02: 100ms … 0xFF: 12.8s

EE_PROG (R/W)

Address	Bit	Register Name	Default	Description
0x6A	7 – 0	EE_PROG<7:0>	0x00	Write '1E' to this register to start EEPROM Programming. Automatically cleared to '0x00' after programming is finished.

VDD_CHECK (R/W)

Address	Bit	Register Name	Default	Description
0x70	0	VDD_CHECK	1'b0	Write '1' to force AVDD/2 as the input of temperature ADC

5.2. EEPROM Registers

SYS_CONFIG1 (R/W)

Address	Bit	Register Name	Default	Description
0xA1	7	CAL_MODE	1'b0	0: One segment calibration with the 2nd order temperature coefficients; 1: Two segment calibration with the 1st order temperature coefficients
	6	BURNOUT_EN	1'b0	1: Enable the 100nA burnout current sources and diagnosis
	5	FAULT_ON	1'b0	1: When any fault is detected, pull analog output to a fixed level of voltage or loop current.
	4	FAULT_LVL	1'b0	0: Low alarm output (voltage output), 3.375mA (current output); 1: High alarm output (voltage output), 21.75mA (current output)
	3	OWI_AC_EN	1'b0	0: Single-port OWI communication mode; 1: Dual-port OWI communication mode
	2	OWI_WINDOW	1'b0	0: OWI can be entered during a 10ms~80ms window after powering up or soft reset; 1: Infinite window, OWI can be entered any time after powering up
	1	OWI_DIS	1'b0	1: OWI disabled (won't be effective until next power on reset or soft reset after EEPROM is programmed)
	0	INT_EN	1'b0	1: Enable data ready interruption (through SDO/DRYB pin, active low)

SYS_CONFIG2 (R/W)

Address	Bit	Register Name	Default	Description
0xA2	7	JFET_DIS	1'b0	1: Disable JFET regulator
	6	JFET_LVL	1'b0	0: JFET regulator outputs 5V; 1: JFET regulator outputs 3.3V
	5	VREF_DIS	1'b0	1: Disable reference buffer, and reference voltage can be forced externally
	4	VREF_LVL	1'b0	0: VREFP = 4V; 1: VREFP = 2.5V
	3	T_OUT_EN	1'b0	1: When not in OWI mode, TADC data outputs through OWI pin in PWM format
	2 - 0	OUT_MODE<2:0>	3'b000	000: Voltage output; 001: Reserved, should not be used; 010/011: Current loop output;

				100: PDM output; 101: PWM output; 110: Reserved, should not be used; 111: Disable DAC

CV_CONFIG (R/W)

Address	Bit	Register Name	Default	Description
0xA3	7	CV_MODE	1'b0	0: Drive mode C/V conversion; 1: Grounding mode C/V conversion
	6 - 0	CAPOFF<6:0>	0'x0	CAPOFF<6:0>: Sets the input of the internal offset CAPDAC CAPOFF = CAPOFF<6:0>*0.5pF

PCH_CONFIG1

Address	Bit	Register Name	Default	Description
0xA4	7 –6	Reserved	2'b00	Reserved. Must be 0
	5 - 4	CV_RANGE<1:0>	2'b00	00: C_{RANGE} = ±16pF, C_{CM_RANGE} = 192/VREF; 01: C_{RANGE} = ±12pF, C_{CM_RANGE} = 144/VREF; 10: C_{RANGE} = ±8pF, C_{CM_RANGE} = 96/VREF; 11: C_{RANGE} = ±4pF, C_{CM_RANGE} = 96/VREF;
	3 –0	ODR_P<3:0>	4'b0000	PADC output data rate setting 0000:2.4kHz, 0001: 1.2kHz, 0010: 600Hz, 0011: 300Hz, 0100: 150Hz, 0101:75Hz, 0110:37.5Hz, 0111:18.75Hz, 1000:10Hz (with 60Hz notch), 1001:10Hz (with 50Hz notch), 1010:5Hz (with 60Hz notch), 1011:5Hz (with 50Hz notch), 1100:2. 5Hz (with 60Hz notch), 1101：2.5Hz (with 50Hz notch) 1110,1111: PADC disabled.

PCH_CONFIG2(R/W)

Address	Bit	Register Name	Default	Description
0xA5	7 – 6	DAC_REF<1:0>	2'b00	DAC full scale reference 00: 5V, 01: 3.3V, 10: 1.2V, 11: AVDD (ratio-metric)
	5 – 1	RESERVED	5'b00000	Reserved.
	0	RAW_P	1'b0	0: update calibrated sensor data into 'PDATA' register. 1: update raw PADC data into 'PDATA' register after conversion.

TCH_CONFIG(R/W)

Address	Bit	Register Name	Default	Description
0xA6	7	EXT_TEMP	1'b0	0: internal temperature sensor selected. 1: external temperature sensor selected (TEMP pin as external temperature sensor input).
	6 – 5	GAIN_T<1:0>	2'b00	Gain for temperature channel. (TEMP pin as external temperature sensor input) 00:1X, 01:2X, 10/10:4X

	4 – 1	ODR_T	4'b0000	TADC output data rate, similar as ODR_P 0000: 2.4kHz, 0001: 1.2kHz, 0010: 600Hz, 0011: 300Hz, 0100: 150Hz, 0101: 75Hz, 0110: 37.5Hz, 0111: 18.75Hz, 1000: 10Hz (with 60Hz notch), 1001: 10Hz (with 50Hz notch), 1010: 5Hz (with 60Hz notch), 1011: 5Hz (with 50Hz notch), 1100: 2.5Hz (with 60Hz notch), 1101: 2.5Hz (with 50Hz notch), 1110, 1111 : TADC disabled When TADC is disabled, the negative reference voltage (VREFN) for PADC is driven externally through TEMP pin.
	0	RAW_T	1'b0	1: store the raw TADC output into 'TDATA' register. 0: store the calibrated TADC data into 'TDATA' register.

CLAMPH(R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0xA7	7 – 0	CLAMPH<7:0>	0x00	Set clamping high level. (1- CLAMPH *2^(-9))* VFSDAC

CLAMPL(R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0xA8	7 – 0	CLAMPL<7:0>	0x00	Set clamping low level, CLAMPL *2^(-9) * VFSDAC

OFFSET0 (R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0xa9	7 – 0	OFF0<15:8>	0x00	Sensor calibration coefficient, offset at T0. LSB = 1/2^15, RANGE (-1, +1)
0xaa	7 – 0	OFF0<7:0>	0x00	

CTC1 (R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0xab	7 – 0	CTC1<15:8>	0x00	Sensor calibration coefficient, CAL_MODE = 0: the 1st order temperature coefficient of offset. LSB = 1/2^22, RANGE (-0.00781, +0.00781); CAL_MODE = 1: the 1st order temperature coefficient of offset for segment 0. LSB = 1/2^22, RANGE (-0.00781, +0.00781)
0xac	7 – 0	CTC1<7:0>	0x00	

CTC2 (R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0xad	7 – 0	CTC2<15:8>	0x00	Sensor calibration coefficient, CAL_MODE = 0: the 2nd order temperature coefficient of offset. LSB = 1/2^29, RANGE (-6.1e-5, 6.1e-5); CAL_MODE = 1: the 1st order temperature coefficient of offset for segment 1. LSB = 1/2^22, RANGE (-0.00781, +0.00781)
0xae	7 – 0	CTC2<7:0>	0x00	

S0 (R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0xaf	7 – 0	S0<15:8>	0x00	Sensor calibration coefficient, sensitivity at T0. LSB = 1/2^15 (unsigned), RANGE (0, 2)
0xb0	7 – 0	S0<7:0>	0x00	

STC1 (R/W)

Address	Bit	Register Name	Default	Description
0xb1	7 – 0	STC1<15:8>	0x00	Sensor calibration coefficient, CAL_MODE = 0: the 1st order temperature coefficient of sensitivity. LSB = 1/2^22, RANGE (-0.00781, +0.00781); CAL_MODE = 1: the 1st order temperature coefficient of sensitivity for segment 0. LSB = 1/2^22, RANGE (-0.00781, +0.00781)
0xb2	7 – 0	STC1<7:0>	0x00	

STC2 (R/W)

Address	Bit	Register Name	Default	Description
0xb3	7 – 0	STC2<15:8>	0x00	Sensor calibration coefficient, CAL_MODE = 0: the 2nd order temperature coefficient of sensitivity. LSB = 1/2^29, RANGE (-6.1e-5, 6.1e-5); CAL_MODE = 1: the 1st order temperature coefficient of sensitivity for segment 1. LSB = 1/2^22, RANGE (-0.00781, +0.00781)
0xb4	7 – 0	STC2<7:0>	0x00	

KS (R/W)

Address	Bit	Register Name	Default	Description
0xb5	7 – 0	KS<15:8>	0x00	Sensor calibration coefficient, the 2nd order nonlinearity coefficient. LSB = 1/2^15, RANGE (-1, +1)
0xb6	7 – 0	KS<7:0>	0x00	

KSS (R/W)

Address	Bit	Register Name	Default	Description
0xb7	7 – 0	KSS<15:8>	0x00	Sensor calibration coefficient, the 3rd order nonlinearity coefficient. LSB = 1/2^16, RANGE (-0.5, +0.5)
0xb8	7 – 0	KSS<7:0>	0x00	

SCALE_OFF (R/W)

Address	Bit	Register Name	Default	Description
0xb9	7 – 0	SCALE_OFF<23:16>	0x00	SCALE offset coefficient, LSB = 1/2^23, RANGE (-1, +1)
0xba	7 – 0	SCALE_OFF<15:8>	0x00	
0xbb	7 – 0	SCALE_OFF<7:0>	0x00	

SCALE_S (R/W)

Address	Bit	Register Name	Default	Description
0xbc	7 – 0	SCALE_S<23:16>	0x00	SCALE sensitivity coefficient (unsigned), LSB = 1/2^16 (unsigned), RANGE (0, 256)
0xbd	7 – 0	SCALE_S<15:8>	0x00	
0xbe	7 – 0	SCALE_S<7:0>	0x00	

T0 (R/W)

Address	Bit	Register Name	Default	Description
0xbf	7 – 0	T0<7:0>	0x00	Sensor calibration coefficient, reference temperature point. Real reference temperature: REAL_T0 = T0+25. LSB = 1, RANGE (-128, +127)

KTS (R/W)

Address	Bit	Register Name	Default	Description
0xc0	7 – 0	KTS<7:0>	0x00	Sensor calibration coefficient, the 2nd order nonlinearity coefficient for external temperature sensor. LSB = 1/2^7, RANGE (-1, +1)

MTO (R/W)

Address	Bit	Register Name	Default	Description
0xc1	7 – 0	MTO<15:8>	0x00	Sensor calibration coefficient, offset coefficient of external temperature sensor. MTO: LSB = 1/2^15, RANGE (-1, +1)
0xc2	7 – 0	MTO<15:8>	0x00	

KT (R/W)

Address	Bit	Register Name	Default	Description
0xc3	7 – 0	KT<15:8>	0x00	Sensor calibration coefficient, sensitivity coefficient of external temperature sensor. KT: LSB = 1/2^12, RANGE (-8, +8)
0xc4	7 – 0	KT<15:8>	0x00	

DAC_OFF (R/W)

Address	Bit	Register Name	Default	Description
0xc5	7 – 0	DAC_OFF<15:8>	0x00	DAC calibration coefficient, DAC offset. LSB = 1/2^15, RANGE (-1, +1)
0xc6	7 – 0	DAC_OFF<7:0>	0x00	

DAC_GAIN (R/W)

Address	Bit	Register Name	Default	Description
0xc7	7 – 0	DAC_GAIN<15:8>	0x00	DAC calibration coefficient, DAC gain coefficient. LSB = 1/2^16, RANGE (-0.5, +0.5)
0xc8	7 – 0	DAC_GAIN<7:0>	0x00	

PADC_OFF (R/W)

Address	Bit	Register Name	Default	Description
0xc9	7 – 0	PADC_OFF<23:16>	0x00	PADC calibration coefficient, PADC offset. LSB = 1/2^23, RANGE (-1, +1)
0xca	7 – 0	PADC_OFF<15:8>	0x00	
0xcb	7 – 0	PADC_OFF<7:0>	0x00	

PADC_GAIN (R/W)

Address	Bit	Register Name	Default	Description
0xcc	7 – 0	PADC_GAIN<15:8>	0x00	

0xcd	7 – 0	PADC_GAIN<7:0>	0x00	PADC calibration coefficient, PADC gain. LSB = 1/2^16, RANGE (-0.5, +0.5)

P0 (R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0xce	7 – 0	P0 <7:0>	0x00	Sensor calibration coefficient, reference pressure point for nonlinearity calibration. LSB = 1/2^7, RANGE (-1, 1)

SPARE (R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0xcf	7 – 0	SPARE1<7:0>	0x00	SPARE Register 1
0xd0	7 – 0	SPARE2<7:0>	0x00	SPARE Register 2
0xd1	7 – 0	SPARE3<7:0>	0x00	SPARE Register 3
0xd2	7 – 0	SPARE4<7:0>	0x00	SPARE Register 4
0xd3	7 – 0	SPARE5<7:0>	0x00	SPARE Register 5
0xd4	7 – 0	SPARE6<7:0>	0x00	SPARE Register 6
0xd5	7 – 0	SPARE7<7:0>	0x00	SPARE Register 7
0xd6	7 – 0	SPARE8<7:0>	0x00	SPARE Register 8

PDM_FREQ (R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0xd7	7 – 6	DIG_GAIN<1;0>	2'b00	ADC digital gain 00: 1X, 01: 2X, 10: 4X, 11: 8X
	5 – 4	PDM_FREQ<1:0>	2'b00	PDM modulation frequency 00: 19.2kHz, 01: 38.4kHz, 10: 76.8kHz, 11: 153.6kHz
	3 – 0	Reserved	2'b00	

RESERVED

Address	*Bit*	*Register Name*	*Default*	*Description*
0xd8	7 – 0	RESERVED	-	NOVOSENSE Information, customer should not erase these bits

EEPROM_LOCK (R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0xd9	7	EEPROM_LOCK	1'b0	1: EEPROM lock, set 1 and then EEPROM can't be programmed (won't be effective until next power on reset or soft reset after EEPROM is programmed).
	6 – 0	PartID (read only)	7'b0000001	NOVOSENSE chip ID, customer should not erase these bits

6. Function Description

6.1. Overview

The NSC2860 is a highly integrated capacitive sensor conditioner for industrial application. The NSC2860 uses differential inputs with at most ±16pF differential input capacitance range and 48pF common mode capacitance range. The chip incorporates five parts: analog front-end module, digital module, analog output module, power supply module and serial interfaces. The block diagram of the NSC2860 is shown in Figure6 .1.

Analog front-end module includes a primary signal measurement channel with a C/V converter followed by a 24-bit ∑Δ ADC, a temperature measurement channel with also a 24-bit ∑Δ ADC, for precision sensor signal and temperature measurement.

The digital module is composed of registers, EEPROM, control logic, and a built-in MCU. The sensor calibration algorithm is implemented with the built-in MCU and can supports up to 2nd order temperature drift compensation of offset and sensitivity for the sensor. It can also compensate the nonlinearity of sensor output up to 3rd order. The configuration parameters and coefficients for calibration are stored at in the EEPROM of 64 bytes.

The analog output module includes a 16-bit DAC and a flexible configurable output driver which can be configured to support analog output with several types of full-scale range and PWM output.

The power supply module includes a high precision voltage reference, a sensor voltage driver, over-voltage and reverse voltage protection block and JFET controller.

The NSC2860 supports OWI serial interface, writing and reading registers of configuration, calibration coefficients and data. Through the highly integrated and flexible interface, the NSC2860 only needs one wire to realize sensor calibration, field verification and full-scale range modification.

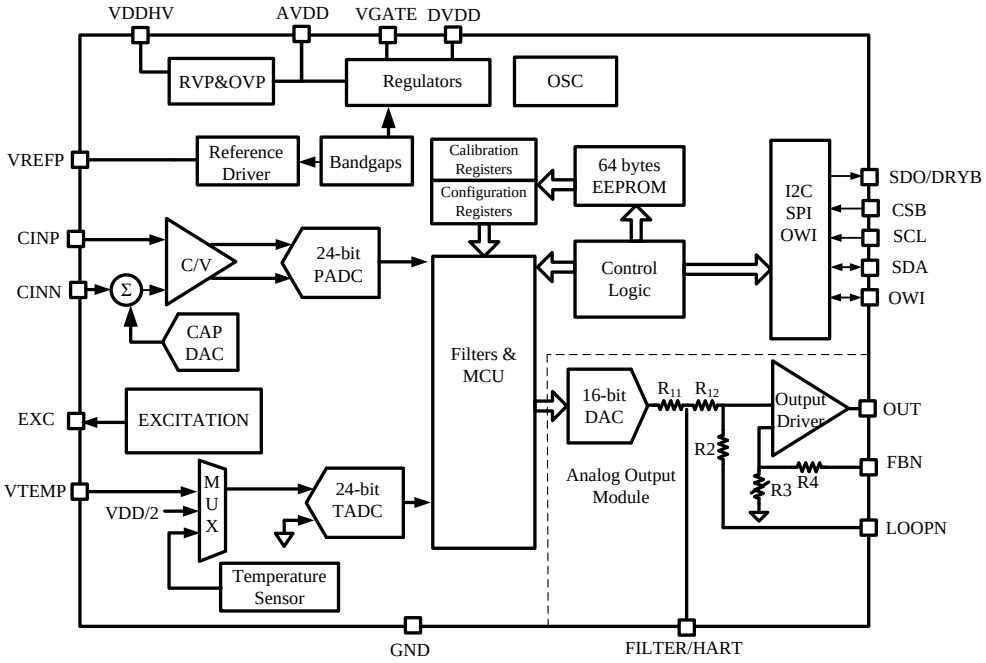


Figure 6.1 Block diagram of the NSC2860

6.2. Analog Front-end Module 1: Primary Signal Channel

6.2.1. Capacitance Measurement Mode

The NSC2860 supports two types of capacitance measurement modes: Drive Mode and Ground Mode. The NSC2860 generates a square wave at EXC pin with 38.4kHz or 76.8kHz frequency and VREF amplitude, which is used to drive input capacitor at Drive Mode or shield parasitic capacitor at Ground Mode.

When CV_MODE = 0, the NSC2860 is at Drive Mode, where the external input capacitors are connected as shown in Figure 6.2. The common end of the differential capacitor is driven by the square wave at EXC pin at Drive Mode. Since the voltage at CINP and CINN keep constant, the input parasitic capacitance would not affect the output.

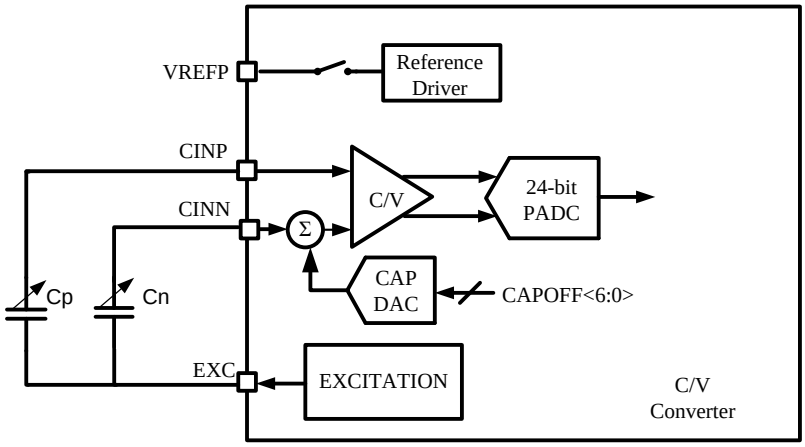


Figure 6.2 C/V converter at Drive Mode (CV_MODE = 0)

When CV_MODE = 1, the NSC2860 is at Ground Mode, where the common plate of the external differential input capacitors is grounded as shown in Figure 6.3. Both CINP and CINN are driven by the square wave at EXC pin, so the differential input capacitance is converted to voltage through charge and discharge. The 24-bit ADC then converts the voltage to digital output. Since the NSC2860 measures the capacitance between CINP/CINN and ground, the parasitic capacitance at CINP/CINN would affect the measurement directly. Worse, the parasitic capacitance may be large and susceptible to environment interfere (such as displacement, humidity and so on). To exclude the parasitic capacitance, CINP and CINN can be shielded with EXC pin as shown in Figure 6.3. Ground Mode is more suitable especially when the common plate of the differential input capacitor cannot be driven by the chip directly.

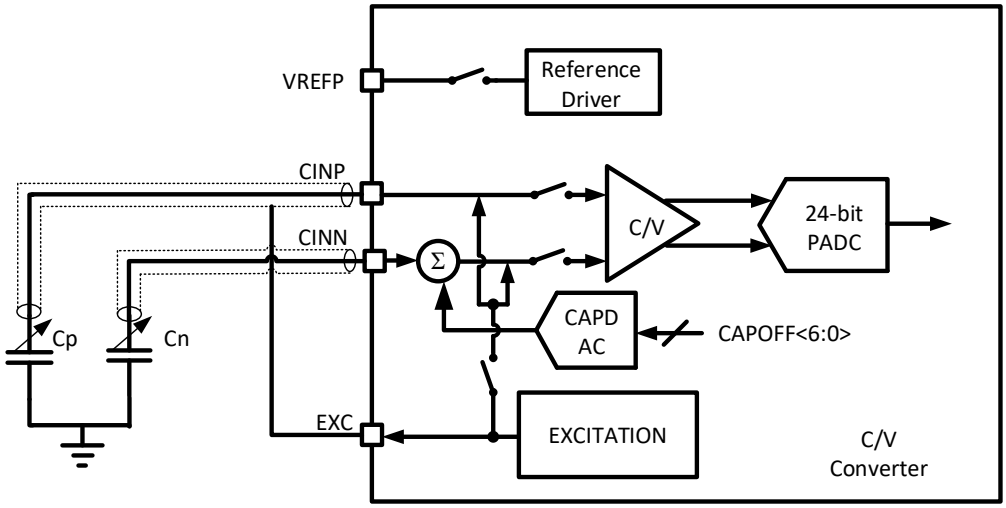


Figure 6.3 C/V converter at Drive Mode (CV_MODE = 1)

6.2.2. The Measurement Range of C/V Converter

6.2.2.1. The Differential Input Capacitance Range

The PADC converts the analog output of C/V converter to digital output, which is filtered by digital filter with 24-bit digital output PDATARAW. $PDATA_{RAW}$ is expressed by the following expression.

$$PDATA_{RAW} = \frac{C_P - C_N - CAPOFF}{|C_{RANGE}|} * 2^{23}$$

CAPOFF is an internal offset compensated capacitance configured by CAPOFF<6:0>. The unit capacitance of CAPDAC is 0.5pF, so it's as large as 127*0.5pF = 63.5pF. CRANGE is the full-scale range of C/V measurement configured by CV_RANGE<1:0>. $PDATA_{RAW}$ can be read from P channel data registers (Reg0x06, 07, 08) when RAW_P = 1. When RAW_P = 0, the built-in MCU will calibrate the sensor using sensor calibration coefficients and the data of temperature measurement. So the content of PDATA registers are the sensor output after temperature calibration.

6.2.2.1. The Common Mode Input Capacitance Range

When the differential input capacitance is not out of range ($PDATA_{RAW}$ is in between±1), the common mode capacitance range is expressed by the following expression.

$$C_{CM} = \frac{C_P + C_N + CAPOFF}{2} < C_{CM\_RANGE}$$

C_{CM_RANGE} is also related to CV_RANGE<1:0> as referred to Section 5.2.

6.2.3. Digital Filter

The bandwidth and output data rate (ODR) of the digital filter can be set by 'ODR_P'. ODR can be set from 2.4 kHz to 2.5 Hz. The lower ODR, the lower noise the PADC output will have, in the cost of slower time response. Table 6.1 shows the effective number of bits (ENOB) of PADC output with different ODR_P settings. The relationship of ENOB with RMS noise is:

$$ENOB_{RMS} = 24 - log_2(RMS_{ADC})$$

RMSADC is the RMS value of ADC output noise in LSB. The relationship between RMS ENOB ($ENOB_{RMS}$) and noise free ENOB ($ENOB_{NF}$) is shown as below:

$$ENOB_{NF} = ENOB_{rms} - 2.7$$

Table 6.1 $ENOB_{RMS}$ of PADC under different ODR settings

ODR_P(Hz)	CRANGE=±16pF	CRANGE=±12pF	CRANGE=±8pF	CRANGE=±4pF
2400	15.6	15.7	16.0	15.9
1200	15.9	15.9	16.2	16.0
600	16.3	16.2	16.7	16.6
300	16.7	16.6	17.1	17.0
150	17.1	17.2	17.6	17.4
75	17.6	17.6	18.0	17.8
37.5	18.1	18.1	18.5	18.4
18.75	18.6	18.6	19.1	18.7
10	19.0	19.1	19.4	19.3
5	19.6	19.5	19.9	19.8
2.5	20.1	20.0	20.4	20.1

*For ODR of 10Hz, two filter settings can be selected but with the same $ENOB_{RMS}$

*When ODR_P≤10Hz, the 50 or 60Hz notch filter will be activated. User can choose the proper notch filter for different applications. The error of the clock rate is designed to be less than 1% to minimize the effect to notch filter ability.

6.3. Analog Module 2: Temperature Measurement Channel

The temperature measurement channel is to measure the working temperature of the sensor for the temperature compensation of the sensed signal. This channel works independently of the primary channel. The NSC2860 supports both internal temperature sensor and external temperature sensor, selected by register bit 'EXT_TEMP' bit. The temperature sensor's output is digitized by a 24-bit ADC (TADC) and also digital filtered. The ODR setting of the temperature measurement channel is the same as the primary signal channel, set by 'ODR_T'. When the temperature difference between the sensor element and the NSC2860 chip is acceptable, internal temperature sensor can be used. Otherwise, a proper external temperature measurement scheme should be chosen, such as RTD. Through different 'RAW_T' setting, either the direct TADC data or the calibrated temperature data can be read from 'TDATA' registers.

6.3.1. Internal Temperature Sensor

The internal temperature sensor is factory calibrated, with its calibration coefficients stored at EEPROM registers (0xC1,0xC2,0xC3) When 'RAW_T' is set to 0 and 'GAIN_T' is set to 4X, the NSC2860 can provide a temperature reading in degree Celsius, in the following format:

$$T = TDATA/2\,\hat{}\,16 + 25℃$$

For example, 'TDATA=0x1FF24B' corresponding to 56.95°C. The relationship between the noise of the internal temperature sensor and 'ODR_T' setting is shown in Table 6.2.

Table 6.2 RMS Noise of Internal Temperature Sensor under different ODR_T

ODR (Hz)	2400	1200	600	300	150	75	37.5	18.75	10	5	2.5
RMS Noise in ℃	0.0079	0.0060	0.0045	0.0038	0.0032	0.0020	0.0015	0.0011	0.0008	0.0008	0.0007

6.3.2. External Temperature Sensor

When external temperature sensor mode is selected, the temperature sensing signal input from the TEMP pin is buffered for TADC conversion.

The reference voltage of the TADC is also VREF. The gain of the TADC can be 1X, 2X and 4X. The relationship between TDATARAW and the temperature input is

$$TDATA_{RAW} = VTEMP * GAIN\_T/VREF * 2^{23}$$

External temperature sensors can come in many forms, including the use of thermistors, thermal resistors (pt100, pt1000, etc.) and so on. Figure 6.4 shows an example of using a low-temperature bleach resistor Rt as an external temperature input.

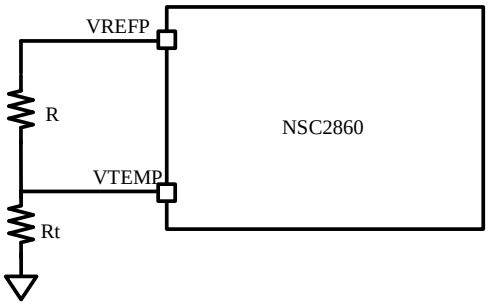


Figure 6.4 The use of external thermistors as external temperature sensors

When RAW_T = 0, the built-in MCU calibrated the offset, sensitivity and nonlinearity of the measured temperature signal. Please refer to calibration application note for the detailed description.

The output data rate of TADC can be set by 'ODR_T', similar as the primary signal channel. The relationship between ODR_T and the ENOB of TADC is shown in Table 6.3.

Table 6.3 ENOB of TADC under different ODR_T (External temperature sensor mode)

ODR_T (HZ)	*ENOB*		
	GAIN_T=1	*GAIN_T=2*	*GAIN_T=4*
2400	17.7	17.5	16.9
1200	18.1	17.9	17.2
600	18.5	18.1	17.2
300	18.8	18.3	17.4
150	19.1	18.5	17.6
75	19.5	18.9	18.0
37.5	19.4	18.6	17.6
18.75	19.9	18.7	18.1
10	20.2	19.4	18.5
5	20.2	19.6	18.5
2.5	20.9	19.9	18.8

6.4. Analog Output Stage

The analog output stage of the NSC2860 consists of a 16-bit DAC and an output buffer with feedback network. Through register configuration and external connection, the NSC2860 provides a lot of output modes such as absolute voltage output (0~5V, 0~3.3V, 0~1.2V), ratio-metric voltage output (0~AVDD), 0~10V voltage output, PDM output, PWM output, 4~20mA current loop. The output mode of analog output stage can be configured by 'OUT_MODE' registers, which is an independent configuration from analog front-end ADC.

6.4.1. 16-bit DAC

The voltage output of the DAC is expressed by the following equation.

$$VOUT = \frac{DAC\_DATA < 15:0 >}{2\ \hat{}\ 16} * VFSDAC$$

'DAC_DATA' stores the DAC input data in unsigned format. VFSDAC is DAC full scale range, which is configured by 'DAC_REF'. When 'RAW_P' = 0, the 'DAC_DATA' is updated by the internal MCU with the calibrated output data. The DAC full scale range is clamped by the clamping voltage configured by 'CLAMP_HIGH' and 'CLAMP_LOW'.

The low clamping voltage is defined by the following equation.

$$VOUT\_LOW = \frac{CLAMP\_LOW<7:0>}{2\ \hat{}\ 9} * VFSDAC$$

The high clamping voltage is defined by the following equation.

$$VOUT\_HIGH = \left(1 - \frac{CLAMP\_HIGH < 7:0 >}{2\ \hat{}\ 9}\right) * VFSDAC$$

When RAW_P =1, DAC_DATA registers are no longer automatically refreshed, but can be configured by external devices via serial communication interfaces. This mode can be used to calibrate zero and full-scale analog output modules, and can also support external MCU calibration modes. The DAC input itself has a latching function, and configuring DAC_DATA will not take effect immediately if the DAC_BLANK register is set to 1. When using an external MCU calibration mode, this position should be set to 1 before refreshing DAC_DATA each time, and then set DAC blank back to 0 after both bytes of DAC_DATA have been written, in this way glitch caused by two bytes asynchronistic DAC data can be avoided.

DAC output noise can be reduced by adding a low pass filter formed with a grounded capacitor on pin FILTER/HART and an internal 120 kohm resistor. For low frequency response requirements applications, a 47nF capacitor can be used to limit the signal bandwidth to about 30Hz. For high frequency response requirements applications, the signal bandwidth can be adjusted a bit by reducing filter capacitance appropriately.

6.4.2. Voltage Output

When OUT_MODE=000b, analog output stage is configured as voltage output mode. A class-AB output buffer is used to drive large load and the OUT pin and FBN pin should be shorted together as shown in Figure 6.5. The OUT pin and FBN pin can be also shorted internally as to reduce the chip pin count by setting OUT_MODE=001b. The gain of output buffer is configured by 'DAC_REF' to provide several types of full-scale output range, such as absolute output (0~5V, 0~3.3V, 0~1.2V) and ratio-metric output (0~AVDD), as listed in Table 6.4. The internal bandgap reference is used for absolute output.

Table 6.4 DAC_REF and output mode

DAC_REF<1:0>	*Output Mode*	*Output Voltage Range*
2'b00	Absolute	0~5V
2'b01	Absolute	0~3.3V
2'b10	Absolute	0~1.2V
2'b11	Ratio-metric	0~AVDD

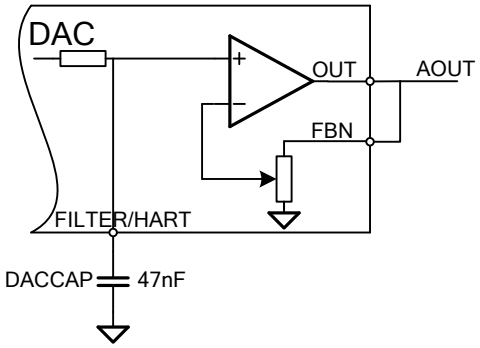


Figure 6.5 Configuration for voltage output mode(external feedback mode)

0~10V full scale output range is also available as shown in Figure 6.6 with a few external components, where DAC_REF<1:0>= 2'b00

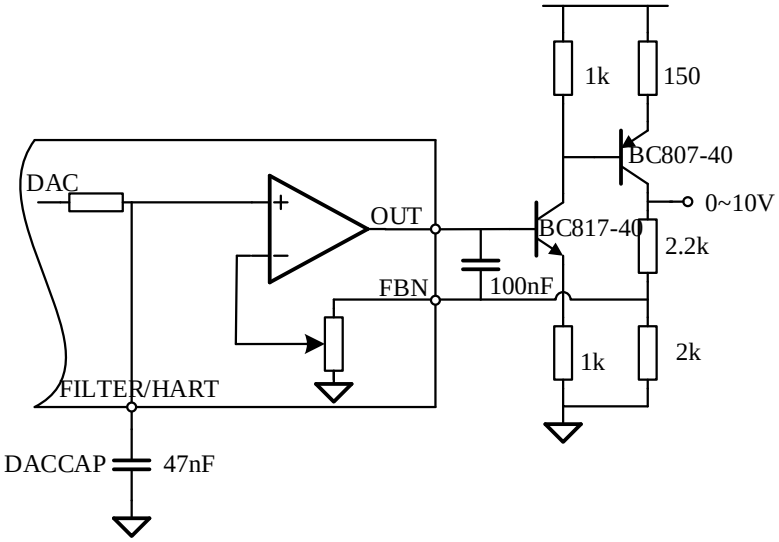


Figure 6.6 Configuration for 0~10V output mode

0~10V full scale output range is also available as shown in Figure 6.7 with a few external components, where DAC_REF<1:0>= 2'b00.

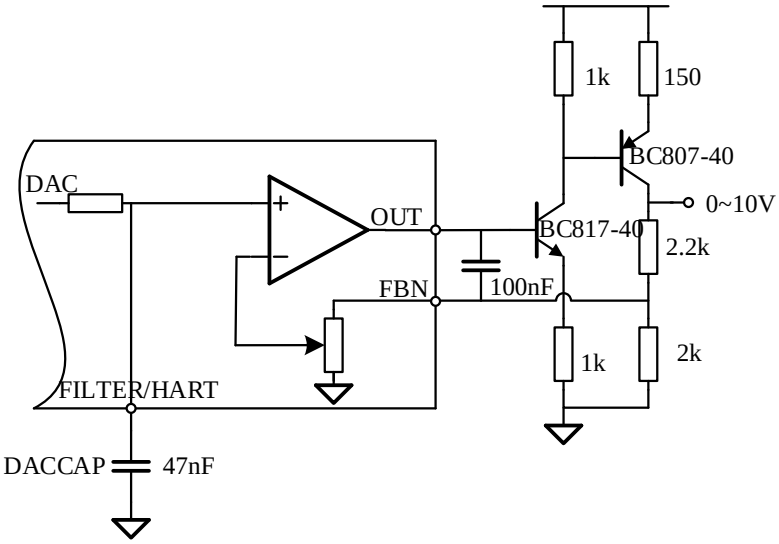


Figure 6.7 Configuration for 0~10V output mode

6.4.3. 4~20 mA Current Loop

When OUT_MODE=01xb and DAC_REF<1:0>=00b, analog output stage is configured as 4~20mA current loop mode. Internal bandgap reference with very low temperature drift is used for DAC reference. When using 50ohm external reference resistor, the loop current can be expressed as followed.

$$ILOOP = \frac{DAC\_DATA < 15:0 >}{2\text{^}16} * 24mA$$

The loop current transfer function is also shown in Figure 6.9. The minimum of ILOOP is about 1.5mA, which is determined by the self-operation current of the NSC2860. To not exceed 4mA lower limit for 4~20mA current loop, the total current consumed by the NSC2860 and sensor element should be less than 3.5mA.

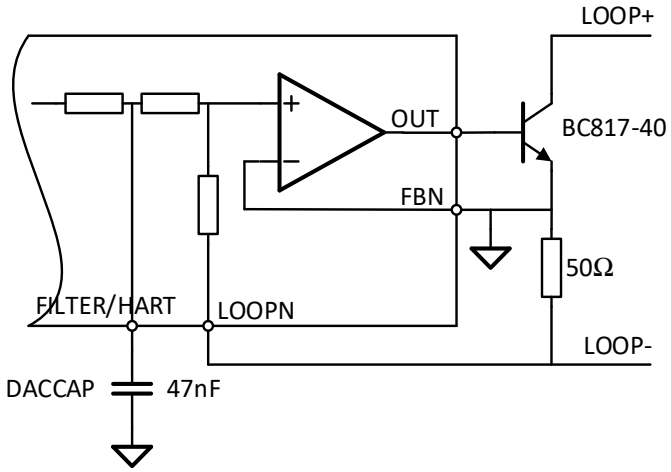


Figure 6.8 Configuration for 4~20mA current loop mode

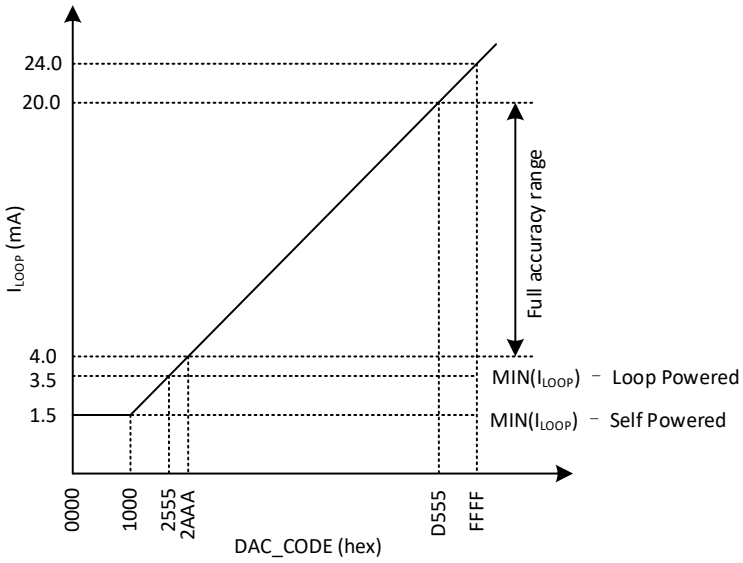


Figure 6.9 Loop current transfer function

The FILTER/HART pin can not only be used for noise filtering, but also for HART communication in current loop mode. As shown in Figure 6.10, the 500mVpp HART signal can be modulated into current loop as 1mApp current through a 470pF capacitor.

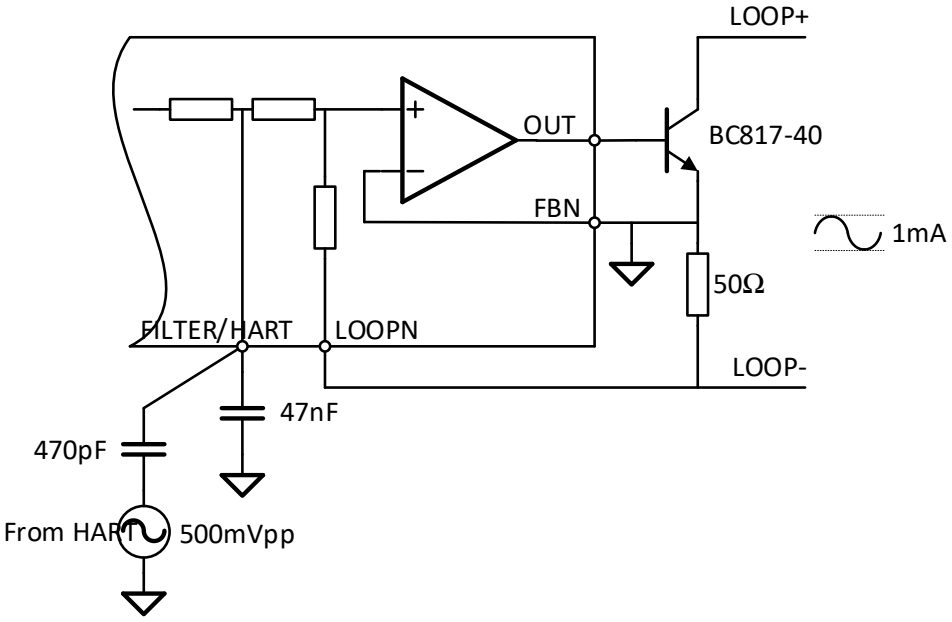


Figure 6.10 Configuration for HART communication

6.4.4. PDM

When 'OUT_MODE' = 100b, analog output stage is configured as PDM output mode, The 'DAC_DATA' is converted to 1 bit PDM single by a 1-order modulator internally and outputted through OUT pin. An external RC filter should be connected to OUT pin to filter the PDM signal to analog voltage. Digital isolation output can also be realized by external level shifter and isolation device. 'PDM_FREQ' is used to set the PDM output frequency. The equivalent output resistance at OUT pin is about 20ohm. As a result, when using external RC filter, the equivalent resistance load should be less than 20kohm as to make sure the output error is less than 1‰. Two-stage low pass RC filter in series is recommended as shown Figure 6.11. Some RC filter examples are provided in Table 6.5.

Table 6.5 RC filter examples for PDM output

R1 (kOhm)	*C1 (nF)*	*R2 (kOhm)*	*C2 (nF)*	*Ripple（mV/V）*	*0~90% Settling Time(us)*
100	22	100	22	0.12	14
100	100	0	0	2.5	24
100	220	0	0	1.2	50

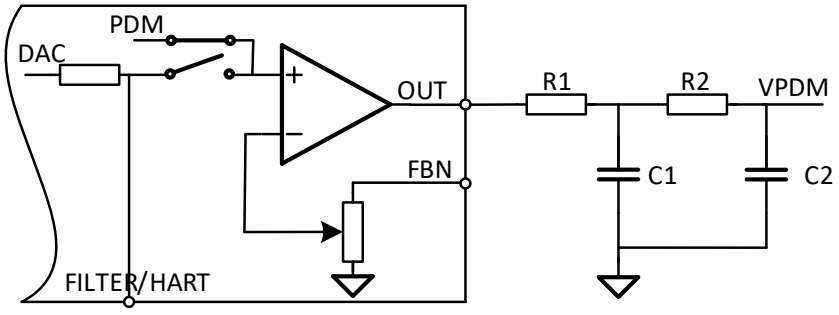


Figure 6.11 RC filter for PDM output

6.4.5. PWM

Both primary signal channel and temperature measurement channel support PWM output.

When 'OUT_MODE'=101b, primary channel output data will present on the OUT pin in the PWM format. The PWM carrier frequency is fixed at 300Hz, and the PWM output duty cycle is decided by DAC_DATA<15:4> with 12-bit resolution.

$$Duty\_Cycle = \frac{DAC\_DATA<15:4>}{4096}$$

When 'TOUT_EN'= 1 and the chip is not in OWI mode, the OWI pin is used as the output pin for Temperature Channel data in PWM format and the PWM output duty cycle is defined as follow:

$$Duty\_Cycle = \frac{TDATA<23:12>}{4096}$$

6.5. Power Management and Sensor Driver

The NSC2860 internally includes a precision bandgap reference with very low temperature drift, less than 0.1% during full temperature range (-40~85°C). This reference voltage is used in the constant voltage or current driving circuits for sensors, JFET regulator, clock generator and ADC/DAC etc.

6.5.1. JFET Regulator

By tuning the gate of external JFET (for example, BSS169) through VGATE pin, the JFET regulator integrated in the NSC2860 can convert the external high voltage supply to 5V (JFET_LVL=0) or 3.3V (JFET_LVL=1) and supply it to the VDDHV pin (Figure 6.12). The voltage of VSUP can be up to 36V. The user can also use an NPN triode (such as BCX5610) and a resistance of about 50 kohm instead of JFET to achieve this voltage regulator circuit, as shown in Figure 6.14, in the case of 5V output, the external supply voltage must be at least greater than 8V.

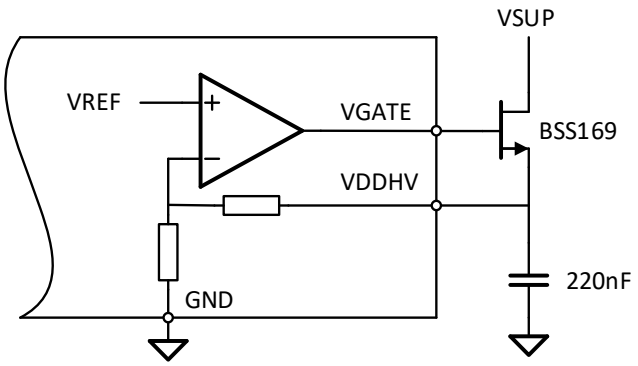


Figure 6.12 Regulation with external JFET

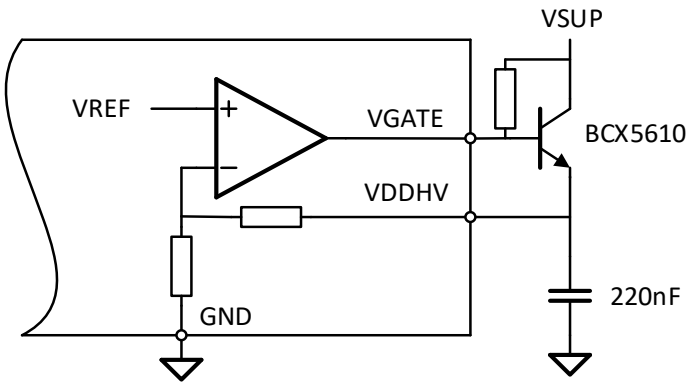


Figure 6.13 Regulation with external NPN Bipolar

6.5.2. Internal LDO

A 1.8V LDO is integrated in the NSC2860 to provide power supply for the internal digital circuits. A 100nF decoupling capacitor should be connected at DVDD pin externally.

6.5.3. Power on Reset

A POR block is integrated in the NSC2860 for power on reset and EEPROM loading. When AVDD<2.5V, the chip is in reset state. After AVDD > 2.5V, the POR output is released and EEPROM is loaded afterwards. The POR circuits have 100mV hysteresis, that is, the chip won't go into the reset state again until the AVDD is dropped as low as 2.4V.

6.6. Built-in MCU Core and Control Logics

6.6.1. Function Mode

The NSC2860 has five different working modes: single mode, continuous mode, command mode and programming mode. User can choose alternate mode by writing different values in COMMAND register CMD<7:0>.

6.6.1.1. Single Mode (CMD<7:0> = 0x01/0x02)

Writing 0x01 or 0x02 to register CMD<7:0> will make the NSC2860 enter single mode from command mode. In this mode, the chip will enter command mode after data conversion being completed once. CMD<7:0> will return to 0x00 simultaneously. The conversion time of single mode depends on ODR_P and ODR_T settings.

6.6.1.2. Continuous Mode (CMD<7:0> = 0x03)

Writing 0x03 to CMD<7:0> will make NSC2860 enter continuous mode. In this mode, the primary signal ADC channel and temperature ADC channel will refresh the PDATA and TDATA registers at a stated ODR continuously. Writing 0x00 to CMD<7:0> can make NSC2860 exit continuous mode.

If RAW_P or RAW_T is set to 1, the ADC conversion results will be put into the 'PDATA' or 'TDATA' directly. Otherwise, the embedded MCU will use the latest temperature data to calibrate primary ADC channel output data every time its measurement completed. .

When the register bit 'INT_EN' = 1, the SDO_DRDYB pin is used to indicate that a new data is ready for reading via the serial interface with an active low voltage level, and this pin will come back to high level after the data reading or about 100μs before next new data's coming.

Even without the SDO_DRDYB pin, the shadow registers inside the NSC2860 can also guarantee a non-glitch reading by keeping the 'PDATA' and 'TDATA' registers stable during once serial interface reading. Note that, the multiple bytes of one measured data should be read out together in once multi-byte serial interface reading command.

6.6.1.3. Command Mode (CMD<7:0> = 0x00)

In this mode, access to all configuration registers is allowable and the chip keeps in a relative low power state.

6.6.1.4. Programming Mode (CMD<7:0> = 0x33)

Only in this mode, EEPROM can be programmed. Please refer to chapter 5.5 for detailed information about EEPROM operation.

6.6.2. EEPROM

64 bytes EEPROM is contained in the NSC2860 to store the chip configurations and sensor calibration coefficients.

6.6.2.1. Loading

The contents of the EEPROM will be loaded into the EEPROM registers automatically after power up or soft reset with the CRC checking. If the calculated CRC result does not match with what stored in the EEPROM, the 'CRC_ERROR' bit will be set. Another status register bit 'LOADING_END' will be set after the loading completes.

6.6.2.2. Programming

Writing EEPROM registers will not program the EEPROM directly. The contents of the EEPROM registers will be programmed into the EEPROM by following sequence:

1. Set the register byte 'COMMAND' (Reg0x30) with 0x33, to enter EEPROM programming mode.
2. Writing the register byte 'EE_PROG' (Reg0x6A) with 0x1E or 0x9E, to start EEROM programming.

When 0x1E is used, the built-in MCU will first compare the register contents with the EEPROM contents, and only erase and program the bytes with the difference. If 0x9E is used, all EEPROM contents will be erased and then programmed. The programming time is different in these two modes. It is recommended to use 0x7E for programming.

During EEPROM programming, a new CRC check code will be generated according to the contents of the EEPROM registers and will be programmed to the EEPROM simultaneously. The content of the 'EE_PROG' register will automatically come back to 0x00 to indicate the programming is done. A re-powering up or soft reset is needed to reload the EEPROM contents back to the EEPROM registers to check the programmed value.

6.6.2.3.Lock and Unlock

The EEPROM inside the NSC2860 can be locked by setting the 'EEPROM_LOCK' bit then programming it into the EEPROM. After locked, the EEPROM cannot be programmed again, and only a special EVA-kits provided by NOVOSENSE can unlock it.

6.6.3. Built-in MCU Core

The NSC2860 is integrated with a built-in MCU core, which performs the signal processing, sensor calibration, EEPROM loading and programming etc. The MCU's program code is pre-stored in the internal ROM, which cannot be modified by customers. Please contact NOVOSENSE if a customized MCU program code is needed.

6.6.4. Calibration

The calibration flow inside the NSC2860 is divided into two steps. The first is the ADC calibration, which can erase the offset and sensitivity error induced by the ADC. The other is sensor calibration, which can compensate the sensor with offset, sensitivity, up to the 2nd order offset temperature drift, up to the 2nd order sensitivity temperature drift, up to the 3rd order non-linearity. Please refer to application note details.

7. Serial Interface

Three different serial interfaces (OWI, SPI and I²C) are supported in the NSC2860 to configure registers, program EEPROM and read measured data. When register bit 'OWI_WINDOW' = 0, the time between 10ms and 80ms after powering up is defined as the OWI entering window. If a specific 24 bits OWI entering pattern is detected via OWI pin in this window, the chip enters OWI communication mode, otherwise enters I²C or SPI communication mode. Then, CSB pin is used to further select between I²C and SPI methods: high voltage level or floating indicates the I²C method, low voltage level indicates the SPI method. When 'OWI_WINDOW' = 1, the OWI window's length becomes infinite.

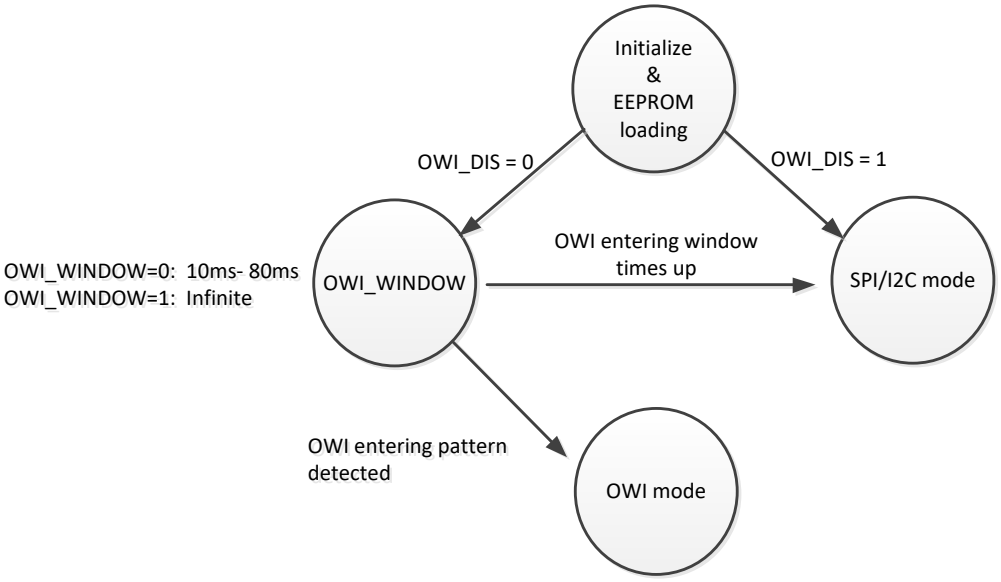


Figure 7.1 Definition of serial communication mode

7.1. OWI Protocol

The NOVOSENSE self-owned One Wire Interface (OWI) protocol integrated in the NSC2860 can support serial communication under all 0~5V, 0~10V and 4~20mA output modes with no extra communication wires added. This protocol identifies the data bit transferred by the duty cycle of one rising-to-rising period. Duty cycle more than 5/8 means a logical 1, and less than 3/8 means a logical 0.

7.1.1.Timing Spec

Table 7.1 OWI Timing Spec

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
t_{period}	OWI bit period		20		4000	μs
t_{pulse_0}	Duty cycle for 0		1/8	1/4	3/8	t_{period}
t_{pulse_1}	Duty cycle for 1		5/8	3/4	7/8	t_{period}
t_{start}	Start low pulse time		20		4000	μs
t_{stop}	Stop condition time		2			t_{period}

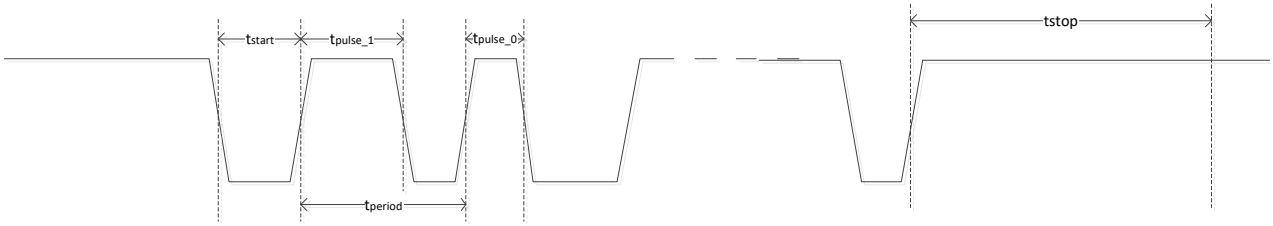


Figure 7.2 OWI Timing

7.1.2.Enter OWI Mode

If 'OWI_WINDOW' = 0, the time between 10ms and 80ms after powering up is OWI entering window. If a special 24 bits OWI entering pattern (0xB5A6C0, as shown below) is detected via OWI pin in this window, the chip enters OWI communication mode. Under this setting, the OUT pin is disabled during the OWI window and OWI mode; the OWI pin and the OUT pin can be shorted together to support 3-wire sensor products.

If 'OWI_WINDOW' = 1, the OWI window's length becomes infinite, the OUT pin is activated during OWI window and OWI mode, and the OWI pin and OUT pin cannot be shorted together.

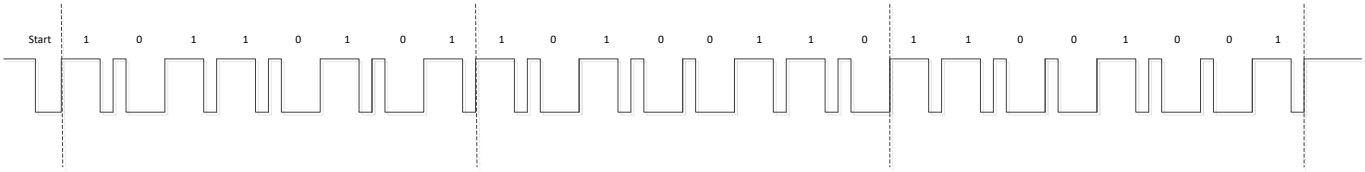


Figure 7.3 OWI Entering Pattern

In OWI communication, the bit period is determined by the period of the last bit of OWI entering pattern, and cannot be changed during the entire communication, so the bit period during OWI communication should keep the same as the OWI entering pattern.

7.1.3.OWI Protocol

The OWI protocol used is defined as follows:

a) Idle State

During inactivity of the bus, OWI line is pulled-up to high voltage level.

b) Start Condition

When OWI line is in idle state, a low pulse (return to high) with a pulse width between20μs to 4ms indicates a start condition. Every command has to be initiated by a start condition sent by the master. The master can only generate the start condition when the OWI line is in idle state.

c) Stop Condition

After the write or read operation ends, the bus comes back to the idle state automatically. During any time of a transmission, the bus can be set back to the idle state by forcing the OWI line to reach a constant high or low voltage level for at least two times of the bit period (t_{period})

d) Addressing

After the start condition, the master sends the addressing information, consisting of an 8-bit register address (MSB first), 2-bit byte number and a read/write bit (0–write, 1–read). The register address indicates which register you will write into or read from; the byte number indicates how many bytes will write/read continuously: 00: 1 byte, 01: 2 bytes, 10: 3 bytes, 11: 4 bytes; the read/write-bit indicates it a read operation (0) or write operation (1).

e) Write Operation

During transmission from master to slave (WRITE), the read/write bit is followed by 1/2/3/4 bytes (according to the byte NO. bits) transmitted data (MSB first), and the addressed register and follows will be refreshed to the written data after a stop condition.

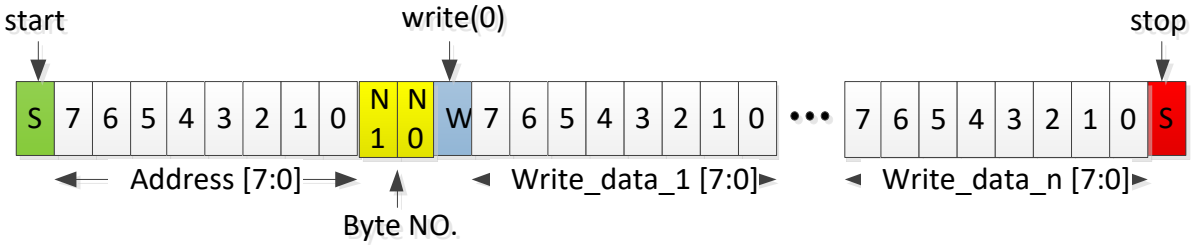


Figure 7.4 OWI Write Operation

f) Read Operation

During transmission from slave to master (READ), the master should set its OWI port as input after the read/write bit is sent, then the slave begins to transmit 1/2/3/4 bytes (according to the byte NO. bits) data (MSB first), which is the content in the addressed register and CRC data. Each data byte includes 8 bits of data and 2 bits of parity check code C1 and C0,

C1 = Read_data [7] ^ Read_data [5] ^ Read_data [3] ^ Read_data [1];

C0 = Read_data [6] ^ Read_data [4] ^ Read_data [2] ^ Read_data [0].

The master can check the transmission with the parity check code. After all data bytes transmitted, the slave goes back to idle state automatically.

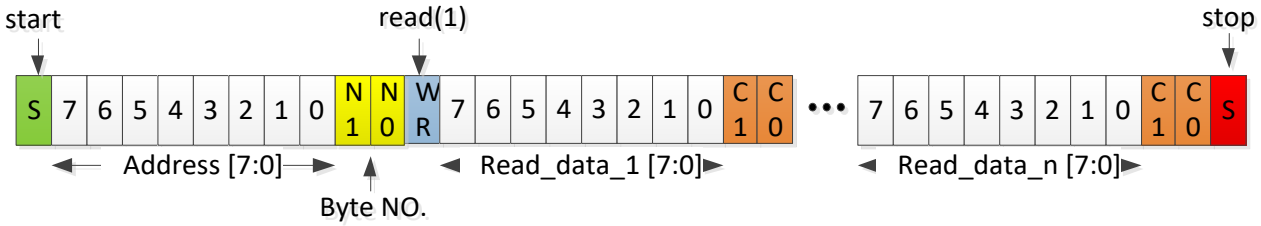


Figure 7.5 OWI Read Operation

7.1.4.Pins and Configurations

There are two pins (OWI and OUT) and two register bits (OWI_AC_EN and OWI_WINDOW) related to the OWI communication. Different applications can be supported via different configurations. Please refer to Table 7.2 for details.

OWI_AC_EN:

0, single-port communication method with the OWI pin used for both input and output port, which is typically used in 0~5V analog-output products;

1, dual-port communication method with the OWI pin as the slave input port and the OUT pin as the slave output port, which is typically used in the 0~10V and 4~20mA products.

OWI_WINDOW:

0, OWI mode should be entered between a 10ms and 80ms window after powering up;

1, the window is infinite and the OWI mode can be entered any time after powering up.

Table 7.2 Pin configurations for OWI communications

OWI_AC_EN	OWI_Window	Windows	Input Port	Output Port	Output Mode	OUT Pin State Mode	Shorten OUT and OWI	Typical Applications
0	0	10ms-80ms	OWI	OWI	OD	Hz	Supported	3-wire modules with 0~5V output (short OUT and OWI pins), external pull-up resistor is needed.
0	1	Infinite	OWI	OWI	OD	Signal Output	Not Supported	Cases that signal out and OWI communication are used simultaneously, external pull-up resistor is needed.
1	0	10ms-80ms	OWI	OUT	Push-Pull	OWI output	Supported	3-wire modules with 0~10V output, 2-wire modules with 4~20mA output. 0~5V output modules with big load capacitor.
1	1	Infinite	OWI	OUT	Push-Pull	OWI output	Supported	Isolated Transmitter using OWI/OUT pins for isolated communication.

7.1.5.Dual-Port OWI Communication (OWI_AC_EN = 1)

The special dual-port OWI communication is supported by the NSA2860 for applications in 4~20mA and 0~10V output products with no extra communication wires added. The protocol is shown in Figure 7.6, with the OWI pin as the slave input port, and the OUT pin as the slave output port.

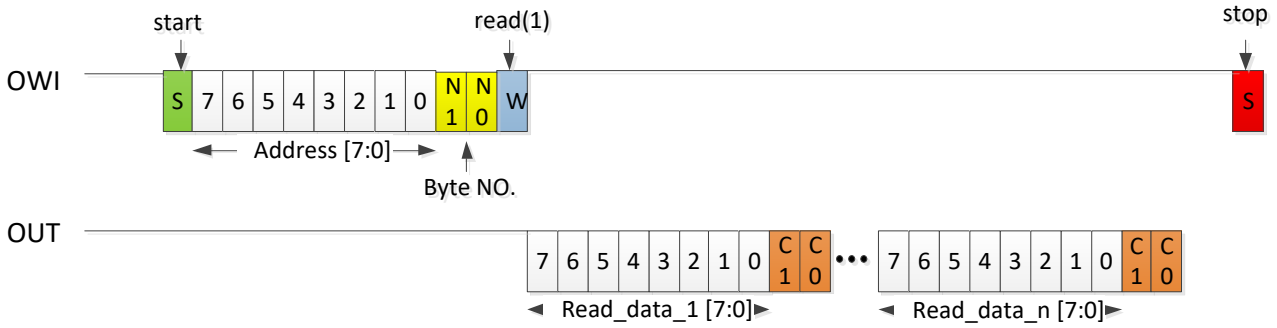


Figure 7.6 Dual Ports OWI Communication

As shown in Figure 7.7, in 4~20mA output applications, data transmission from the master to the chip is implemented by adding a square-waved signal on the power supply wire and AC coupling it onto the OWI pin with an external capacitor. The chip to master transmission data is modulated to the loop current (1: 10mA, 0: 4mA) and can be read out by the master through a comparator circuit. Limited by the response time of the current loop, the bit period of this OWI communication method should be no less than 100μs. The advantage of this kind of communication method is that the LOOP+/LOOP- wires are multiplexed for communications and no extra communication wires are needed. Similarly, in the 0~10V output applications, data transmission from the master to chip is also implemented by signal coupling from the power supply to the OWI pin, and data from chip to the master is put on the OUT pin. Also, only three wires (VDD, GND, OUT) are needed for a 0~10V product with no extra communication wires.

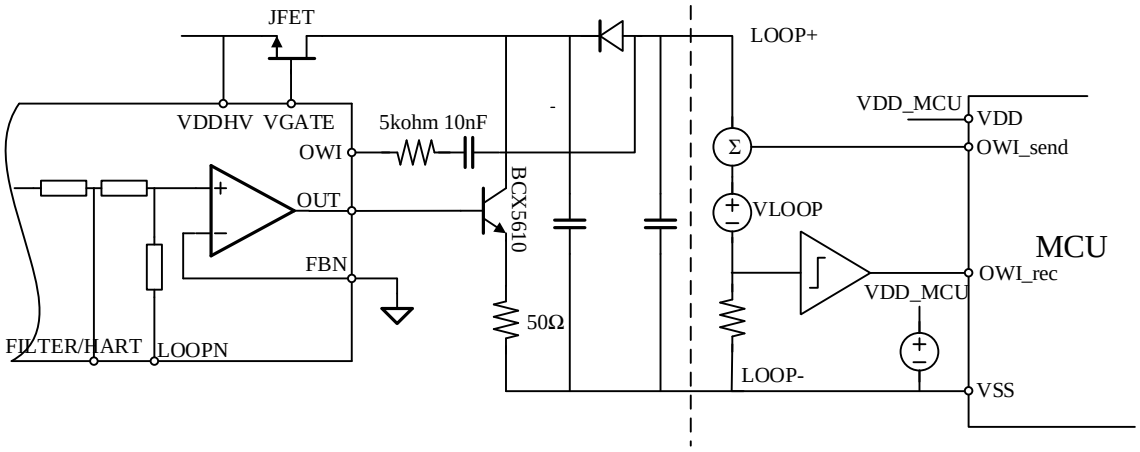


Figure 7.7 Typical circuit for the dual ports OWI communication in the 4~20mA applications

7.1.6.Quit OWI Communication

Writing Reg0x61 with 0x5d during OWI mode can temporarily or permanently quit the OWI communication for output voltage or current measuring. The register byte 'OWI_QUIT_CNT' is used to set the quit time with the LSB = 50ms (0x00 means permanently quit), and the chip will be back into OWI mode again after the quit time's up.

7.2. SPI Interface

7.2.1.Interface Specification

Table 7.3 SPI interface specifications

Symbol	*Parameter*	*Condition*	*Min*	*Max*	*Unit*
f_{sclk}	Clock frequency	Max load on SDIO or SDO = 25pF		10	MHz
t_{sclk_l}	SLCK low pulse		20		ns
t_{sclk_h}	SLCK high pulse		20		ns
T_{sdi_setup}	SDI setup time		20		ns
T_{sdi_hold}	SDI hold time		20		ns
T_{sdo_od}	SDO/SDI output delay	Load = 25pF		30	ns
		Load = 250pF		40	ns
T_{csb_setup}	CSB setup time		20		ns
T_{csb_hold}	CSB hold time		40		ns

The figure below shows the definition of the SPI timing given in Table 7.3.

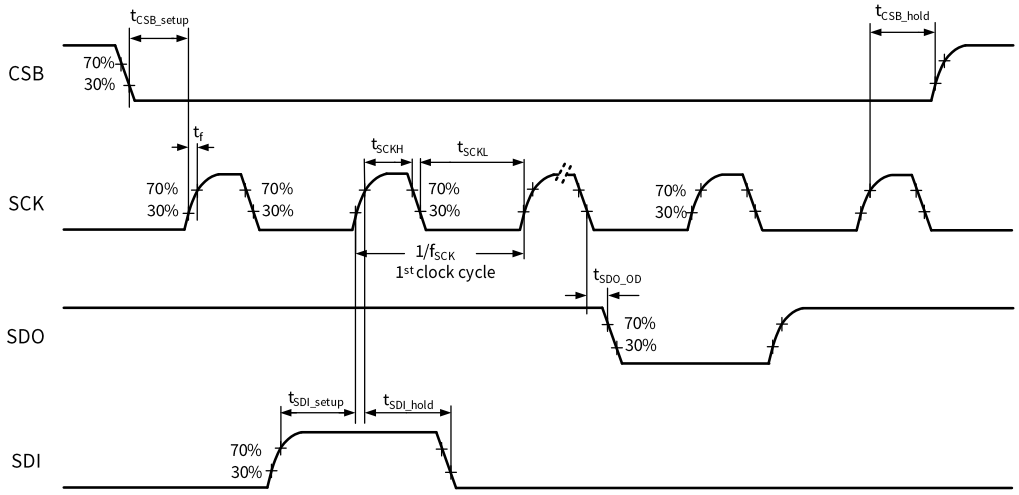


Figure 7.8 SPI Timing diagram

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of framing. Once the beginning of the frame has been determined, timing is straightforward. The first phase of the transfer is the instruction phase, which consists of 16 bits followed by data that can be of variable lengths in multiples of 8 bits. If the device is configured with CSB tied low, framing begins with the first rising edge of SCLK.

The instruction phase is the first 16 bits transmitted. As shown in Figure 7.9, the instruction phase is divided into a number of bit fields.

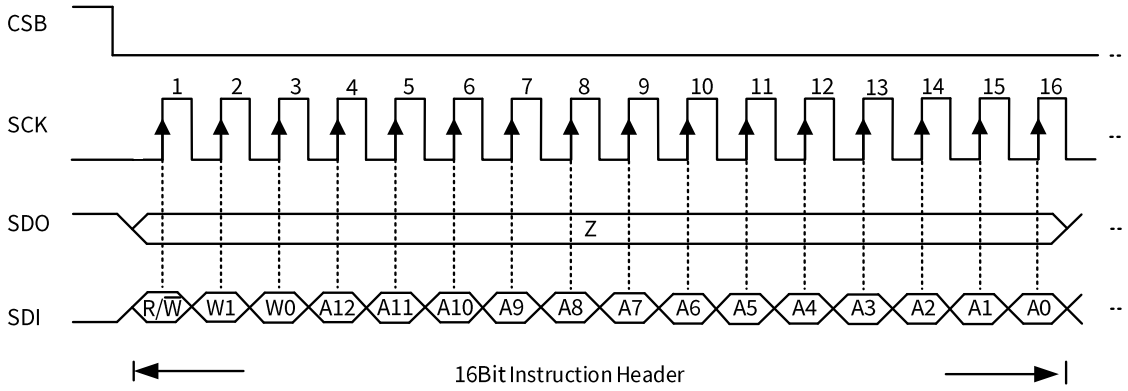


Figure 7.9 Instruction Phase Bit Field

The first bit in the stream is the read/write indicator bit (R/W). When this bit is high, a read operation is being requested; otherwise a write operation is requested.

W1 and W0 represent the number of data bytes to transfer for either read or write (Table 7.4). If the number of bytes to transfer is three or less (00, 01, or 10), CSB can stall high on byte boundaries. Stalling on a non-byte boundary terminates the communications cycle. If these bits are 11, data can be transferred until CSB transitions to high. CSB is not allowed to stall during the streaming process.

The remaining 13 bits represent the starting address of the data sent. If more than one word is being sent, sequential addressing is used, starting with the one specified, and it either increments (LSB first) or decrements (MSB first) based on the mode setting.

Table 7.4 W1 and W0 settings

W1:W0	*Action*	*CSB Stalling*
00	1 byte of data can be transferred.	Optional
01	2 bytes of data can be transferred.	Optional
10	3 bytes of data can be transferred.	Optional

11	4 or more bytes of data can be transferred. CSB must be held low for the entire sequence; otherwise, the cycle is terminated.	No

Data follows the instruction phase. The amount of data sent is determined by the word length (Bit W0 and Bit W1). There can be one or more bytes of data. All data is composed of 8-bit words.

Data can be sent in either MSB-first mode or LSB-first mode (by setting 'LSB_first' bit). On power up, MSB-first mode is the default. This can be changed by programming the configuration register. In MSB-first mode, the serial exchange starts with the highest-order bit and ends with the LSB. In LSB-first mode, the order is reversed (Figure 7.10).

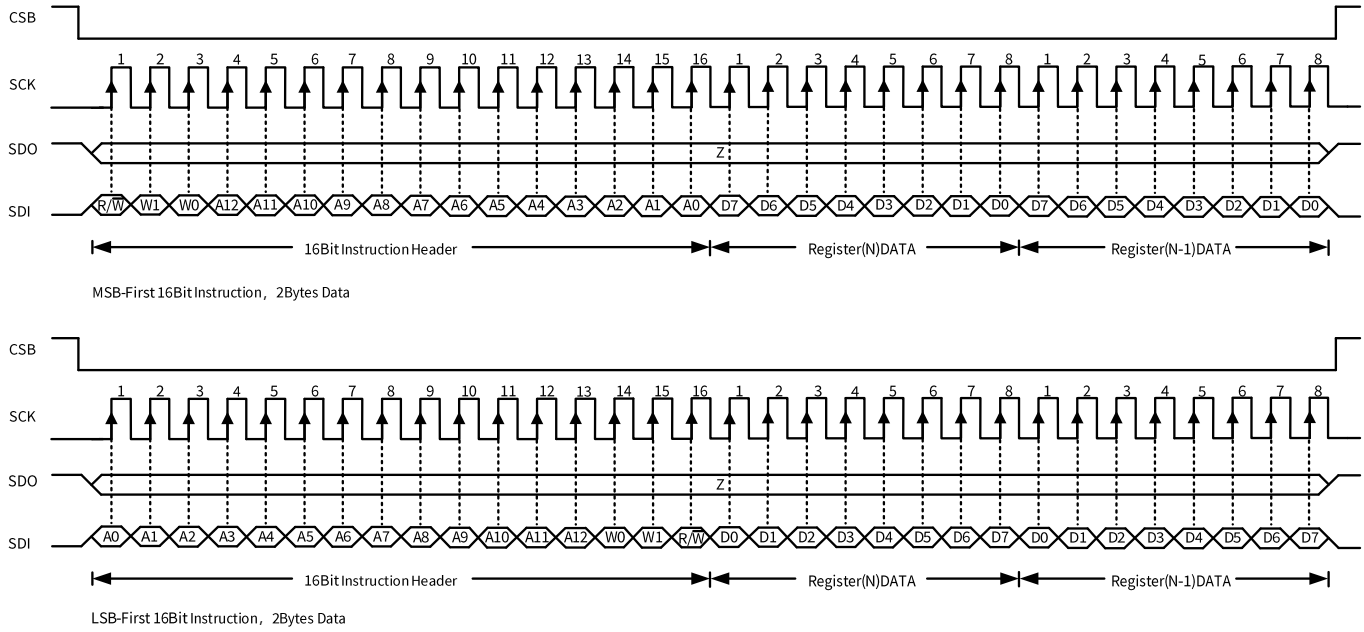


Figure 7.10 MSB First and LSB First Instruction and Data Phases

Register bit 'SDO_active' is responsible for activating SDO on devices. If this bit is cleared, then SDO is inactive and read data is routed to the SDIO pin. If this bit is set, read data is placed on the SDO pin. The default for this bit is low, making SDO inactive.

7.3. I²C Interface

I²C bus uses SCL and SDA as signal lines. Both lines are connected to VDDIO externally via pull-up resistors so that they are pulled high when the bus is free. The I²C device address of NSC2860 is shown below. The LSB bit of the 7-bit device address is configured via SDO/ADDR pin.

Table 7.5 I²C Address.

A7	*A6*	*A5*	*A4*	*A3*	*A2*	*A1*	*W/R*
1	1	0	1	1	0	1	0/1

Table 7.6 Electrical specification of the I²C interface pins

Symbol	*Parameter*	*Condition*	*Min*	*Max*	*Unit*
f_{scl}	Clock frequency			400	kHz
t_{LOW}	SCL low pulse		1.3		μs
t_{HIGH}	SCL high pulse		0.6		μs
t_{SUDAT}	SDA setup time		0.1		μs

t_{HDDAT}	SDA hold time		0.0		μs
t_{SUSTA}	Setup Time for a repeated start condition		0.6		μs
t_{HDSTA}	Hold time for a start condition		0.6		μs
t_{SUSTO}	Setup Time for a stop condition		0.6		μs
t_{BUF}	Time before a new transmission can start		1.3		μs

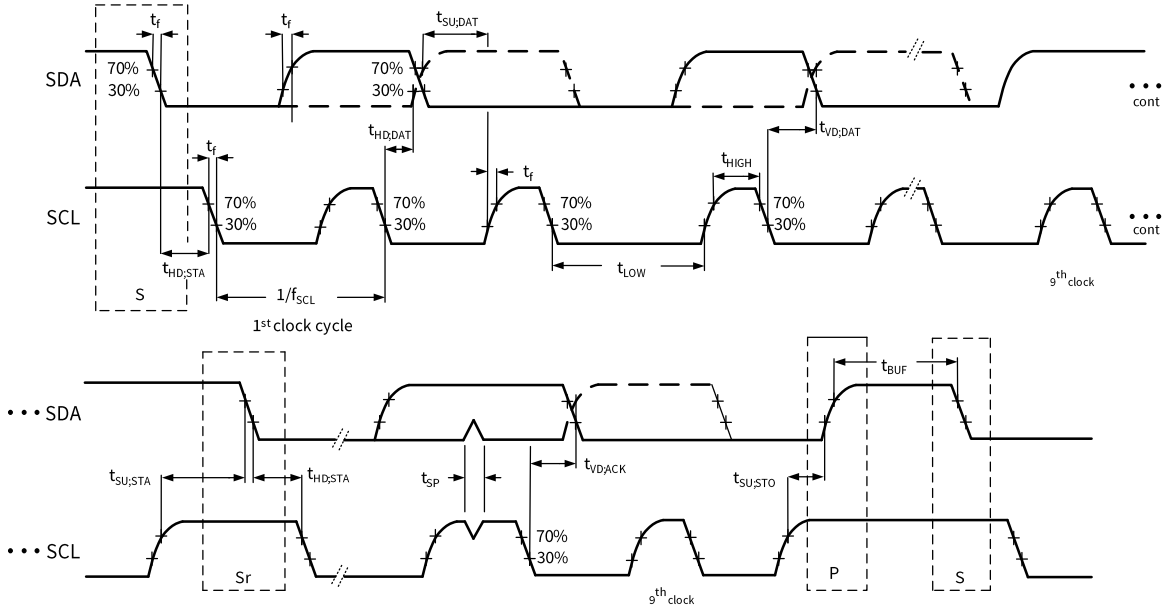


Figure 7.11 I²C Timing Diagram

The I²C interface protocol has special bus signal conditions. Start (S), stop (P) and binary data conditions are shown below. At start condition, SCL is high and SDA has a falling edge. Then the slave address is sent. After the 7 address bits, the direction control bit R/W selects the read or write operation. When a slave device recognizes that it is being addressed, it should acknowledge by pulling SDA low in the ninth SCL (ACK) cycle.

At stop condition, SCL is also high, but SDA has a rising edge. Data must be held stable at SDA when SCL is high. Data can change values at SDA only when SCL is low.

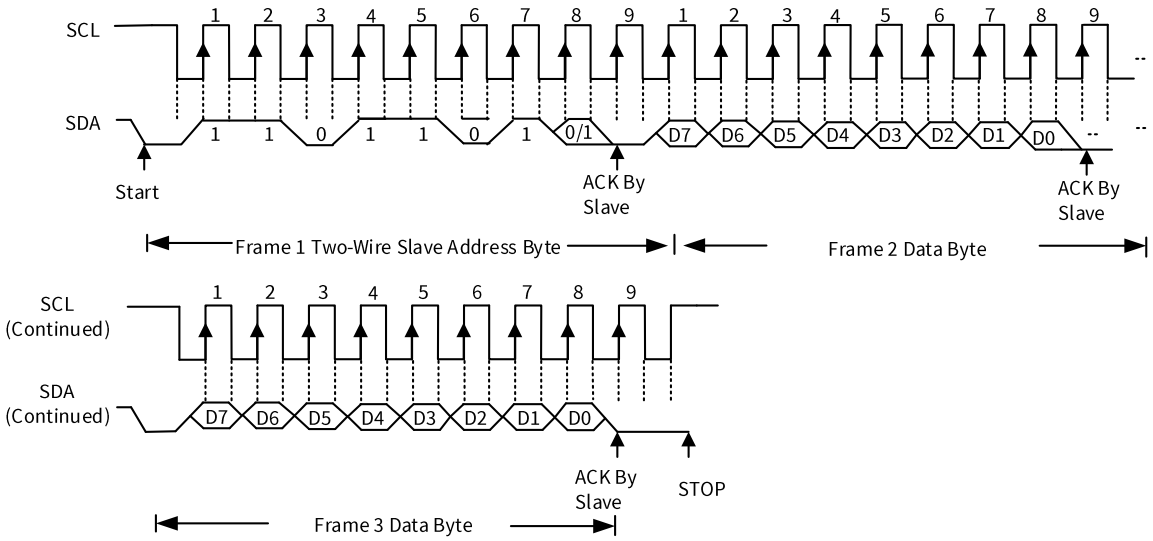


Figure 7.12 I²C Protocol

NSC2860 can support single-byte read/write and multi-byte read/write operations. The transfer format is shown in Figure 7.13 and Figure 7.14.

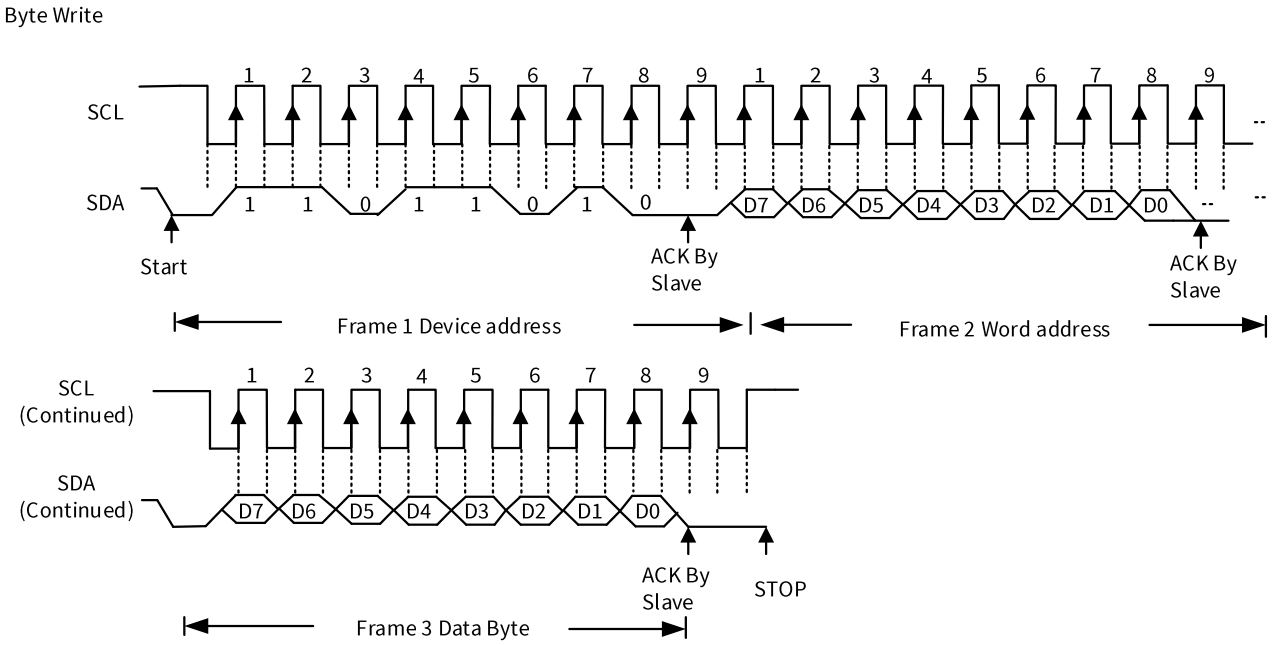


Figure 7.13 I²C Write Byte

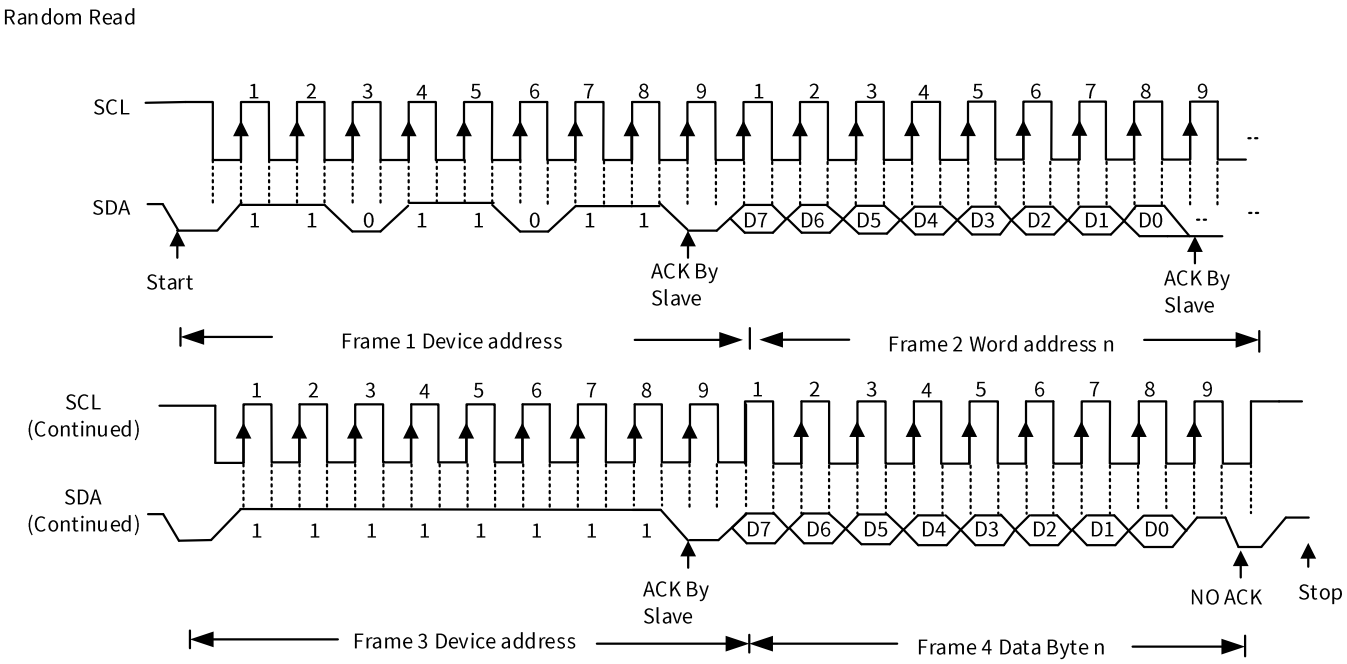


Figure 7.14 I²C Read Byte

8. Application Note

8.1. Application Case 1:4 ~20mA Drive Mode Capacitive Pressure Transmitter

The external JFET is used to generate AVDD, the sensor is powered by a constant current source, the internal temperature sensor is selected, and the drive mode capacitance detection mode is used. R5 is a 50ohm precision resistor for current converter feedback. Using the two-pin OWI communication mode, there is no need to add additional external leads.

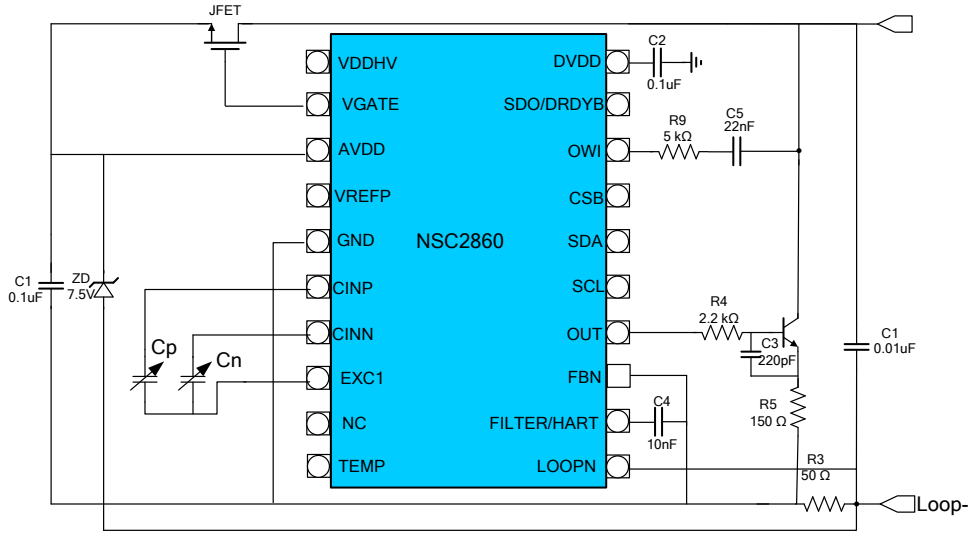


Figure8.1 4~20mA output pressure transmitter (JFET, drive mode)

8.2. Application Case 2:4 ~20 mA Ground Mode Capacitive Pressure Transmitter 2

Compared with Case 1, the NPN triode plus a 50kΩ resistor is used instead of JFET, the capacitance detection is in ground mode, and the capacitor upper plate lead can use EXC to shield the interference of external stray parasitic capacitors.

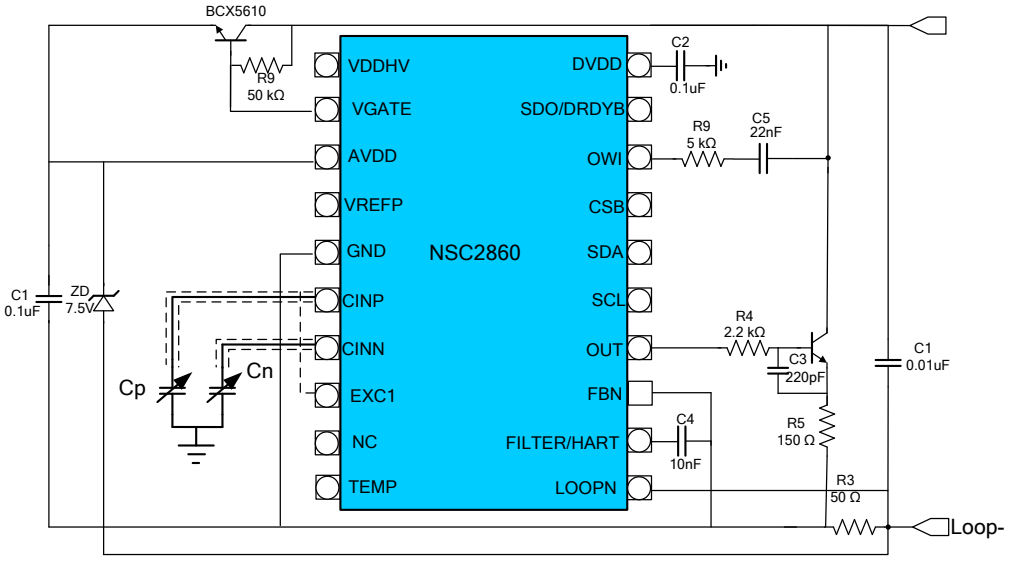
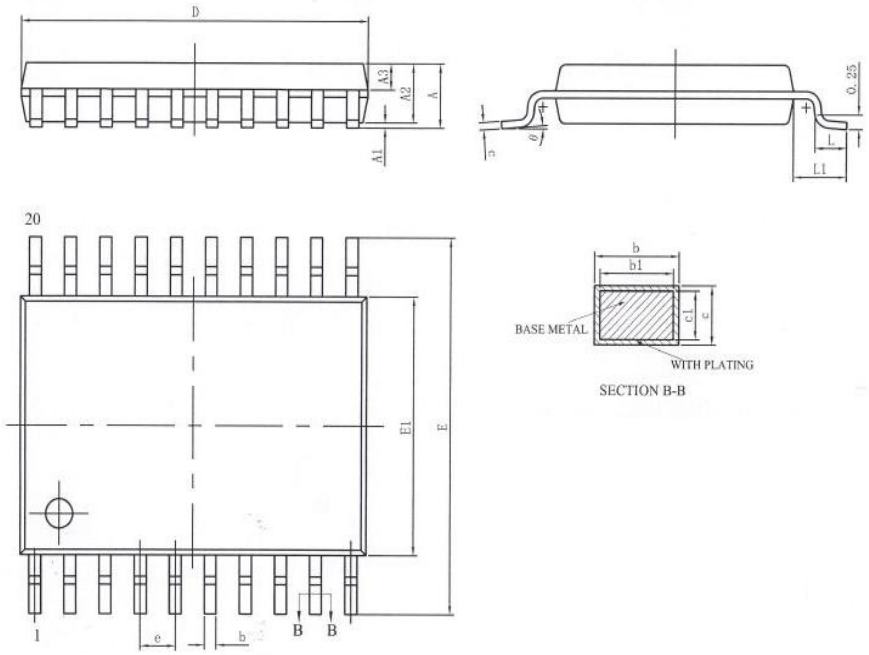


Figure8.2 4~20mA output pressure transmitter (Biploar, ground mode)

9. Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.29
b1	0.19	0.22	0.25
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°

Figure 9.1 TSSOP20 Package

10. Tape/Reel Information

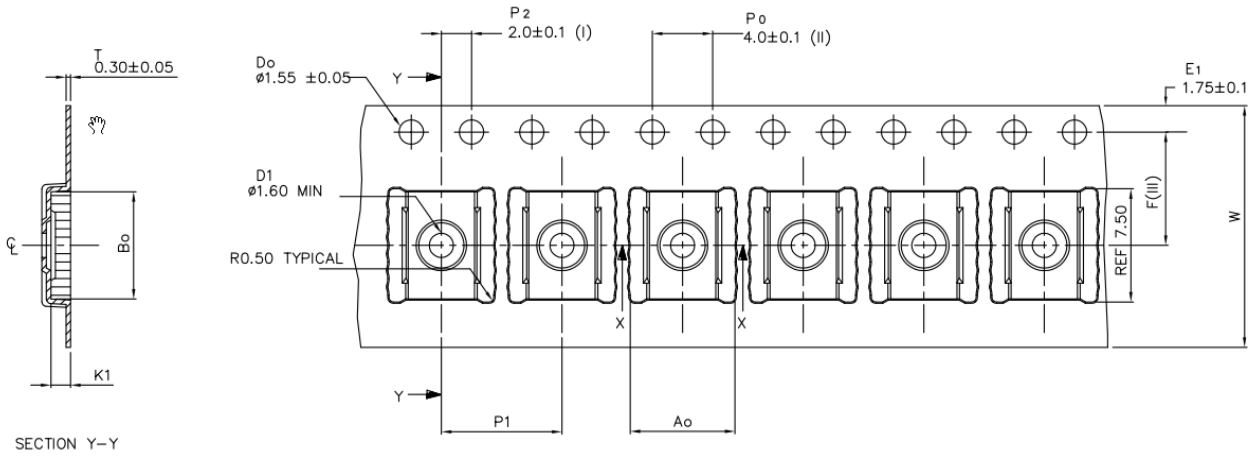
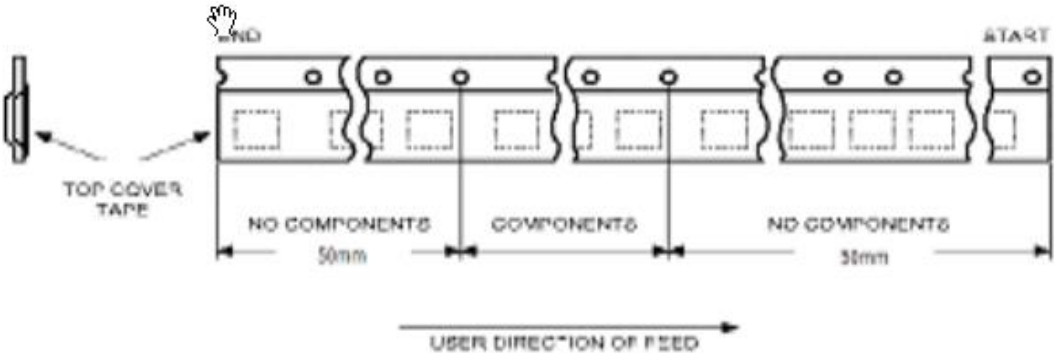


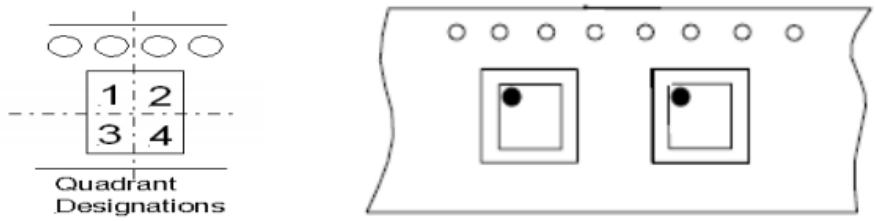
Figure10.1 TSSOP20 tape braid diagram

Part No.	*Package type*	*A0 (mm)*	*B0 (mm)*	*K0 (mm)*	*K1 (mm)*	*F (mm)*	*P1 (mm)*	*W (mm)*
NSC2860_TSSOP	TSSOP20	6.95±0.1	7.1±0.1	1.6±0.1	1.3±0.1	7.5±0.1	8.0±0.1	16.0±0.3

At the beginning and end of each braid, a blank braid is needed. The front and rear space is 50cm. See the following figure for specific style specifications:



The Pin 1 direction is in Quadrant 1, as shown below:



11. Ordering Information

Part Number	*Temperature*	*MSL*	*Package Type*	*SPQ*
NSC2860_TSSOP	-40℃ to 125℃	1	TSSOP20	2500

12. Revision History

Revision	Description	Date
1.0	Initial Version.	2023.9.11

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