NOVOSENSE

NLA9502

3V LVDS Quad CMOS Differential Line Receiver

Datasheet (EN) 1.0

Product Overview

The NLA9502 is a quad-channel, CMOS low voltage differential signaling (LVDS) line receiver offering data rates of over 400 Mbps (200 MHz) and ultralow power consumption.

The NLA9502 can accept low voltage (350 mV typical) differential input signals and translate them to a single-ended 3 V COMS logic level.

The NLA9502 offers active high and active low enable/disable inputs (EN and EN*) that control all four receivers. The EN and EN* are OR-ed together. When all receivers are disabled, the outputs show high impedance state, while the supply current is also significantly reduced. Each receiver support TRI-STATE function.

The NLA9502 provides three fail-safe functions, including floating, shorted, or terminated (100 Ω) receiver inputs. The NLA9502 is paired with differential line driver for high-speed point-to-point interface application.

Key Features

- >400 Mbps (200 MHz) switching rate
- 100 ps differential pulse skew (typical)
- 100 ps differential channel-to-channel skew (typical)
- 3.3 ns propagation delay (maximum)
- 3.3 V ± 0.3 V power supply
- Power down high impedance on LVDS inputs
- Low power design (40 mW at 3.3 V quiescent typical)
- Interoperable with existing 5 V LVDS drivers
- Accepts small swing (350 mV typical) differential input signal levels
- Supports open, short, and terminated input fail-safe
- Compatible with TIA/EIA-644 LVDS standard
- Industrial temperature operating range (–40 °C to 85 °C)
- ESD protection exceeds 6000 V HBM per JESD22-A114 and 2000 V CDM perJESD22-C101
- Latch-up performance exceeds 100 mA per JESD 78
- RoHS-compliant packages: TSSOP16

Applications

- Point-to-point data transmission
- Building and factory automation
- Multidrop buses
- Clock distribution networks

Device Information

Part Number	Package	Body Size
NLA9502-DTSPR	TSSOP16	5.00 mm × 4.40 mm

Function Block Diagram

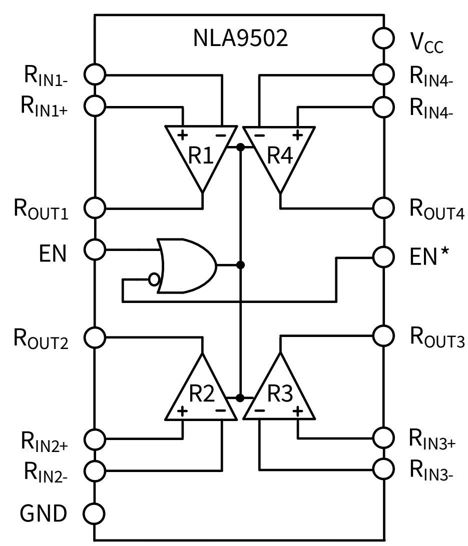

Figure 1 NLA9502 Block Diagram

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1. Pin Configuration and Functions

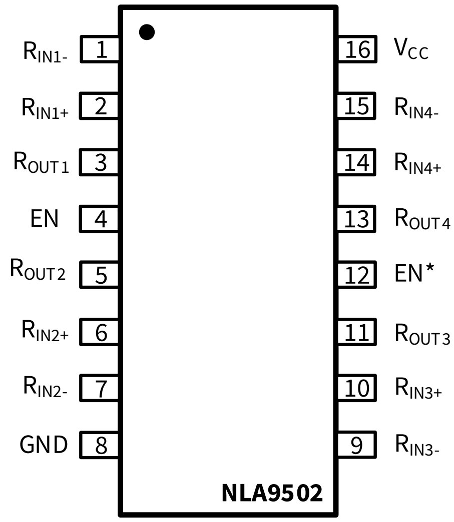


Figure 1. 1 TSSOP16 Package of NLA9502

Table 1. 1 NLA9502 Pin Configuration and Description

NLA9502 PIN NO.	SYMBOL	FUNCTION
1, 7, 9, 15	R_{INx-}	Receiver inverting input of channel 1-4.
2, 6, 10, 14	R_{INx+}	Receiver noninverting input of channel 1-4.
3, 5, 11, 13	R_{OUT}	Receiver Output (3 V CMOS) of channel 1-4.
4	EN	EN is active high enable. EN* is active low enable. The receiver outputs are disabled: EN = GND & EN*= V_{CC}. The receiver outputs are enabled: all other combinations of EN and EN*.
12	EN*	
8	GND	Ground reference point for all circuitry on the part.
16	V_{CC}	Power supply pin, 3.3 V ± 0.3 V.

2. Absolute Maximum Ratings

T_A = 25°C, unless otherwise noted. See [1].

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply voltage	V_{CC}	-0.3		4	V	With respect to GND
Voltage on pin R_{INx+} or R_{INx-}	V_{RINx-} / V_{RINx+}	-0.3		3.9[2]	V	With respect to GND
Voltage on pin EN or EN*	V_{EN^*} / V_{EN}	-0.3		V_{CC} + 0.3	V	With respect to GND
Voltage on pin R_{OUTx}	V_{ROUTx}	-0.3		V_{CC} + 0.3	V	With respect to GND
Operating temperature range	T_A	-40		85	℃	
Junction temperature	T_j	-40		150	℃	
Storage temperature	T_{stg}	-65		150	℃	

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] The device operates for receiver input voltages up to V_{CC}, but exceeding V_{CC} turns on the ESD protection circuitry which clamps the bus voltages.

3. ESD ratings

Symbol	Ratings	Value	Unit
$V_{ESD-HBM1}$	Human body model (JESD22/A114) – 100pF, 1.5kΩ ● All pins	± 6.0	kV
$V_{ESD-CDM1}$	Charged device model (JESD22/C101): ● All pins	± 2.0	kV

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3	3.3	3.6	V
Voltage on pin R_{INx+} or R_{INx-}	V_{RINx-} / V_{RINx+}	0		3	V
Operating temperature range	T_A	-40	25	85	℃

5. Thermal Characteristics

Parameters	Symbol	TSSOP16	Unit
Junction-to-ambient thermal resistance	θ_{JA}	110	°C / W
Junction-to-case (top) thermal resistance	$\theta_{JC\ (top)}$	47	°C / W
Junction-to-board thermal resistance	θ_{JB}	55	°C / W

6. Specifications

6.1.Electrical Characteristics

Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground. All typical are given for V_{CC} =3.3 V and T_A = 25 °C, unless otherwise noted.

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Current (V_{CC} pin)						
Current with receivers enabled	I_{CC}		12	17	mA	No load, EN = EN* = V_{CC} or GND, inputs open
			12	17	mA	No load, EN = EN* = 2.4 V or 0.5 V, inputs open
Current with receivers disabled	I_{CCZ}		0.7	5	mA	No load, EN = GND, EN* = V_{CC}, inputs open
Input pins R_{INx+} / R_{INx-}						
Differential input high threshold	V_{TH}		20	100	mV	V_{CM} = 1.2 V[1], the differential voltage between R_{INx+} and R_{INx-}
Differential input low threshold	V_{TL}	-100	-20		mV	
Common mode voltage range[2]	V_{CMR}	0.1		2.3	V	V_{ID} = 200 mV, the peak-peak differential voltage between R_{INx+} and R_{INx-}
Input current	I_{IN}	-10	±1	10	μA	V_{IN} = 2.8 V, V_{CC} = 3.6 V or 0 V
		-20	±1	20		V_{IN} = 0 V, V_{CC} = 3.6 V or 0 V
		-20		20		V_{IN} = 3.6 V, V_{CC} = 0 V
Output pins R_{OUTx}						
Output high voltage	V_{OH}	2.7	3		V	I_{OH} = −0.4 mA, V_{ID} = 200 mV
		2.7	3			I_{OH} = −0.4 mA, input terminated[3]
		2.7	3			I_{OH} = −0.4 mA, input shorted / open
Output low voltage	V_{OL}		0.1	0.25	V	I_{OL} = 2 mA, V_{ID} = −200 mV
Output short circuit current [4]	I_{OS}	-15	-48	-120	mA	Receiver enabled, V_{ID} = 200 mV, V_{OUT} = 0 V

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Output TRI-STATE current	I_{OZ}	-10	±1	10	μA	Receiver disabled, V_{OUT} = V_{CC} or 0 V
Input pins EN / EN*						
High level input voltage	V_{IH}	2		V_{CC}	V	
Low level input voltage	V_{IL}	GND		0.8	V	
Input current	I_{IN}	-10	±1	10	μA	V_{IN} = 0 V or V_{CC}, other input = V_{CC} or GND
Input clamp voltage	V_{CL}	-1.5	-0.8		V	I_{CL} = –18 mA

[1] V_{CC} is always higher than R_{INx+} and $R_{INx–}$ voltage. R_{INx+} and $R_{INx–}$ are allowed to have a voltage range –0.2 V to V_{CC} – V_{ID} / 2. However, to be compliant with AC specifications, the common voltage range is 0.1 V to 2.3 V.

[2] V_{CMR} is reduced for larger input differential voltage (V_{ID}). For example, if V_{ID} is 400 mV, V_{CMR} is 0.2 V to 2.2 V. The fail-safe condition with inputs shorted is not supported over the common-mode range of 0 V to 2.4 V. However, it is supported only with inputs shorted and no external common-mode voltage applied. A V_{ID} up to V_{CC} can be applied to the R_{INx+} / $R_{INx–}$ inputs with the common-mode voltage set to V_{CC}/2. Propagation delay and differential pulse skew decrease when V_{ID} is increased from 200 mV to 400 mV. Skew specifications apply for 200 mV ≤ V_{ID} ≤ 800 mV over the common-mode range.

[3] The termination resistance which is placed between R_{INx+} and R_{INx-} to match the differential impedance of transmission medium.

[4] Output short-circuit current (I_{OS}) is specified as magnitude only. Minus sign indicates direction only. Note that only one output should be shorted at a time. Do not exceed the maximum junction temperature specification (150 °C).

6.2. Switching Electrical Characteristics

V_{CC} = 3 V to 3.6 V, T_j=-40℃ to 150℃. All typical are given for V_{CC} =3.3 V and T_A = 25 °C, unless otherwise noted[1].

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Propagation delay						
Receiver propagation delay of falling edge	t_{PHLD}			3.3	ns	V_{CM} = 1.2 V, V_{ID} = 200 mV, C_L = 10 pF[2], see Figure 5. 2
Receiver propagation delay of rising edge	t_{PLHD}			3.3	ns	
Differential pulse skew $\lvert t_{PHLD} – t_{PLHD}\rvert$[3]	t_{SKD1}	0	0.1	0.35	ns	
Differential channel-to-channel skew[4]	t_{SKD2}	0	0.1	0.5	ns	Guaranteed by design
Differential part-to-part skew[5]	t_{SKD3}			1	ns	
Differential part-to-part skew[6]	t_{SKD4}			1.5	ns	
Transition time						
Rise Time	t_{TLH}		0.65	1.2	ns	From 20% to 80%[9], see Figure 5. 2
Fall Time	t_{THL}		0.65	1.2	ns	From 80% to 20%[9], see Figure 5. 2
Disable and enable time						

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Disable time high to Z	t_{PHZ}		11	17	ns	R_L = 2 kΩ[8], C_L = 10 pF[2] See Figure 5. 3 and Figure 5. 4
Disable time low to Z	t_{PLZ}		9	17	ns	
Enable time Z to high	t_{PZH}		6	12	ns	
Enable time Z to low	t_{PZL}		6	12	ns	
Operating frequency						
Maximum operating frequency[7]	f_{MAX}	200	250		MHz	All channels switching

[1] The waveform of generator for all tests, unless otherwise specified: f = 1 MHz, Z_O = 50 Ω, t_{TLH} and t_{THL} (0% to 100%) ≤ 3 ns for R_{INx+} or R_{INx-}.

[2] C_L includes load and jig capacitance.

[3] t_{SKD1} is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

[4] t_{SKD2}, channel-to-channel skew, is defined as the difference between the propagation delay of one channel and that of the others on the same chip with any event on the inputs.

[5] t_{SKD3}, part-to-part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same V_{CC}, and within 5°C of each other within the operating temperature range.

[6] t_{SKD4}, part-to-part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Maximum –Minimum| differential propagation delay.

[7] f_{MAX} generator input conditions: f = 200 MHz, t_{TLH} = t_{THL} < 1 ns (0% to 100%), 50% duty cycle, differential (1.05 V to 1.35 V, peak to peak). Evaluation criteria: 60%/40% duty cycle, V_{OL} (maximum = 0.4 V), V_{OH} (minimum = 2.7 V), and load = 15 pF (load and jig capacitance).

[8] R_L is connected to V_{CC} for measuring t_{PLZ} and t_{PZL}. R_L is connected to GND for measuring t_{PHZ} and t_{PZH}.

[9] There is no additional external C_L load on the R_{OUT} port.

6.3.Parameter Measurement Information

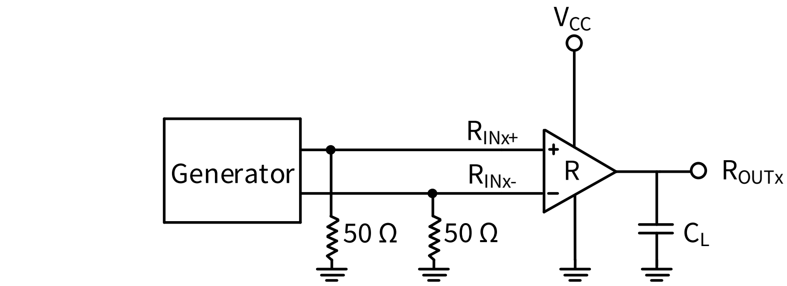


Figure 5. 1 Test circuit for receiver propagation delay and transition time

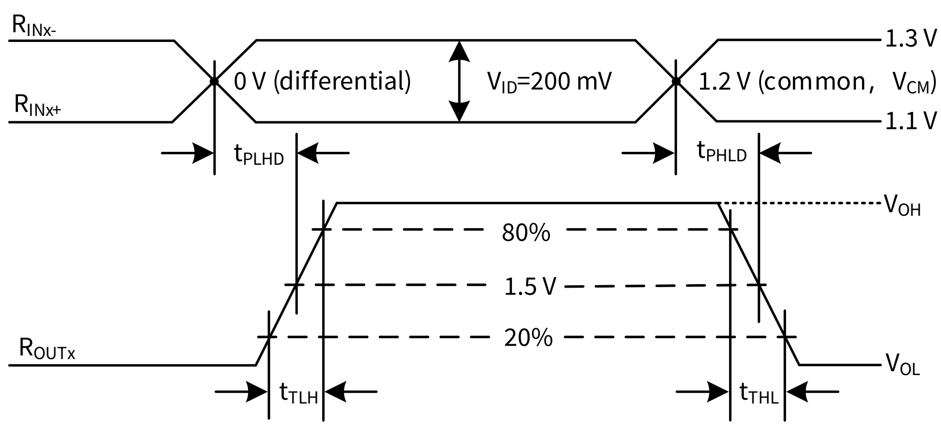
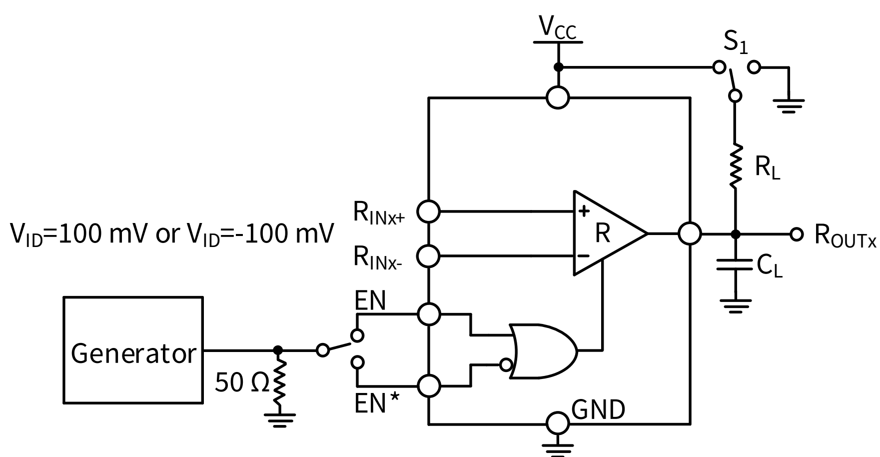


Figure 5. 2 Waveforms of receiver propagation delay and transition time



NOTES

1.CL includes load and test jig capacitors.

2.S1 connected to VCC for tPZL and tPLZ measurments.

3.S1 connected TO GND for tPZH and tPHZ measurments.

Figure 5. 3 Test circuit for receiver enable / disable time

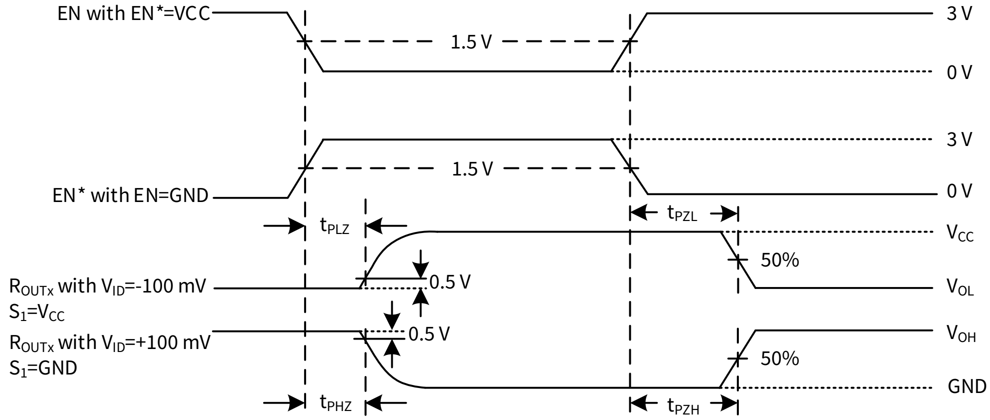


Figure 5. 4 Waveforms of receiver enable / disable time

7. Function Description

7.1. Overview

The NLA9502 is a quad-channel LVDS receiver. It can accept small swing (350 mV typical) differential input signal levels and convert it into a single-ended 3 V COMS logic signal.

Typically, the receiver and driver are used in combination for point-to-point data transmission. Given that the driver is a current output type, a terminal resistor must be connected in parallel to the receiver input and as close to the receiver as possible. LVDS does not work without resistor termination. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic impedance of the media is in the range of 100 Ω. Consequently, a 100 Ω termination resistor is used to match the transmission medium.

The NLA9502 differential line receiver can detect signals as low as 100 mV, over a ± 1 V common-mode range centered around 1.2 V. This is because the driver bias voltage is usually 1.2 V and fluctuates ± 1 V around the center point.

The NLA9502 has active high (EN) and active low (EN*) enable inputs (OR-ed together). When EN = GND and EN* = V_{CC}, all the logic outputs behave high impedance state.

7.2. Functional block diagram

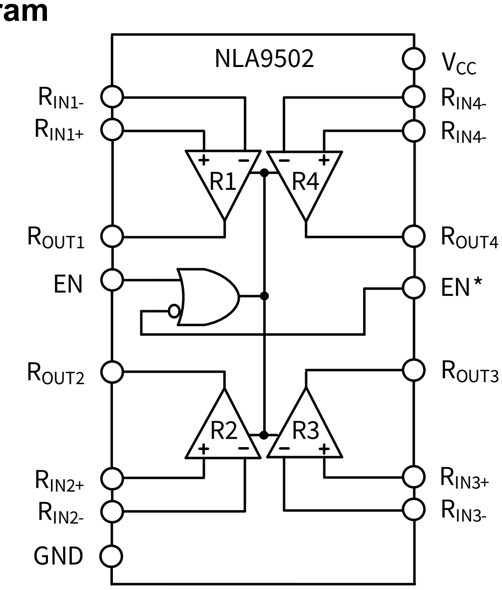


Figure 6. 1 Block diagram of NLA9502

7.3. Functional modes

Table 6. 1 lists the functional modes of NLA9502.

Table 6. 1 Truth table

EN	EN*	INPUT (R_{INx+} - R_{INx-})	OUTPUT (R_{OUTx})
L	H	X	Z
All other combinations of EN and EN*		V_{ID} ≥ 100 mV	H
		V_{ID} ≤ -100 mV	L
		Input fail-safe: open / terminated/ shorted	H

Notes: H = high level, L = low level, Z = high impedance, X = irrelevant.

7.4. Fail-safe features

The LVDS receiver NLA9502 is a high-gain, high-speed device that amplifies a small differential signal (20 mV) to CMOS logic levels. To prevent noise from appearing as a valid signal, The internal fail-safe circuitry of the receiver is designed to source or sink a small amount of current, providing fail-safe protection for open, terminated, or shorted receiver inputs.

(1) Open input: The input is biased by internal high value pull-up and pull-down resistors to set the output to a high state. High and stable high-level output is guaranteed by internal circuitry, under open circuit input conditions.

(2) Terminated input: If the driver is disconnected (the cable is unplugged), or the driver is in TRI-STATE or off, the output of the receiver will be in a high-level state, even if the 100 Ω terminal resistance at the end of the cable crosses the input pin. The unplugged cable becomes a floating antenna that picks up noise. If the differential noise picked up by the cable exceeds 10 mV, the receiver may perceive the noise as a valid signal. To ensure that any noise is treated as common mode rather than differential, a balanced interconnection must be used.

(3) Shorted input: If a fault situation occurs that shorts the receiver input, resulting in a differential input voltage of 0 V, the receiver output remains at a high-level state. Short circuit input fault protection is not supported within the common model circumference of the device (0 V to 2.4 V). It is only supported when the input is short-circuited, and no external common-mode voltage is applied.

8. Application and Implementation

8.1. Typical Application

Figure 7. 1 shows a typical application for point-to-point data transmission using LVDS driver and LVDS receiver.

The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic impedance of the media is in the range of 100 Ω. Therefore, the receiver input uses a 100 Ω terminal resistor to match the transmission medium.

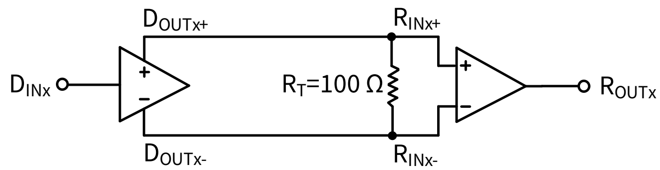


Figure 7. 1 Typical Application Circuit

8.2. Layout Guidelines

The NLA9502 requires a 0.1 μF bypass capacitors between V_{CC} and GND. The capacitor should be placed as close as possible to the package.

For differential traces, it is recommended to match the electrical lengths between traces for better EMI performance and less phase difference. Meanwhile, the differential traces should be placed as close and constant as possible to eliminate refection and ensure noise is coupled as common mode.

For termination resistor, it should be located as close to the receiver input pins as possible. The distance between the termination resistor and the receiver must be < 10 mm (12 mm maximum).

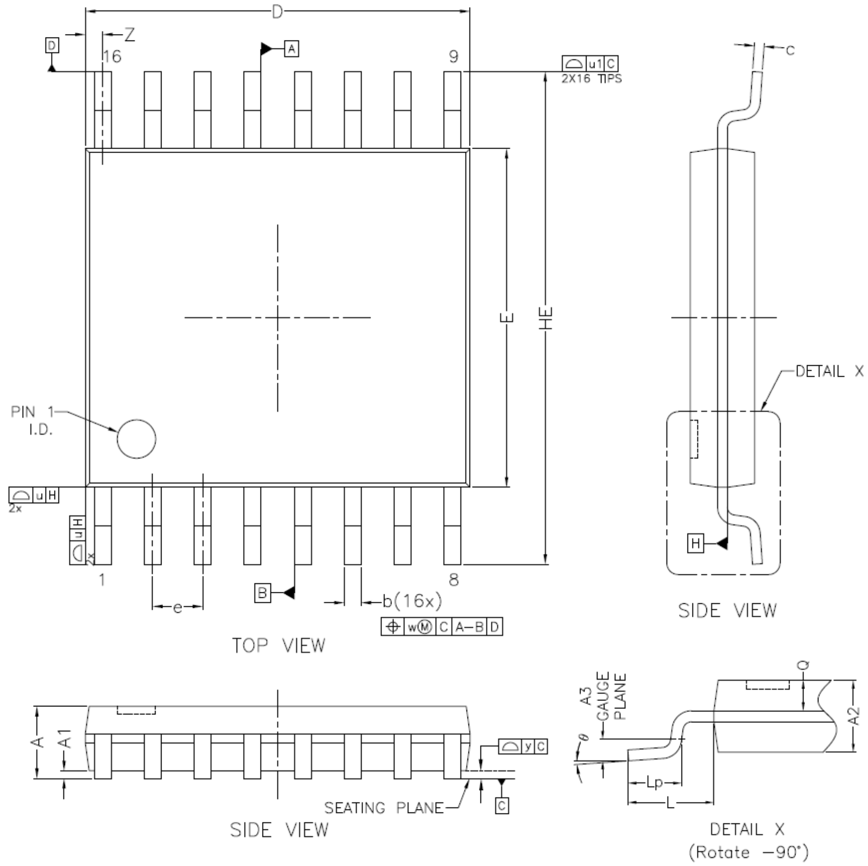
For routing, avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

For R_{OUTx}, a serial resistor is optional to use.

8.3. Oscilloscope and probe requirements

Considering the high communication rate of LVDS, oscilloscope and probe are required to ensure the reliability of test results. Always use high impedance (> 100 kΩ), low capacitance (< 2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing gives deceiving results.

9. Package Information



* CONTROLLING DIMENSION : MM

SYMBOL	MM		
	MIN.	NOM.	MAX.
A	--	--	1.10
A1	0.05	--	0.15
A2	0.80	--	0.95
b	0.19	--	0.30
c	0.10	--	0.20
D	4.90	5.00	5.10
E	4.30	4.40	4.50
HE	6.20	--	6.60
Q	0.30	--	0.40
e	0.65 BSC		
A3	0.25 REF		
L	1.00 REF		
Lp	0.50	--	0.75
w	0.13		
y	0.10		
u	0.10		
u1	0.20		
Z	0.225		
θ	0°	--	8°

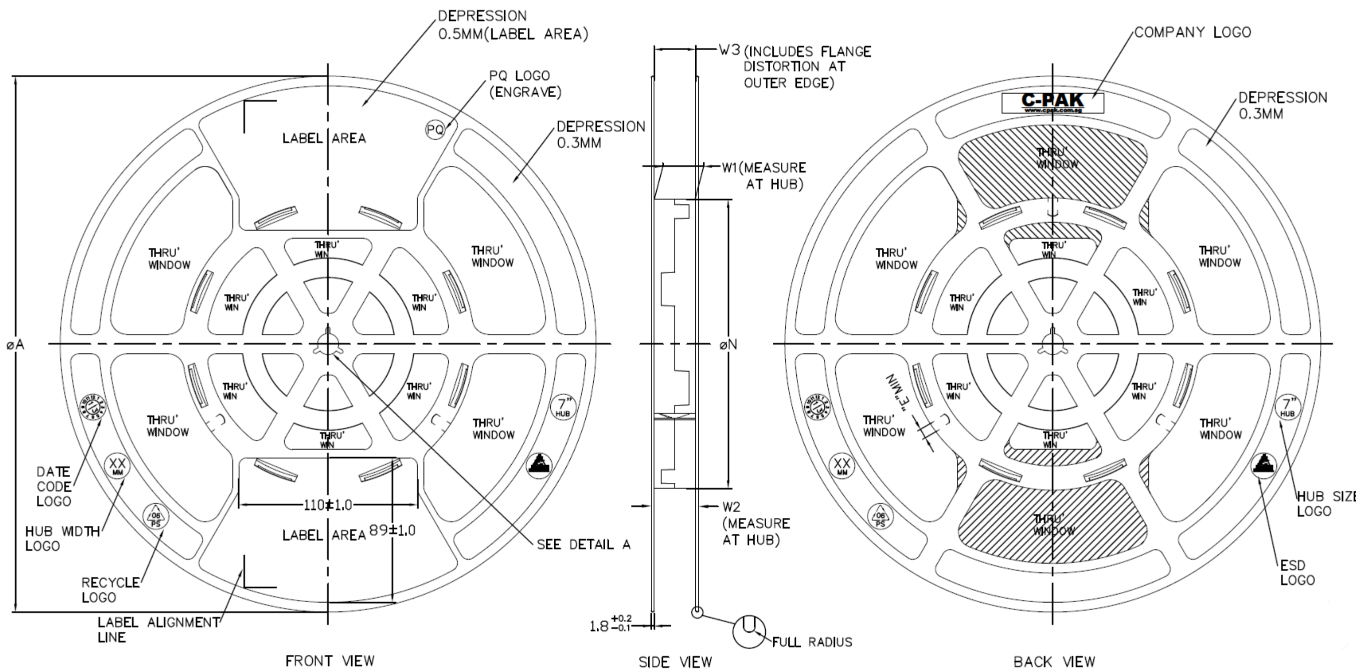
NOTES:
1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
2.0 PLASTIC OR METAL PROTRUSIONS OF 0.15MM MAXIMUM PER SIDE ARE NOT INCLUDED

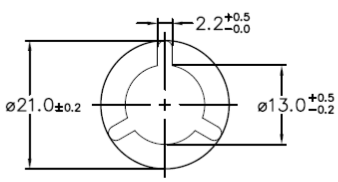
Figure 8. 1 TSSOP16 Package Shape and Dimension in millimeters

10. Order Information

Part Number	Pins	Operating Temperature	MSL	Package	SPQ
NLA9502-DTSPR	16	-40℃ to 85℃	1	TSSOP16	2500

11. Tape and Reel Information





ARBOR HOLE
DETAIL A
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	ØA ±2.0	ØN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	$8.4^{+1.5}_{-0.0}$	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	$12.4^{+2.0}_{-0.0}$	18.4		5.5
16MM	330	178	$16.4^{+2.0}_{-0.0}$	22.4		5.5
24MM	330	178	$24.4^{+2.0}_{-0.0}$	30.4		5.5
32MM	330	178	$32.4^{+2.0}_{-0.0}$	38.4		5.5

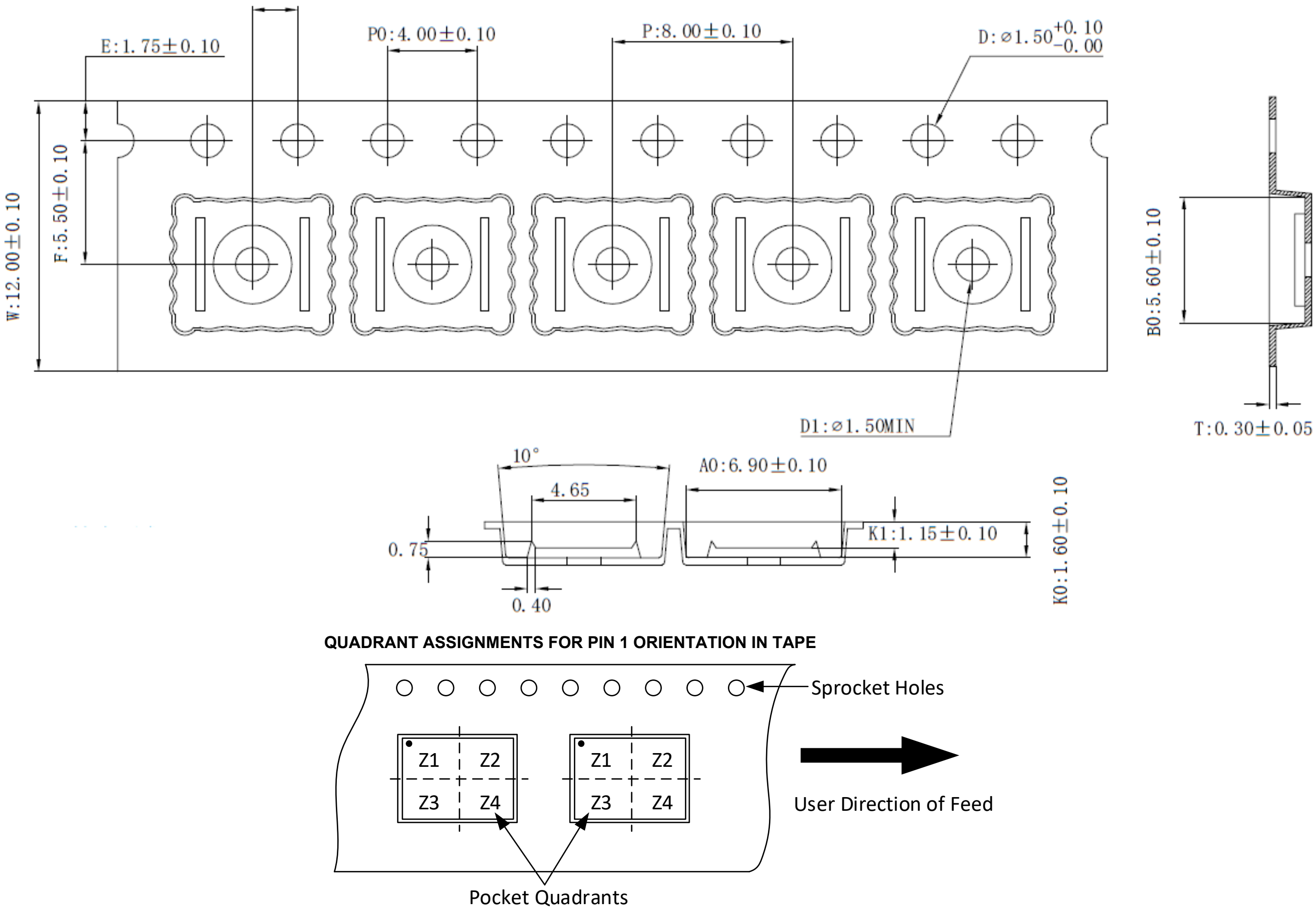


Figure 10. 1 Tape and Reel Information of TSSOP16 in millimeters

12. Revision History

Revision	Description	Date
1.0	Initial version.	2025/3/24

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