# NCA8245L
# Octal Buffers and Line Drivers With 3-State Outputs
Datasheet (EN) 1.0

## Product Overview

NCA8245L is an octal buffer/driver used for improving driver ability of bus-oriented receivers and transmitters, clock drivers etc. and ensuring the accuracy of signal timing. The device provides a direction-control (DIR) input for transmitting data bidirectionally. When DIR is logic high, it transmits data from A to B, and from B to A when DIR is logic low. When /OE is high, the outputs are in the high-impedance state. During power up and power down, /OE should be tied to VCC through a pull-up resistor to ensure the high impedance state.

NCA8245L can tolerate up to 5.5V input voltage and each channel supports maximum 24 mA current drive. All unused inputs must be held at $V_{CC}$ or GND to prevent excess supply current.

## Key Features

- Qualified for Automotive applications:
  NCA8245L-Q1TSTR
- Inputs are TTL compatible
- Power supply voltage: 1.65V to 3.6V
- 5.5 V Tolerant Inputs
- ESD Protection Exceeds JESD 22
  - 4000V Human-Body Model (A114-A)
  - 2000V Charged-Device Model (C101)
- Operation temperature: -40℃~125℃
- RoHS-compliant packages: TSSOP20

## Applications

- Motor driver
- Traction inverter
- I/O modules
- LED displays

## Device Information

| Part Number | Package | Body Size |
|---|---|---|
| NCA8245L-DTSTR | TSSOP20 | 6.50mm × 4.50mm |
| NCA8245L-Q1TSTR | TSSOP20 | 6.50mm × 4.50mm |

## Functional Block Diagrams

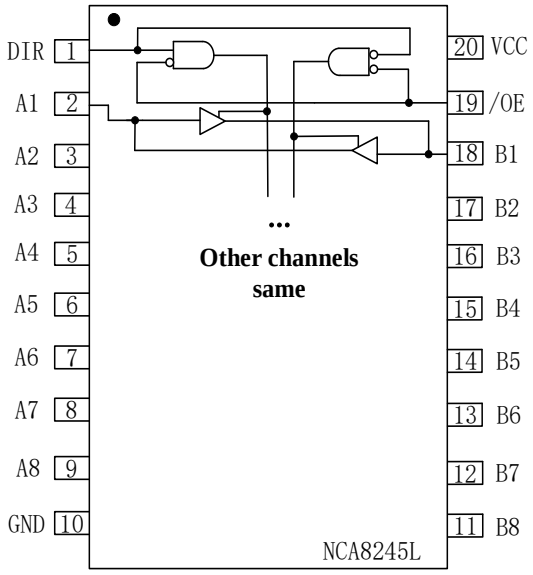



Figure 1. NCA8245L Block Diagram

# INDEX

# 1. Pin Configuration and Functions

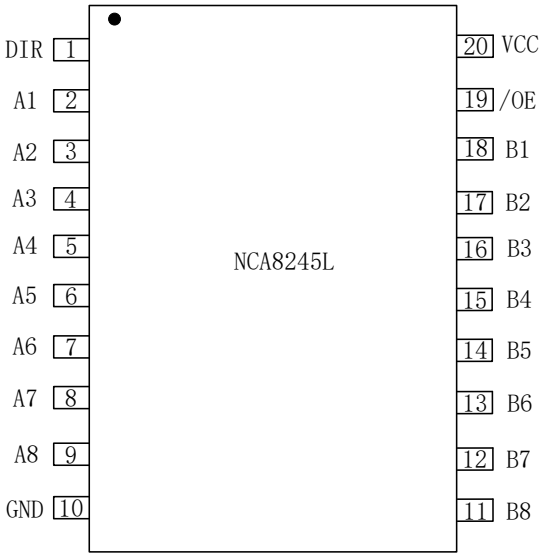



Figure 1.1 NCA8245L Package

Table 1.1 NCA8245L Pin Configuration and Description

| *NCA8245L PIN NO.* | *SYMBOL* | *FUNCTION* |
|---|---|---|
| 1 | DIR | Direction control, referenced to $V_{CCA}$. DIR is logic high, direction is from A to B and DIR is logic low, transmission is from B to A. |
| 2 | A1 | Input/Output of B1 |
| 3 | A2 | Input/Output of B2 |
| 4 | A3 | Input/Output of B3 |
| 5 | A4 | Input/Output of B4 |
| 6 | A5 | Input/Output ofB5 |
| 7 | A6 | Input/Output of B6 |
| 8 | A7 | Input/Output of B7 |
| 9 | A8 | Input/Output of B8 |
| 10 | GND | Ground |
| 11 | B8 | Input/Output of A8 |
| 12 | B7 | Input/Output of A7 |
| 13 | B6 | Input/Output of A6 |
| 14 | B5 | Input/Output of A5 |
| 15 | B4 | Input/Output of A4 |
| 16 | B3 | Input/Output of A3 |

| | | |
|---|---|---|
| 17 | B2 | Input/Output of A2 |
| 18 | B1 | Input/Output of A1 |
| 19 | /OE | Active low Output enable |
| 20 | $V_{CC}$ | Power |

## 2. Absolute Maximum Ratings

| *Parameters* | *Symbol* | *Min* | *Typ* | *Max* | *Unit* | *Comments* |
|---|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | -0.5 | | 7 | V | |
| Maximum Input Voltage | $V_I$ | -0.5 | | $V_{CC}$ +0.5 | V | The maximum voltage must not exceed 7V |
| Maximum Output Voltage | $V_O$ | -0.5 | | $V_{CC}$ +0.5 | V | The maximum voltage must not exceed 7V |
| Input clamp current | $I_{IK}$ | -20 | | 20 | mA | $V_I < 0$ or $V_I > V_{CC}$ |
| Output clamp current | $I_{OK}$ | -20 | | 20 | mA | $V_I < 0$ or $V_I > V_{CC}$ |
| Continuous output current | $I_O$ | -50 | | 50 | mA | $V_O$=0 to $V_{CC}$ |
| Ambient Temperature | $T_a$ | -40 | | 125 | ℃ | |
| Junction Temperature | $T_J$ | | | 150 | ℃ | |
| Storage Temperature | $T_{stg}$ | -65 | | 150 | ℃ | |
| Electrostatic discharge | HBM | -4000 | | 4000 | V | Per ANSI/ESDA/JEDEC JS-001 |
| | CDM | -2000 | | 2000 | V | Per JEDEC specification JESD22- C101 |

## 3. Recommended Operating Conditions

Over recommended operating free-air temperature range (unless otherwise noted)(1)

| *Parameters* | *Symbol* | *Min* | *Typ* | *Max* | *Unit* | *Comments* |
|---|---|---|---|---|---|---|
| Power Supply Voltage | VCC | 1.65 | | 3.6 | V | |
| High-level output current | $I_{OH}$ | -4 | | | mA | $V_{CC}$ =1.65V |
| | | -8 | | | | $V_{CC}$ =2.3V |
| | | -12 | | | | $V_{CC}$ =2.7V |
| | | -24 | | | | $V_{CC}$ =3V |
| Low-level output current | $I_{OL}$ | | | 4 | mA | $V_{CC}$ =1.65V |
| | | | | 8 | | $V_{CC}$ =2.3V |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | | 12 | | $V_{CC}$ =2.7V |
| | | | | 24 | | $V_{CC}$=3V |
| Input transition rise or fall rate | Δt/Δv | | | 10 | ns/V | |
| Operating free-air temperature | $T_A$ | -40 | | 125 | ℃ | |

(1) All unused inputs of the device must be held at VCC or GND to ensure proper device operation.

# 4. Thermal Information

| *Parameters* | *Symbol* | *TSSOP20* | *Unit* |
|---|---|---|---|
| Junction-to-ambient thermal resistance | $R_{\theta JA}$ | 103 | °C/W |
| Junction-to-case(top) thermal resistance | $R_{\theta JC(top)}$ | 37.7 | °C/W |
| Junction-to-board thermal resistance | $R_{\theta JB}$ | 54 | °C/W |
| Junction-to- top characterization parameter | $\Psi_{JT}$ | 6.8 | °C/W |
| Junction-to- board characterization parameter | $\Psi_{JB}$ | 65.1 | °C/W |

# 5. Specifications

## 5.1. Electrical Characteristics

($V_{CC}$=1.65V~3.6V ,$T_a$=-40℃ to 125℃. Unless otherwise noted, Typical values are at Ta = 25℃)

| *Parameters* | *Symbol* | *Min* | *Typ* | *Max* | *Unit* | *Comments* |
|---|---|---|---|---|---|---|
| Supply current | $I_{CC}$ | | | 40 | uA | $V_{CC}$=3.6V， $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 |
| | | | | 40 | | $V_{CC}$=3.6V， 3.6V≤$V_I$≤ 5.5V(1)， $I_O$ = 0 |
| Increasing supply current(2) | $\Delta I_{CC}$ | | | 5 | mA | One input at $V_{CC}$-0.6V, Other inputs at GND or $V_{CC}$, 2.7V≤$V_{CC}$≤3.6V |
| High-level input voltage | $V_{IH}$ | 0.65*VCC | | | V | $V_{CC}$ =1.65V to 1.95V |
| | | 1.7 | | | | $V_{CC}$ =2.3V to 2.7V |
| | | 2 | | | | $V_{CC}$ =2.7V to 3.6V |
| Low-level input voltage | $V_{IL}$ | | | 0.35*VCC | V | $V_{CC}$ =1.65V to 1.95V |
| | | | | 0.7 | | $V_{CC}$ =2.3V to 2.7V |
| | | | | 0.8 | | $V_{CC}$ =2.7V to 3.6V |

| | | | | | | |
|---|---|---|---|---|---|---|
| High-level output voltage | $V_{OH}$ | $V_{CC}$-0.2 | | | V | 1.65V≤$V_{CC}$≤3.6V，$I_{OH}$=-100uA |
| | | 1.1 | | | V | $V_{CC}$=1.65V，$I_{OH}$=-4mA |
| | | 1.6 | | | V | $V_{CC}$ =2.3V，$I_{OH}$=-8mA |
| | | 2.1 | | | V | $V_{CC}$=2.7V，$I_{OH}$=-12mA |
| | | 2.3 | | | V | $V_{CC}$=3V，$I_{OH}$=-12mA |
| | | 2.1 | | | V | $V_{CC}$=3V，$I_{OH}$=-24mA |
| Low-level output voltage | $V_{OL}$ | | | 0.2 | V | 1.65V≤$V_{CC}$≤3.6V，$I_{OL}$=100uA |
| | | | | 0.6 | V | $V_{CC}$=1.65V，$I_{OL}$=4mA |
| | | | | 0.75 | V | $V_{CC}$ =2.3V，$I_{OL}$=8mA |
| | | | | 0.6 | V | $V_{CC}$=2.7V，$I_{OL}$=12mA |
| | | | | 0.75 | V | $V_{CC}$=3V，$I_{OL}$=24mA |
| Three-state output current | $I_{OZ}$ | -20 | | 20 | uA | $V_{CC}$=3.6V，$V_O$=0 to 5.5V |
| Off-state leakage output current | $I_{Off}$ | -20 | | 20 | uA | $V_{CC}$=0V，$V_I$/$V_O$ = 5.5V |
| Input current | $I_I$ | -10 | | 10 | uA | $V_{CC}$=3.6V，$V_I$ = 0 to 5.5V |
| Input capacitance | $C_i$ | | 4 | | pF | |
| Output capacitance | $C_O$ | | 8.5 | | pF | |

(1) This applies in the disabled state only.

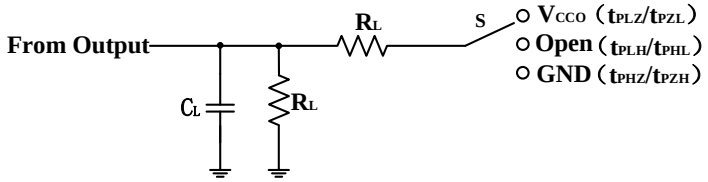
(2) The increasing of supply current for each input that is at one of the specified TTL voltage levels, rather than 0V or $V_{CC}$.

## 5.2. Dynamic Characteristics

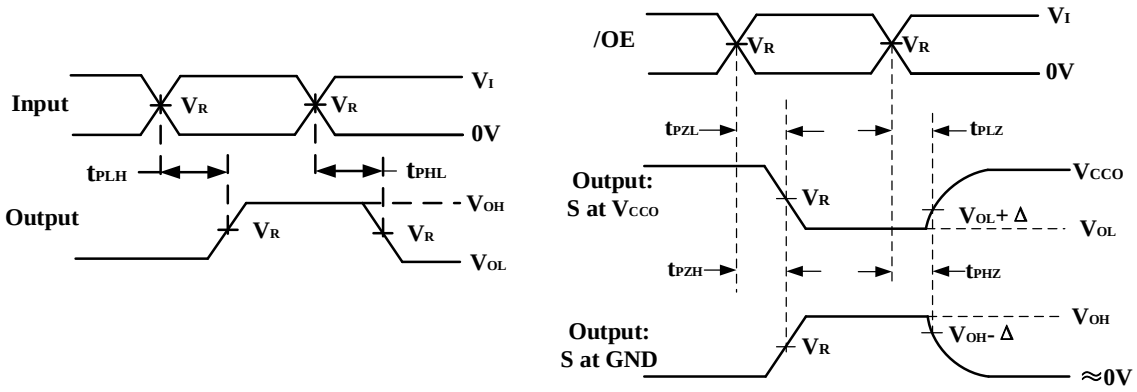
($T_a$=-40℃ to 125℃. Unless otherwise noted, Typical values are at $T_a$ = 25℃， See figure 1)

| *Parameters* | *Symbol* | *Min* | *Typ* | *Max* | *Unit* | *Comments* |
|---|---|---|---|---|---|---|
| Propagation Delay | $t_{pd}$ | | 6.8 | 15 | ns | $V_{CC}$=1.65V |
| | | | 7.2 | 15 | | $V_{CC}$=2.7V |
| | | | 7.4 | 15 | | $V_{CC}$=3.3V |
| Enable to Data Valid | $t_{EN}$ | | | 25 | ns | $V_{CC}$=1.65V |
| | | | | 18 | | $V_{CC}$=2.7V |
| | | | | 18 | | $V_{CC}$=3.3V |
| Disable to tri-state | $t_{DIS}$ | | | 25 | | $V_{CC}$=1.65V |
| | | | | 18 | | $V_{CC}$=2.7V |
| | | | | 18 | | $V_{CC}$=3.3V |

### 5.3. Parameter measurement information




| VCC | Input | | VR | VCCO | CL | RL | Δ |
|---|---|---|---|---|---|---|---|
| | VI | tr/tf | | | | | |
| 1.65 | VCC | ≤2ns | VCC/2 | 2*VCC | 15pF | 1kΩ | 0.15V |
| 2.7V | 2.7V | ≤2.5ns | 1.5V | 6V | 20pF | 500Ω | 0.3V |
| 3.3V | 2.7V | ≤2.5ns | 1.5V | 6V | 25pF | 500Ω | 0.3V |




Note:
1) All input pulses with the following characteristics: PRR ≤1MHz, ZO = 50 Ω, tr ≤ 2.5ns, tf ≤ 2.5ns;
2) CL includes probe and test-fixture capacitance.

Figure 5.1. Load Circuit and Voltage Waveforms for NCA8245L

# 6. Function Description

## 6.1. Overview

NCA8245L is an octal buffer used for improving driver ability of 3-state memory address, clock drivers, and bus-oriented receivers and transmitters and ensuring the accuracy of signal timing. The device provides a direction-control (DIR) input for transmitting data bidirectionally. When DIR is logic high, it transmits data from A to B, and from B to A when DIR is logic low. When /OE is high, the outputs are in the high-impedance state. During power up and power down, /OE should be tied to VCC through a pull-up resistor to ensure the high impedance state. All unused inputs of NCA8245L must be held at VCC or GND to prevent excess ICC.

Table 6.1 Function Table

| *A_IN(1)* | */OE status* | *VCC status* | *B_OUT* | *Comment* |
|---|---|---|---|---|
| L | L | Ready | L | Normal operation. |
| H | L | Ready | H | |
| X | H | Ready | Z | Output Disabled, the output is high impedance. |
| X | X | Unready | Z | The output follows the same status with the input after VCC is powered on and output is enabled. |

(1) L=Logic low; H=Logic high; X=Logic low or logic high.

# 7. Application Note

## 7.1. Application Information

The NCA8245L can be used in Motor driver, Traction inverter, IO modules and LED displays. The maximum output current can be up to 24 mA.

## 7.2. Typical Application Circuit

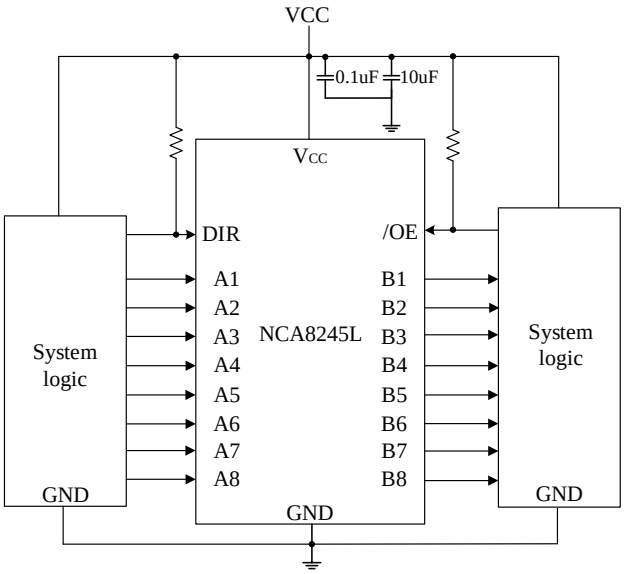
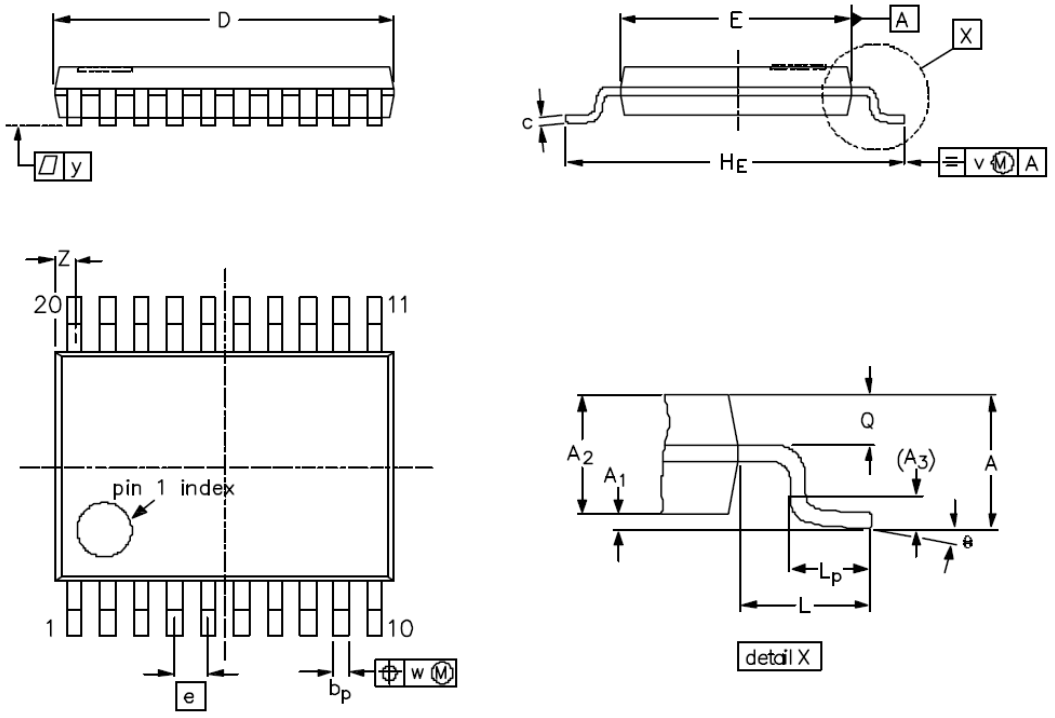



Figure 7.1 Typical application circuit for NCA8245L

# 8. Package Information



DIMENSIONS (mm are the original dimensions)

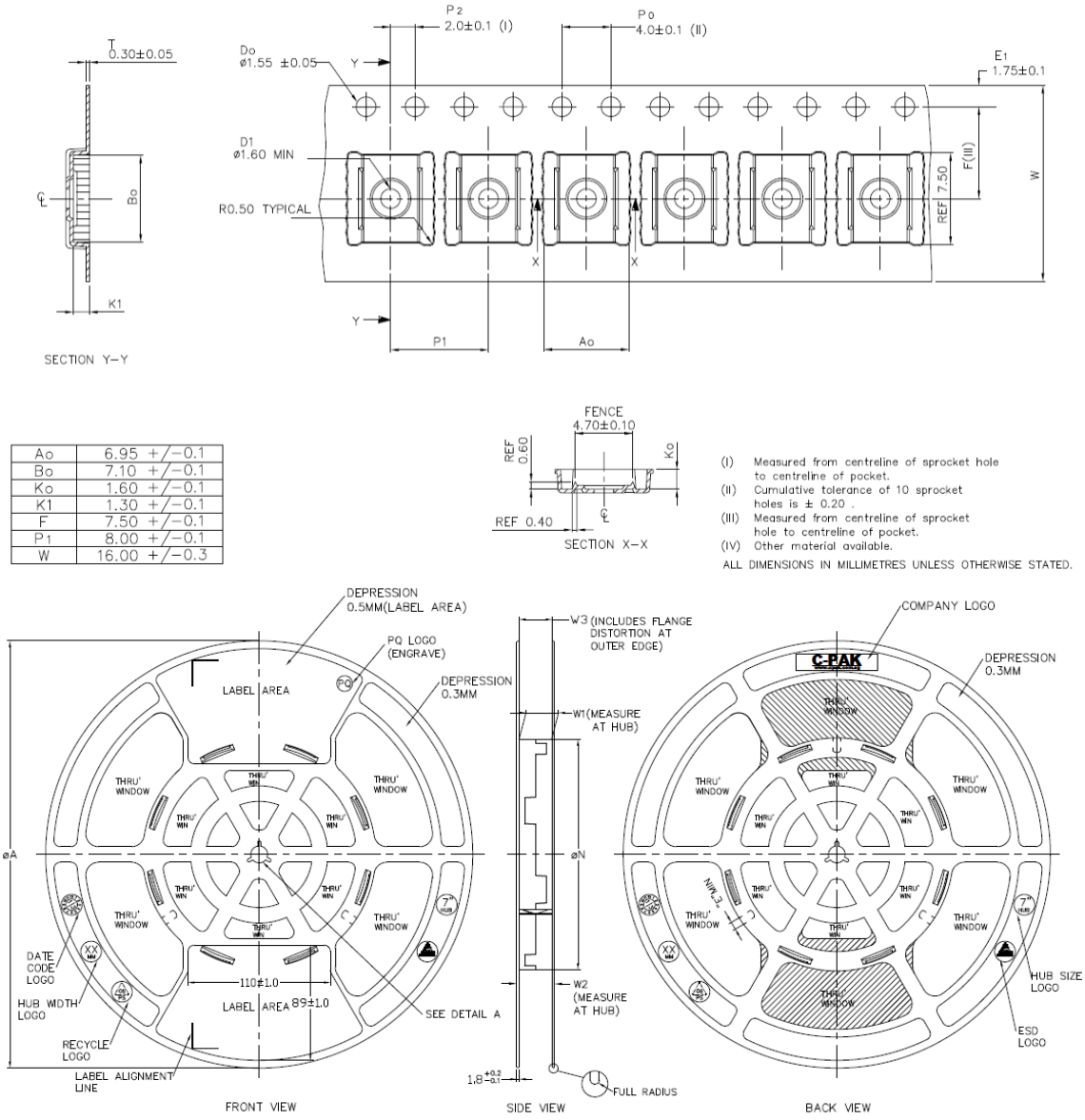
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.10 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 6.6<br>6.4 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1.0 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.5<br>0.2 | 8°<br>0° |

Figure 8.1 TSSOP20 Package Shape and Dimension in millimeters

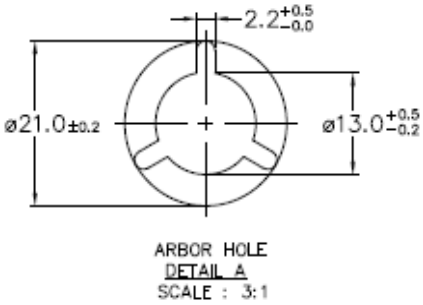
# 9. Ordering Information

| *Part Number* | *PINS* | *Temperature* | *MSL* | *Package Type* | *Package Drawing* | *SPQ* |
|---|---|---|---|---|---|---|
| NCA8245L-DTSTR | 20 | -40 to 125℃ | 1 | TSSOP20 | TSSOP20 | 2500 |
| NCA8245L-Q1TSTR | 20 | -40 to 125℃ | 1 | TSSOP20 | TSSOP20 | 2500 |
| NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures. | | | | | | |

# 10. Tape and Reel Information




| | |
|---|---|
| Ao | 6.95 +/−0.1 |
| Bo | 7.10 +/−0.1 |
| Ko | 1.60 +/−0.1 |
| K1 | 1.30 +/−0.1 |
| F | 7.50 +/−0.1 |
| P1 | 8.00 +/−0.1 |
| W | 16.00 +/−0.3 |




| PRODUCT SPECIFICATION | | | | | | |
|---|---|---|---|---|---|---|
| TAPE WIDTH | øA ±2.0 | øN ±2.0 | W1 | W2 (MAX) | W3 | E (MIN) |
| 08MM | 330 | 178 | 8.4 +1.5 −0.0 | 14.4 | SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE | 5.5 |
| 12MM | 330 | 178 | 12.4 +2.0 −0.0 | 18.4 | | 5.5 |
| 16MM | 330 | 178 | 16.4 +2.0 −0.0 | 22.4 | | 5.5 |
| 24MM | 330 | 178 | 24.4 +2.0 −0.0 | 30.4 | | 5.5 |
| 32MM | 330 | 178 | 32.4 +2.0 −0.0 | 38.4 | | 5.5 |

| SURFACE RESISTIVITY | | | |
|---|---|---|---|
| LEGEND | SR RANGE | TYPE | COLOUR |
| A | BELOW $10^{12}$ | ANTISTATIC | ALL TYPES |
| B | $10^{8}$ TO $10^{11}$ | STATIC DISSIPATIVE | BLACK ONLY |
| C | $10^{5}$ & BELOW $10^{8}$ | CONDUCTIVE (GENERIC) | BLACK ONLY |
| E | $10^{8}$ TO $10^{11}$ | ANTISTATIC (COATED) | ALL TYPES |

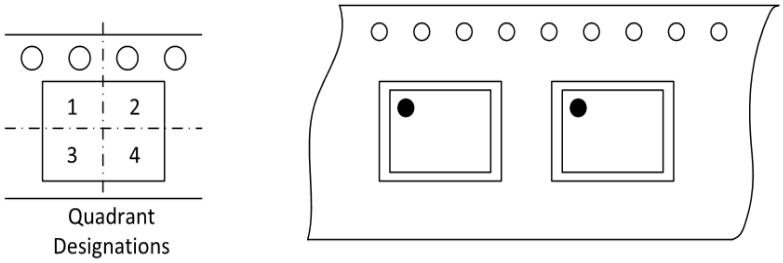



Figure 10.1 Tape and Reel Information of TSSOP

## 11. Revision History

| Revision | Description | Date |
|---|---|---|
| 1.0 | Initial Version | 2023/4/23 |
| | | |
| | | |

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