NOVOSENSE

NCA1462-Q1
CAN FD Signal Improvement Transceiver with Standby Mode
Datasheet (EN) 1.2

Product Overview
NCA1462-Q1 is a high-speed CAN transceiver with Normal and Standby modes and a VIO supply pin. It meets the physical layer requirements of the ISO 11898-2-2024 high speed CAN specification and meets the CiA 601-4 Signal Improvement Capability (SIC) specification, and is fully interoperable with high-speed Classical CAN and CAN FD transceivers. The CAN signal improvements significantly reduce signal ringing on the network, allowing reliable CAN FD communication at 5 Mbit/s in larger topologies. In addition, the NCA1462 has a much tighter bit timing symmetry, enabling CAN FD communication up to 8 Mbit/s.
The NCA1462 is intended as a simple replacement for high-speed Classical CAN and CAN FD transceivers, such as the NCA1042.

Key Features
- Fully compatible with the ISO11898-2 standard
- I/O voltage range supports 1.8V, 3.3V and 5V MCU
- Power supply voltage
- V_{IO}: 1.7V to 5.5V
- V_{CC}: 4.5V to 5.5V
- Bus fault protection of -58V to +58V
- Short circuit protection
- Bus common-mode voltage of -12V to +12V
- Transmit data (TXD) dominant time out function
- Bus dominant time out function in standby mode
- Very low-current Standby mode with wake-up capability
- Over temperature protection
- Data rate: up to 8Mbps
- Operation temperature: -40°C to +125°C
- AEC-Q100 qualified for automotive, Grade 1
- RoHS & REACH compliant

Applications
- CAN bus standards such as CANopen, DeviceNet, NMEA2000, ARNIC825, ISO11783 and CANaerospace
- Highly loaded CAN networks down to 10 kbps networks
- Automotive gateway
- Body control modules
- Advanced Driver Assistance Systems (ADAS)
- Infotainment system

Device Information

Part Number	*Package*	*Body Size*
NCA1462-Q1SPR[I]	SOP8	4.90mm × 3.90mm
NCA1462-Q1DNR[I]	DFN8	3.00mm × 3.00mm
NCA1462N-Q1SPR[I]	SOP8	4.90mm × 3.90mm
NCA1462N-Q1DNR[I]	DFN8	3.00mm × 3.00mm
NCA1462-Q1SPRH[II]	SOP8	4.90mm × 3.90mm
NCA1462-Q1DNRH[II]	DFN8	3.00mm × 3.00mm
NCA1462N-Q1SPRH[II]	SOP8	4.90mm × 3.90mm
NCA1462N-Q1DNRH[II]	DFN8	3.00mm × 3.00mm

[I] Not VeLIO verified part number

[II] Could pass VeLIO test part number

Functional Block Diagrams

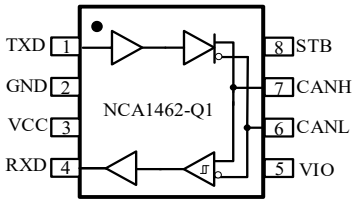

Figure 1. NCA1462-Q1 Block Diagram

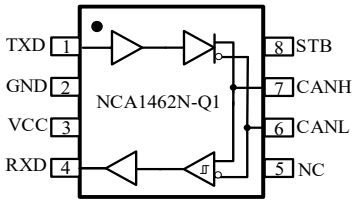

Figure 2. NCA1462N-Q1 Block Diagram

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1. Pin Configuration and Functions

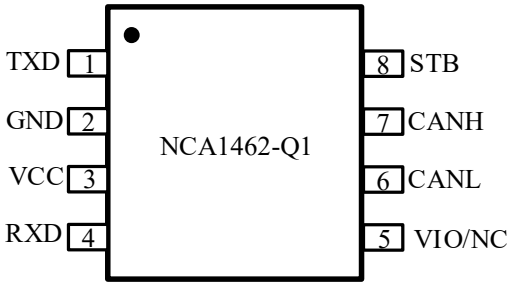


Figure 1-1 NCA1462(N)-Q1, SOP8 Package, Top view

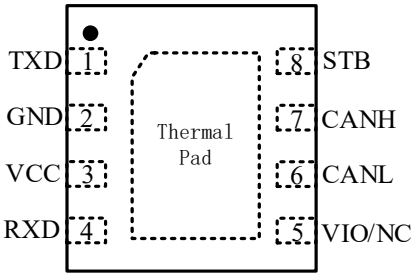


Figure 1-2 NCA1462 (N)-Q1,DFN8 Package, Top view

Table 1-1 NCA1462-Q1 Pin Configuration and Description

NCA1462-Q1 PIN NO.	***NCA1462N-Q1 PIN NO.***	***SYMBOL***	***FUNCTION***
1	1	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
2	2	GND	Ground
3	3	VCC	Power Supply
4	4	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
5	\	VIO	Logic I/O supply voltage
\	5	NC	No connection
6	6	CANL	Low-level CAN bus line
7	7	CANH	High-level CAN bus line
8	8	STB	STB (standby mode) select pin (active high)

2. Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) [1] [2].

Parameters	*Symbol*	*Min*	*Max*	*Unit*
Power Supply Voltage	VCC, VIO	-0.3	7	V
Logic I/O Voltage	TXD, RXD, STB	-0.3	7	V
Maximum bus Pin Voltage	V_{CANH}, V_{CANL}	-58	58	V
Voltage between pin CANH and pin CANL	V_{CANH} - V_{CANL}	-58	58	V
Junction temperature	T_J	-40	150	°C
Storage Temperature	T_{stg}	-65	150	°C

[1] Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Rating condition for extended periods may affect device reliability.

[2] All voltage values, except for “Voltage between pin CANH and pin CANL”, are with respect to GND terminal.

3. EMC Ratings

Parameters	Ratings	Value	Unit	
Electrostatic discharge	Human Body Model (HBM), per AEC-Q100-002 ● on any pin ● on pins CANH and CANL	 ±4 ±8	 kV kV	[I] Not VeLIO verified part number
	Human Body Model (HBM), per AEC-Q100-002 ● on any pin ● on pins CANH and CANL	 ±4 ±6	 kV kV	[II] Could pass VeLIO test part number
	Charged Device Model (CDM), per AEC-Q100-011 ● All pins	 ±2	 kV	
	Machine Model (MM), per JESD22-A115C ● All pins	 ±400	 V	
	System, per IEC 61000 4 2 (150 pF, 330 Ω at pins CANH and CANL to GND	±8.0	kV	[I] Not VeLIO verified part number
	System, per IEC 61000 4 2 (150 pF, 330 Ω at pins CANH and CANL to GND	±3.0	kV	[II] Could pass VeLIO test part number
Electrical disturbances	Electrical transient conduction, per ISO 7637-2, on CANH and CANL ● Pulse 1 ● Pulse 2a ● Pulse 3a ● Pulse 3b	 -100 75 -150 100	 V V V V	

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	VCC	4.5	5	5.5	V
I/O Level-Shifting Voltage	VIO	1.7	3.3	5.5	V
Operating Temperature	T_{opr}	-40	-	125	°C

5. Thermal Characteristics

Parameters	Symbol	SOP8	DFN8	Unit
IC Junction-to-Air Thermal Resistance	$R_{\theta JA}$	120	52.8	°C /W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	57.8	58.9	°C /W
Junction-to-board thermal resistance	$R_{\theta JB}$	64.2	25.2	°C /W

6. Specifications

6.1. Electrical Characteristics

V_{CC}=4.5V to 5.5V, V_{IO}=1.7 to 5.5V[1], Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at V_{CC}=5V, V_{IO}=3.3V, R_L=60Ω, Ta = 25°C.

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Supply; pin VCC						
V_{CC}	Supply voltage		4.5	-	5.5	V
I_{CC}	Supply current	Normal mode, recessive, V_{TXD}=V_{IO}[2], V_{STB}=0V	-	5	7	mA
		Normal mode, dominant, V_{TXD} =0V	-	45	60	mA
		Normal mode, dominant, V_{TXD} =0, short circuit on bus lines, -3V < (V_{CANH} = V_{CANL}) <18V	-	-	110	mA
		Standby mode, V_{TXD} =V_{IO}, NCA1462-Q1	-	0.7	2	μA
		Standby mode, V_{TXD} =V_{IO}, NCA1462N-Q1		13.5	21	μA
$V_{uvd(VCC)}$	Undervoltage detection voltage on pin VCC	Rising	4	4.27	4.5	V
		Falling	4	4.18	4.5	V
		Hysteresis	50	90	200	mV
I/O level adapter supply; pin V_{IO}; only for NCA1462-Q1						
V_{IO}	Supply voltage on pin VIO		1.7	-	5.5	V
I_{IO}	Supply current on pin VIO	Normal mode, recessive, V_{TXD}=V_{IO}	-	60	140	μA
		Normal mode, dominant, V_{TXD}=0V	-	175	360	μA
		Standby mode; V_{TXD}=V_{IO}	-	6	19	μA
$V_{uvd(VIO)}$	Undervoltage detection voltage on pin VIO	Rising	1.4	1.56	1.7	V
		Falling	1.4	1.50	1.7	V
		Hysteresis	20	60	200	mV
Standby mode control input; pin STB						
V_{IH}	High level input voltage		0.7*V_{IO}[2]	-	V_{IO}+0.3[2]	V
V_{IL}	Low level input voltage		-0.3	-	0.3*V_{IO}[2]	V

V_{hys}	Hysteresis voltage		200	480	800	mV
R_{pu}	Pull-up resistance		40	55	80	kΩ
C_i	Input capacitance	[3]	-	-	10	pF
CAN transmit data input; pin TXD						
V_{IH}	High level input voltage		0.7*V_{IO}[2]	-	V_{IO}+0.3[2]	V
V_{IL}	Low level input voltage		-0.3	-	0.3*V_{IO}[2]	V
V_{hys}	Hysteresis voltage		50	150	600	mV
R_{pu}	Pull-up resistance		40	55	80	kΩ
C_i	Input capacitance	[3]	-	-	10	pF
CAN receive data output; pin RXD						
I_{OH}	High level output current	V_{RXD} = V_{IO} - 0.4V [2]	-10	-3	-1	mA
I_{OL}	Low level output current	V_{RXD} = 0.4V; bus dominant	1	3.5	10	mA
Bus lines; pins CANH and CANL; Driver						
$V_{OH(D)}$	CANH output voltage (Dominant)	V_{TXD} =0V, R_L =50Ω to 65Ω[4]	2.89	3.6	4.26	V
$V_{OL(D)}$	CANL output voltage (Dominant)	V_{TXD} =0V, R_L =50Ω to 65Ω[4]	0.77	1.4	2.13	V
$V_{OH(R)}$	CANH output voltage (Recessive)	Normal mode, no load[4]	2.0	0.5*V_{CC}	3.0	V
		Standby mode, no load[4]	-0.1	-	0.1	V
$V_{OL(R)}$	CANL output voltage (Recessive)	Normal mode, no load[4]	2.0	0.5*V_{CC}	3.0	V
		Standby mode, no load[4]	-0.1	-	0.1	V
$V_{OD(D)}$	Differential output voltage (Dominant)	Normal mode				
		R_L = 50Ω to 65Ω[4]	1.5	-	3.0	V
		R_L = 45Ω to 70Ω[4]	1.4	-	3.3	V
		R_L = 2240Ω[4]	1.5	-	5.0	V
$V_{OD(R)}$	Differential output voltage (Recessive)	Normal mode, no load[4]	-50	-	50	mV
		Standby mode, no Load[4]	-0.2	-	0.2	V
V_{TXsym}	Transmitter voltage symmetry	V_{TXsym} = V_{CANH} + V_{CANL}, [3] f_{TXD} = 1MHz, R_L =60Ω, C_{SPLIT} = 4.7nF, V_{CC} = 4.75V to 5.25V [4] [5]	0.9*V_{CC}	-	1.1*V_{CC}	V

$V_{cm(step)}$	Common mode voltage step	[3]	-150	-	150	mV
$V_{cm(p-p)}$	Peak-to-peak common mode voltage	[3]	-400	-	400	mV
$I_{OSH(R)}$	CANH short-circuit output current, recessive	Normal mode, V_{CANH} = V_{CANL} = -27V to 32V	-2	-	2	mA
$I_{OSL(R)}$	CANL short-circuit output current, recessive	Normal mode, V_{CANH} = V_{CANL} = -27V to 32V	-2	-	2	mA
$I_{OSH(D)}$	CANH short-circuit output current, dominant	Normal mode, V_{CANH} = -15V to 40V, CANL open[4]	-100	-	100	mA
$I_{OSL(D)}$	CANL short-circuit output current, dominant	Normal mode, V_{CANL} = -15V to 40V, CANH open[4]	-100	-	100	mA
Bus lines; pins CANH and CANL; Receiver						
$V_{ID(R)}$	Differential input threshold voltage, recessive	-12V < V_{CANH} < 12V, -12V < V_{CANL} < 12V				
		Normal mode[4]	0.5	-	0.9	V
		Standby mode[4]	0.4	-	1.1	V
$V_{ID(D)}$	Differential input threshold voltage, dominant	-12V < V_{CANH} < 12V, -12V < V_{CANL} < 12V				
		Normal mode[4]	0.5	-	0.9	V
		Standby mode[4]	0.4	-	1.1	V
$V_{ID(hys)}$	Differential input hysteresis voltage	-12V < V_{CANH} < 12V, -12V < V_{CANL} < 12V, Normal mode	-	50	100	mV
$V_{RX(R)}$	Receiver recessive voltage	-12V < V_{CANH} < 12V, -12V < V_{CANL} < 12V				
		Normal mode[3]	-4	-	0.5	V
		Standby mode[3]	-4	-	0.4	V
$V_{RX(D)}$	Receiver dominant voltage	-12V < V_{CANH} < 12V, -12V < V_{CANL} < 12V				
		Normal mode[3]	0.9	-	9	V
		Standby mode[3]	1.1	-	9	V
$I_{LKG(OFF)}$	Power-off (unpowered) bus input leakage current	V_{CANH} = V_{CANL} = 5V, V_{CC} = V_{IO} = 0V[4]	-10	-	10	μA
R_I	Input resistance	-2V ≤ V_{CANH} ≤ 7V, -2V ≤V_{CANL} ≤ 7V [4]	25	41	50	kΩ

$R_{I(match)}$	Input resistance matching	V_{CANH} = 5V, V_{CANL} = 5V, $R_{I(match)}$=2*(R_{CANH}-R_{CANL}) /(R_{CANH}+R_{CANL})	-3	-	3	%
R_{ID}	Differential input resistance	-2V ≤ V_{CANH} ≤ 7V, -2V ≤V_{CANL} ≤ 7V, R_{ID}=R_{CANH}+R_{CANL} [4]	50	83	100	kΩ
$R_{i(dif)actrec}$	active recessive phase differential input resistance	2<V_{CANH}<VCC-2，2<V_{CANL}<VCC-2 [3]		103		Ω
C_I	Input capacitance to ground	CANH or CANL[3]	-	-	30	pF
C_{ID}	Differential input	[3]	-	-	15	pF
Temperature detection						
T_{SD}	Thermal shutdown threshold	[3]	-	193	-	°C
$T_{SD(hys)}$	Thermal shutdown hysteresis	[3]	-	11	-	°C

[1] Only NCA1462-Q1 has a VIO pin. For NCA1462N-Q1, the VIO input is internally connected to VCC.

[2] V_{IO}=V_{CC} for the version without VIO pin.

[3] Not tested in production; guaranteed by design.

[4] Required in ISO 11898-2-2024.

[5] The test circuit used to measure the bus output voltage symmetry (which includes C_{SPLIT}) is shown in Figure 6-1, Figure 6-3.

6.2. Switching Electrical Characteristics

V_{CC} =4.5V~5.5V, V_{IO}=1.7~5.5V[1], Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at V_{CC} = 5V, V_{IO} = 3.3V, R_L=60Ω, Ta = 25°C.

Symbol	*Parameters*	*Comments*	*Min*	*Typ*	*Max*	*Unit*
Driver						
$t_{d(TXD-bus, dom)}$	Delay time from TXD to bus dominant	Normal mode[3]	-	45	80	ns
$t_{d(TXD-bus, rec)}$	Delay time from TXD to bus recessive	Normal mode[3]	-	45	80	ns
$t_{d(TXD-bus, rec)end}$	Delay time from TXD to bus recessive end	Normal mode[2]	258	-	487	ns
$t_{bit(bus)}$	Transmitted recessive bit width	2Mbps, $t_{bit(TXD)}$ = 500 ns; VCC=4.75V~5.25V	490	-	510	ns
		2Mbps, $t_{bit(TXD)}$ = 500 ns; VCC=4.5V~5.5V	435	-	530	ns

		5Mbps, $t_{bit(TXD)}$ = 200 ns; VCC=4.75V~5.25V	190	-	210	ns
		5Mbps, $t_{bit(TXD)}$ = 200 ns; VCC=4.5V~5.5V	170	-	230	ns
		8Mbps, $t_{bit(TXD)}$ = 125 ns	115	-	135	ns
dv/dt	Bus differential voltage change rate	Normal mode[2]				
Receiver						
$t_{d(bus-RXD, dom)}$	Delay time from bus to RXD dominant	[3]	-	80	110	ns
$t_{d(bus-RXD, rec)}$	Delay time from bus to RXD recessive	[3]	-	80	110	ns
$t_{d(TXD-RXD, dom)}$	Delay time from TXD to RXD dominant	Normal mode[3]	-	125	190	ns
$t_{d(TXD-RXD, rec)}$	Delay time from TXD to RXD recessive	Normal mode[3]	-	125	190	ns
$t_{bit(RXD)}$	Bit time on pin RXD	2Mbps, $t_{bit(TXD)}$ = 500 ns; VCC=4.75V~5.25V	470	-	520	ns
		2Mbps, $t_{bit(TXD)}$ = 500 ns; VCC=4.5V~5.5V	400	-	550	ns
		5Mbps, $t_{bit(TXD)}$ = 200 ns; VCC=4.75V~5.25V	170	-	220	ns
		5Mbps, $t_{bit(TXD)}$ = 200 ns; VCC=4.5V~5.5V	150	-	240	ns
		8Mbps, $t_{bit(TXD)}$ = 125 ns	95	-	145	ns
CAN FD timing characteristics						
$\Delta t_{bit(bus)}$	Transmitted recessive bit width deviation	$\Delta t_{bit(bus)} = t_{bit(bus)} - t_{bit(TXD)}$ [3] [4]	-10	-	10	ns
Δt_{rec}	Receiver timing symmetry	$\Delta t_{rec} = t_{bit(RXD)} - t_{bit(bus)}$ [3] [4]	-20	-	15	ns
$\Delta t_{bit(RXD)}$	Received recessive bit width deviation	$\Delta t_{bit(RXD)} = t_{bit(RXD)} - t_{bit(TXD)}$ [3] [4]	-30	-	20	ns
Dominant time-out time; pin TXD						
$t_{to(dom)TXD}$	TXD dominant time-out	Normal mode[3]	0.8	2.8	5	ms
Bus wake-up time; pins CANH, CANL						
$t_{wake(busdom)}$	Bus dominant wake-up time	Standby mode[2] [3]	0.5	-	1.8	µs
$t_{wake(busrec)}$	Bus recessive wake-up time	Standby mode[2] [3]	0.5	-	1.8	µs
$t_{to(wake)bus}$	Bus wake-up time-out time	Standby mode[2] [3]	0.8	-	9	ms

$t_{fltr(wake)bus}$	Bus wake-up filter time	Standby mode[2] [3]	-	-	1.8	µs
Mode transition						
$t_{t(moch)}$	Mode change transition time	[2]	-	-	50	µs
$t_{startup}$	Start-up time	[2]	-	-	1.5	ms
$t_{startup(RXD)}$	RXD start-up time	After wake-up detected[2]	-	-	50	µs
IO filter; pin STB						
$t_{fltr(IO)}$	IO filter time		1	-	5	µs
Undervoltage detection						
$t_{det(uv)}$	Undervoltage detection time	[2]	-	-	30	µs
$t_{rec(uv)}$	Undervoltage recovery time	[2]	-	-	50	µs

[1] Only NCA1462-Q1 has a VIO pin. For NCA1462N-Q1, the VIO input is internally connected to VCC.

[2] Ⅰ Not VeLIO verified part number, not tested in production; guaranteed by design.

[3] Required in ISO 11898-2-2024.

[4] Required in CiA 601-4-2019; ForⅡ could pass VeLIO test part number.

6.3. Parameter Measurement Information

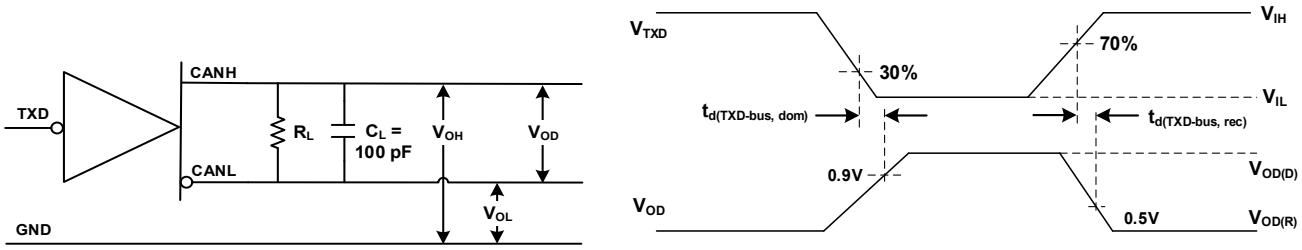


Figure 6-1 Driver Test Circuit and Voltage Waveforms

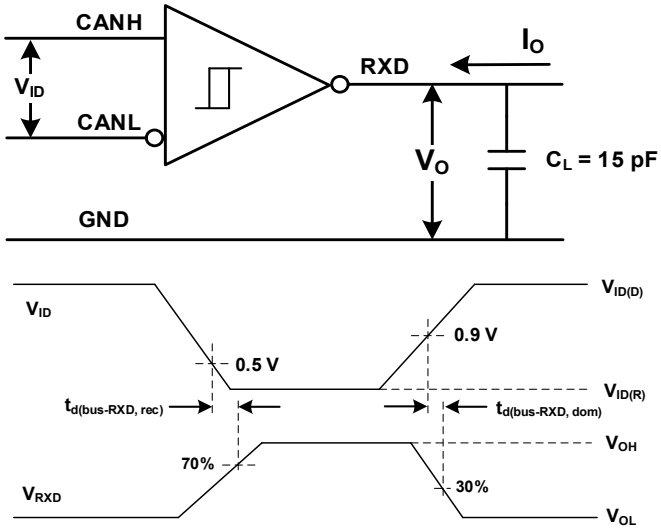


Figure 6-2 Receiver Test Circuit and Voltage Waveforms

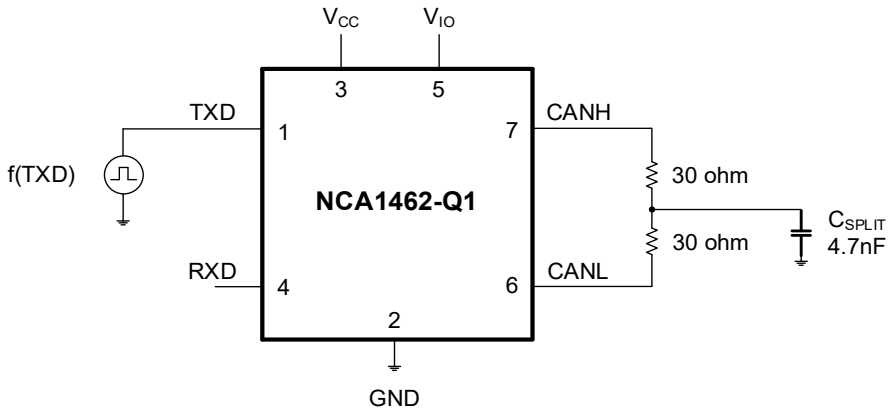


Figure 6-3 Transceiver Driver Symmetry Test Circuit

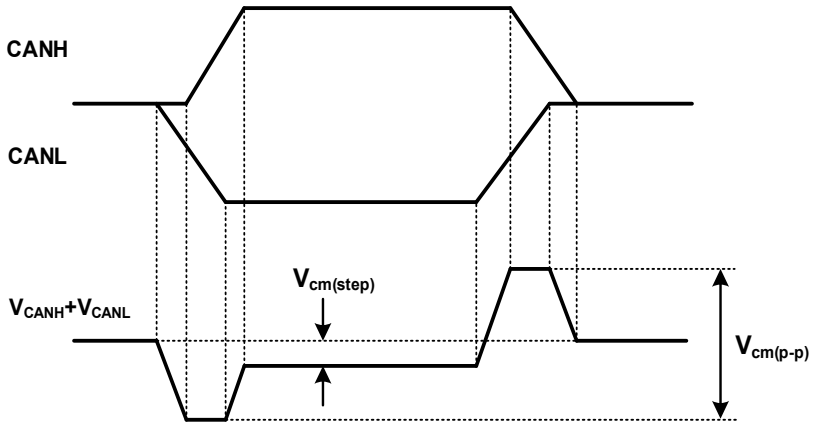


Figure 6-4 CAN bus common-mode voltage

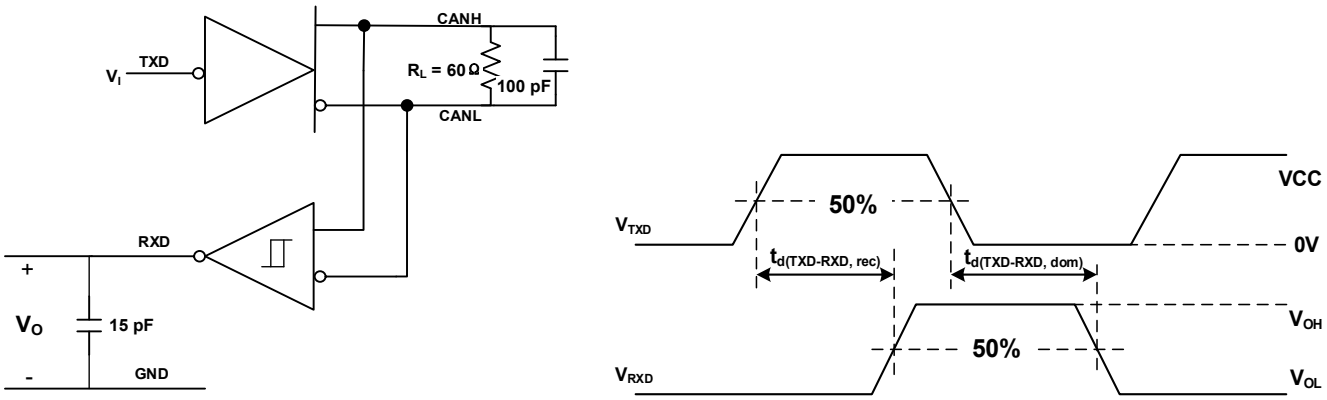


Figure 6-5 Loop Time Test Circuit and Voltage Waveforms

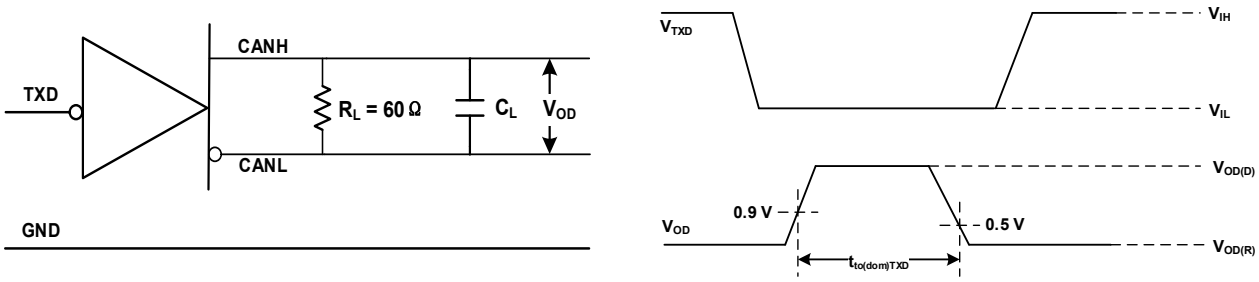


Figure 6-6 TXD Dominant Time-out Test Circuit and Voltage Waveforms

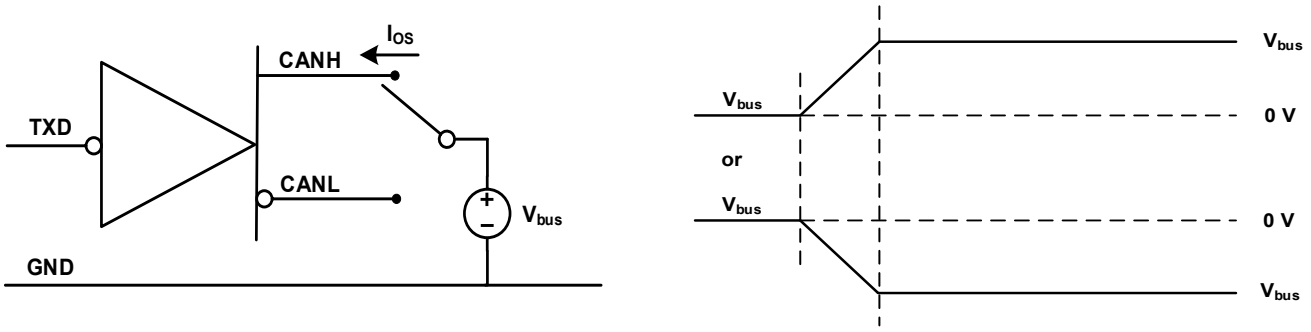


Figure 6-7 Driver Short-Circuit Current Test Circuit and Waveforms

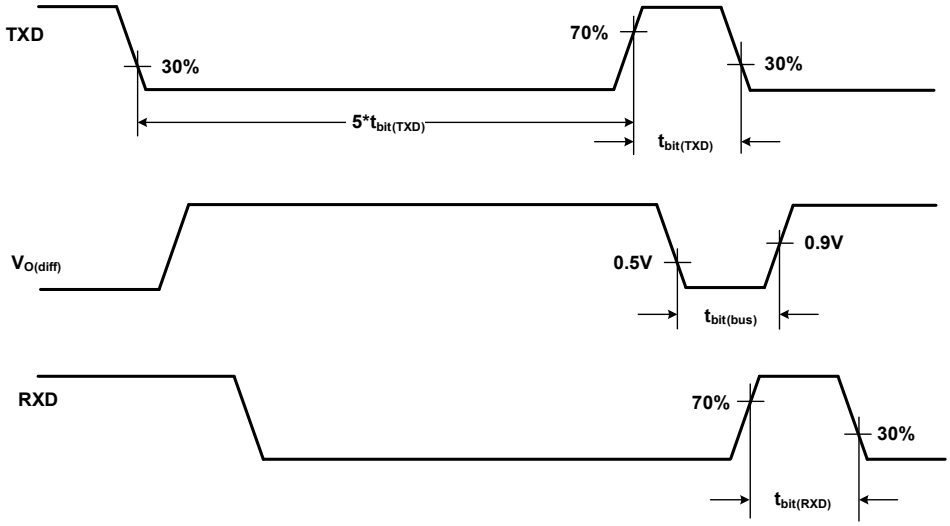
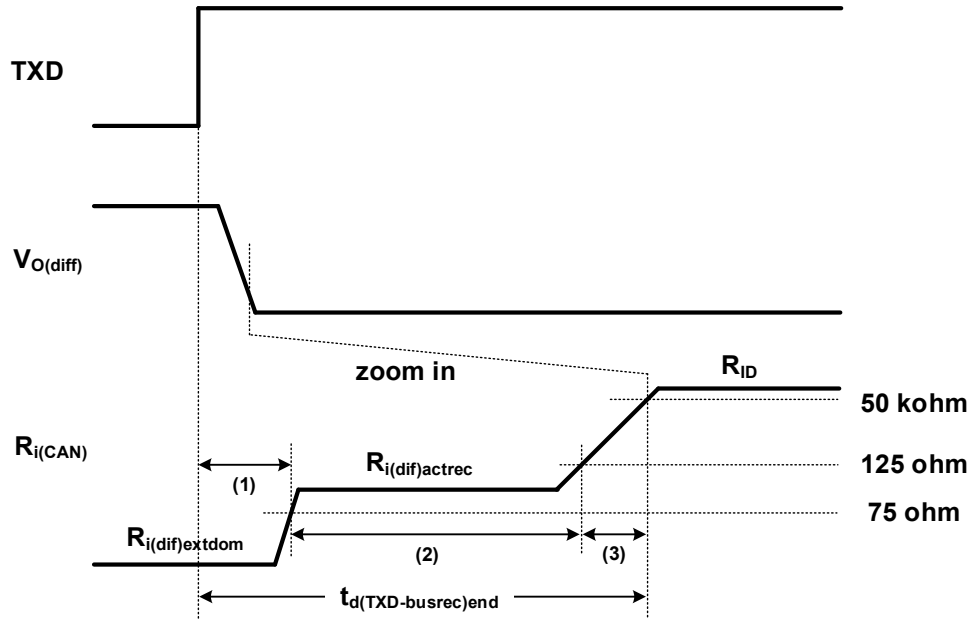


Figure 6-8 $t_{bit(RXD)}$ Test Circuit and Waveforms



(1) Extended dominant phase (2) Active recessive phase (3) Slow release phase

Figure 6-9 Impedance and Timing diagram for dominant to passive recessive transition

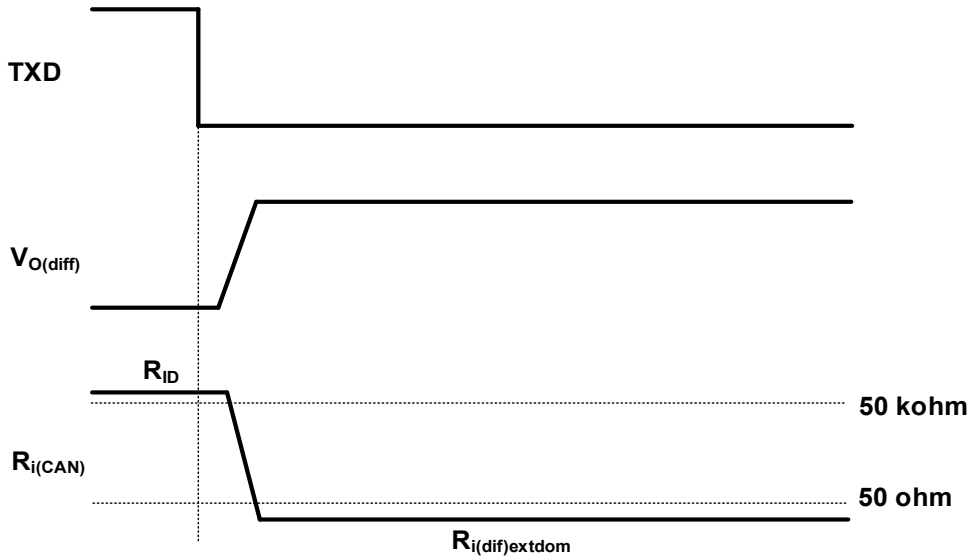


Figure 6-10 Impedance and Timing diagram for passive recessive to dominant transition

7. Function Description

7.1. Overview

The NCA1462-Q1 is a CAN transceiver which is compatible with ISO11898-2 the high-speed CAN specification, as well as CiA 601-4 the Signal Improvement Capability (SIC) specification. The CAN signal improvements significantly reduces signal ringing on the network, allowing reliable CAN FD communication at 5 Mbit/s. In addition, the NCA1462-Q1 has a much tighter bit timing symmetry, enabling CAN FD communication up to 8 Mbit/s. Meanwhile, the maximum transmission rate of the CAN bus is limited by the bus load, the quantity of nodes, the cable length, and other factors. The NCA1462-Q1 has a ±12V input common-mode range, enabling reliable communication between bus nodes with large ground potential deviations. NCA1462-Q1 has a low-current standby mode with CAN BUS waked-up capability.

Comprehensive protection features are designed to enhance the device and network robustness in harsh operating conditions. The transmit data dominant time-out function prevents the bus from lock-up by the faults on micro-controller. Moreover, the NCA1462-Q1 provides thermal protection and short-circuit protection.

7.2. Functional Block Diagram

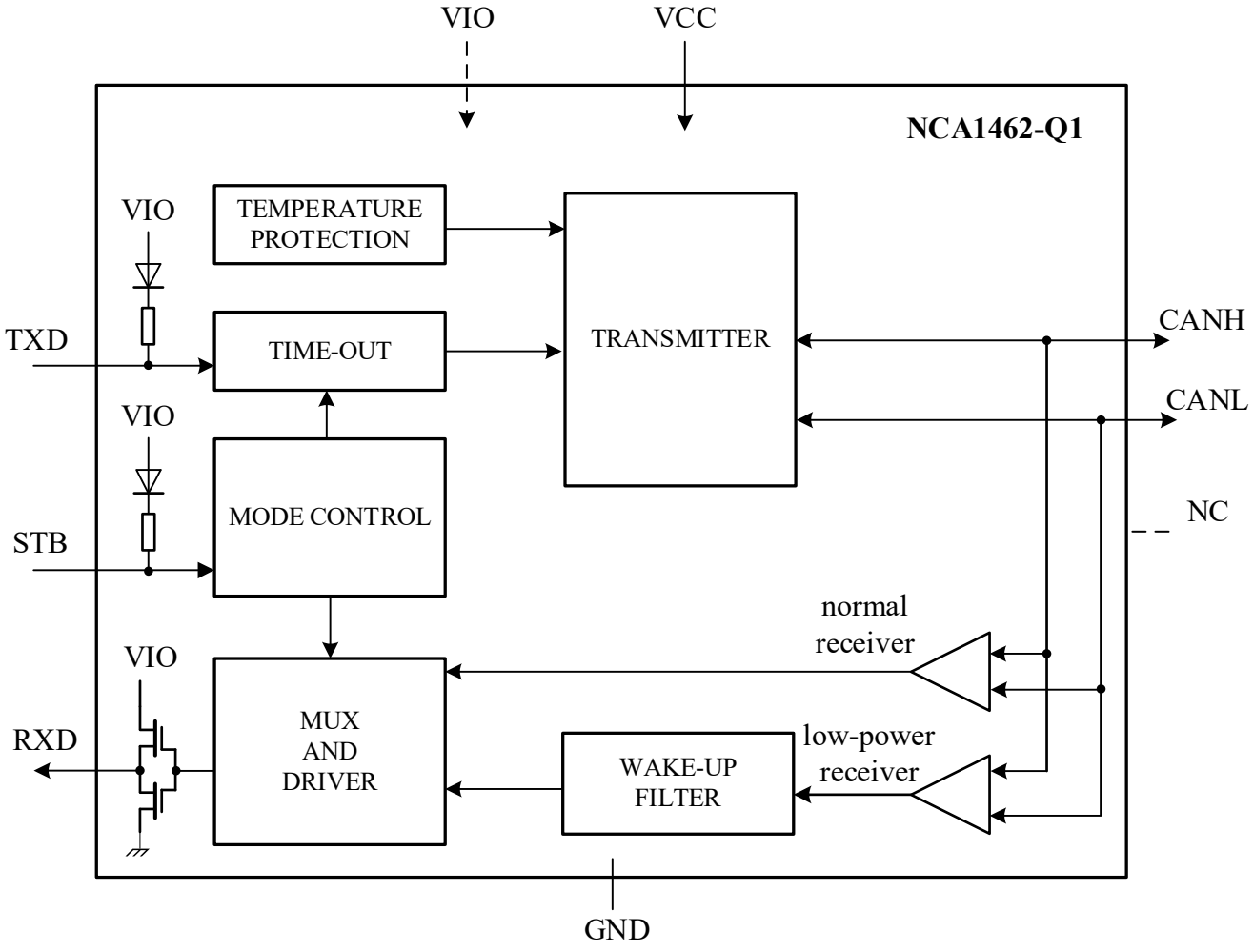


Figure 7-1 Block diagram of NCA1462-Q1

7.3. Signal Improvement

Signal improvement is to enhance the maximum data rate achievable in complex star topologies by minimizing signal ringing. The signal ringing is caused by the reflection due to the impedance mismatch of the nodes in the CAN network, which usually occurs at the dominant-to-recessive signal edge. This is due to dominant-to-recessive edge is when the driver output impedance goes to 50 kΩ and signal reflected back experiences impedance mismatch which causes ringing. NCA1462 resolves this issue by TX-based Signal improvement capability (SIC). In the active recessive phase, transmitter output impedance is 100 Ω and matches to the network characteristic impedance. After this phase is over and device goes to recessive phase, driver output impedance goes to high-Z so that reflections die down and recessive bit is clean at sampling point. This phenomenon is explained in Figure 6-9.

7.4. VIO Supply Pin

Two versions of the NCA1462-Q1 are available, only differing in the function of a single pin. Pin 5 is either a VIO supply pin or a NC pin.

Pin VIO should be connected to the microcontroller supply voltage (see Figure 8-1 and Figure 8-2). This will adjust the signal levels of pins TXD, RXD and STB to the I/O levels of the microcontroller. Pin VIO also provides the internal supply voltage for the low-power differential receiver of the transceiver. For applications running in low-power mode, this allows the bus lines to be monitored for activity even if there is no supply voltage on pin VCC.

For versions of the NCA1462N-Q1 without a VIO pin, the VIO input is internally connected to VCC. This sets the signal levels of pins TXD, RXD and STB to levels compatible with 5 V microcontrollers.

7.5. Device Operating Modes

The device has three main operating modes: Normal mode, Standby mode and Off mode. Operating mode is selected via the STB input pin. Table 7-1 shows a description of the operating modes under normal supply conditions.

Table 7-1 Operating Modes

Mode	STB pin	TXD pin	CAN driver	RXD pin
Normal	LOW	LOW	dominant	LOW
		HIGH	recessive	LOW when bus dominant
				HIGH when bus recessive
Standby	HIGH	X	GND	Follow bus when wake-up detected
				HIGH when no wake-up detected
Off [1]	X	X	Hi-Z	Hi-Z

[1] Off mode is entered when VIO voltage is below the switch-off undervoltage detection threshold.

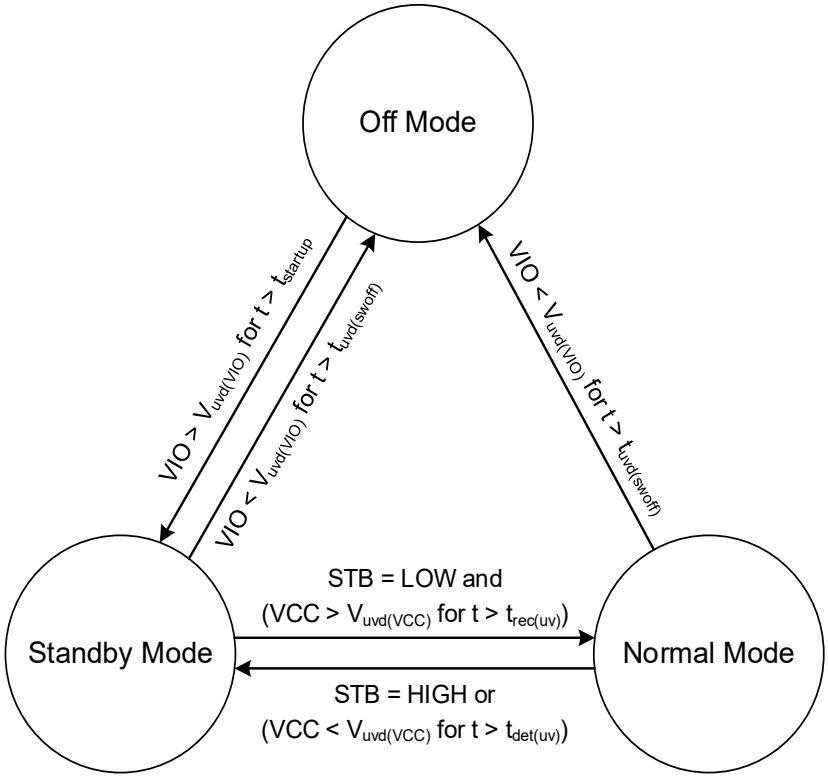


Figure 7-2 State Diagram

7.5.1.Off mode

NCA1462-Q1 switches to Off mode from any mode when the supply voltage falls below the switch-off undervoltage threshold. This is the default mode when the supply is first connected. In Off mode, the CAN pins and pin RXD are in a high-ohmic (Hi-Z) state.

7.5.2.Standby Mode

A HIGH level on pin STB selects Standby mode. In this mode, the transceiver is unable to transmit or receive data and a low-power receiver is activated to monitor the bus for a wake-up pattern. The transmitter and Normal-mode receiver blocks are switched off and the bus pins are biased to ground to minimize system supply current. Pin RXD follows the bus after a wake-up request has been detected. In NCA1462-Q1, the low-power receiver is supplied from VIO and can detect CAN bus activity when VIO is above $V_{uvd(VIO)}$. Pending wake-up events will be cleared and differential data on the bus pins converted to digital data via the low-power receiver and output on pin RXD.

When the supply voltage rises above the switch-off undervoltage detection threshold, the NCA1462-Q1 starts to boot up, triggering an initialization procedure. The NCA1462-Q1 switches to the selected mode after $t_{startup}$. A transition to Normal mode is triggered when STB is forced LOW. If VCC is below $V_{uvd(VCC)}$ when STB goes LOW, the NCA1462-Q1 will remain in Standby mode.

7.5.3.Normal Mode

A LOW level on pin STB selects Normal mode, provided the supply voltage on pin VCC is above the standby undervoltage detection threshold $V_{uvd(VCC)}$. In this mode, the transceiver can transmit and receive data via bus lines CANH and CANL. Pin TXD must be HIGH at least once in Normal Mode before transmission can begin. The differential receiver converts the analog data on the bus lines into digital data on pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME. In order to support high bit rates, especially in CAN FD systems, the Signal Improvement function largely eliminates topology-related reflections and impedance mismatches. In recessive state, the output voltage on the bus pins is VCC/2.

After entering normal mode, it is recommended to firstly pull up TXD pin to a high level for at least 200ns before communications, for fear of unwanted TXD timeout caused by unstable TXD level during the power-on phase.

7.6. Remote wake-up

The NCA1462-Q1 wakes up from Standby mode when a dedicated wake-up pattern is detected on the bus (see Figure 7-3). This filtering helps avoid spurious wake-up events. A spurious wake-up sequence could be triggered by, for example, a dominant clamped bus or by dominant phases due to noise or spikes on the bus. The wake-up pattern must have a complete dominant-recessive-dominant pattern, in which the dominant phase at least has $t_{wake(busdom)}$ and the recessive phase at least has $t_{wake(busrec)}$, otherwise it will be ignored.

At the same time, the complete dominant-recessive-dominant pattern must be received within $t_{to(wake)bus}$ to prevent recognition as an invalid signal and thus resetting the internal wake-up logic. The complete wake-up pattern then needs to be retransmitted to trigger a wake-up event. Pin RXD remains HIGH until the wake-up event has been triggered.
After a wake-up sequence has been detected, the NCA1462-Q1 will remain in standby mode with the bus signals reflected on RXD after $t_{startup(RXD)}$. During $t_{startup(RXD)}$, the low-power receiver is on but pin RXD is not active (i.e. HIGH/recessive). The first dominant pulse width ≥ $t_{fltr(wake)bus}$ that ends after $t_{startup(RXD)}$ will trigger RXD to go LOW/dominant. Note that dominant or recessive phases lasting less than $t_{fltr(wake)bus}$ will not be detected by the low-power differential receiver and will not be reflected on RXD in Standby mode.

A wake-up event is not flagged on RXD if any of the following events occurs while a valid wake-up pattern is being received:

- The NCA1462 switches to Normal mode.
- The complete wake-up pattern was not received within $t_{to(wake)bus}$.
- A VCC or VIO undervoltage is detected.

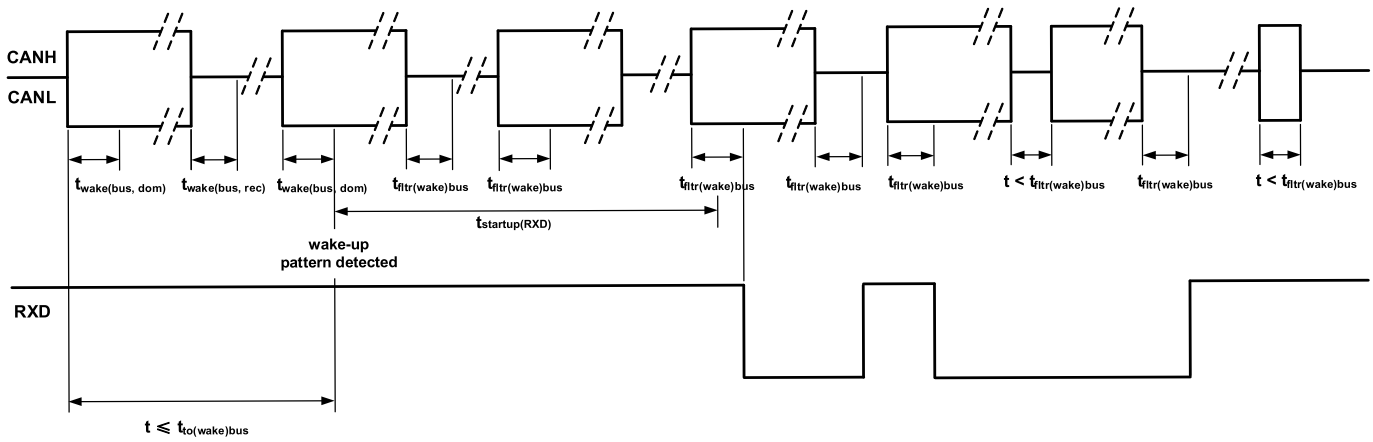


Figure 7-3 Wake-Up Timing

7.7. Fail-safe features

7.7.1.TXD Dominant Time-Out Function (TXD DTO)

A 'TXD dominant time-out' timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD. If the duration of the LOW level on pin TXD exceeds the internal timer value $t_{to(dom)TXD}$, the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD. The TXD dominant time-out time also defines the minimum possible bit rate of 10 kbit/s.

7.7.2.Internal Biasing of TXD and STB Input Pins

Pins TXD and STB have internal pull-ups to VIO to ensure a safe, defined state, in case one or both of these pins are left floating. Pull-up currents flow in these pins in all states; both pins should be held HIGH in Standby mode to minimize standby current.

7.7.3.Undervoltage Detection on Pins VCC and VIO

The supply terminals have undervoltage detection that places the device in protected mode. This protects the bus during an undervoltage event on either the VCC or VIO supply terminals. When VCC drop below the VCC undervoltage detection level $V_{uvd(VCC)}$, the transceiver will switch to Standby mode. The logic state of pin STB will be ignored until VCC has recovered. When VIO drop below the VIO undervoltage detection level $V_{uvd(VIO)}$, the transceiver will switch off and disengage from the bus (zero load) until VIO has recovered.

After an undervoltage condition is cleared and the supplies have returned to valid levels, the device typically resumes normal operation within 50 µs.

Table 7-2 Undervoltage Lockout 5V Only Devices (NCA1462N-Q1)

VCC	Device State	Bus Output	RXD
>UV_{VCC}	Normal	Per TXD	Mirrors Bus[1]
<UV_{VCC}	Off	High Impedance	High Impedance

[1] Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

Table 7-3 Undervoltage Lockout I/O Level Shifting Devices (NCA1462-Q1)

VCC	VIO	Device State	Bus Output	RXD
>UV_{VCC}	>UV_{VIO}	Normal	Per TXD	Mirrors Bus[1]
<UV_{VCC}	>UV_{VIO}	Standby Mode	GND	Bus Wake RXD Request[2]
>UV_{VCC}	<UV_{VIO}	Off	High Impedance	High Impedance
<UV_{VCC}	<UV_{VIO}	Off	High Impedance	High Impedance

[1] Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

[2] Refer to Section 7.6.

7.7.4.Unpowered Device

The device is designed to be 'ideal passive' or 'no load' to the CAN bus if it is unpowered. The bus terminals (CANH, CANL) have extremely low leakage currents when the device is unpowered to avoid loading down the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains in operation. The logic terminals also have extremely low leakage currents when the device is unpowered to avoid loading down other circuits that may remain powered.

7.7.5.Over-Temperature Protection (OTP)

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature T_{SD}, the output drivers will be disabled until the virtual junction temperature becomes lower than T_{SD} and TXD becomes recessive again. By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.

7.7.6.Short circuit protection

The current limiting circuit of the CANH and CANL can protect the transceiver from damage when they are short to GND or a supply voltage during communication. If the device heats up to over temperature threshold due to a continuous short on the CANH or CANL, the internal overtemperature protection switches off the bus transmitter.

8. Application Information

8.1. Typical Application

The NCA1462-Q1 requires a 0.1 μF bypass capacitors between VCC and GND. The capacitor should be placed as close as possible to the package. The Figure 8-1 and Figure 8-2 are the typical applications of NCA1462-Q1.

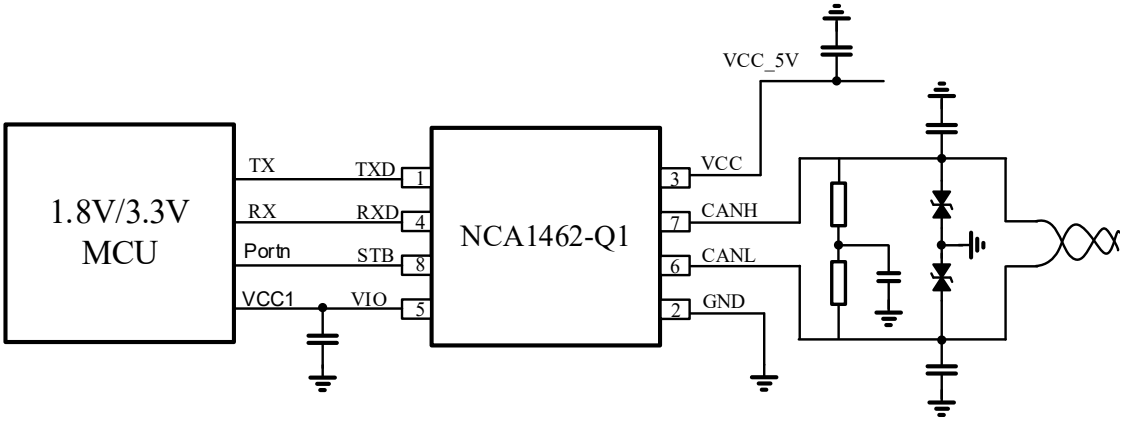


Figure 8-1 Typical CAN Bus Application Using 1.8V/3.3V CAN Controller

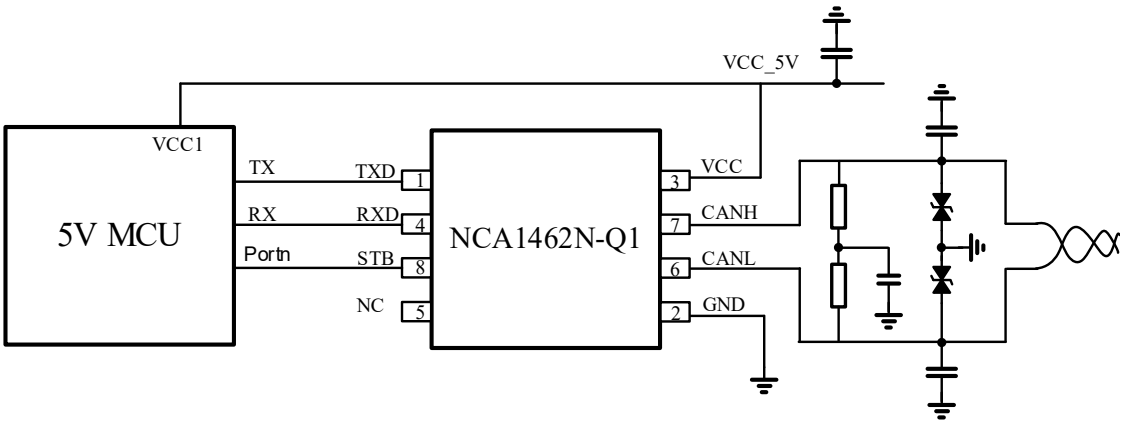
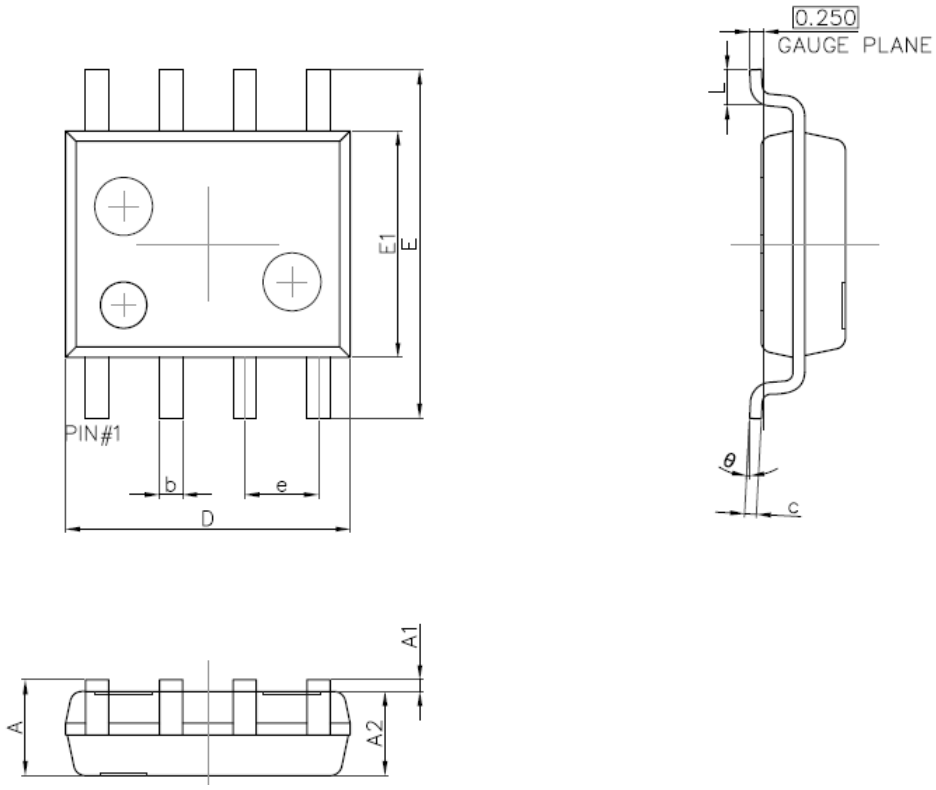


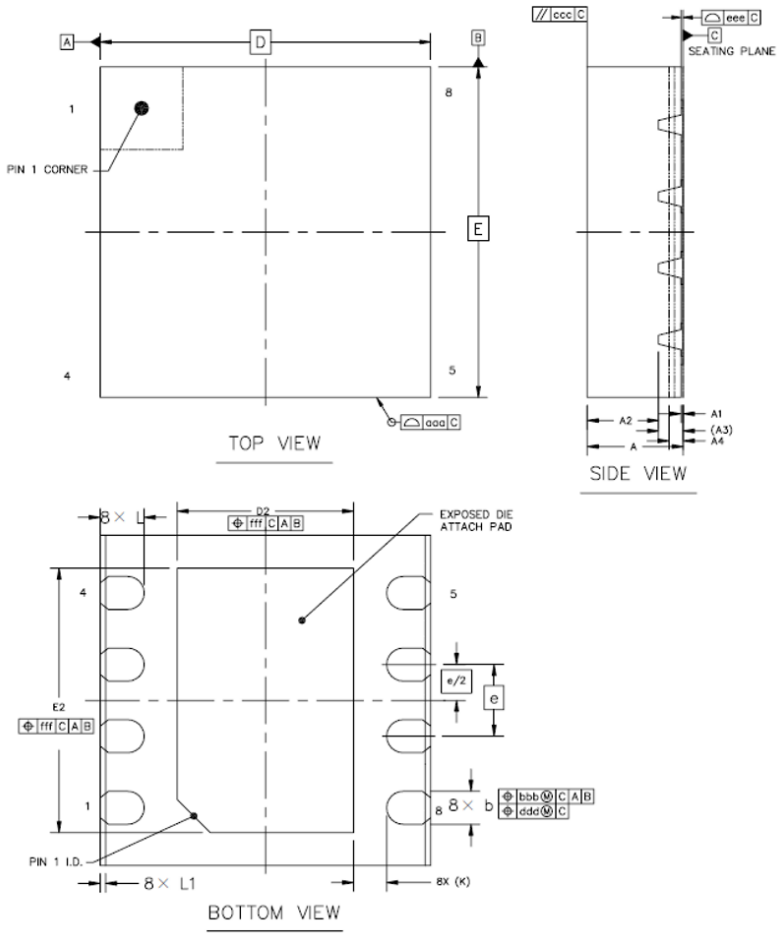
Figure 8-2 Typical CAN Bus Application Using 5V CAN Controller

9. Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.450	1.750	0.057	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Figure 9-1 SOP8 Package Shape and Dimension



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.80	0.85	0.90
STAND OFF		A1	0	0.02	0.0500
MOLD THICKNESS		A2	---	0.6	---
L/F THICKNESS		A3		0.203 REF	
SIDE WETTABLE DEPTH		A4	0.075	---	0.18
BODY SIZE	X	D		3 BSC	
	Y	E		3 BSC	
LEAD WIDTH		b	0.25	0.30	0.35
LEAD PITCH		e		0.65 BSC	
EP SIZE	X	D2	1.5	1.6	1.7
	Y	E2	2.3	2.4	2.5
LEAD LENGTH		L	0.35	0.4	0.45
SIDE WETTABLE WIDTH		L1	0.01	---	0.09
LEAD TIP TO EXPOSED PAD EDGE		K		0.3 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1000	
MOLD FLATNESS		ccc		0.1000	
COPLANARITY		eee		0.0800	
LEAD OFFSET		bbb		0.1000	
		ddd		0.0500	
EXPOSED PAD OFFSET		fff		0.1000	

Figure 9-2 DFN8 Package Shape and Dimension

10. Order Information

Part Number	Operation Temperature	MSL	Package Type	SPQ
NCA1462-Q1SPR[I]	-40 to 125°C	3	SOP8	2500
NCA1462-Q1DNR[I]	-40 to 125°C	2	DFN8	6000
NCA1462N-Q1SPR[I]	-40 to 125°C	3	SOP8	2500
NCA1462N-Q1DNR[I]	-40 to 125°C	2	DFN8	6000
NCA1462-Q1SPRH[II]	-40 to 125°C	3	SOP8	2500
NCA1462-Q1DNRH[II]	-40 to 125°C	2	DFN8	6000
NCA1462N-Q1SPRH[II]	-40 to 125°C	3	SOP8	2500
NCA1462N-Q1DNRH[II]	-40 to 125°C	2	DFN8	6000

[I] Not VeLIO verified part number

[II] Could pass VeLIO test part number

11. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents
NCA1462-Q1	Click here	Click here	Click here

12. Tape and Reel Information

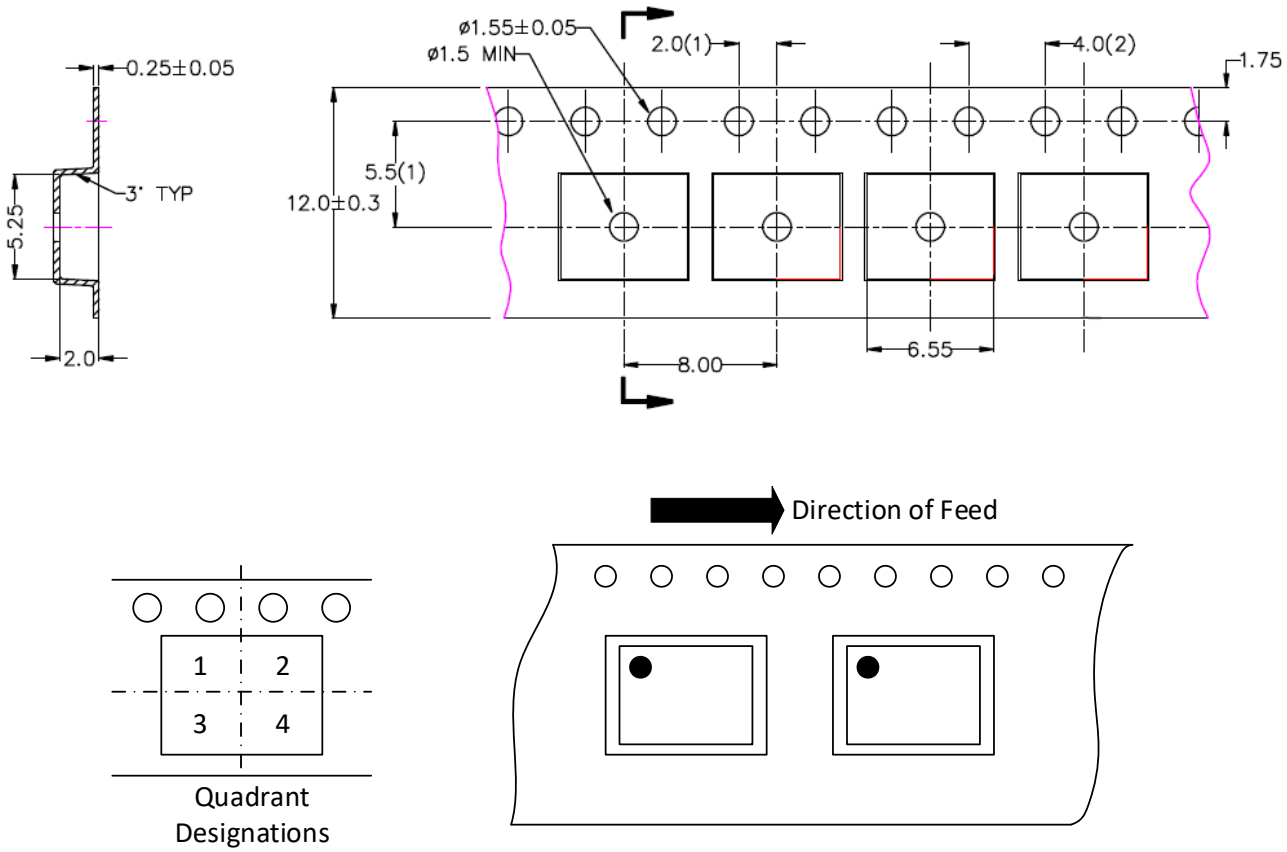
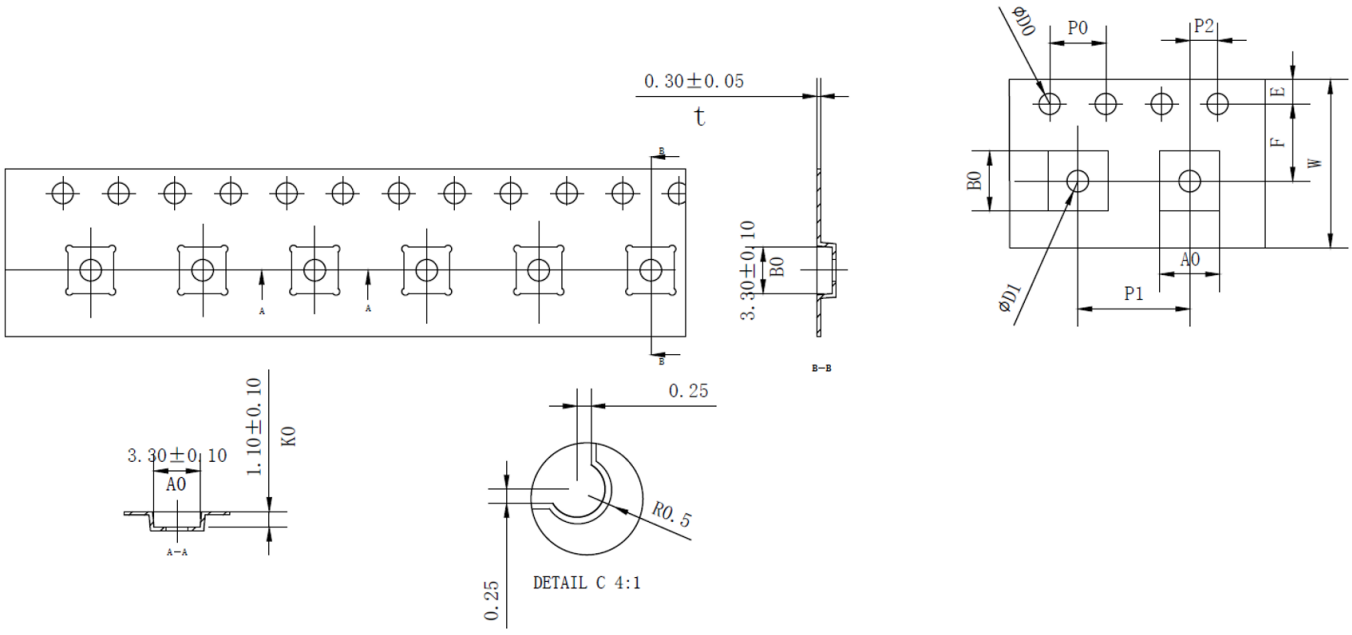


Figure 12-1 Tape Information of SOP8



W	E	F	D0	D1	P0	P2	10P0	P1	A0	A1	B0	B1	K0	K1	t
12.00 ±0.10	1.75 ±0.10	5.50 ±0.10	1.55 ±0.05	1.55 ±0.05	4.00 ±0.10	2.00 ±0.10	40.00 ±0.20	8.00 ±0.10	3.30 ±0.10		3.30 ±0.10		1.10 ±0.10		0.30 ±0.05

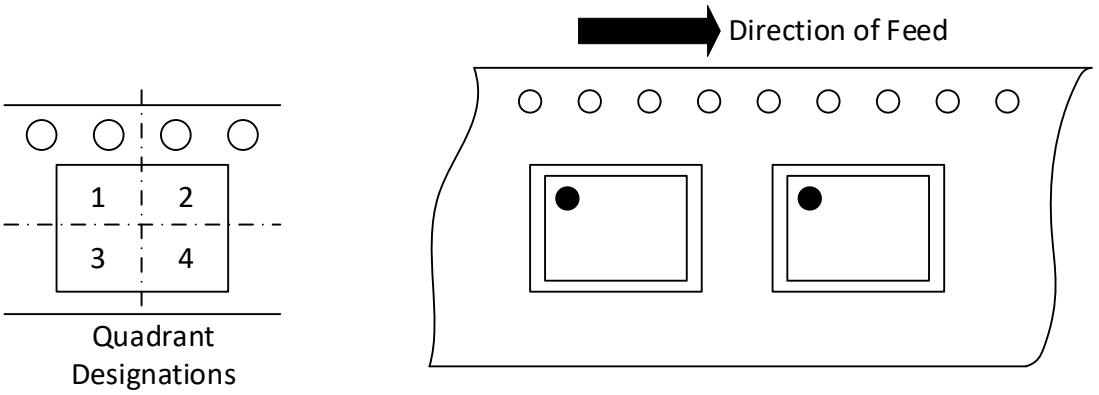
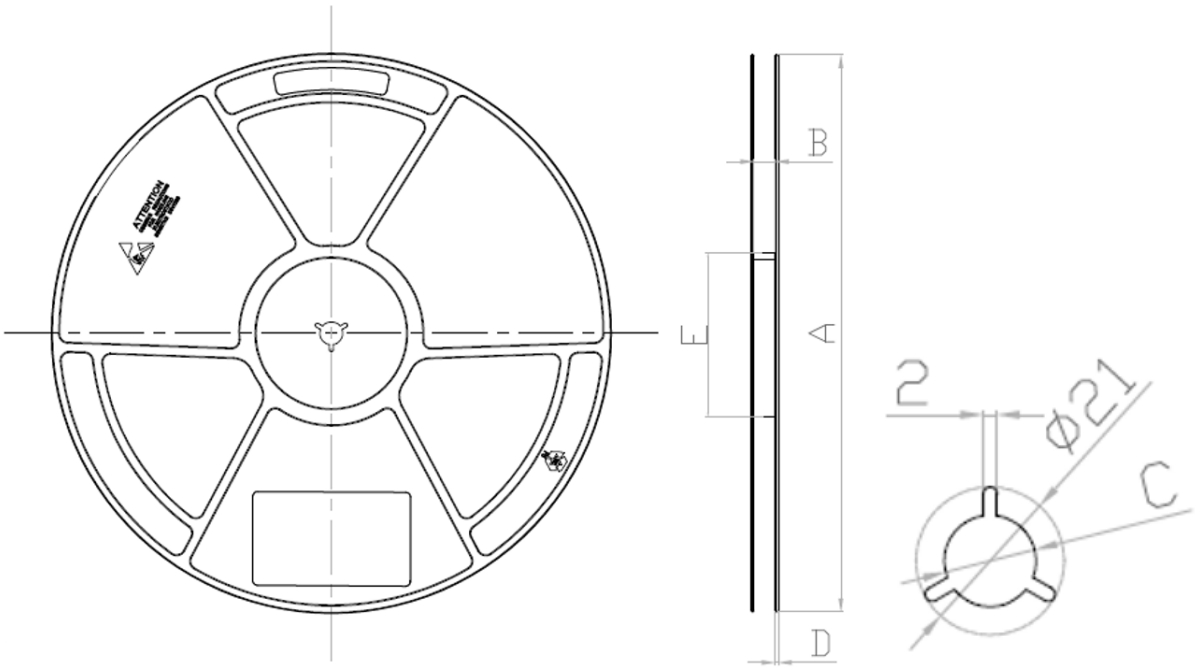


Figure 12-2 Tape Information of DFN8



规格	A	B	C	D	E
12W	330±2.0	12.5±1.00	13.5±1.00	1.9±1.00	100±1.00
16W	330±2.0	16.5±1.00	13.5±1.00	1.9±1.00	100±1.00
24W	330±2.0	24.5±1.00	13.5±1.00	1.9±1.00	100±1.00
32W	330±2.0	32.5±1.00	13.5±1.00	1.9±1.00	100±1.00
44W	330±2.0	44.5±1.00	13.5±1.00	1.9±1.00	100±1.00

Figure 12-3 Reel Information of SOP8 and DFN8

13. Revision History

Revision	Description	Date
1.0	Initial Version.	2024/9/30
1.1	Add the description of short circuit protection, Add system-level ESD parameters and modified SOP8 carrier information. Adjust SIC time	2024/12/24
1.12	Correct common mode voltage information error on page 1 and page17; Add 'H' version device could pass VeLIO test part number and modify ESD parameters; Add the DFN8 diagram and modify the diagram notes; Add dv/dt parameter for VeLIO version Device; Add Order Information of 'H' version device	2025/10/24

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