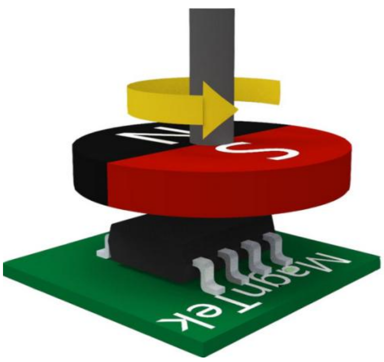
MT6511

AEC Qualified | ISO26262 ASIL Ready | MagnTek | Now Part of NOVOSENSE

Magnetic Angle Sensor IC for Automotive Application

Features and Benefits

- ISO26262 ASIL Ready， SEooC ASIL-B for Single Die SOP-8 Package, ASIL-B(D) for Dual Die TSSOP-16 Package
- Selectable Analog (Ratio metric), PWM (Pulse Width Modulation) or Switch Output (SWO)
- Programmable Linear Transfer Characteristic (8 Multi-points or 16 Segments Piece-Wise-Linear)
- ABZ Incremental Output Resolution 1~4,096 Pulses per Revolution User Programmable
- UVW Output Resolution 1~16 Pole-Pairs per Revolution User Programmable
- SENT Output Compatible with SAE J2716
- Output One-Wire Interface or 3-Wire SPI Interface
- 48-bit Unique Chip ID Number
- Immunity to Stray Magnetic Field Interference, MFI testing can pass 4000 A/M
- SOP-8/TSSOP-16 Package RoHS Compliant



SOP-8

TSSOP-16

Applications

- Throttle Position Sensor
- Pedal Position Sensor
- Steering Angle Sensor for EPS
- Ride Height Position Sensor
- Float-Level Sensor

General Description

Magntek’s 2nd generation automotive grade angle sensor IC MT6511 is based on differential Hall technology. It contains 4 Hall plates that sense the differential magnetic field vertical to chip surface from a diametrically-magnetized round magnet and generate sine/cosine outputs that are used to calculate the angle between the magnetic field and the chip.

The MT6511 can provide Analog, PWM or SENT interface which is programmable. And the output characteristic of all these three types could be programmed with free 8-points or 16-segments (17-points) piece-wise-linear.

The incremental ABZ output mode is available in this sensor IC series, the maximum resolution is 4,096 pulses or 16,384 steps per revolution user programmable. And UVW output with 1~16 pole-pairs can be configured.

Also 3-Wire SPI and OWI (output one wire interface) are provided to read the 0~360° raw angle data or to program the internal registers of MT6511. A programmable Switch Output (SWO) is provided for special applications.

MT6511 for Automotive application offers a series of safety functions to support ASIL B (Single Die) and ASIL-B(D) (Dual Die) system requirements.

Table of Contents

1. Pin Configuration

1. 1 SOP-8 Package

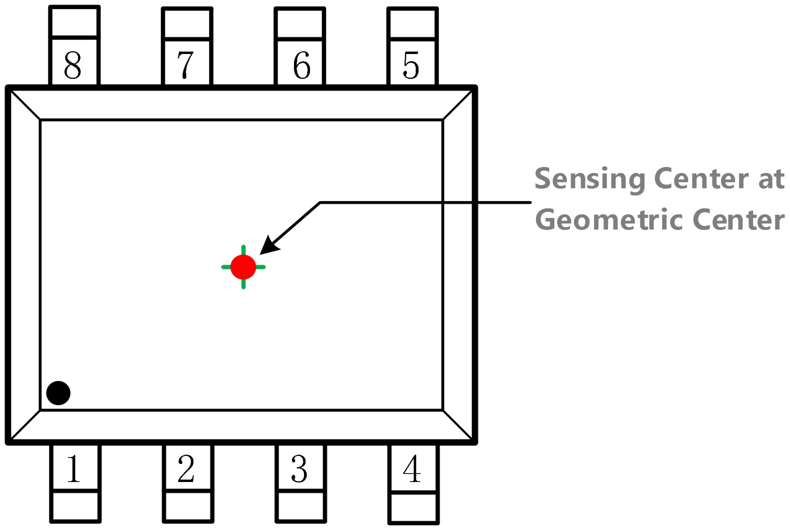


Figure-1: Pin Configuration for SOP-8 Package

Table-1: SOP-8 Package Pin List

Name	Number	Type	Description
VDD	1	Supply	5V Supply
CSN	2	Digital GPIO	SPI Chip Select
SWO	3	Digital GPIO	Switch Output, Incremental Signal B or V
SCK	4	Digital GPIO	SPI Clock
OUT	5	Analog Output	Analog/PWM /OWI/SENT, Incremental Signal A or U
SDAT	6	Digital GPIO	SPI Bi-direction Data Line
TEST	7	Digital GPIO	MagnTek Test Pin or Incremental Signal Z or W
VSS	8	Ground	Ground

1.2 TSSOP-16 Package

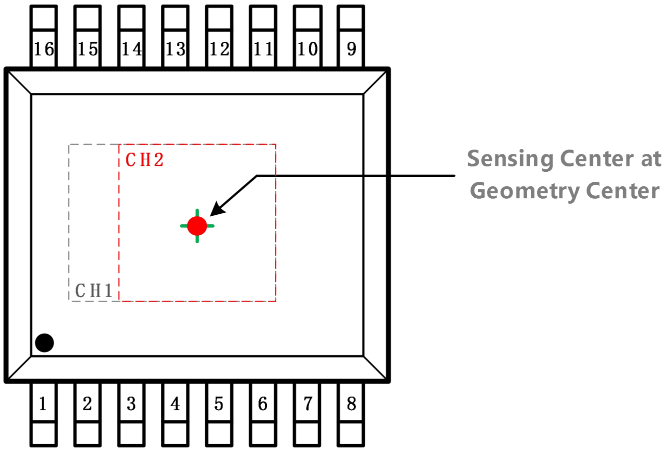


Figure-2: Pin Configuration for TSSOP-16 Package
(CH1&CH2 are the Symbols for the Two Dies in the Same Package)

Table-2: TSSOP-16 Package Pin List

Name	Number	Type	Description
TEST_CH1	1	Digital GPIO	CH1 MagnTek Test Pin or Incremental Signal Z or W
VSS_CH1	2	Ground	CH1 Ground
VDD_CH1	3	Supply	CH1 5V Supply
CSN_CH1	4	Digital GPIO	CH1 SPI Chip Select
SWO_CH2	5	Digital GPIO	CH2 Switch Output, Incremental Signal B or V
OUT_CH2	6	Analog Output	CH2 Analog/PWM /OWI/SENT, Incremental Signal A or U
SCK_CH2	7	Digital GPIO	CH2 SPI Clock
SDAT_CH2	8	Digital GPIO	CH2 SPI Bi-direction Data Line
TEST_CH2	9	Digital GPIO	CH2 MagnTek Test Pin or Incremental Signal Z or W
VSS_CH2	10	Ground	CH2 Ground
VDD_CH2	11	Supply	CH2 5V Supply
CSN_CH2	12	Digital GPIO	CH2 SPI Chip Select
SWO_CH1	13	Digital GPIO	CH1 Switch Output, Incremental Signal B or V
SCK_CH1	14	Digital GPIO	CH1 SPI Clock
OUT_CH1	15	Analog Output	CH1 Analog/PWM /OWI/SENT, Incremental Signal A or U
SDAT_CH1	16	Digital GPIO	CH1 SPI Bi-direction Data Line

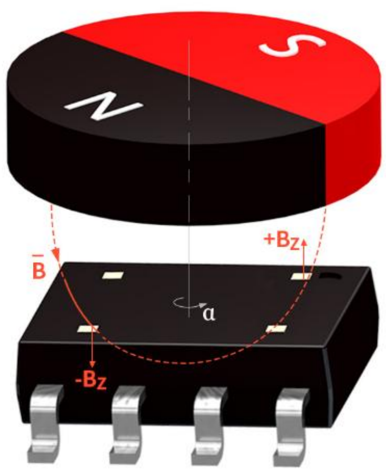
2. Part Number List

MT6511CT has a single die in SOP-8 package and MT6511GT has two dies in TSSOP-16 package. Both MT6511CT and MT6511GT are in tape & reel pack (3000pcs/reel).

Table-3: Part Number List

Part Number	Single/Dual	Magnetic Field	Output
MT6511CT-STD	Single Die	10mT~50mT	Analog
MT6511GT-STD	Dual Dies	10mT~50mT	Analog
MT6511CT-STW	Single Die	20mT~90mT	Analog
MT6511GT-STW	Dual Dies	20mT~90mT	Analog
MT6511CT-PMP	Single Die	10mT~50mT	PWM(Push-Pull)
MT6511GT-PMP	Dual Dies	10mT~50mT	PWM(Push-Pull)
MT6511CT-STP	Single Die	10mT~50mT	SENT(Push-Pull)
MT6511GT-STP	Dual Dies	10mT~50mT	SENT(Push-Pull)
MT6511CT-SPI	Single Die	10mT~50mT	SPI
MT6511GT-SPI	Dual Dies	10mT~50mT	SPI

The simulation result of vertical component magnetic field strength B_Z of common NdFeB magnets (N35) and common ferrite magnets (Y30BH) on the chip surface varies with the change of magnets and chip airgap (AG) is shown in Figure-3



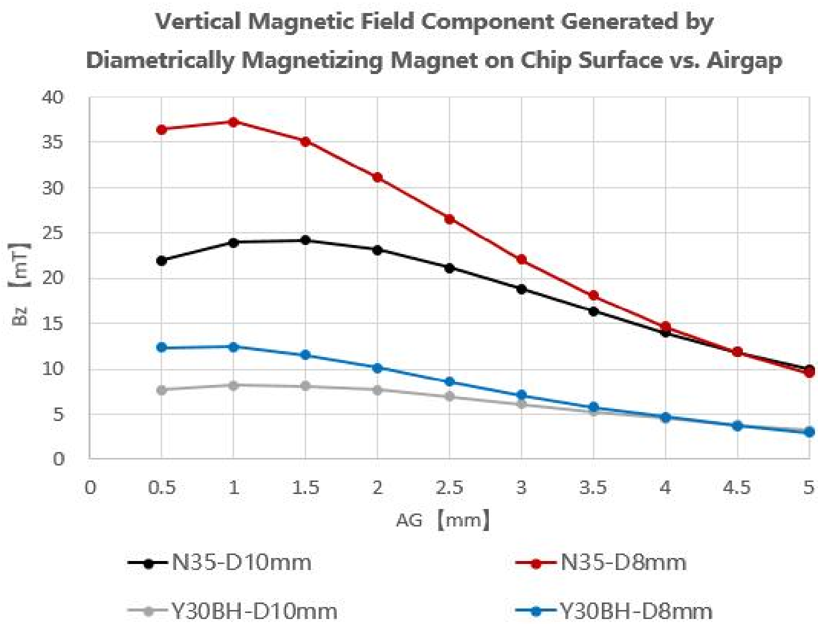


Figure-3: Vertical Magnetic Field Component B_Z vs. Airgap

3. Functional Description

The MT6511 is manufactured in a CMOS standard process, the integrated magnetic sensing element array delivers a voltage representation of the magnetic field at the surface of the IC. Figure-4 shows a simplified block diagram of the chip, consisting of the magnetic sensing element realized by four horizontal Hall plates to generate cosine and sine signals, gain stages, analog-to-digital converters (ADC) for signal conditioning, a digital signal processing (DSP) unit for angle calculation and digital-to-analog convert (DAC) to generate linear voltage output. Other supporting blocks such as LDO, EEPROM etc. are also included. An on-chip temperature sensor also be designed to compensate the temperature drift of INL.

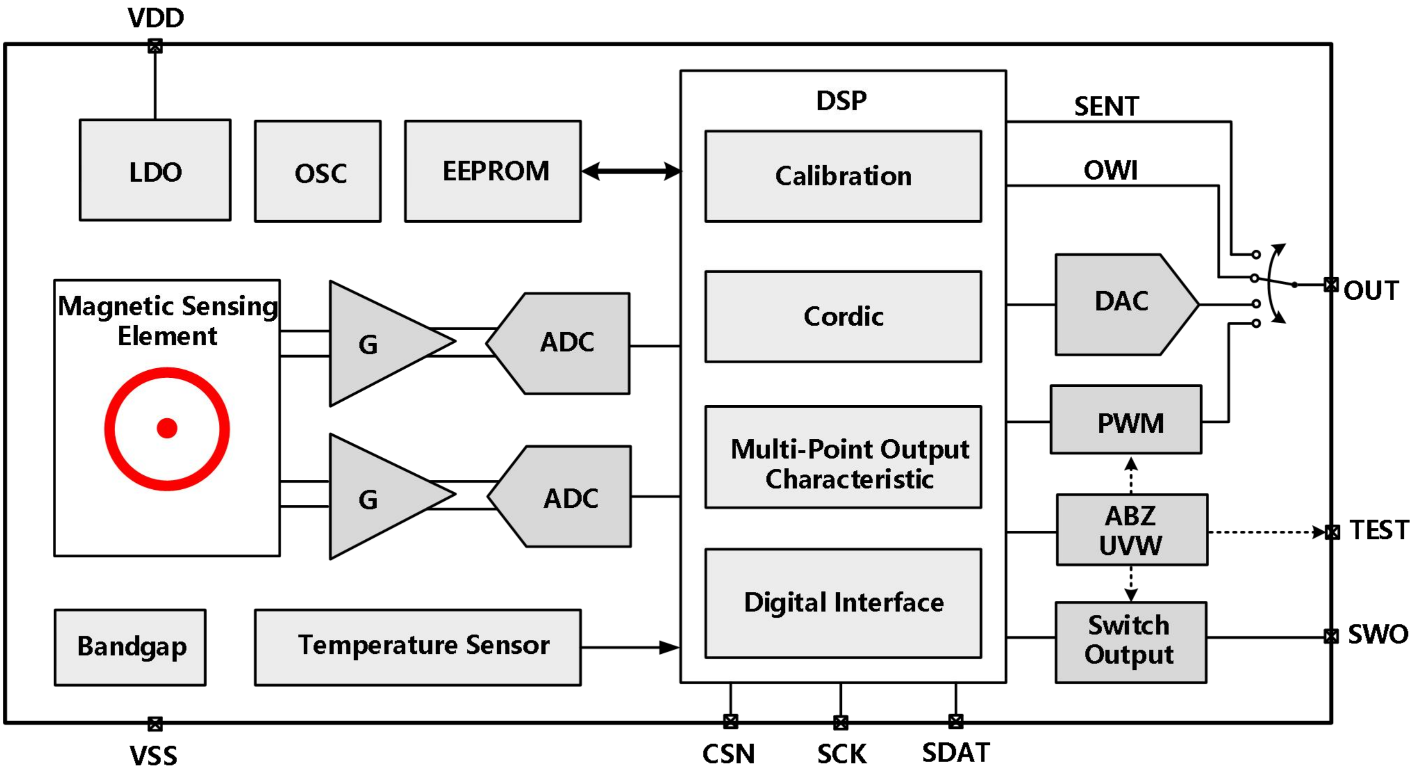


Figure-4: Block Diagram

4. Absolute Maximum Ratings (Non-Operating)

Table-4: Non-Operating Maximum Ratings

Description	Symbol	Min.	Max.	Unit	Notes
DC Voltage at Pin VDD	VDD	-18	30	V	Supply Voltage
DC Voltage at Pin OUT	V_{OUT}	-0.3	30	V	Pin: OUT
DC Voltage at All Other Pins		-0.3	6.5	V	Pin: SWO, CSN, SDAT, SCK, TEST
Output Current	I_{OUT}	-25	25	mA	Pin: OUT (Analog Mode)
		-50	50	mA	Pin: OUT (PWM/SENT Mode)
		-30	30	mA	Pin: SWO, CSN, SDAT, SCK, TEST
Ambient Temperature	T_{AMB}	-40	150	℃	-
Junction Temperature	T_J	-40	160	℃	-
Storage Temperature	$T_{Storage}$	-55	150	℃	-
ESD Voltage: Human Body Mode	V_{HBM}	-	±6.0	kV	AEC-Q100-002
ESD Voltage: Charge Device Mode	V_{CDM}	-	±1.0	kV	AEC-Q100-011

1) Consider current consumption and mounting situation for T_{AMB} and in relation to T_J
2) Please contact MagnTek for other temperature requirements

Operation beyond these limits may cause permanent damage to the device. Even if it does not lead to destruction, reliability and life may be adversely affected. Normal operation is not guaranteed at these extremes.

5. Electrical Characteristics

Operation conditions: T_{AMB}=-40 to 150℃, VDD=4.5~5.5V unless otherwise noted.

Table-5: Electrical Characteristics

Symbol	Description	Conditions/Notes	Min.	Typ.	Max.	Unit
VDD	Supply Voltage	-	4.5	5.0	5.5	V
IDD	Supply Current	Single Die with Analog Output Enabled	8	11	14	mA
		Single Die with Analog Output Disabled	7	10	13	mA
		Dual Die with Analog Output Enabled	16	22	28	mA
		Dual Die with Analog Output Disabled	14	20	26	mA
V_{TH_UV}	Undervoltage detection		4.0	4.15	4.30	V
V_{HYS_UV}	Undervoltage Hysteresis		-	180	-	mV
T_{SU} (Start-up Time)	Output Settle to Current Temperature (Default 27℃)	with Temperature Compensation	-	32	-	ms
	Analog Output Mode (Exclude Slew Rate Effect)	without Temperature Compensation	-	0.66	-	ms
	PWM Output Mode		-	1.1	-	ms
	SENT Output Mode		-	3.3	-	ms
	ABZ/UVW Output Mode		-	0.65	-	ms
General Timing Specification						
ΔFS	Clock Frequency Variation	Overall VDD and T_{AMB}	-5	-	5	%
T_{DELAY}	Propagation Delay for Constant Rotation Speed		-	50	-	us
T_{STEP}	Step Response Time (Exclude Slew Rate Effect)		-	650	-	us
Analog Output Specification						
FR	Analog Output Refresh Rate	-	-	8	-	kHz
I_{SHORT_ANA}	Analog Output Short Current with On-chip Over Current Protection	Vout=0V	-	-18	-	mA
		Vout=VDD	-	18	-	

Operation conditions: T_{AMB}=-40 to 150℃, VDD=4.5~5.5V unless otherwise noted.

Symbol	Description	Conditions/Notes	Min.	Typ.	Max.	Unit
R_L	Output Load	Pull-down to Ground	5	-	-	kΩ
		Pull-up to VDD	5	-	-	
VSAT_LO	Analog Output Low Saturation Level	Pull-up R_L≥5KΩ	-	2	4	%VDD
VSAT_HI	Analog Output High Saturation Level	Pull-down R_L≥5KΩ	96	98	-	%VDD
CLAMP_LO	Output Clamp Low Level	Programmable	2	-	-	%VDD
CLAMP_HIGH	Output Clamp High Level	Programmable	-	-	98	%VDD
SR	Analog Output Slew Rate	C_L≤10nF	400	-	-	V/ms
		C_L≤100nF	120	-	-	
R_{OUT}	Analog Output Resistance	DC	-	15	35	Ω
PWM/SENT Output Specification						
F_{PWM}	PWM Frequency	Programmable	-5%	125 ~ 2000	+5%	Hz
T_{TICK}	SENT Tick Time	Programmable	-	1.5 3.0 6.0	-	us
I_{SHORT_PWM}	PWM/SENT Output Short Current with On-chip Over Current Protection	V_{OUT}=0V	-	-50	-	mA
		V_{OUT}=VDD	-	50	-	
PWM_VOH SENT_VOH	PWM/SENT Output Voltage High Level	Push-pull (I_{OUT}=2mA)	VDD-0.3	-	-	V
PWM_VOL SENT_VOL	PWM/SENT Output Voltage Low Level	Push-pull (I_{OUT}=-2mA)	-	-	0.3	V
R_{PU}	PWM/SENT External Pull-up Resistor for Open-Drain Mode	**Keep external VCC≤5V which R_{PU} connected to**		1.0		KΩ

Operation conditions: T_{AMB}=-40 to 150℃, VDD=4.5~5.5V unless otherwise noted.

Symbol	Description	Conditions/Notes	Min.	Typ.	Max.	Unit
T_{RISE}	PWM/SENT Output Rising Time	Push-pull, C_L=1nF	-	-	0.5	us
		Open-Drain, R_{PU}=1.0K, C_L=1nF	-	-	3	us
T_{FALL}	PWM/SENT Output Falling Time	Push-pull, C_L=1nF	-	-	0.5	us
		Open-Drain, R_{PU}=1.0K, C_L=1nF	-	-	0.5	us
Encoder ABZ/UVW, SPI Input/Output Specification						
AB_{RES}	A or B Pulses per Round	Programmable	1	-	4,096	Pulse/ Round
AB_{Freq}	A or B Pulse Frequency	**Note[1]**	-	-	512	KHz
GPIO_VOL	GPIO Output Low Level	Push-pull (Iout=-5mA)	-	-	1.0	V
GPIO_VOH	GPIO Output High Level	Push-pull (Iout=5mA)	VDD-1.0	-	-	V
GPIO_VIL	GPIO Input Low Level		-	-	30	%VDD
GPIO_VIH	GPIO Input High Level		70	-	-	%VDD
T_{RISE}	Digital Output Rising Time	Push-pull, C_L=20pF	-	-	40	Ns
T_{FALL}	Digital Output Falling Time	Push-pull, C_L=20pF	-	-	40	Ns
Accuracy Specification						
INL	Integral Non-Linearity	Typical, See Figure-5	-1	-	1	Deg.
INL_TD	Integral Non-Linearity Temperature Drift	Full Temperature Range	-0.5	-	0.5	Deg.
DNL	Differential Non-Linearity	See **Figure-5**	-0.01		0.01	Deg.
ANG_NOISE	Angle Noise (Excluding DAC Noise)	B=10mT	-	0.02	-	Deg.-rms
ERM	Radiometric Error of Analog Output	**Note[2]**	-0.2	-	0.2	%VDD
DAC_RES	DAC Resolution	-	-	12	-	Bit
DAC_GN	DAC Gain Error	1 sigma	-0.3	-	0.3	%
DAC_GN_TD	DAC Gain Temperature Drift	Full Temperature Range	-	±0.1	-	%

Operation conditions: T_{AMB}=-40 to 150℃, VDD=4.5~5.5V unless otherwise noted.

Symbol	Description	Conditions/Notes	Min.	Typ.	Max.	Unit
DAC_OS	DAC Output Offset	1 sigma	-7	-	7	mV
DAC_OS_TD	DAC Output Offset Temperature Drift	Full Temperature Range	-3	-	3	mV
DAC_NOISE	Noise of DAC	1 sigma	-	-	0.01	VDD%
CMFR	Common Mode Field Rejection		-	30	-	dB
EEPROM Specification						
Data Retention	Data not Corrupted	150℃	10	-	-	Years
Endurance	Erase and Write Cycles		100	-	-	Cycles

Note[1]: The AB_{Freq} is the product of RS(Rotation Speed) and AB_{RES}. So, for maximum AB resolution of 4,096 PPR, the maximum supported rotation speed RS is:

$$RS_{MAX} = \frac{AB_{Freq}}{AB_{Res}} = \frac{512KHz}{4,096} = 125Hz = 7,500RPM$$

Even >512KHz AB_{Freq} is available, but the INL could not be guaranteed when AB_{Freq} is >512KHz

Note [2]: The analog output is by design ratiometric, i.e., it is proportional to the supply voltage VDD. The ratiometric error is calculated as follows:

$$ERM = \left| \frac{Vout(V_{DD})}{V_{DD}} - \frac{Vout(5V)}{5V} \right| \bullet 100\%$$

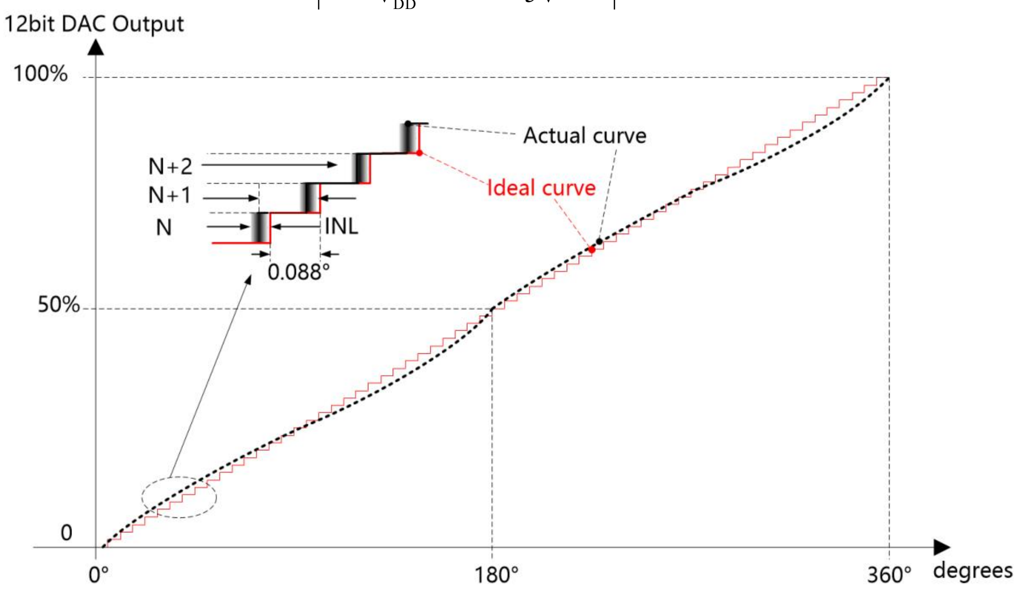


Figure-5: Drawing illustrating of INL

6. Magnetic Input Specifications

Operation conditions: T_{AMB}=-40 to 150℃, VDD=4.5~5.5V unless otherwise noted, two-pole cylindrical diametrically magnetized source.

Table-6: Magnetic Characteristics

Symbol	Description	Conditions/Notes	Min.	Typ.	Max.	Unit
Dmag	Diameter of Magnet	Recommended magnet: Ø10mm x 2.5mm for cylindrical diametrically magnetized magnets	-	10	-	mm
Tmag	Thickness of Magnet		-	2.5	-	mm
Bpk	Input Magnetic Field Amplitude (The Vertical Compenent Measure at the IC surface)	MT6511CT/GT-STD MT6511CT/GT-PMP MT6511CT/GT-STP MT6511CT/GT-SPI	±10	-	±50	mT
		MT6511CT/GT-STW	±20	-	±90	mT
AG	Air Gap	Magnet to IC surface distance	-	2.5	-	mm
DISP	Off Axis Misalignment	Misalignment Error Between Sensor Sensing Center and Magnet Axis (See Figure-6)	-	-	0.3	mm
RS	Rotation Speed	-	-	-	30,000	RPM
TCmag1	Recommended magnet material and temperature drift coefficient	NdFeB (Neodymium Iron Boron)	-	-0.12	-	%/℃
TCmag2		SmCo (Samarium Cobalt)	-	-0.035	-	

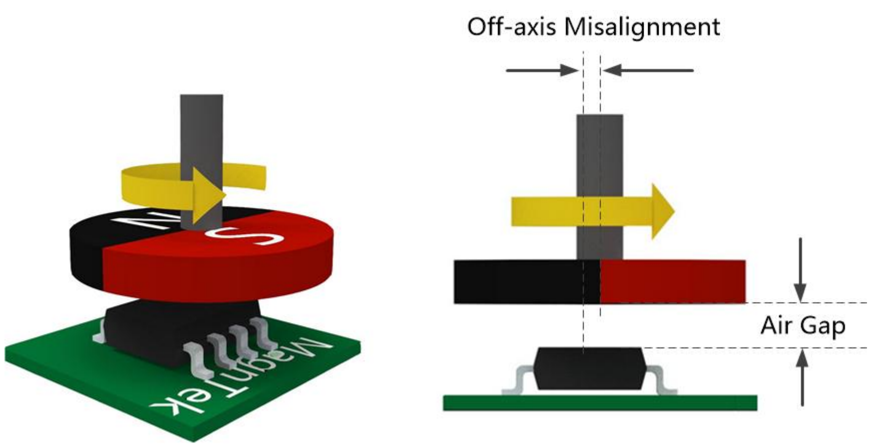


Figure-6: Magnet Arrangement

7. Output Mode

The MT6511 provides Analog, PWM, SENT, ABZ, UVW and SWO output signals at output pins, and the absolute angle position data could be transferred by the 3-Wire SPI interface (CSN, SCK, SDAT) which is always effective.

7.1 I/O Pin Configuration

For SOP-8/TSSOP-16 packages, the Analog, PWM, SENT, ABZ, UVW, SWO and SPI Interface are configured as below Table-7 & Table-8.

Table-7: SOP-8 Package I/O Configure

Pin#	Analog Mode	PWM Mode	SENT Mode	ABZ Mode	UVW Mode	SWO Mode
2	CSN	CSN	CSN	CSN	CSN	CSN
3	-	-	-	B	V	SWO
4	SCK	SCK	SCK	SCK	SCK	SCK
5	Analog	PWM	SENT	A	U	Analog/PWM/SENT
6	SDAT	SDAT	SDAT	SDAT	SDAT	SDAT
7	-	-	-	Z	W	-

Table-8: TSSOP-16 Package I/O Configure

Pin#	Analog Mode	PWM Mode	SENT Mode	ABZ Mode	UVW Mode	SWO Mode
1	-	-	-	Z_CH1	W_CH1	-
4	CSN_CH1	CSN_CH1	CSN_CH1	CSN_CH1	CSN_CH1	CSN_CH1
5	-	-	-	B_CH2	V_CH2	SWO_CH2
6	Analog_CH2	PWM_CH2	SENT_CH2	A_CH2	U_CH2	Analog_CH2/ PWM_CH2/SENT_CH2
7	SCK_CH2	SCK_CH2	SCK_CH2	SCK_CH2	SCK_CH2	SCK_CH2
8	SDAT_CH2	SDAT_CH2	SDAT_CH2	SDAT_CH2	SDAT_CH2	SDAT_CH2
9	-	-	-	Z_CH2	W_CH2	-
12	CSN_CH2	CSN_CH2	CSN_CH2	CSN_CH2	CSN_CH2	CSN_CH2
13	-	-	-	B_CH1	V_CH1	SWO_CH1
14	SCK_CH1	SCK_CH1	SCK_CH1	SCK_CH1	SCK_CH1	SCK_CH1
15	Analog_CH1	PWM_CH1	SENT_CH1	A_CH1	U_CH1	Analog_CH1/ PWM_CH1/SENT_CH1
16	SDAT_CH1	SDAT_CH1	SDAT_CH1	SDAT_CH1	SDAT_CH1	SDAT_CH1

The MT6511's Analog, PWM, SENT and OWI output are at the same OUT PIN (Pin.5 of SOP-8 package and Pin.6 & Pin.15 of TSSOP-16 package) which defined by the register 'Output_Mode[1:0]' as shown in Table-9. The MT6511 will automatically check if OWI interface is activated during a certain time window when MT6511 is powered up, it has the highest priority, OWI is mainly used for output programming. When OWI communication finished, the OUT PIN will change to Analog, PWM or SENT which defined by the register 'Output_Mode[1:0]'.

Table-9: Output @Pin.5 of SOP-8 Package (Pin.6 & Pin.15 of TSSOP-16 Package)

Register	Value	Description
Output_Mode[1:0]	0	Analog Output with C_{LMAX}=100nf
	1	PWM Output (Push-Pull or Open-Drain Configurable)
	2	SENT without Pause (Push-Pull or Open-Drain Configurable)
	3	SENT with Pause (Push-Pull or Open-Drain Configurable)

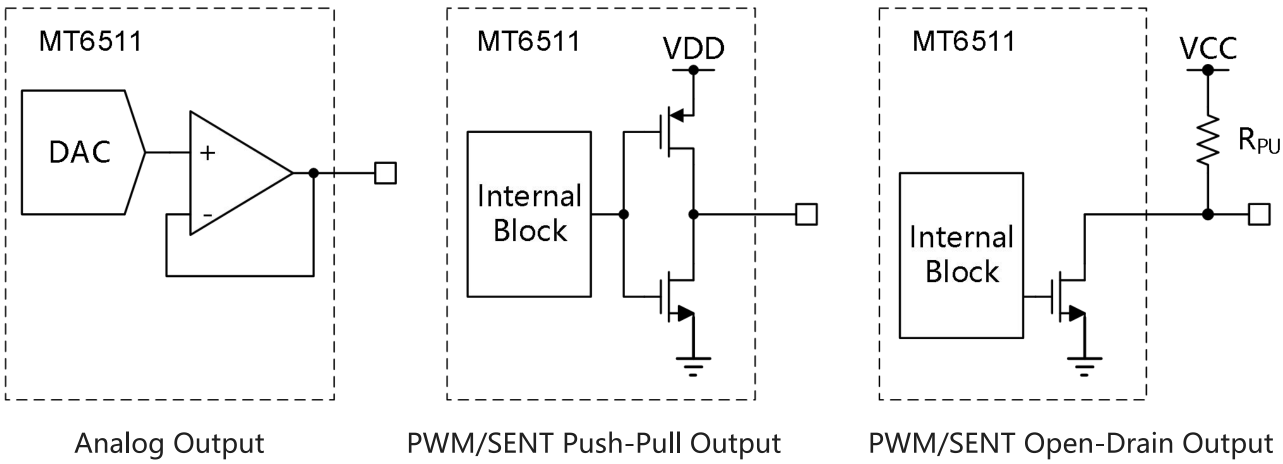


Figure-7. Output Type of Analog, PWM and SENT

As shown in Figure-7, the analog output of MT6511 is driven by a buffer with the output of the internal 12-bit DAC. The output type of PWM/SENT could be configured by the register 'Output_Type' shown in Table-10 as push-pull or open drain. When in open-drain type, it is necessary to connect an external pull-up resister RPU (**recommend 1.0KΩ & Keep External VCC≤5V**). **In the open drain mode, the chip cannot be programmed through the 'OUT' pin.**

Table-10: Output @Pin.5 of SOP-8 Package (Pin.6 & Pin.15 of TSSOP-16 Package)

Register	Value	Description
Output_Type	0	Push-Pull of PWM/SENT Output
	1	N-Side Open-Drain of PWM/SENT Output

The encoder output ABZ and UVW of MT6511 could be enabled by the register 'Encoder_Output_Enable' as shown in Table-11. When encoder mode is enabled, Analog, PWM and Sent Modes are disabled. Table-12 shows the register 'Encoder_Output_SEL' defines ABZ or UVW mode which one is activated.

Table-11: Encoder Output Enable

Register	Value	Description
Encoder_Output_Enable	0	Analog/PWM/SENT Output Mode
	1	Encoder Output Mode (ABZ or UVW)

Table-12: Encoder Output Select (ABZ or UVW)

Register	Value	Description
Encoder_Output_SEL	0	ABZ Output Mode
	1	UVW Output Mode

The switch output of MT6511 could be enabled by the register 'Switch_Output_Enable' as shown in Table-13.

Table-13: Output @Pin.3 of SOP-8 Package (Pin.5 & Pin.13 of TSSOP-16 Package)

Register	Value	Description
SW_Output_Enable	0	Switch Output Mode Disabled
	1	Switch Output Mode Enabled

The priority of switch output mode is higher than encoder mode ABZ and UVW. The SWO Pin's (Pin 3# of SOP-8, Pin.5 and Pin.13 of TSSOP-16) truth table is shown in Table-14.

Table-14: SWO @Pin.3 of SOP-8 Package (Pin.5 & Pin.13 of TSSOP-16 Package) Truth Table

SWO Pin	Register SWO_Output_Enable	Register Encoder_Output_Enable	Register Encoder_Output_SEL
Switch Output	1	X	X
Encoder output 'B'	0	1	0
Encoder output 'V'	0	1	1
Factory Test	0	0	X

7.2 Analog Output Mode

Analog output is the most used output mode in automotive applications. The default analog output of MT6511 (without customer programming) is 0~360°, 0%~100%VDD. The analog output is based on an internal 12-bit DAC, 12-bit digital angle data also could be programmed to special curves based on arbitrary 8-point or 17-point piece-wise programming, please refer to Chapter. 8 for the details.

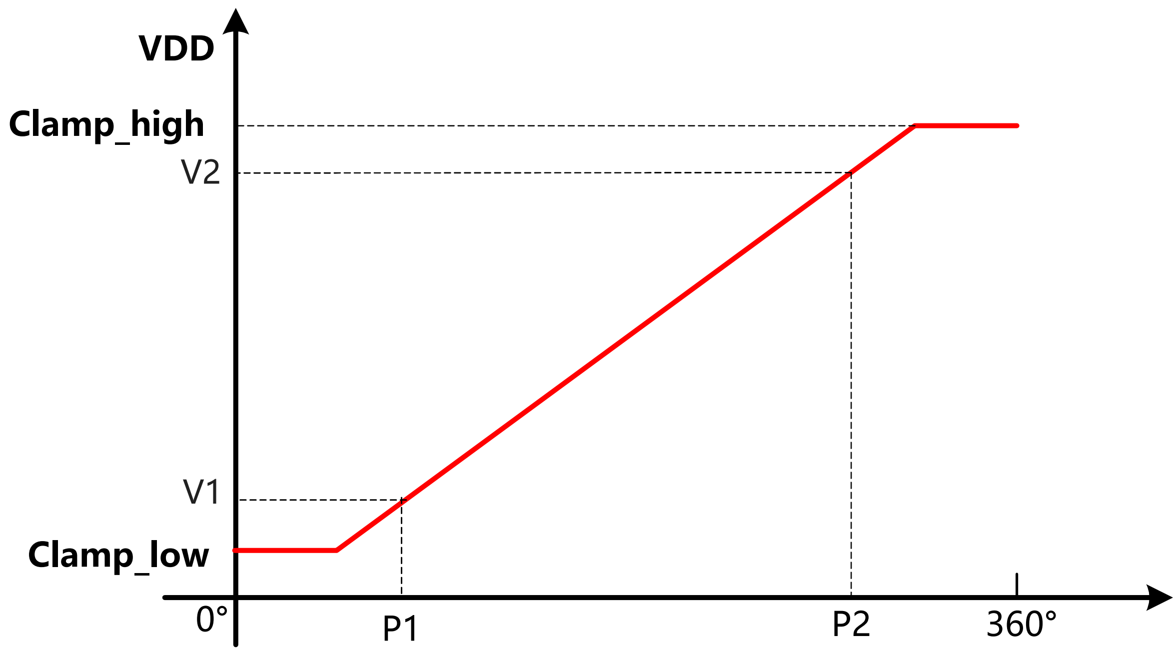


Figure-8: Analog Output

Both overvoltage and overcurrent protection are designed to protect the analog output as shown in Figure-9. The normal operation voltage range is 4.5~5.5V, but the analog output can withstand up to +30V without being damaged. And output current limit to 18mA can ensure that the analog output will not be damaged when it is short circuited.

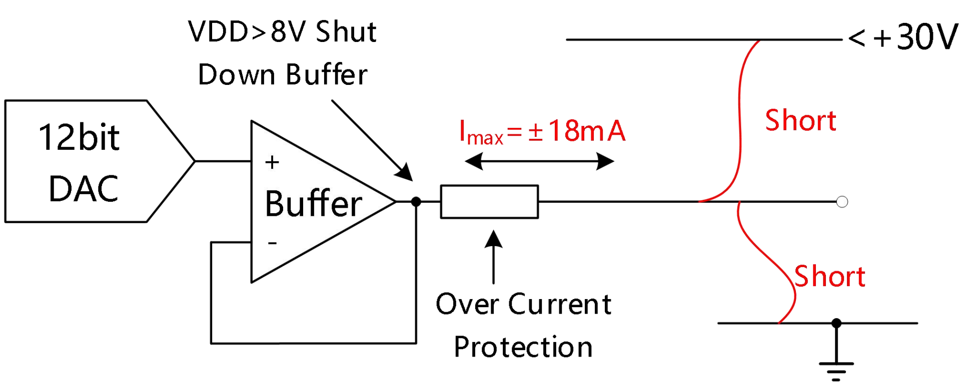


Figure-9: Over-Voltage and Over-Current Protection of Analog Output

7.3 PWM Output Mode

When PWM mode is enabled, the output signal is a digital signal with Pulse-Width-Modulation as shown in Figure-10. The PWM output of MT6511 is push-pull type or open-drain type as shown in Figure-7. The PWM signal has the resolution of 12 bit and with programmable frequency and polarity as shown in Figure-10 and Table-15.

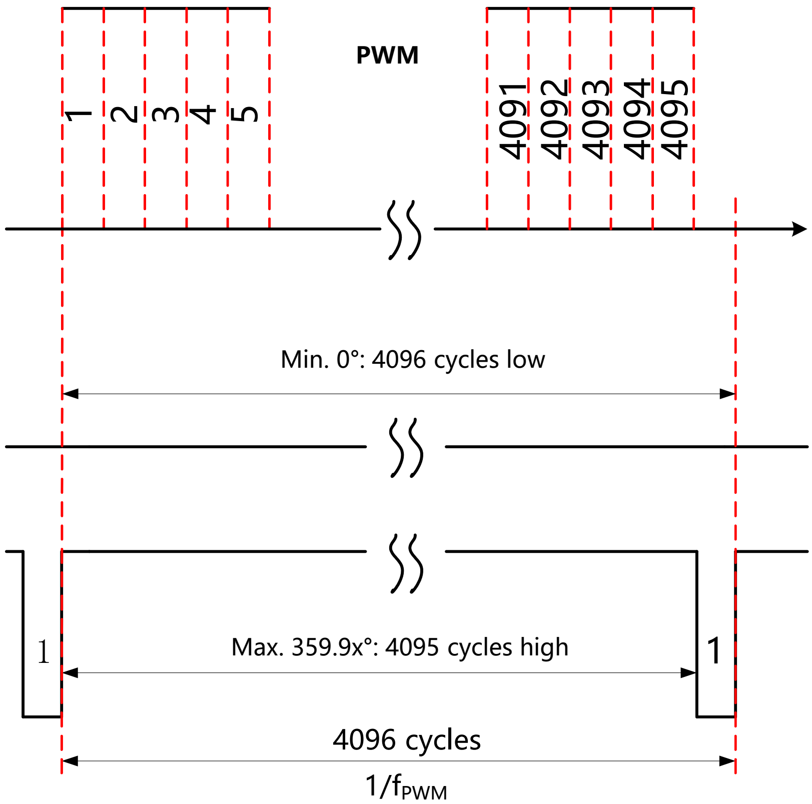


Figure-10: PWM Output

Table-15: The 'PWM_POL' PWM Polarity Register

Register	Value	Description
PWM_POL	0	High Level Valid
	1	Low Level Valid

The PWM frequency can be programmed to arbitrary value from 125Hz to 2KHz by setting the 16-bit register 'PWM_N' as follows.

$$F_{PWM} = 8{,}192{,}000 / PWM\_N \quad (Hz)$$

where PWM_N is an integer number ranging from 4096 to 65,535 (values below 4,096 is clamped).

7.4 Switch Output Mode

When Switch Output Mode of the MT6511 is enabled, the output signal is a digital signal with the switch point selected by 'SW_OP' register and hysteresis selected by 'SW_HYS' register as shown in Figure-11. Switch output could be enabled with Analog, PWM or SENT output at the same time.

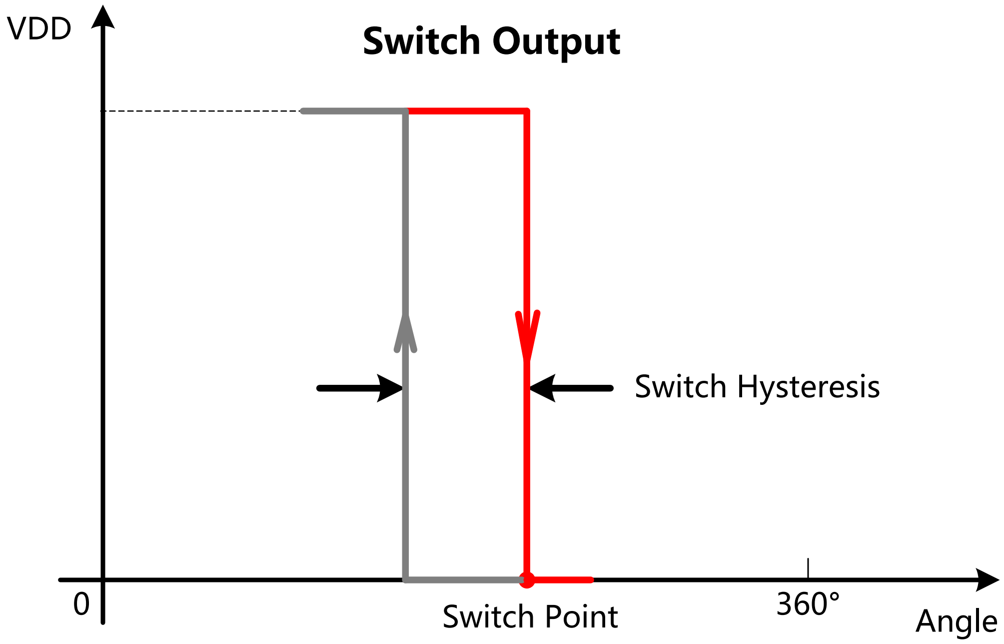


Figure-11: Switch Output

Table-16: The 'Switch_Point[15:0]' Register

Register	Value	Description
Switch_Point[15:0]	16 bits	16-bit for 0~360°

Table-17: The 'SW_Hysteresis[7:0]' Register

Register	Value	Description
Switch_Hysteresis[7:0]	8 bits	1 LSB=0.088°

Table-18: The 'Switch_Output_Polarity' Register

Register	Value	Description
Switch_Output_Polarity	0	Low Level above SW_OP
	1	High Level above SW_OP

7.5 Quadrature A,B and Zero-Position Output (ABZ Mode)

As shown in Figure-12, when the magnet rotates counter-clock-wise (CCW), output B leads output A by 1/4 cycle, when the magnet rotates clock-wise (CW), output A leads output B by 1/4 cycle (or 1 LSB). Output Z indicates the zero position of the magnet. The ABZ output become valid 0.7ms after chip power on to guarantee proper output.

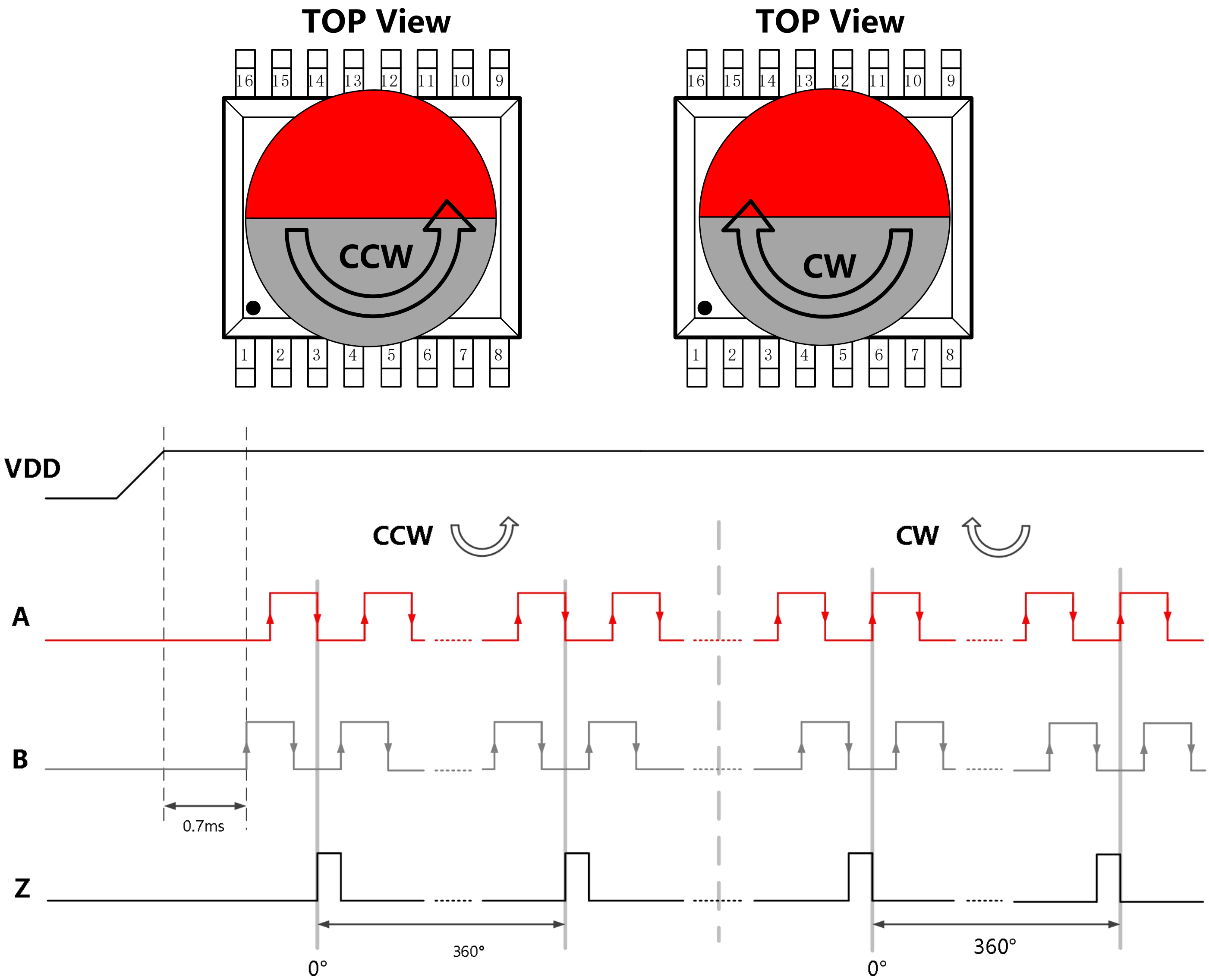


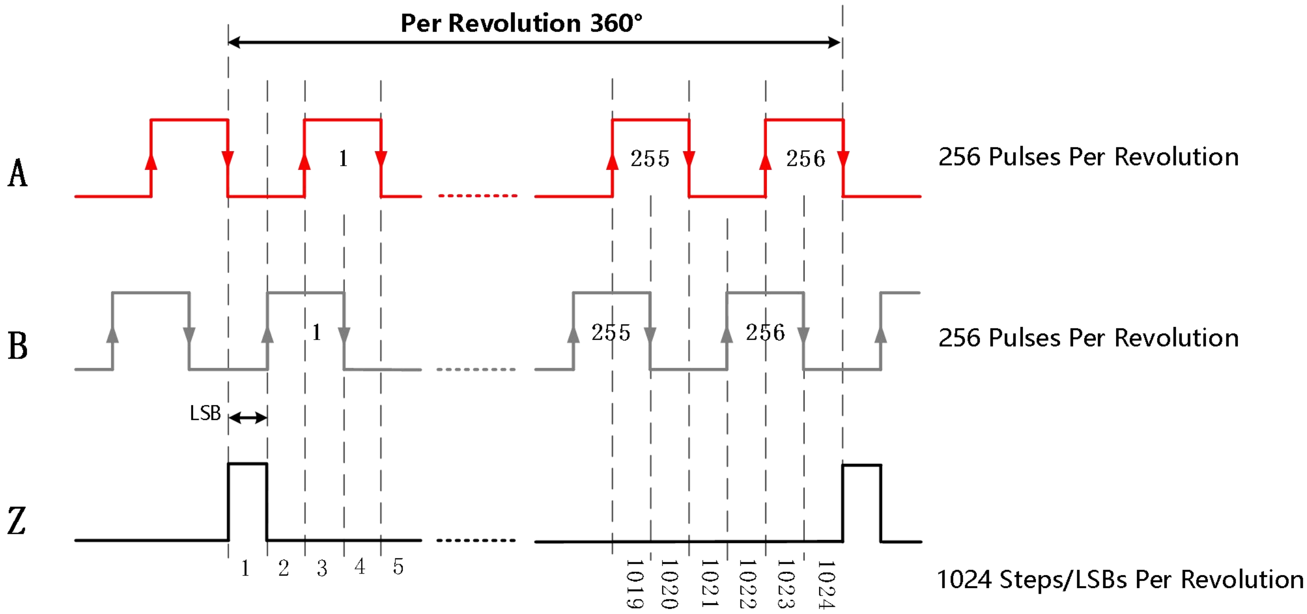
Figure-12: ABZ output with VDD power on

Table-19: The ‘ROT_DIR’ (CCW or CW) Register

Register	Value	Rotation Direction
ROT_DIR	0	Counter-Clock-Wise, Output B leads Output A
	1	Clock-Wise, Output A leads Output B

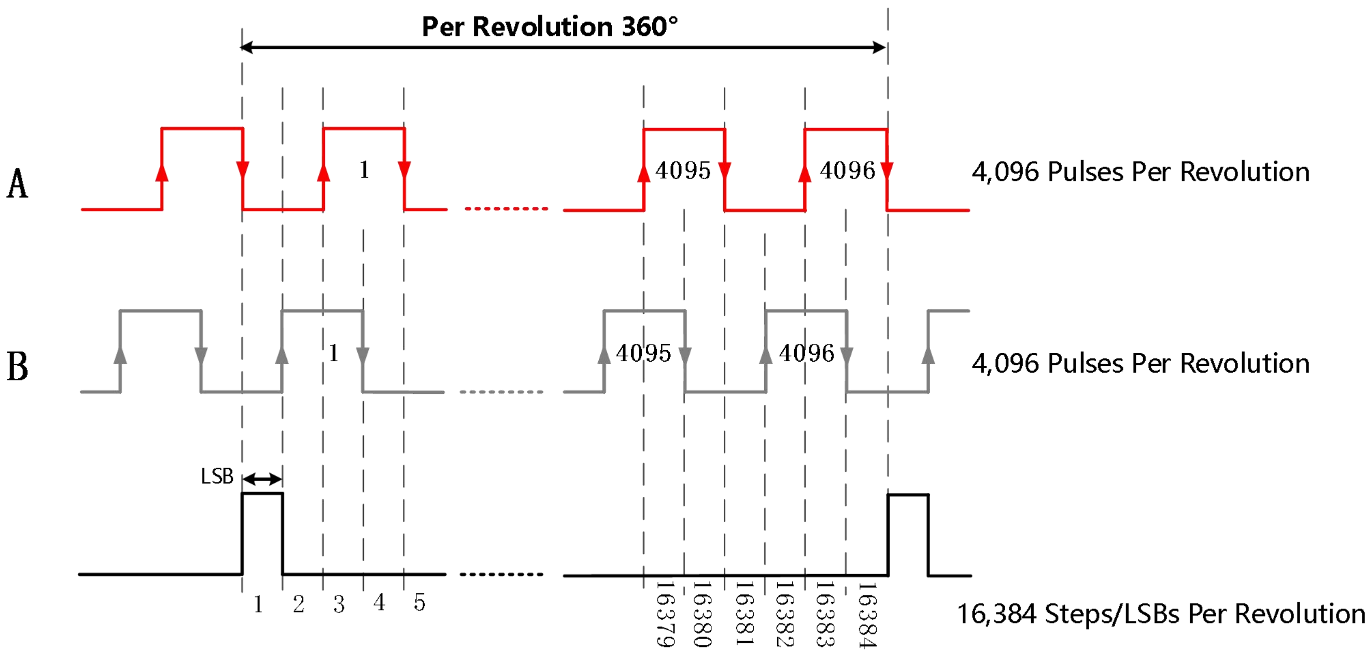
‘ROT_DIR’ is effective for all output types as Analog, ABZ, UVW, PWM, SENT and SPI

ABZ resolution is user programmable from 1~4,096 PPR. The relationship between binary bits, LSBs and PPR resolution of ABZ output are shown in Figure-13 & Figure-14.



10 bit=2^{10} LSBs=1024 Steps=256 PPR

Figure-13: ABZ Output Resolution=10 bit=256 PPR



4096 PPR=16,384 Steps

Figure-14: ABZ Output Resolution=4,096 PPR

The resolution of ABZ is defined by a 12-bit register ‘ABZ_RES[11:0]’;

Table-20: The ‘ABZ_RES[11:0]’ Register

Register	Value	AB Resolution (Pulse per Round)
ABZ_RES[11:0]	0x000	1
	0x001	2
	0x002	3
	. . .	. . .
	0xFFC	4,093
	0xFFD	4,094
	0xFFE	4,095
	0xFFF	4,096

Output Z indicates the zero position of the magnet which is user programmable, and the pulse width of Z is selectable as 1, 2, 4, 8, 16 LSBs or 60°, 120°, 180° as shown in Figure-15 and Figure-16. It is guaranteed that one Z pulse is generated for every rotation.

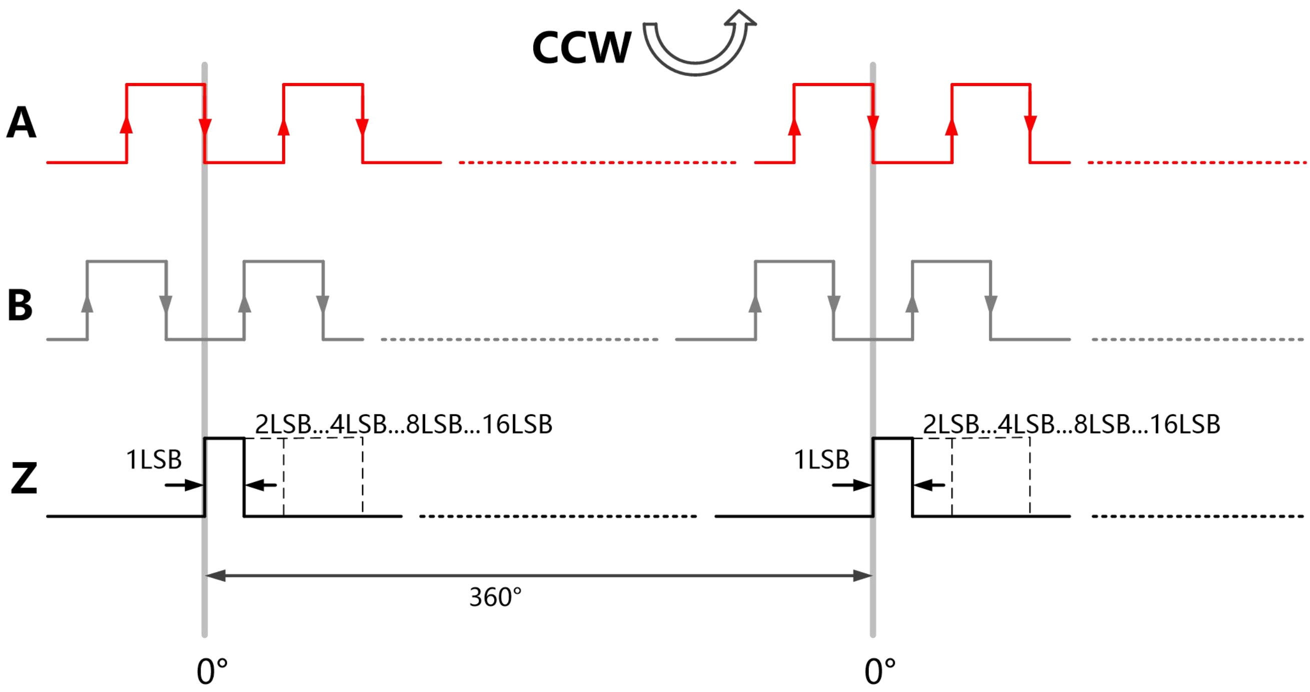


Figure-15: Typical ABZ Output with Z pules width=1,2,4,8 and 16 LSBs

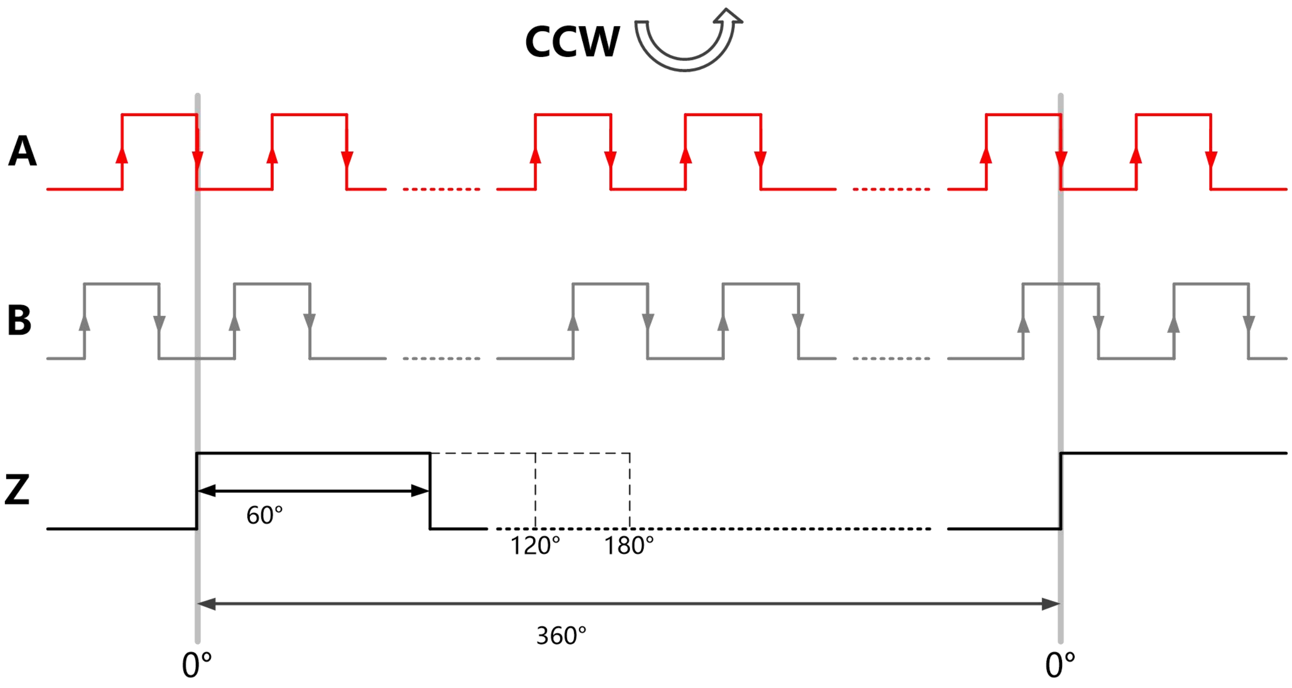


Figure-16: Typical ABZ Output with Z Pulse Width=60°, 120° and 180°

The width of Z pulse is defined by the 3-bit register 'Z_PUL_WID[2:0]';

Table-21: The 'Z_PUL_WID[2:0]' Register

Register	Value	Width (LSBs/°)	Value	Width (LSBs/°)
Z_PUL_WID[2:0]	0x0	1	0x4	16
	0x1	2	0x5	60°
	0x2	4	0x6	120°
	0x3	8	0x7	180°

The absolute position of Z pulse is defined by the 12-bit register 'ZERO_POS[11:0]';

Table-22: The 'ZERO_POS[11:0]' Register

Register	Value	Absolute Position (°)
ZERO_POS[11:0]	0x000	0
	0x001	0.088
	0x002	0.176
	. . .	. . .
	0xFFE	359.824
	0xFFF	359.912

Also, Z pulse phase could be user programmable by ‘Z_PHASE[1:0]’ register as shown in Figure-17.

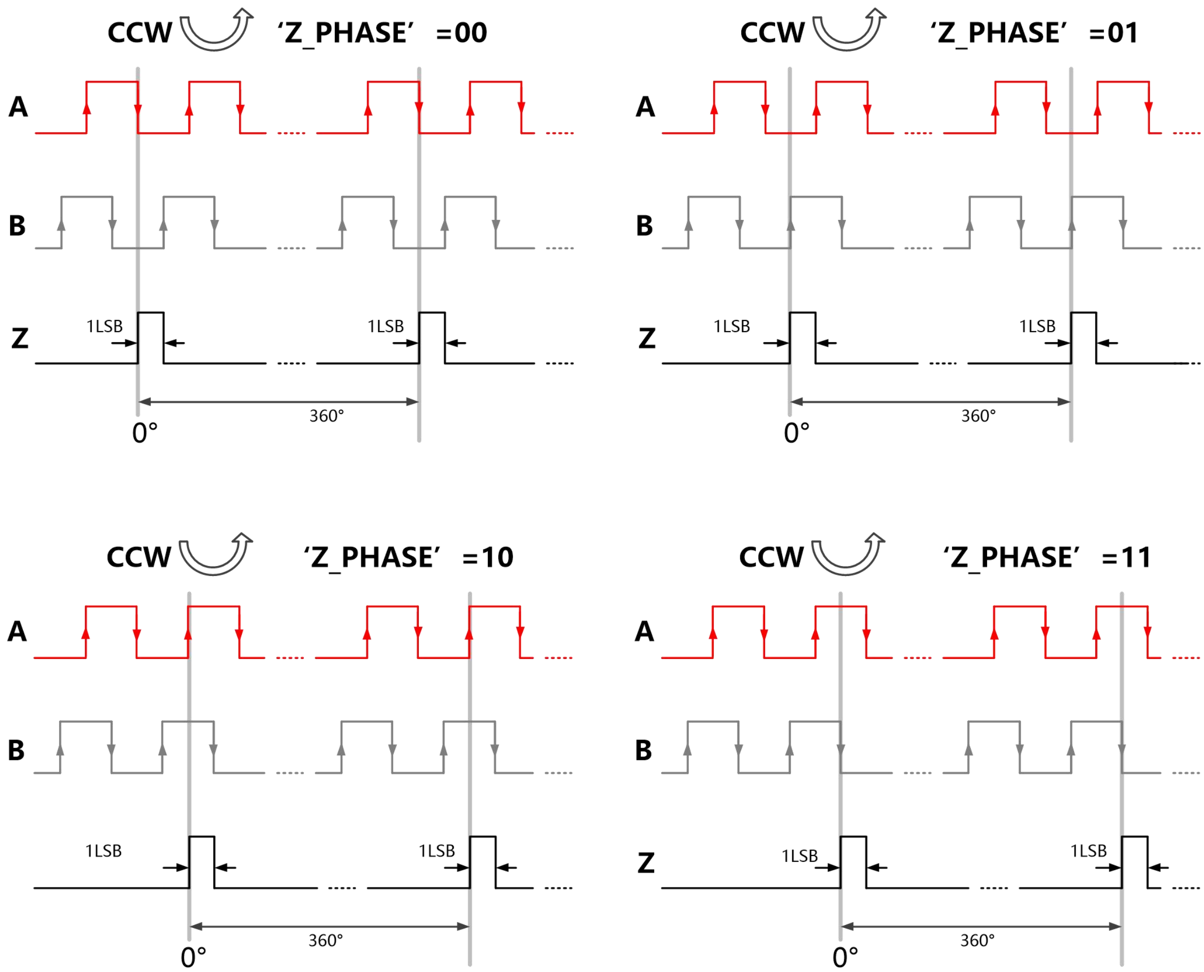


Figure-17: Z Pulse Phase with ‘ROT_DIR’ =0 , ‘SWAP_AB’ =0, ‘Z_EDGE’ =0

The relationship of 0° and Z pulse edge is defined by register ‘Z_EDGE’

Table-23: The ‘Z_EDGE’ Register

Register	Value	Description
Z_EDGE	0x0	Z Pulse Rising Edge Aligned with Zero-Degree (**CCW**)
	0x1	Z Pulse Falling Edge Aligned with Zero-Degree (**CCW**)

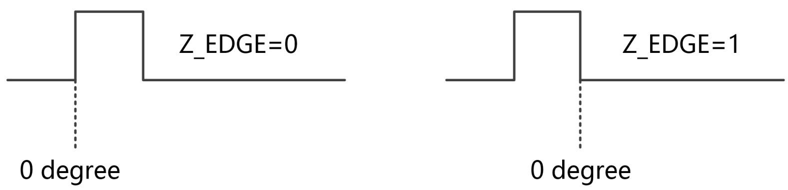


Figure-18: Z Pulse Edge with 0 degree

7.6 UVW Output Mode

The MT6511 provides U, V and W pulses which are 120° (electrical) out of phase as shown in Figure-19. The cycles of UVW per rotation can be programmed as shown in Table-24.

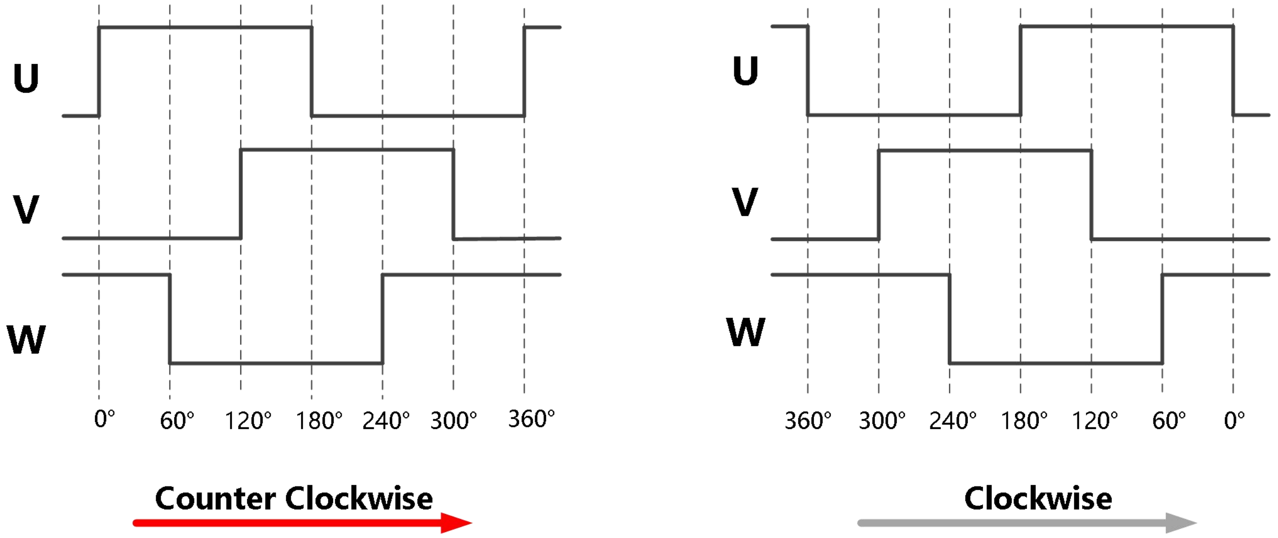


Figure-19: Typical Output Waveform for UVW Mode

Table-24: The ‘UVW_RES[3:0]’ Register

Register	Value	UVW Pole Pairs
UVW_RES[3:0]	0x0	1
	0x1	2
	0x2	3
	0x3	4
	0x4	5
	0x5	6
	0x6	7
	0x7	8
	0x8	9
	0x9	10
	0xA	11
	0xB	12
	0xC	13
	0xD	14
	0xE	15
	0xF	16

7.7. SPI (3-Wire) Interface

The MT6511 provides a 3-Wire SPI interface for a host MCU to read back the absolute angle information and diagnostic status from its internal registers.

7.7.1 SPI (3-Wire) Timing

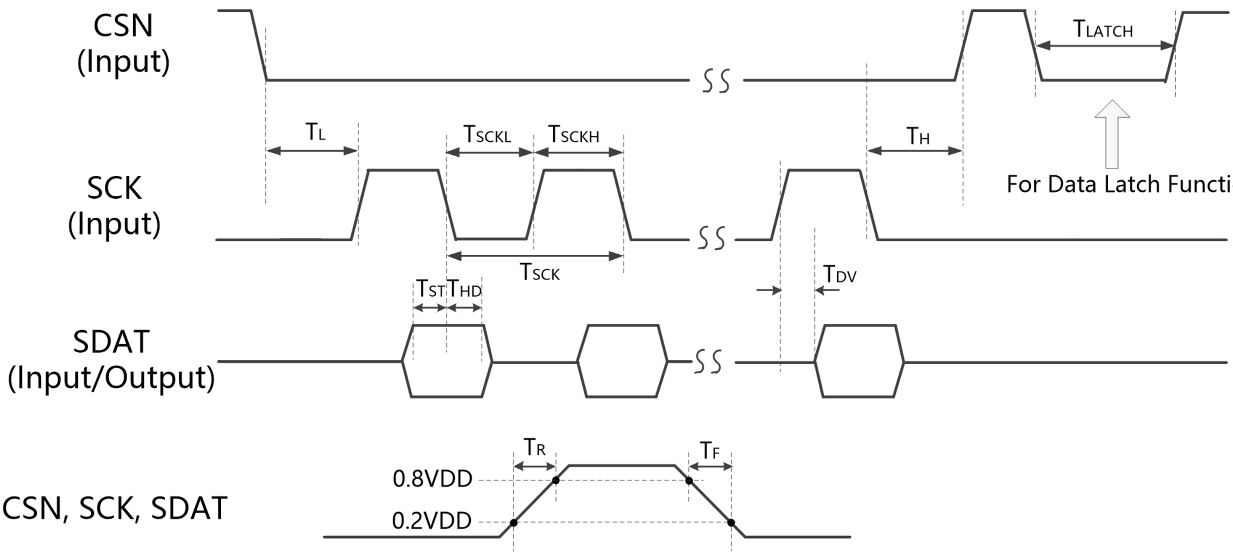


Figure-20: 3-Wire SPI Timing Diagram

Table-25: SPI Timing Specification

Symbol	Description	Min.	Typ.	Max.	Unit
T_L	Time Between CSN Falling Edge and SCK Falling Edge	100		-	ns
T_{SCK}	Clock Period	125		-	ns
T_{SCKL}	Low Period of Clock	50		-	ns
T_{SCKH}	High Period of Clock	50		-	ns
T_H	Time Between SCK Last Rising Edge and CSN Rising Edge	$0.5 \bullet T_{SCK}$		-	ns
T_R	Rise Time of Digital Signal (with 20pf Loading Condition)	-	10	-	ns
T_F	Fall Time of Digital Signal (with 20pf Loading Condition)	-	10	-	ns
T_{DV}	Data Valid Time of SDAT (with 20pf Loading Condition)	-	-	15	ns
T_{ST}	Setup Time of SDAT Data	10	-	-	ns
T_{HD}	Hold Time of SDAT Data	10	-	-	ns
T_{LATCH}	Effective CSN Low Period Time for Latch Angle Function	1	-	-	us
T_W	SDAT Input Output Transition Time	-	$2*T_{SCK}$	-	ns

7.7.2 SPI Protocol

The Reading-Mode and Writing-Mode of the 3-Wire SPI protocol is shown in Figure-21 and Figure-22. An SPI data transfer starts with the falling edge of CSN and stops at the rising edge of CSN; SCK is the serial port clock, and it is always driven by the SPI master, it is low when there is no SPI transmission. And SDAT is the serial port data input and output, it is driven at the rising edge of SCK and should be captured at the falling edge of SCK. The I/O pin 'SDAT' of MT6511 keeps Hi-Z (as input) unless it drives data out.

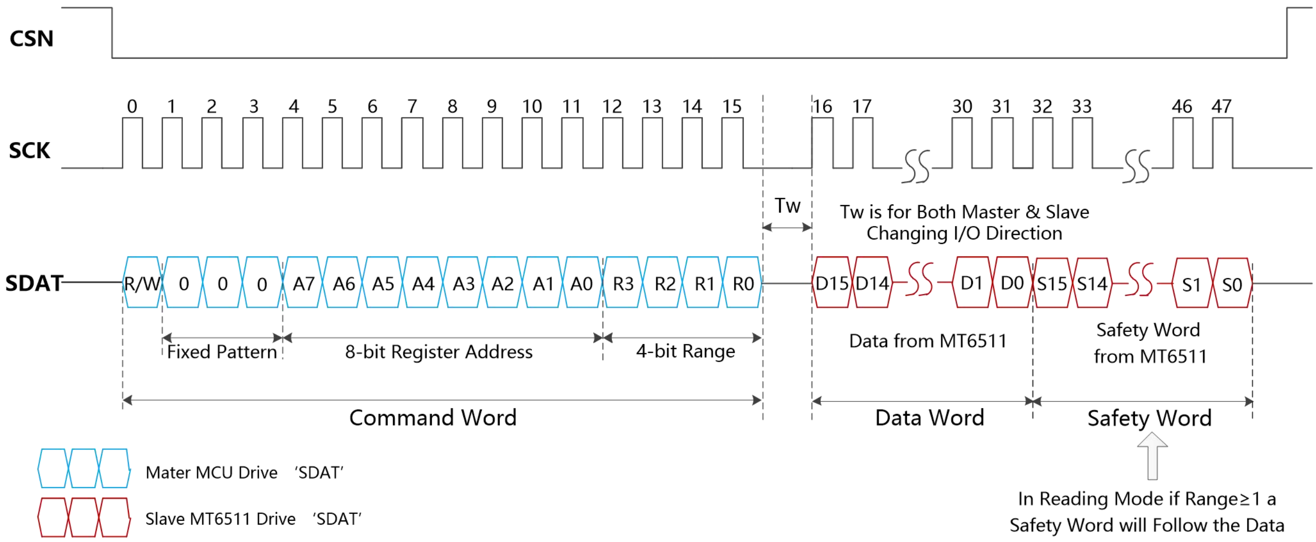


Figure-21: 3-Wire SPI Reading Mode

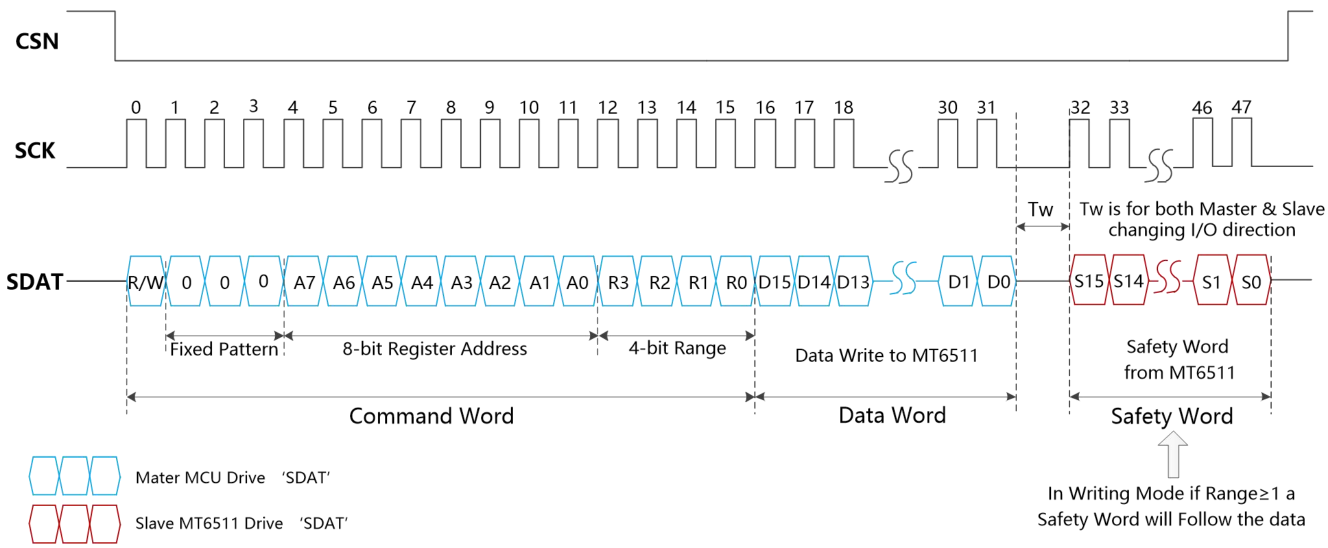


Figure-22: 3-Wire SPI Writing Mode

Table-26: The SPI Command Word Structure

Bit	Name	Description
Bit[15]	R/W	Command Read ('1') or Write ('0')
Bit[14:12]	Fixed '000'	NA
Bit [11:4]	Register Address	Register Address for Read or Write
Bit[3:0]	Read/Write Range N	N=0: Read/Write 1 Word (16 bits) without Safety-Word N=1: Read/Write 1 Word (16 bits) with Safety-Word N=2~15: Read/Write N Words with Safety-Word

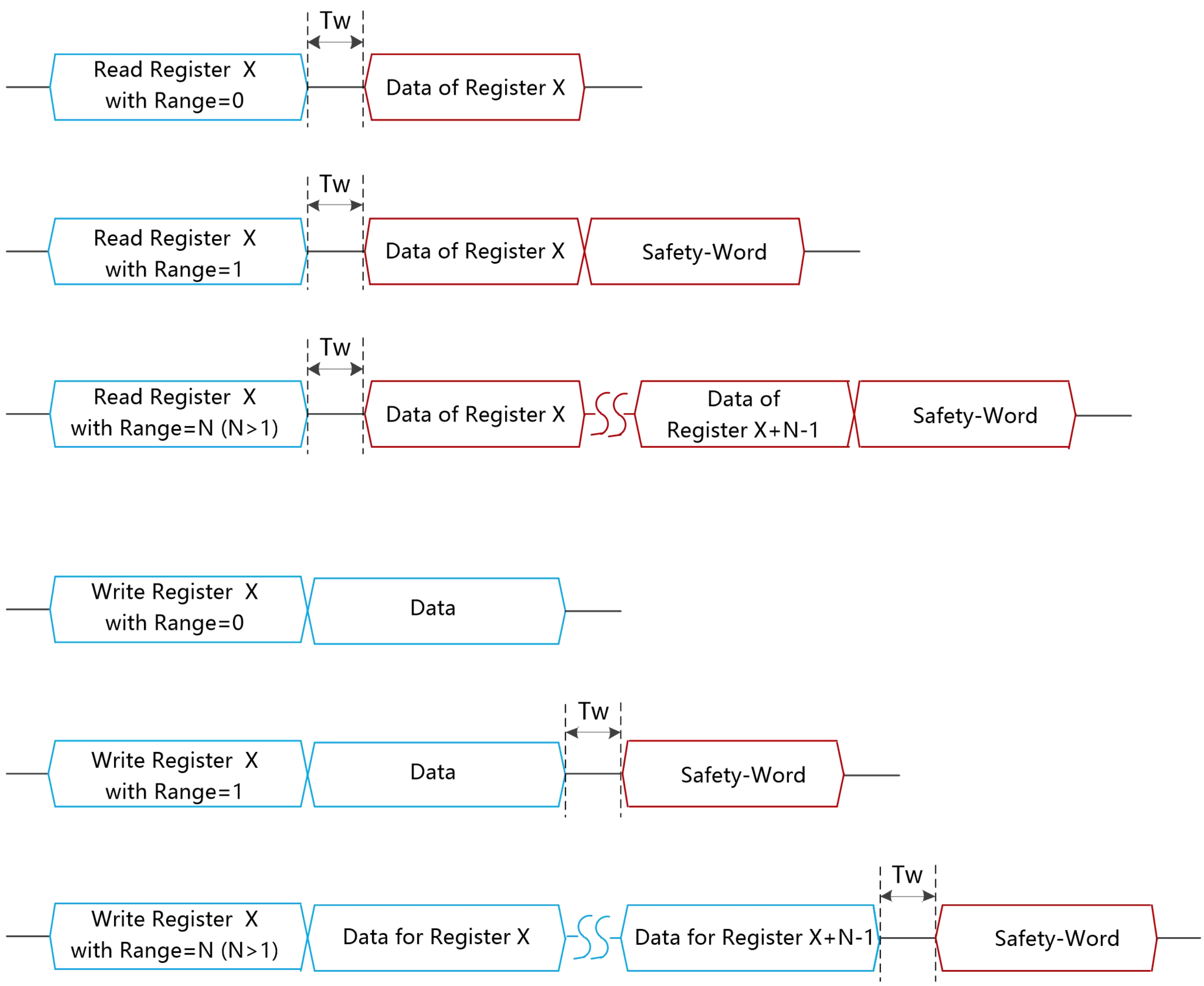


Figure-23: SPI Read/Write with different Range

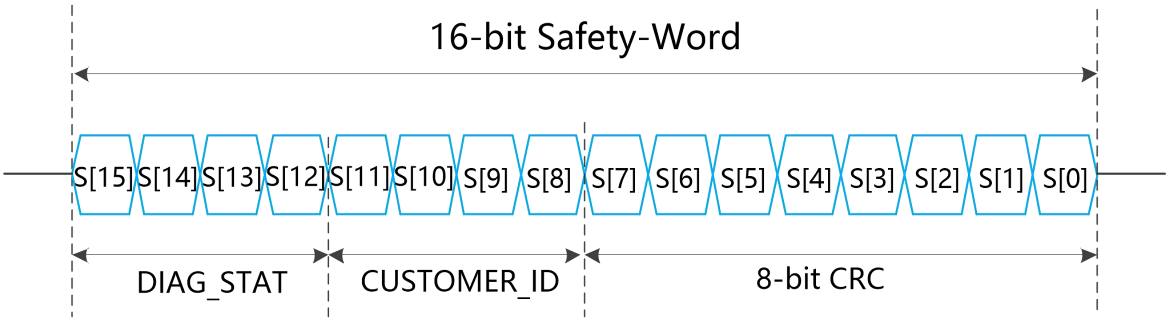


Figure-24: Safety-Word Structure

Table-27: Safety-Word Structure

Name	Bit	Description
DIAG_STAT Note[3]	S[15]	Refer to Chapter-9 Function Safety 'DIAG_CODE[6]' (See Table-36)
	S[14]	Refer to Chapter-9 Function Safety 'DIAG_CODE[5:0]' (See Table-36)
	S[13]	Refer to Chapter-9 Function Safety 'DIAG_CODE[8:7]' (See Table-36)
	S[12]	Refer to Chapter-9 Function Safety 'DIAG_CODE[15:9]' (See Table-36)
CUSTOMER_ID	S[11:8]	4-bit ID for the chip which can be programmed by Register 'CUSTOMER_ID'
CRC	S[7:0]	Cyclic Redundancy Check

Note[3]: DIAG_STAT bit is set to 1 in normal operation and 0 in case of diagnostic failure

CRC

- CRC data range:

  (1) Default with register 'SPI_CRC_SEL' =0, including command word and data words;

  (2) With register 'SPI_CRC_SEL' =1, including command word, data words and S[15:8];

- CRC polynomial: $X^8+X^4+X^3+X^2+1$, the 'R/W' bit of command word shifts in first;
- CRC seed value: '11111111_B';
- The remainder is inverted before transmission;

7.7.3 SPI (3-Wire) Read Angle

Customer can read the angle register inside MT6511 through the 3-wire SPI interface as shown in Figure-25. A read-flag signal also be provided to indicate if the data-to-read is refreshed. In this case, when register 'DATA_FLAG' =0, the register 0x01, 0x02, 0x41 and 0x42 have no read-flag signal; when register 'DATA_FLAG' =1 , Bit15 of the register 0x01, 0x02, 0x41 and 0x42 become read-flag signal to indicate if the data-to-read is refreshed, and only the 15 MSB of angle and speed data is stored. And if the data is refreshed RFA=1 and RFV=1, otherwise no new data is refreshed. A separate CSN low level can latch the value of the angle register, as shown in Figure-26.

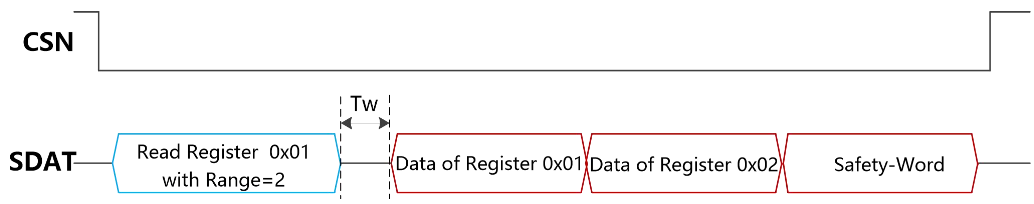


Figure-25: SPI Reading Current Angle Data

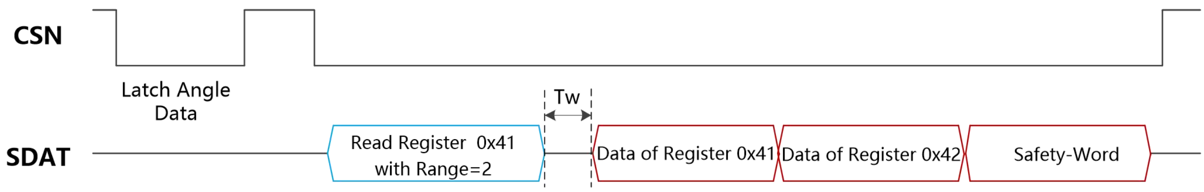


Figure-26: SPI Reading Latched Angle Data

Table-28: Angle Data Related Register

Address	Bit15	Bit14~Bit0
Register 'DATA_FLAG' =0		
0x01	ANGLE[15]	ANGLE[14:0] (data of angle)
0x02	ANGLE_VEL[15]	ANGLE_VEL[14:0] (data of velocity)
0x41	ANGLE_LATCHED[15]	ANGLE_LATCHED[14:0] (lathed data of angle)
0x42	ANGLE_VEL_LATCHED[15]	ANGLE_VEL_LATCHED[14:0] (latched data of velocity)
Register 'DATA_FLAG' =1		
0x01	RFA	ANGLE[15:1] (data of angle)
0x02	RFV	ANGLE_VEL[15:1] (data of velocity)
0x41	RFA	ANGLE_LATCHED[15:1] (latched data of angle)
0x42	RFV	ANGLE_VEL_LATCHED[15:1] (latched data of velocity)

0~360° absolute angle θ could be calculated by the below formula with ANGLE[15:0]:

$$\theta = \frac{\sum_{i=0}^{15} \mathrm{ANGLE} < i > \bullet 2^{i}}{2^{16}} \bullet 360°$$

7.8 SENT Interface

MT6511 encodes a 12-bit angular value into a sequence of pulses based on the encoding scheme of the SAE J2716 SENT standard. Data is split into 4-bit nibbles that are encoded in the time-domain as the duration between two falling edges. The message frame is a sequence of 4-bit nibbles (SENT frame). The length of the SENT frame is defined in clock ticks with a configurable duration of T_{TICK} = 1.5 us, 3 us, and 6 us each clock tick. A calibration pulse (SYNC nibble) followed by a STATUS nibble, a constant number of fast channel DATA nibbles, a CRC nibble, and an optional PAUSE pulse define one message frame of a SENT transmission as shown in Figure-27. The MT6511 is compatible with revisions of the SENT specification SAE J2716 APR2016 and supports data formats in accordance with appendix A.1 and A.3.

Basic Concept

- Use base time unit called tick (typical 3us, programmable).
- Transmission is made of nibbles. Each nibble starts with a falling edge (or rising edge) and a fixed low-level duration (or high-level duration).
- Each nibble carries 4-bit data and has a length of 12+x ticks (x=0, 1, ... , 15).
- Each transmission frame starts with a synchronization nibble and ends with a CRC or pause (optional) nibble.
- Information transmitted in the signal/data nibble is called **fast channel**. Information transmitted in the status nibble is called **slow channel (or serial message)**.

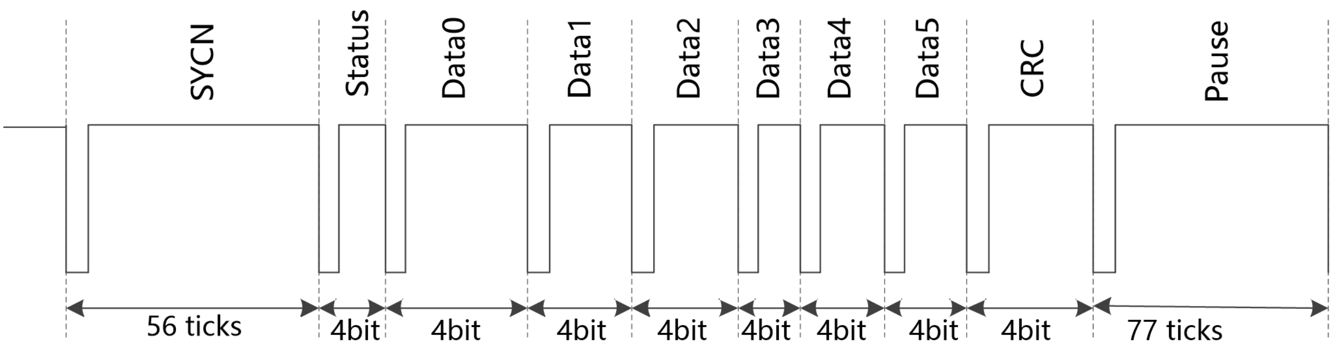


Figure-27: SENT Frame

7.8.1 Dual Throttle Position Sensors Frame Format A.1 (H.1)

The MT6511 SENT transmits a sequence of data nibbles according dual throttle positions sensor defined in SAE J2716 APR2016 appendix A.1. The frame contains 2-bit serial message SM[1:0], 2-bit status S[1:0], two 12-bit data values CH1[11:0] & CH2[11:0] and 4-bit CRC checksum, as shown in Figure-28. CH1 is always delivering the 12-bit angle data of MT6511. CH2 could be enabled/disabled by the register 'SENT_CH2_EN' in Table-29, and when CH2 is enabled , the 12-bit data could be configured by the register 'SENT_CH2_DATA' as shown Table-30.

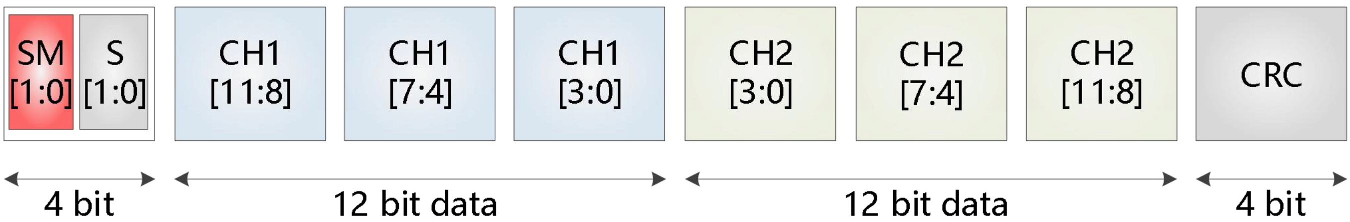


Figure-28: Two 12-bit Fast Channel Frame

Table-29: Register 'SENT_CH2_EN'

Register	Value	CH2 Data Enable
SENT_CH2_EN	0	All '0'
	1	Follow Table-31

Table-30: Register 'SENT_CH2_DATA'

Register	Value	CH2 Data
SENT_CH2_DATA	0	Temperature Sensor 12-bit Code
	1	4089-CH1
	2	12-bit User Programmed Data
	3	4095-CH1

Status S[1:0] Definition

S[1:0] of the status nibble are used to indicate errors detected by the chip. If any error condition is detected, e.g., bit S[0] is set to1, in which case DIAG_CODE[15:0] (refer to Table-36)is also set to a non- zero value. S[1] is currently reserved and always set to 0.

Series Message SM [1:0] Definition

Bit[2] and [3] of the status nibble is used to transmit serial message as defined in Chapter 7.8.3.

CRC Checksum Definition

CRC Data Range: CH1[11:0] and CH2[11:0] total 24 bits

CRC polynomial: $X^4+X^3+X^2+1$ with seed value of '0101_B'

7.8.2 Single Secure Sensors Frame Format A.3 (H.4)

The MT6511 SENT also transmits a sequence of data nibbles according single secure sensor defined in SAE J2716 APR2016 appendix A.3. The frame contains 2-bit serial message SM[1:0], 2-bit status S[1:0], 12-bit data values CH1[11:0], 8-bit rolling counter, 4-bit inverted CH1[11:8] and 4-bit CRC checksum. CH1 is always delivering the 12-bit angle data; COUNT[7:0] is 8-bit rolling counter 0~255 with rollover back to 0, as shown in Figure-29; The SM[1:0], S[1:0] and CRC are the same with A.1.

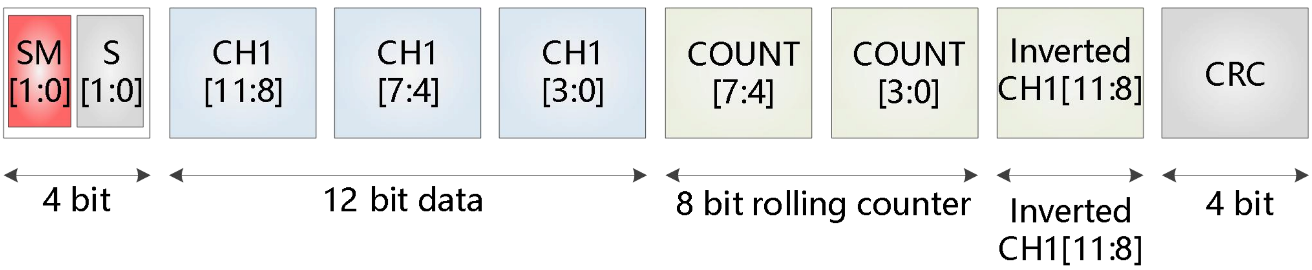


Figure-29: Single Secure Sensors Frame

7.8.3 Enhanced Serial Message Format

An optional enhanced serial message format can be used by sensors, which require a serial communication channel with a larger data field and a larger set of message IDs. If the enhanced serial message format is used, serial data is transmitted in SM[1:0]. A serial message frame stretches over 18 consecutive SENT data messages from the transmitter as shown in Figure-30. All 18 frames must be successfully received (no errors, calibration pulse variation, data nibble CRC error, etc.) for the serial value to be received. The table in Figure-30 defines the frame format. The frame start of a serial message is indicated by the unique pattern "01111110" in SM[1] (SENT message #18, #1 to #7). The first "1" in a series of six ones (after a "0") indicates the start of a serial message frame. The "0" in SENT message #13 is defined to ensure the uniqueness of the start pattern. At initialization, it is recommended that the transmitter send the SM[1] bit sequence '0...01111110' (start with one or more SENT messages equivalent to #18). The serial message frame contains 20 bits of payload data.

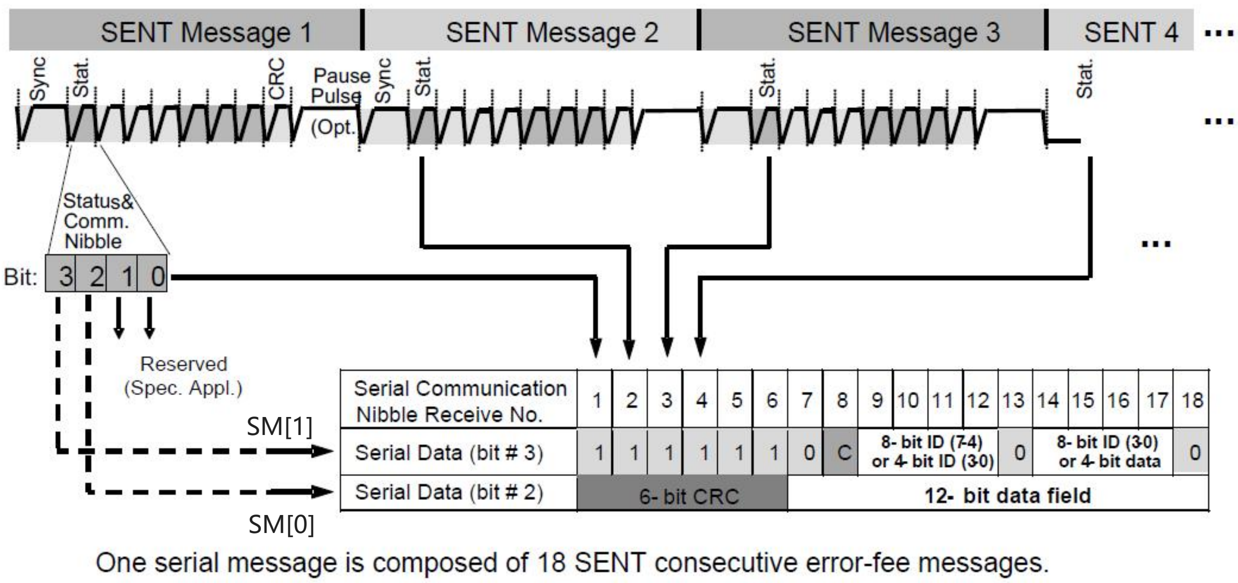


Figure-30: Enhanced Serial Data Message form 18 SENT Messages

CRC Checksum Definition of Series Message

CRC Code: SM[0] of frame 1~6

CRC polynomial: $X^6+X^4+X^3+1$ with seed value of '010101_B'

The list of 8-bit serial message IDs for Enhanced Serial Message Format shall be as given in Table-31. The details please refer to application notes of MT6511 SENT.

Table-31: Serial Message Channel 8-bit Message IDs

#	8-bit ID	12-bit Data Item	Data Source
1	0x01	Diagnostic error code	DIAG_CODE[15:0]
2	0x03	Channel 1/2 sensor type	SENT_SENSOR_TYPE
3	0x05	Manufacturer code	SENT_MAN_CODE
4	0x06	SENT standard revision	SENT_REV
5	0x07	Fast channel: X1	SENT_CHANNEL_X1
6	0x08	Fast channel: X2	SENT_CHANNEL_X2
7	0x09	Fast channel: Y1	SENT_CHANNEL_Y1
8	0x0A	Fast channel: Y2	SENT_CHANNEL_Y2
9	0x23	Temperature code	TS_CODE
10	0x29	Sensor ID1	SENT_SENSOR_ID1
11	0x2A	Sensor ID2	SENT_SENSOR_ID2
12	0x2B	Sensor ID3	SENT_SENSOR_ID3
13	0x2C	Sensor ID4	SENT_SENSOR_ID4
14	0x80	Magnetic field strength	CORDIC_RAD
15	0x81	User ID1	USER_ID[15:4]
16	0x82	User ID2	USER_ID[3:0]

7.9 OWI Interface

MT6511 support One-Wire-Interface via PIN OUT, which can be used to read/wirte register and program EEPROM (SPI Interface could achieve this function too). MagnTek offers the PROGRAMMER PB600-MT6511 with OWI Interface for operation conveniently. MT6511 will check the OWI request during power-on, after confirming no OWI request or OWI finished, PIN OUT of MT6511 will convert to expected mode (Analog, PWM or SENT).

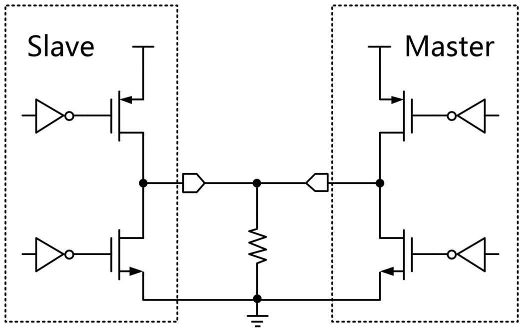


Figure-31: OWI Interface

8. Output Characteristic

Under default configuration of MT6511, the mechanical angle position of 0 ~ 360 ° corresponds to: Analog output 0 ~ 100% VDD, PWM output 0 ~ 99.9% duty cycle and SENT output 12-bit angle 0x000 ~ 0xfff. The output characteristic of Analog output, PWM output and SENT output can be programmed as required (see Chapters 8.1 ~ 8.3). However, the ABZ, UVW and the 15-bit angle data read through the SPI interface always correspond to the linear relationship of the angle position 0 ~ 360 °, which can not be programmed.

8.1 Programmable Output Transfer Characteristic

The analog output transfer function of MT6511 is programmable. It could be defined by 'Clamp_high', 'Clamp_low', '8-Point' (angle and voltage), ZERO and DP parameters, as shown in Figure-32. All angle are referred to 'ZERO' point which can be programmed with the 12-bit register ZERO[11:0] shown in Table-32.

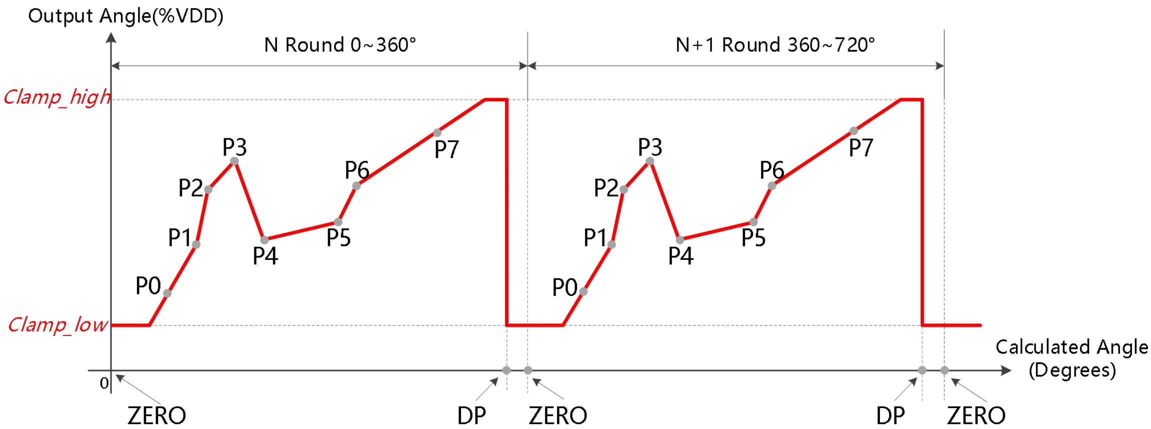


Figure-32: Output Transfer Function(Analog/PWM/SENT)

As shown in Figure-33, the Discontinuity Point (DP) could be programmed and should be placed at an unused angle range between 0~360°.

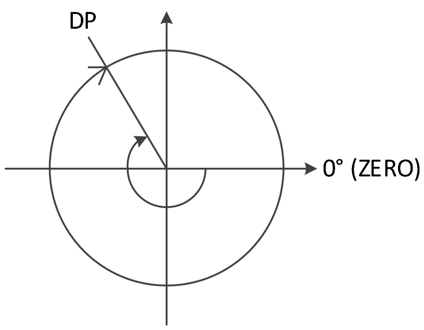


Figure-33: DP Position

Table-32: The 'ZERO[11:0]' and 'DP[15:0]' Register

Register	Value	Description
ZERO[11:0]	12 bits	12-bit Data Represent 0~360°
DP[15:0]	16 bits	16-bit Data Represent 0~360°

8.2 Arbitrary 8-Point Transfer Function and Parameters

The arbitrary '8-Point' register could be programmed for special output shapes or for better linearity as shown in Figure-34.

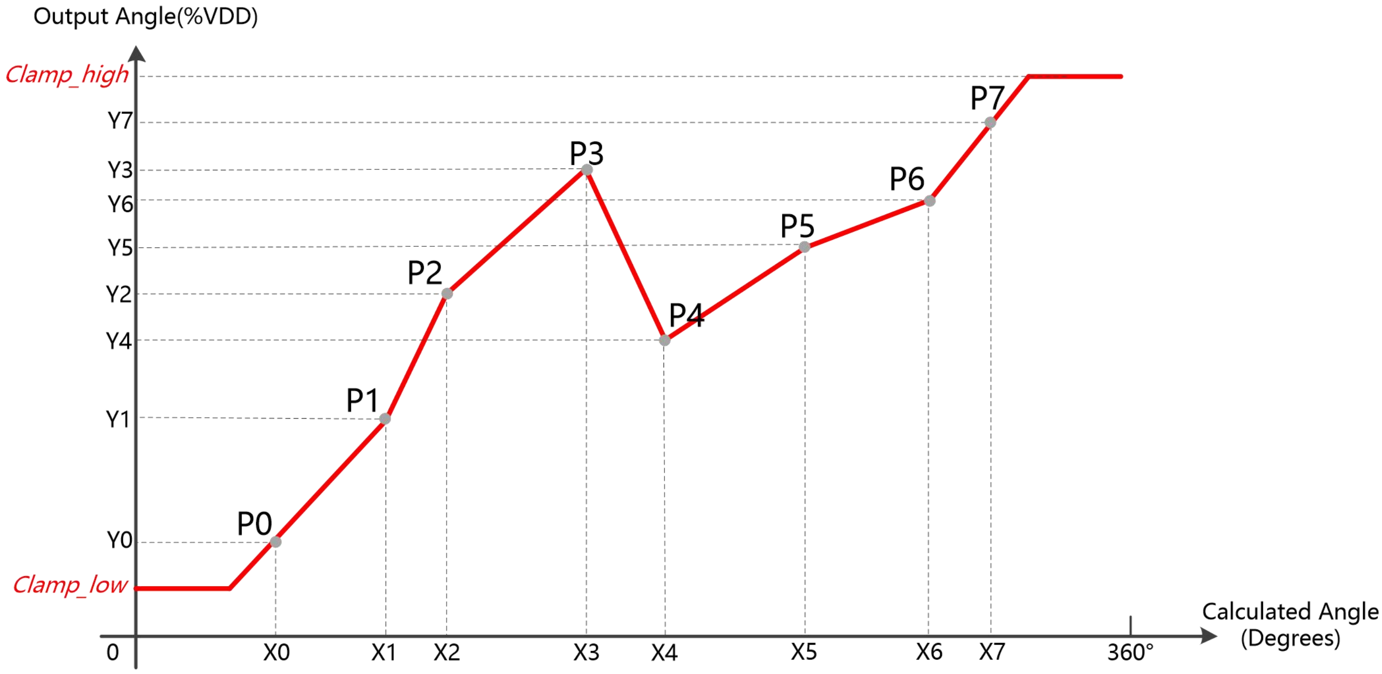


Figure-34: 8-Points Programmable Output Transfer Function (Analog/PWM/SENT)

Table-33: The '8-Point' Register

Register	Value	Description
Angle_P0[15:0]~Angle_P7[15:0]	16 bits	16-bit data represent 0~360°
Voltage_P0[11:0]~Voltage_P7[11:0]	12 bits	12-bit data represent 0~100% VDD

The clamping levels are two independent values to limit the analog output voltage range. Both the parameters have 12 bits data with the resolution of 0.024%VDD.

Table-34: The 'Clamp_High[11:0]', 'Clamp_Low[11:0]' Register

Register	Value	Description
Clamp_High[11:0]	12 bits	12-bit data represent 0~100% VDD
Clamp_Low[11:0]	12 bits	12-bit data represent 0~100% VDD

8.3 17-Point Piece-wise Transfer Function and Parameters

MT6511 also provides the output characteristic of 17-Point piece-wise-linear, as shown in Figure-35. 17-Point programming can significantly improve the angle linearity of the output. 17-Point programming has a total of 16 segments, and the total range is defined by register ' 17P_ SPAN' as shown in Table-35. After each range is selected, the corresponding span ΔR between each two points is also unique. The starting angle point of 17-Point is defined by the register '17P_START '.

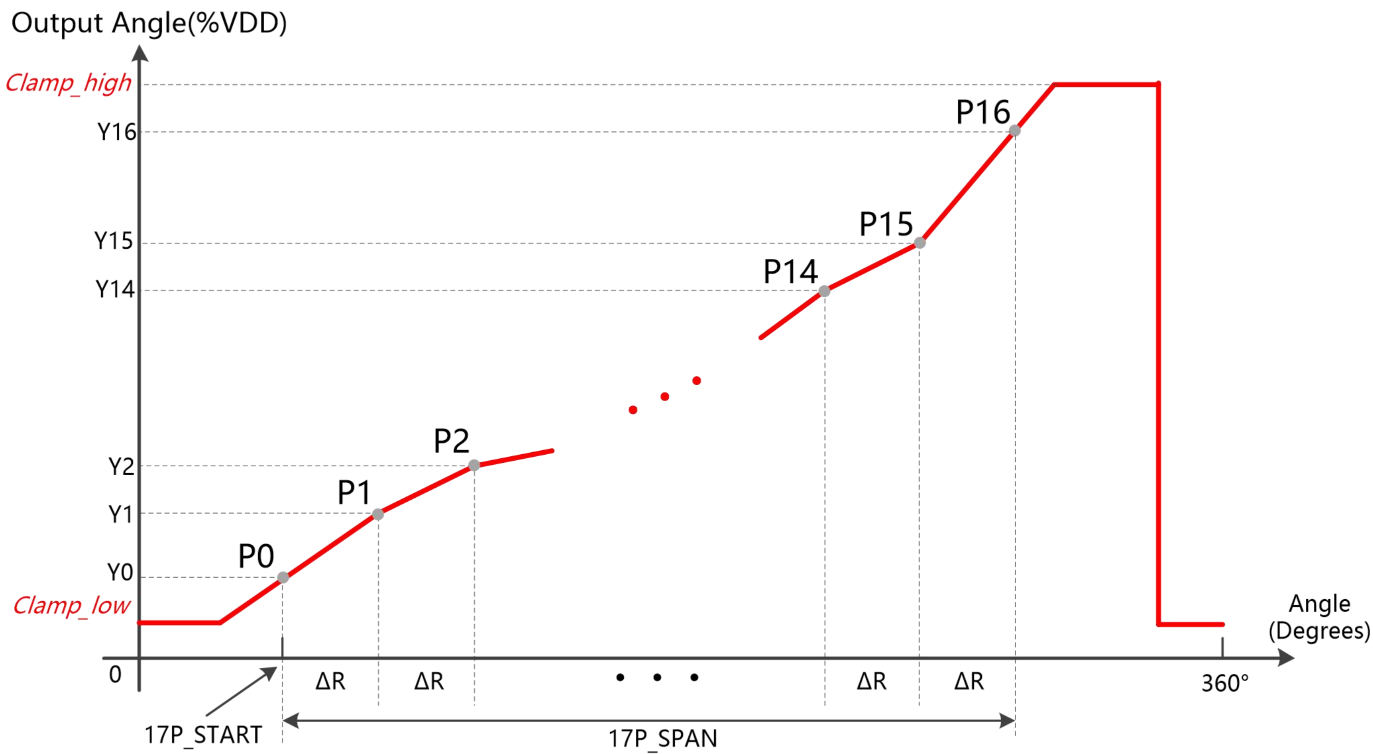


Figure 35: 17-Points Programmable Output Transfer Function (Analog/PWM/SENT)

Table-35: 17-Point Range

17P_SPAN	Range(°)	ΔR(°)	17P_SPAN	Range(°)	ΔR(°)
0x0	360	22.5	0x8	180	11.3
0x1	320	20.0	0x9	144	9.0
0x2	288	18.0	0xA	120	7.5
0x3	261.8	16.4	0xB	102.9	6.4
0x4	240	15.0	0xC	90	5.6
0x5	221.5	13.8	0xD	80	5.0
0x6	205.7	12.9	0xE	72	4.5
0x7	192	12.0	0xF	65.5	4.1

9. Functional Safety

9.1 Safety Manual

The safety manual, available upon customer request, contains the necessary information to integrate the MT6511 component in a safety-compliant application, as Safety Element Out-of-Context (SEooC).

It includes:

- The description of the Product Development lifecycle tailored for the Safety Element.
- An extract of the Technical Safety concept.
- The description of Assumptions-of-User of the element with the respect to its intended use, including:

  (1) assumption on the device safe state;
  (2) assumption on fault tolerant time interval and multiple-point faults detection interval;
  (3) assumption on the context, including its external interface;

- The description of safety analysis results at the device level useful for the system integrator; HW architectural metrics and description of the dependent failures initiators.
- The description and the result of the functional safety assessment process; list of confirmation measures and description of the independency level.

9.2 Integrated Diagnostic Mechanism

According to ISO26262 standard, MT6511 provides numerous self-diagnostic features (safety mechanisms). Those features increase the robustness of the IC functionality as it will prevent the IC from providing erroneous output signal in case of internal or external failure modes. When failure mode is triggered, the output analog signal should be set to >=96%VDD or <=4%VDD (or >=96%DutyCycle or <=4%DutyCycle for PWM). A unique diagnostic code is set in register DIAG_CODE[15:0], each bit indicating a fault condition or failure mode.

After the chip enters to Failure Mode, in most cases, it can recover once the fault condition disappears. But for some faults such as NVM CRC failure, it stays in Failure Mode until system reset or power cycling. Each diagnostic check can be individually turned on and off by setting register ‘DIAG_EN[15:0]’, each bit mapped to the same failure mode as in register ‘DIAG_CODE[15:0]’.

Table-36: The 'DIAG_CODE[15:0]' Register

Bit Number	Function Description (logic '1' means failure)
0	Over-Voltage Detection
1	Under-Voltage Detection
2	Bandgap Failure
3	LDO Failure
4	Temperature Check
5	Oscillator Failure
6	EEPROM Data Loading CRC Failure
7	Magnetic Field too Weak
8	Magnetic Field too Strong
9	Analog Signal Path Check Failure
10	Digital Signal Path Check Failure
11	Loss of Tracking (Angle Velocity Over Speed)
12	NA
13	NA
14	NA
15	NA

Table-37: Failure Modes and Their Responding Reporting and Recovery Method

Failure Mode	Reporting Method	Recovery Method
Over-Voltage Detection	Analog/SPI	Power Supply Voltage Recovery
Under-Voltage Detection	Analog/SPI	Power Supply Voltage Recovery
Bandgap Failure	Analog/PWM/SPI/SENT	Failure Disappears
LDO Failure	Analog/PWM/SPI/SENT	Failure Disappears
Temperature Check	Analog/PWM/SPI/SENT	Failure Disappears
Oscillator Failure	Analog/PWM/SPI/SENT	Failure Disappears

Failure Mode	Reporting Method	Recovery Method
EEPROM Data Loading CRC Failure	Analog/PWM/SPI/SENT	EEPROM Reload Correctly
Magnetic Field too Weak	Analog/PWM/SPI/SENT	Failure Disappears
Magnetic Field too Strong	Analog/PWM/SPI/SENT	Failure Disappears
Analog Signal Path Check Failure	Analog/PWM/SPI/SENT	Failure Disappears
Digital Signal Path Check Failure	Analog/PWM/SPI/SENT	Failure Disappears
Loss of Tracking	Analog/PWM/SPI/SENT	Failure Disappears
Broken Supply Wire Detection (**Note[4]**)	Analog/PWM/SENT	Failure Disappears
Broken Ground Wire Detection (**Note[5]**)	Analog/PWM/SENT	Failure Disappears

Note[4]: If Supply Broken，MT6511(Analog/PWM/SENT) could output low(<4%VDD) ≥10 Seconds (when external pull-up resistor ≥5KΩ) ；

Note[5]: If Ground Broken，MT6511(Analog/PWM/SENT) could output high(>96%VDD) ≥10 Seconds (when external pull-down resistor ≥5KΩ) ；

Table-38: Failure Modes Reporting Method

Reporting Method	Description
Analog	(1) Output to <=4%VDD or >=96%VDD Defined by Register ‘DIAG_DRV_LVL’ ; (2) Over-Voltage/Under-Voltage Detection: Output driver is disabled, an internal 20-Kohm pull-down resistor is present at the output (Appliable to analog, PWM and SENT mode).
PWM	(1) Output the Frame Defined by the 12-bit Register ‘DIAG_PWM_CODE[11:0]’ (2) Over-Voltage/Under-Voltage Detection: Output driver is disabled, an internal 20-Kohm pull-down resistor is present at the output (Appliable to analog, PWM and SENT mode).
SENT	(1) Status Bit[0] is Set to ‘1’ (2) Over-Voltage/Under-Voltage Detection: Output driver is disabled, an internal 20-Kohm pull-down resistor is present at the output (Appliable to analog, PWM and SENT mode).
SPI	The corresponding of Safety-Word Bit[15:12] is Set to ‘0’

10. Recommended Application Diagrams

10.1 Reference Circuit of Analog Output Mode

Figure-36 shows the reference circuit for typical applications that use the analog output. Please be note, the capacitance loading at the analog out should be less than 110nf, otherwise may cause the chip instable.

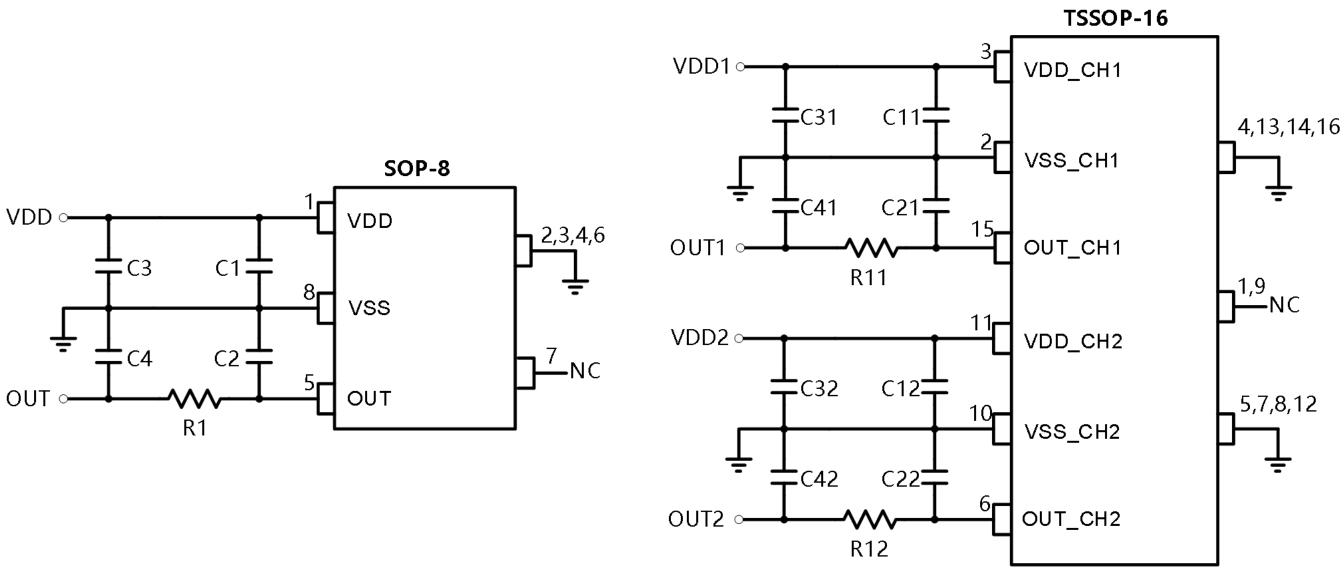


Figure-36: Reference Application Circuit for Analog Output Mode

Table-39: Recommend R, C Component Values for Analog Output

Compact PCB Routing		
C1, C11, C12	100nF	Analog Output Mode
C2, C21, C22	100nF	
Optimal EMC Performance		
C1, C11, C12	100nF	Close to IC Terminals
C2, C21, C22	100nF	Close to IC Terminals
C3, C31, C32 C4, C41, C42	1nF	Close to Connector
R1, R11, R12	51Ω	Increased Ratiometric Error of Analog Output

10.2 Reference Circuit of Analog+SWO Output Mode

Figure-37 shows the reference circuit for typical applications that use analog and SWO output. Please be note, the capacitance loading at the analog out should be less than 110nf, otherwise may cause the chip instable.

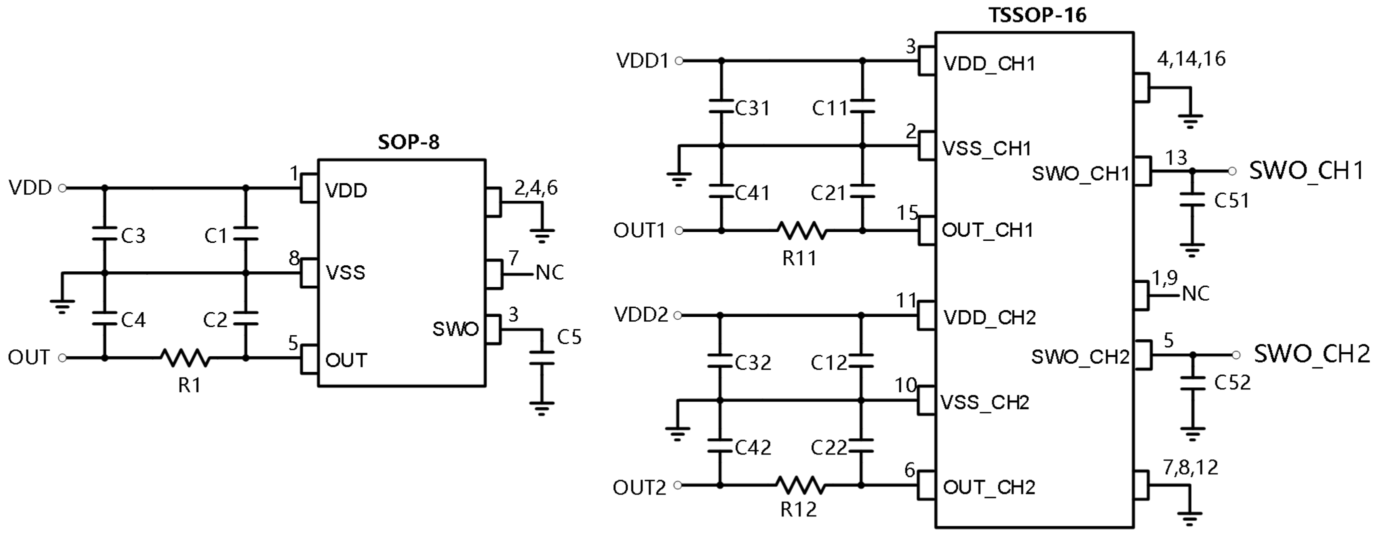


Figure-37: Reference Application Circuit for Analog+SWO Output Mode

Table-40: Recommend R, C Component Values for Analog+SWO Output

Compact PCB Routing		
C1, C11, C12	100nF	Analog+SWO Output Mode
C2, C21, C22	100nF	
C5, C51, C52	1nF	
Optimal EMC Performance		
C1, C11, C12	100nF	Close to IC Terminals
C2, C21, C22	100nF	Close to IC Terminals
C3, C31, C32 C4, C41, C42	1nF	Close to Connector
C5, C51, C52	1nF	Close to Connector
R1, R11, R12	51Ω	

10.3 Reference circuit of PWM/SENT Output Mode

Figure-38 shows the reference circuit for typical applications that use PWM/SEMT Mode with Push-Pull output.

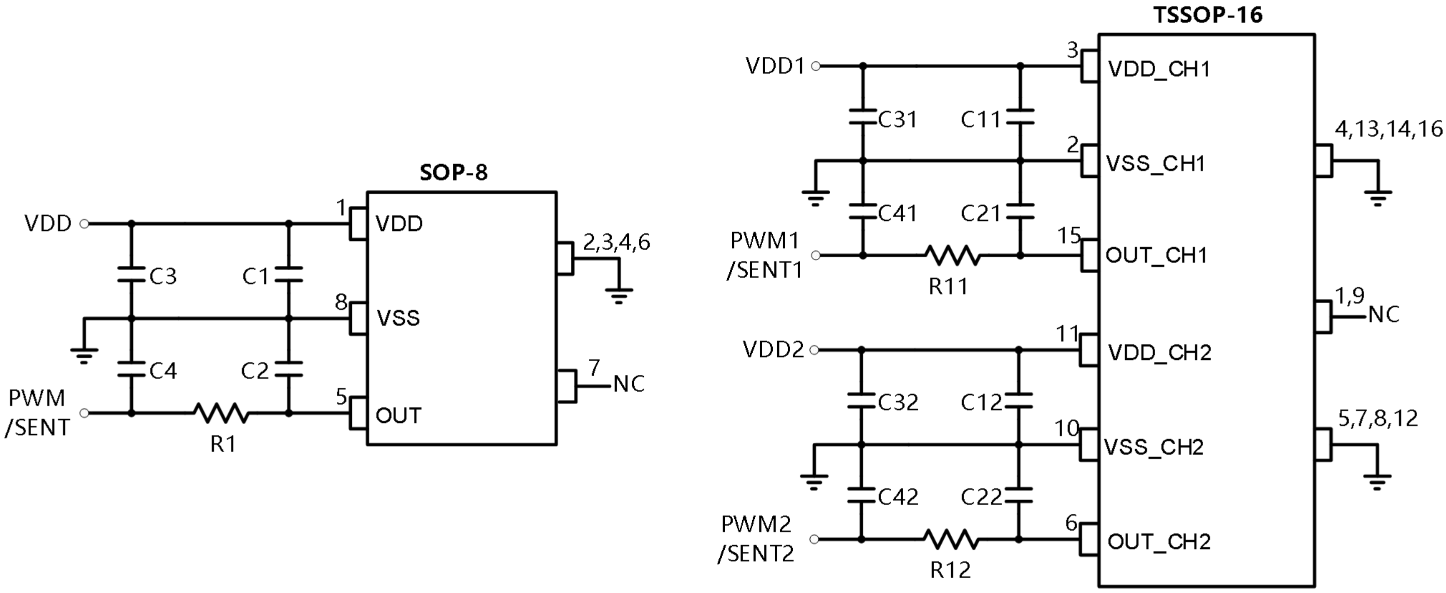


Figure-38: Reference Application Circuit for PWM/SENT Mode with Push-Pull Output

Table-41: Recommend R, C Component Values for PWM/SENT with Push-Pull Output

Compact PCB Routing		
C1, C11, C12	100nF	PWM/SENT Mode with Push-Pull Output
C2, C21, C22	1nF	
Optimal EMC Performance		
C1, C11, C12	100nF	Close to IC Terminals
C2, C21, C22	1nF	Close to IC Terminals
C3, C31, C32	1nF	Close to Connector
C4, C41, C42	1nF	Close to Connector
R1, R11, R12	51Ω	

Figure-39 shows the reference circuit for typical applications that use PWM/SENT Mode with open-drain output.

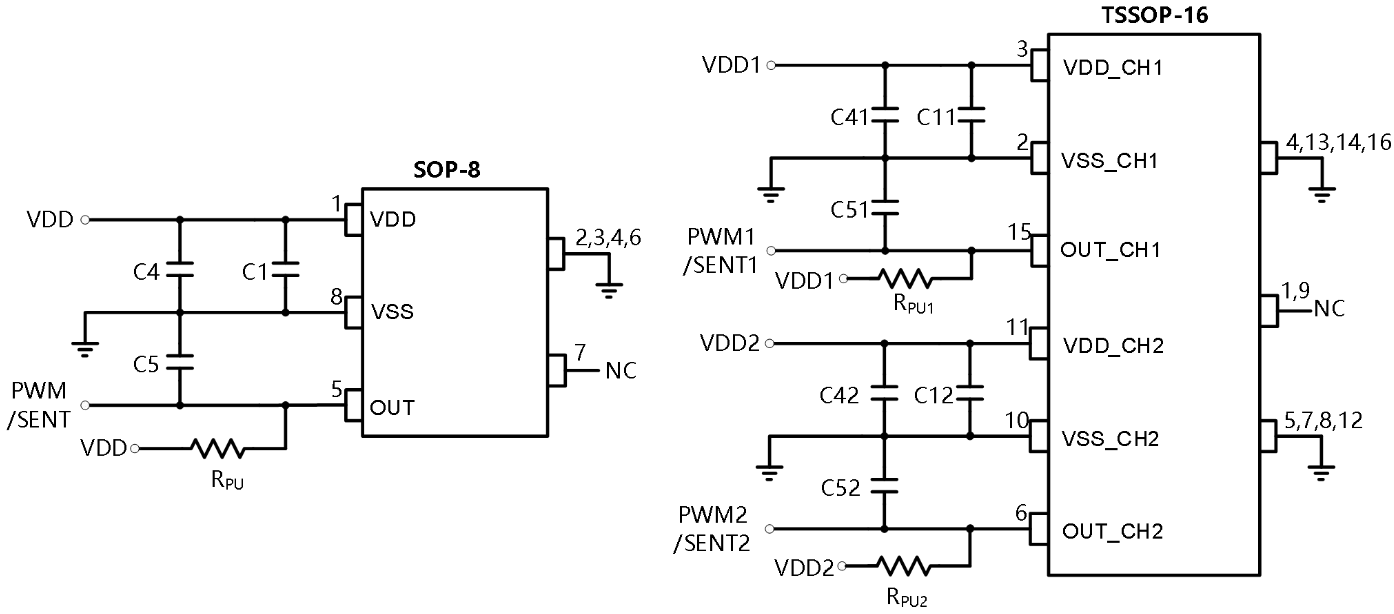


Figure-39: Reference Application Circuit for PWM/SENT Mode with Open-Drain Output

Table-42: Recommend R, C Component Values for PWM/SENT with Open-Drain Output

Compact PCB Routing		
C1, C11, C12	100nF	PWM/SENT Mode with Open-Drain Output
R_{PU}, R_{PU1}, R_{PU2}	1.0kΩ	
Optimal EMC Performance		
C1, C11, C12	100nF	Close to IC Terminals
C4, C41, C42	10nF	Close to Connector
C5, C51, C52	100pF	Close to Connector
R_{PU}, R_{PU1}, R_{PU2}	1.0kΩ	Close to IC Terminals

10.4 Reference circuit of SPI Interface

Figure-40 shows the reference circuit for typical applications that use 3-Wire SPI interface.

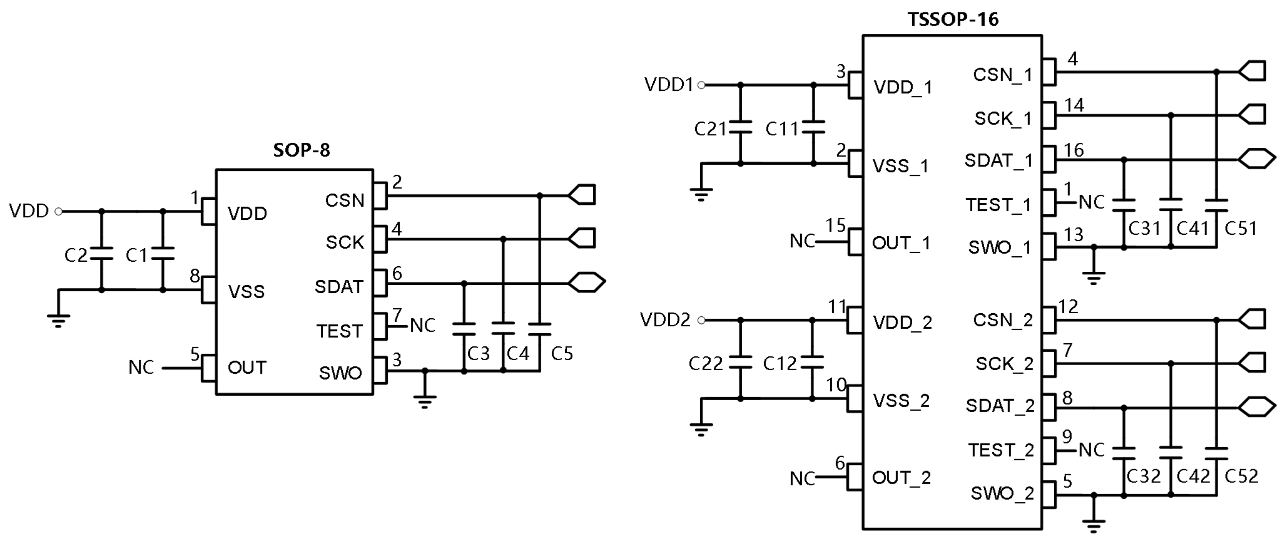


Figure-40: Reference Application Circuit for 3-Wire SPI Interface

Table-43: Recommend R, C Component Values for SPI Interface

Compact PCB Routing		
C1, C11, C12	100nF	3-Wire SPI Mode
Optimal EMC Performance		
C1, C11, C12	100nF	Close to IC Terminals
C2, C21, C22	1nF	Close to Connector
C3, C31, C32	100pF	Close to Connector
C4, C41, C42	100pF	Close to Connector
C5, C51, C52	100pF	Close to Connector

10.5 Reference circuit of ABZ/UVW Output Mode

Figure-41 shows the reference circuit for typical applications that use ABZ or UVW output mode.

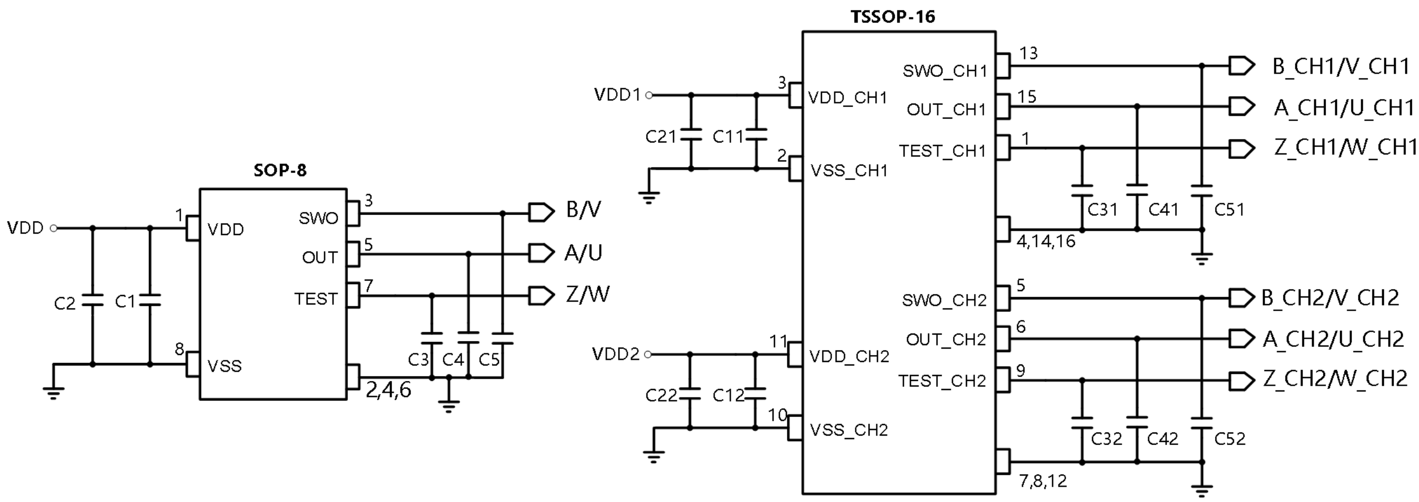


Figure-41: Reference Application Circuit for ABZ/UVW Output Mode

Table-44: Recommend R, C Component Values for ABZ/UVW Output

Compact PCB Routing		
C1, C11, C12	100nF	ABZ or UVW Output Mode
Optimal EMC Performance		
C1, C11, C12	100nF	Close to IC Terminals
C2, C21, C22	1nF	Close to Connector
C3, C31, C32	100pF	Close to Connector
C4, C41, C42	100pF	Close to Connector
C5, C51, C52	100pF	Close to Connector

11. Mechanical Angle and Direction

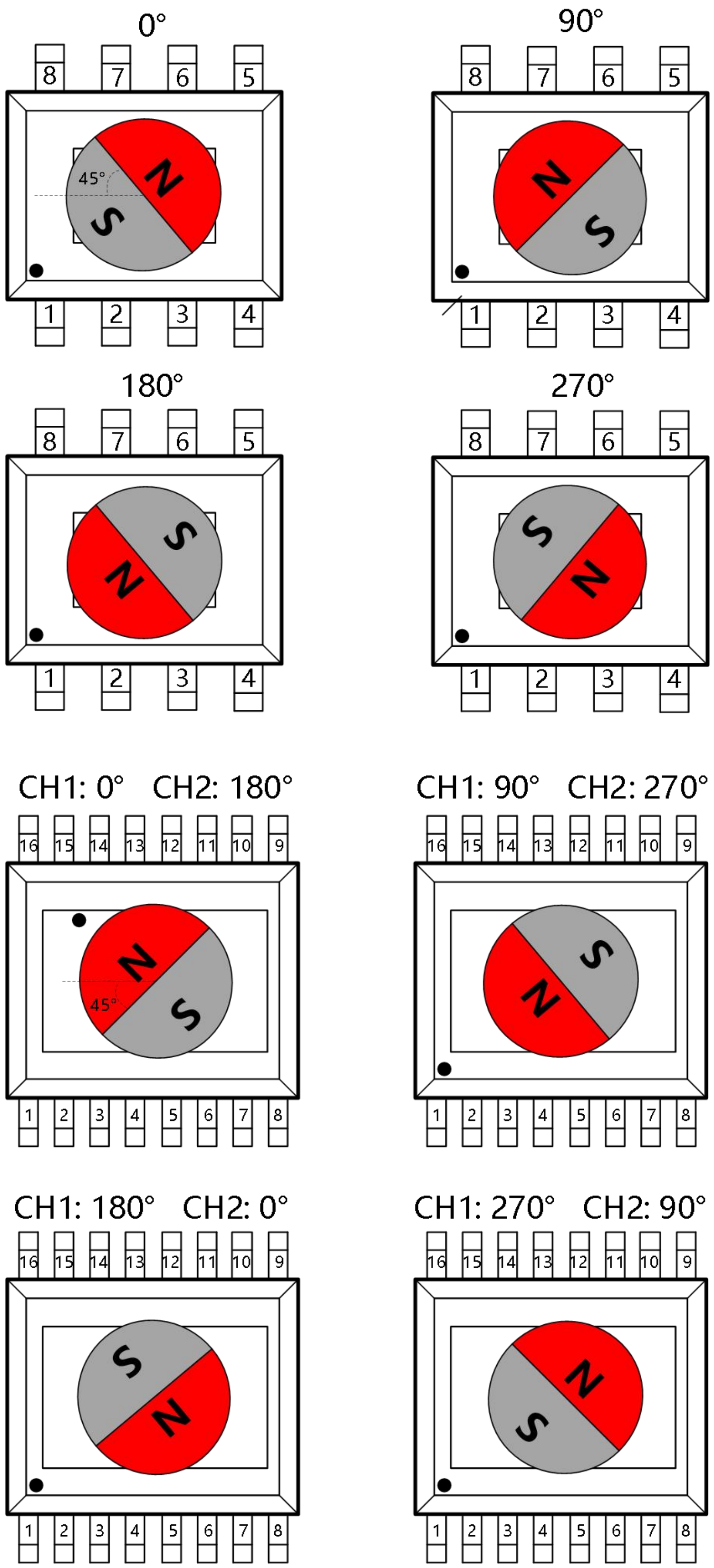
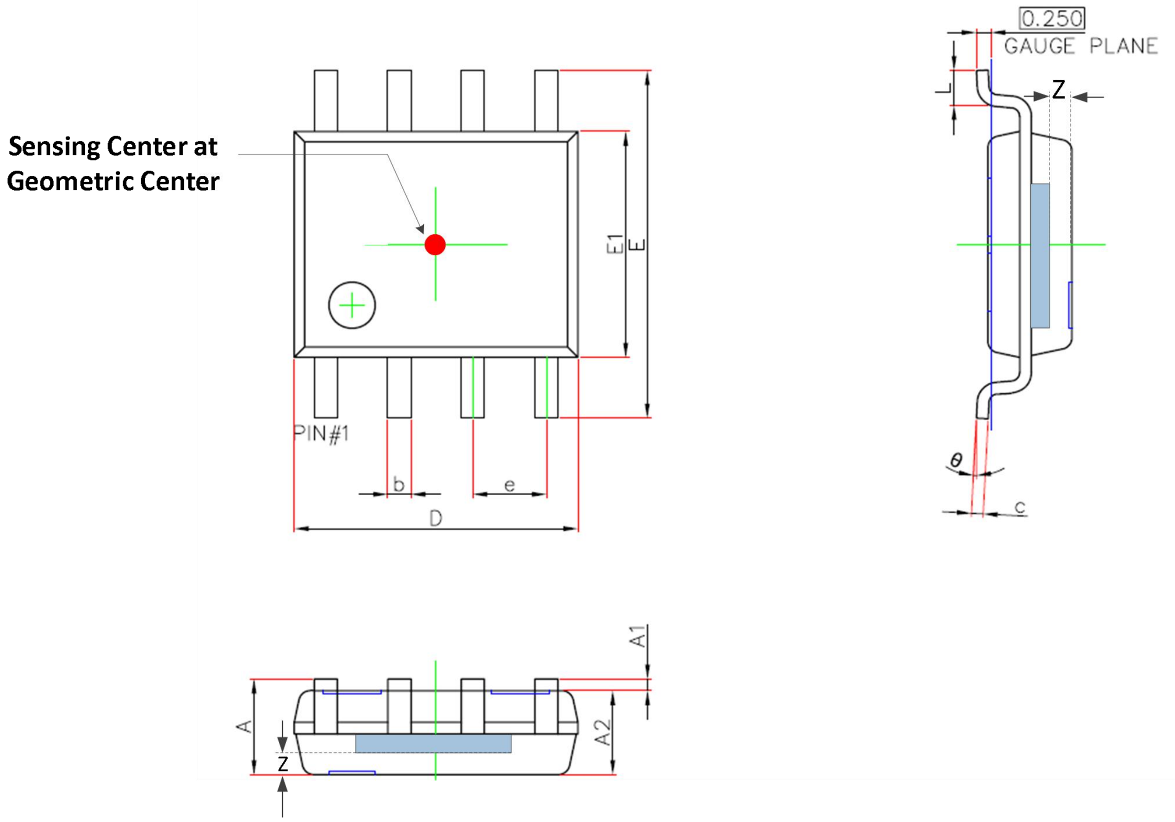


Figure-42: Magnet-Chip Mechanical Angle and Direction

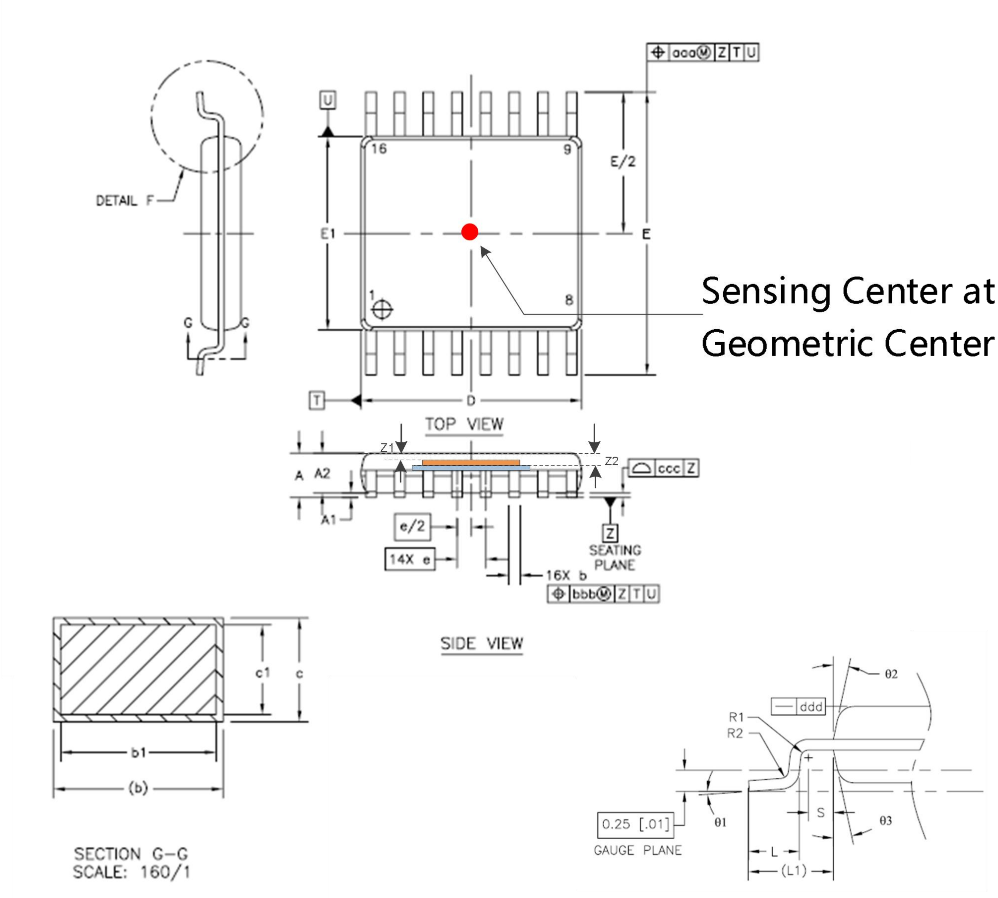
12. Package Information

12.1 SOP-8 Package



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max
A	1.450	1.750	0.057	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.55	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°
Z	0.380	0.580	0.011	0.023

12.2 TSSOP-16 Package



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
D	4.900	5.100	0.193	0.201
E	6.300	6.500	0.248	0.256
b	0.190	0.270	0.007	0.011
c	0.130	0.180	0.005	0.007
E1	4.300	4.500	0.169	0.177
A	-	1.100	-	0.043
A1	0.050	0.150	0.002	0.006
A2	0.850	0.950	0.033	0.037
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
θ1	0°	8°	0°	8°
θ2	12° TYP		12° TYP	
θ3	12° TYP		12° TYP	
Z1	0.100	0.300	0.004	0.012
Z2	0.250	0.450	0.0008	0.0016

13. Copy Rights and Disclaimer

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14. Revision History

Revision	Date	Comments
0.1	2021.06	Initial Release as Draft
0.5	2022.03	Pre-Mass-Production Version
1.0	2022.09	Official Release
1.1	2022.10	Update Part Number Information in Table-6
1.2	2023.06	Update Electrical Characteristics in Table-5