NSI3602D-Q1

High Reliability Reinforced Isolated Amplifier with Integrated Isolated Power Supply

Datasheet (EN) 1.0

Product Overview

The NSI3602D is a high performance isolated amplifier with integrated isolated power supply that accept fully-differential input of ±50mV. The integrated isolated power supply enables single-power operation on the low side of the device without the need for a separate isolated power supply for the high side, effectively reducing the board area. The fully differential input is ideally suited for AC or shunt current monitoring in high voltage applications where isolation is required.

The device has a fixed gain of 41 and provides a differential analog output. The low offset and gain drift ensure the accuracy over the entire temperature range. High common-mode transient immunity ensures that the device is able to provide accurate and reliable measurements even in the presence of high-power switching such as in power supply and motor control applications.

The integrated isolated power supply detection and the open-drain diagnosis output simplify system-level design and diagnostics.

Key Features

- Up to 5000V_{rms} Insulation voltage
- ±50mV linear Input Voltage Range
- Low Offset Error and Drift:

  ±50μV (Max), ±0.6μV/°C (Max)
- Low Gain Error and Drift:

  ±0.25% (Max), ±50ppm/°C (Max)
- Low Nonlinearity and Drift:

  ±0.05% (Max), ±1ppm/°C (Typ)
- SNR: 80dB (Typ, BW=10kHz), 71dB (Typ, BW=100kHz)
- Wide bandwidth: 350kHz (Typ)
- High CMTI: 150kV/μs (Typ)
- System-Level Diagnostic Features: integrated isolated power supply detection
- Operation Temperature: -40°C ~125°C
- AEC-Q100 qualified for automotive applications: Grade 1
- RoHS-Compliant Packages: SOP16(300mil)

Safety Regulatory Approvals

- UL recognition: up to 5000Vrms for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- On Board Chargers
- DC/DC Converters
- Charging Piles
- Traction Inverters
- Battery Management Units

Device Information

Part Number	Package	Body Size
NSI3602D-Q1SWR	SOP16(300mil)	10.30mm × 7.50mm

Functional Block Diagrams

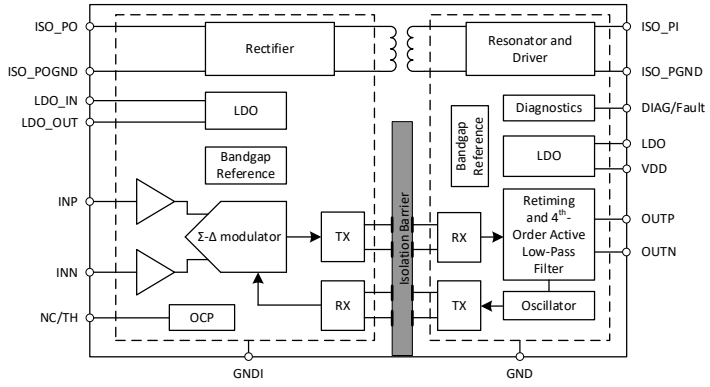

Figure 1. Function Block Diagram of NSI3602D

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1. Pin Configuration and Functions

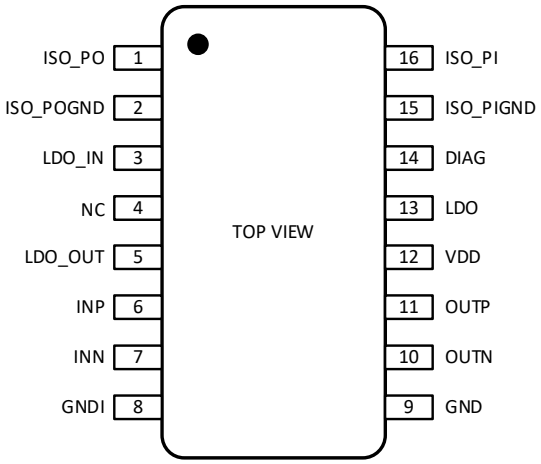


Figure 1.1 NSI3602D Package

Table 1.1 NSI3602D Pin Configuration and Description

NSI3602D PIN NO.	*SYMBOL*	*FUNCTION*
1	ISO_PO	Internal isolated power output (need to be connected to the LDOIN pin)
2	ISO_POGND	Internal isolated power ground reference (need to be connected to the GNDI pin)
3	LDO_IN	Internal input side LDO power input (need to be connected to the ISO_PO pin)
4	NC	Not internal connected, leave this pin floating or connect to GNDI pin.
5	LDO_OUT	Internal input side LDO power output
6	INP	Positive analog input (Either INP or INN must have a DC current path to HGND to define the common-mode input voltage)
7	INN	Negative analog input (Either INP or INN must have a DC current path to GNDI to define the common-mode input voltage)
8	GNDI	Input side ground reference (need to be connected to the ISO_PGND pin)
9	GND	Output side ground reference (need to be connected to the ISO_PGND pin)
10	OUTN	Negative analog output
11	OUTP	Positive analog output
12	VDD	Output side power supply
13	LDO	Internal output side LDO power input (need to be connected to the ISO_PI pin)
14	DIAG	Open-drain diagnosis output (need to be connected to the pull-up supply or floating)
15	ISO_PIGND	Internal isolated power ground reference (need to be connected to the GND pin)
16	ISO_PI	Internal isolated power input (need to be connected to the LDO pin)

2. Absolute Maximum Ratings(1)

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	VDD to GND	-0.3		6.5	V
Analog Input Voltage	INP, INN	AGND-6		AVDD+0.5	V
Analog Output Voltage	OUTP, OUTN	GND-0.5		VDD+0.5	V
Digital Output Voltage	DIAG	GND-0.5		6.5	V
Input current per IO Pin	I_{IN}	-10		10	mA
Junction Temperature	T_J	-40		150	°C
Storage Temperature	T_{STG}	-55		150	°C

(1) The device cannot operate beyond the listed Absolute Maximum Ratings to prevent permanent device damage. The device is not fully functional if operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings. Long-time stress of the absolute maximum conditions may affect the device lifetime.

3. ESD Ratings

Parameters	Test Condition	Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD	±4.0	kV
	Charged device model (CDM), per AEC-Q100-002-RevB	±1.0	kV

(1) Though this device features proprietary protection circuitry, proper ESD precautions should be considered to avoid performance degradation of damage due to high energy ESD event. Charged devices and circuit boards may discharge without detection.

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply	VDD to IGND	3.0	3.3	5.5	V
Differential input voltage before clipping output	$V_{Clipping}$		±64		mV
Linear differential input full scale voltage	V_{FSR}	-50		50	mV
Absolute common-mode input voltage	V_{CM}	-2		V_{LDO_OUT}	V
Operating common-mode input voltage	V_{CM}	-0.16		1	V
DIAG pull-up supply voltage	V_{DIAG}	0		VDD	V
Operating Ambient Temperature	T_A	-40		125	°C

5. Thermal Information

Parameters	Symbol	SOP16(300mil)	Unit
Junction–to-ambient thermal resistance	$R_{\theta JA}$	64	°C/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	30	°C/W

Parameters	Symbol	SOP16(300mil)	Unit
Junction-to-board thermal resistance	$R_{\theta JB}$	33.3	°C/W
Junction–to-top characterization parameter	Ψ_{JT}	10.9	°C/W
Junction-to-board characterization parameter	Ψ_{JB}	28.2	°C/W

6. Specifications

6.1. Electrical Characteristics

(VDD = 3.0V ~ 5.5V, INP =-50mV to +50mV, and INN = GNDI = 0V, T_A = -40°C to 125°C. Unless otherwise noted, Typical values are at VDD = 3.3V, T_A = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Output side supply voltage	VDD	3.0	3.3	5.5	V	
Output side supply current	IDD		31.3	40.9	mA	no external load on LDO_OUT
	IDD		32.6	42.2	mA	1mA external load on LDO_OUT
External load current on Input side LDO	I_E			1	mA	
Isolated power output voltage	V_{ISO_PO}	3	3.5	4.6	V	ISO_PO to IGND
Input side LDO output voltage	V_{LDO_OUT}	3	3.2	3.3	V	LDO_OUT to IGND
Isolated power output undervoltage detection threshold voltage	V_{ISO_POUV}	2.1	2.3	2.8	V	Isolated power output falling
Input side LDO undervoltage detection threshold voltage	V_{LDO_UV}	2.1	2.3	2.8	V	LDO_OUT falling
VDD undervoltage detection threshold voltage	VDD_{UV}			2.95	V	
Analog Input						
Input offset voltage	V_{OS}	-50	±15	50	μV	INP = INN = GND1, at T_A = 25°C
Input offset drift (1)	TCV_{OS}	-0.6	1	0.6	μV/°C	
Common-mode rejection ratio	$CMRR_{dc}$		-100		dB	INP = INN, f_{IN} = 0 Hz, $V_{CM\ min} \le VIN \le V_{CM\ max}$
	$CMRR_{ac}$		-98		dB	INP = INN, f_{IN} = 10 kHz, $V_{CM\ min} \le VIN \le V_{CM\ max}$
Single-ended input resistance	R_{IN}		4.75		kΩ	INN = GND1
Differential input resistance	R_{IND}		4.9		kΩ	
Input capacitance	C_I		3.75		pF	Single-ended input capacitance, fin=310kHz

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Input capacitance	C_{ID}		1.875		pF	Differential input capacitance, fin=310kHz
Input bias current	I_{IB}	-25	-20	-16	μA	INP = INN = GND1, I_{IB} = (I_{IBP} + I_{IBN}) / 2
Input bias current drift (1)	TCI_{IB}		±1		nA/°C	
Input offset current	I_{IO}		10		nA	I_{IO} = |I_{IBP} - I_{IBN} |
Analog Output						
Nominal Gain			41		V/V	
Gain error	E_G	-0.25%	±0.05%	0.25%		at T_A = 25°C
Gain error thermal drift (1)	TCE_G	-50	±15	50	ppm/°C	
Nonlinearity		-0.05%	±0.01%	0.05%		
Nonlinearity drift (1)			1		ppm/°C	
Total harmonic distortion (3)	THD		-88		dB	V_{IN} =100mVpp, f_{IN} = 10kHz, BW = 100kHz
Output noise			360		$μV_{RMS}$	INP = INN = GND1, BW = 100kHz
Signal to noise ratio	SNR	75	80		dB	V_{IN} = 100mVpp, f_{IN} = 1kHz, BW = 10kHz
	SNR		71		dB	V_{IN} = 100mVpp, f_{IN} = 10kHz, BW = 100kHz, 1MHz filter
Common-mode output voltage	V_{CMout}	1.37	1.45	1.51	V	
Differential clipping output voltage	V_{CLout}		±2.49		V	V_{OUT} = (V_{OUTP} – V_{OUTN}), |V_{IN}| = |V_{INP} – V_{INN}| > $V_{Clipping}$
Failsafe differential output voltage	$V_{FAILSAFE}$		-2.6	-2.5	V	
Output bandwidth	BW		350		kHz	
Power supply rejection ratio (2)	$PSRR_{dc}$		-127		dB	PSRR vs VDD, from 3.0~5.5V at DC
	$PSRR_{ac}$		-116		dB	PSRR vs VDD, 100mV and 10kHz ripple
Output resistance	R_{OUT}		0.3		Ω	
Output limit current	I_{lim}		±20		mA	
Common-mode transient immunity	CMTI	100	150		kV/μs	Common-mode transient immunity
Timing						
Rising time of OUTP, OUTN	t_r		1.3		μs	
Falling time of OUTP, OUTN	t_f		1.3		μs	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
INP, INN to OUTP, OUTN signal delay (50% - 50%)	t_{PD}		1.3	1.8	μs	
Analog setting time	t_{AS}		0.9		ms	VDD1 step to 3.0 V with VDD2 ≥ 3.0 V, to OUTP, OUTN valid, 0.1% settling

(1) The temperature drift is calculated with the whole temperature range (-40°C to 125°C).

(2) Input referred.

(3) THD is defined as the ratio of the sum of the rms value of first five higher harmonics to the amplitude of the fundamental (input referred).

6.2. Timing Diagrams

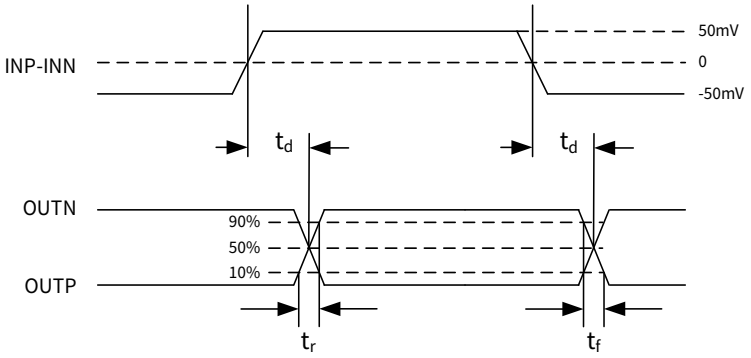


Figure 6.1 Propagation Delay and Output Fall Time Definition

6.3. Typical Performance Characteristics

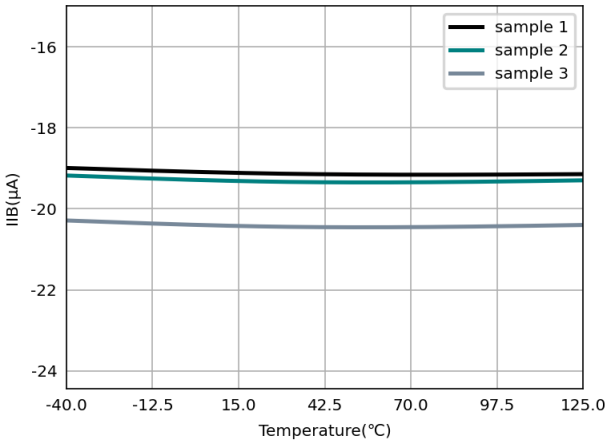


Figure 6.2 Input Bias Current vs Temperature

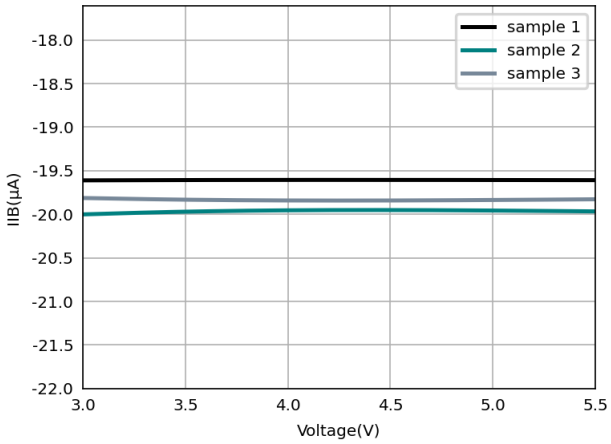


Figure 6.3 Input Bias Current vs Supply Voltage

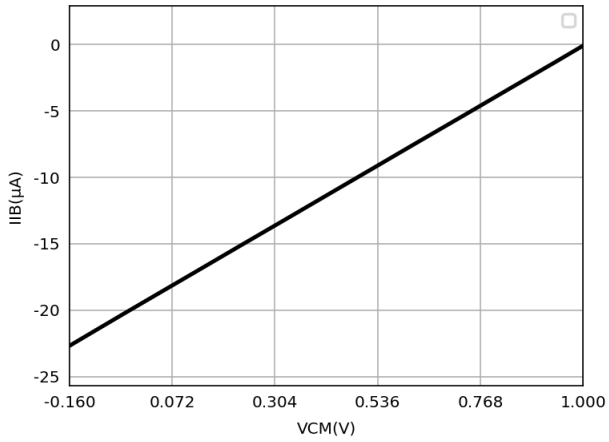


Figure 6.2 Input Bias Current vs Common-Mode Input Voltage

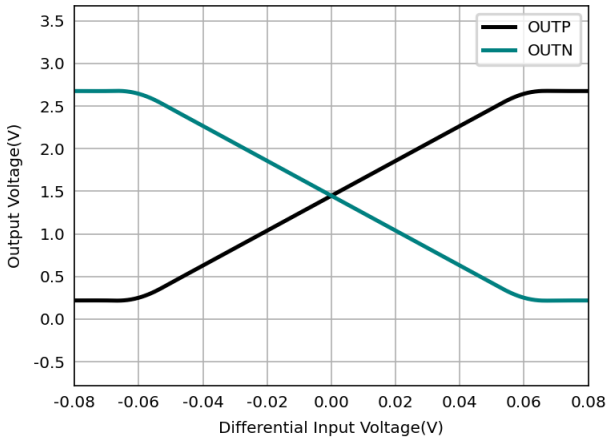


Figure 6.5 Output vs Differential Input Voltage

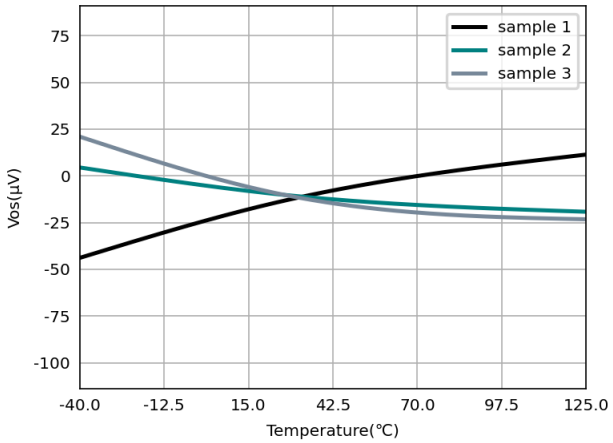


Figure 6.3 Input Offset Voltage vs Temperature

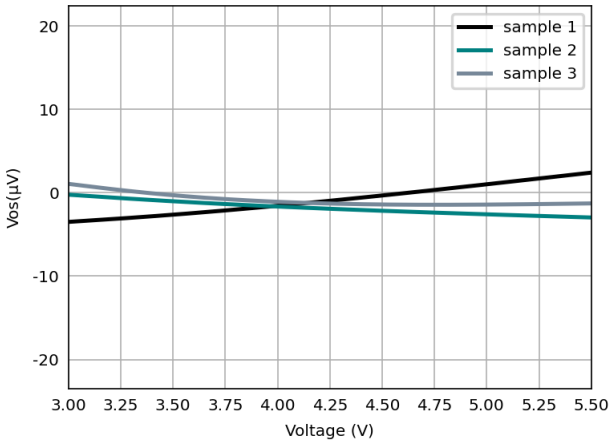


Figure 6.4 Input Offset Voltage vs Supply Voltage

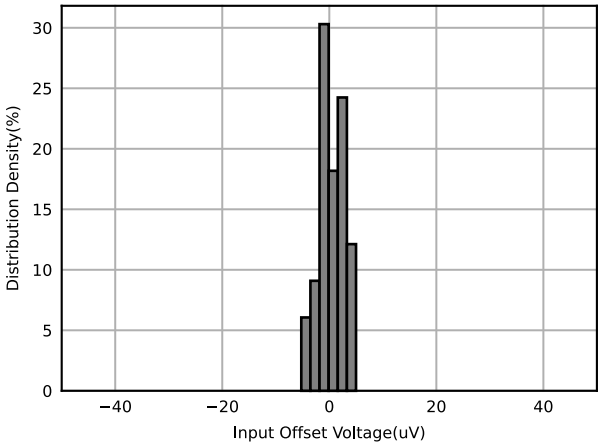


Figure 6.5 Input Offset Voltage Distribution(1)

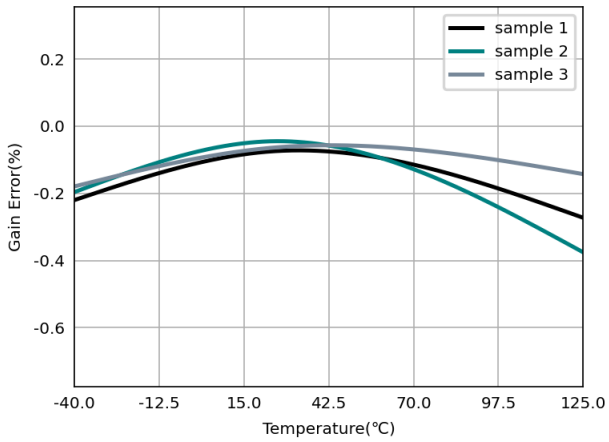


Figure 6.6 Gain Error vs Temperature

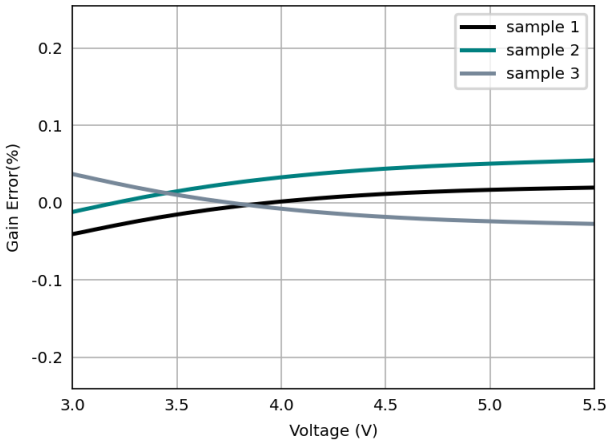


Figure 6.7 Gain Error vs Supply Voltage

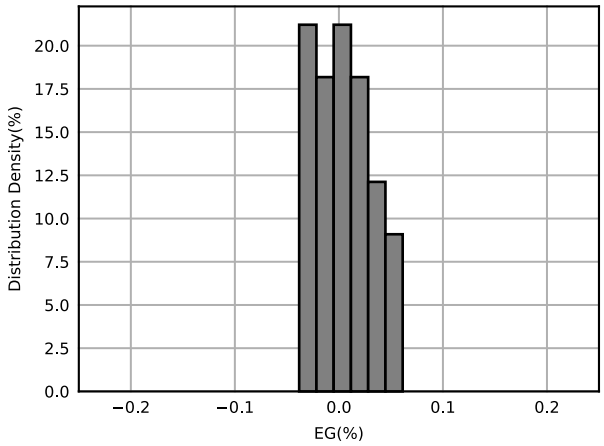


Figure 6.8 Gain Error Distribution(1)

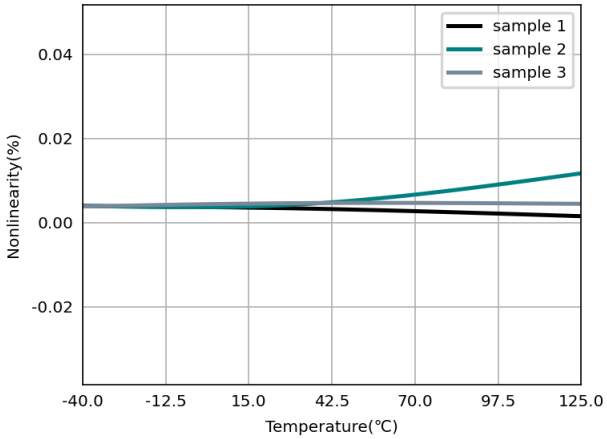


Figure 6.9 Nonlinearity vs Temperature

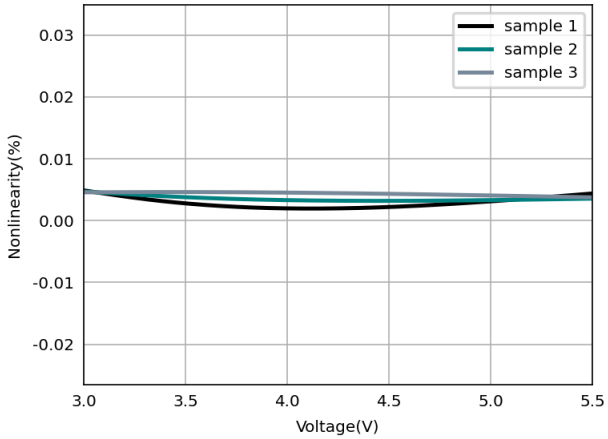


Figure 6.10 Nonlinearity vs Supply Voltage

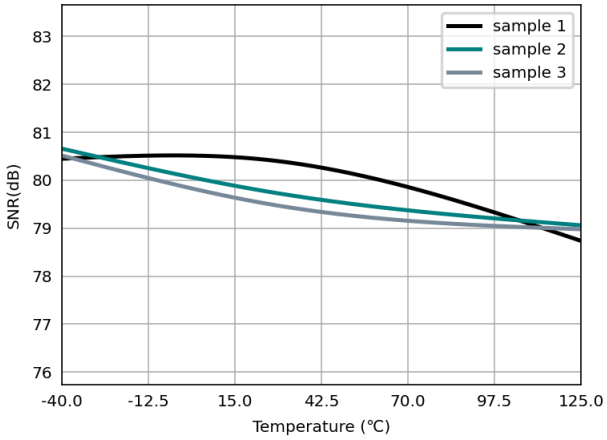


Figure 6.11 Signal to Noise Ratio vs Temperature

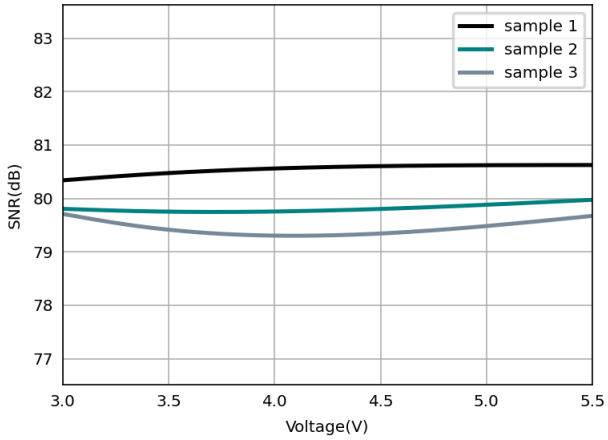


Figure 6.12 Signal to Noise Ratio vs Supply Voltage

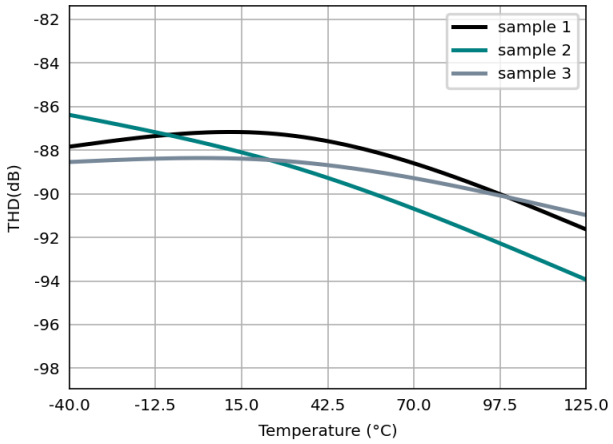


Figure 6.13 Total Harmonic Distortion vs Temperature

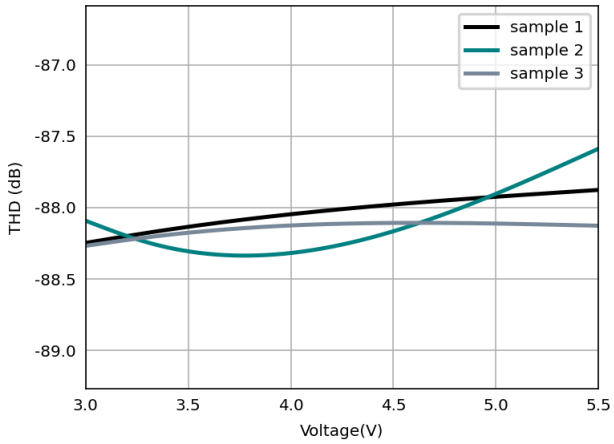


Figure 6.14 Total Harmonic Distortion vs Supply Voltage

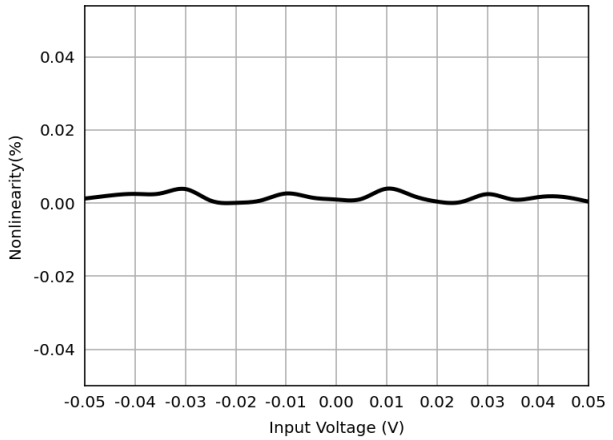


Figure 6.15 Nonlinearity vs Input Voltage

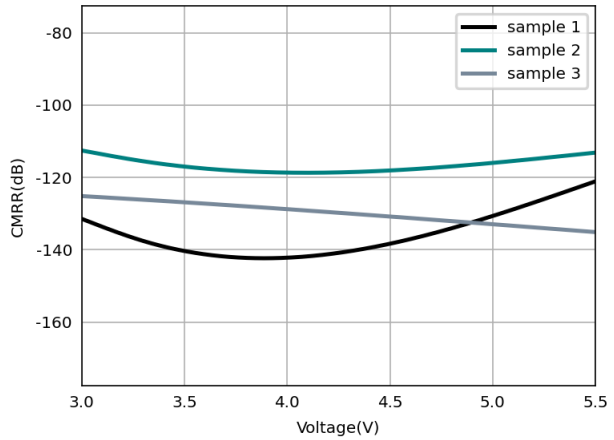


Figure 6.16 Common-Mode Rejection Ratio vs Supply Voltage

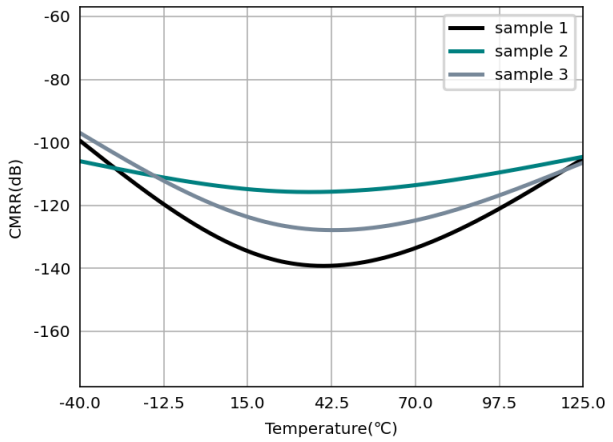


Figure 6.17 Common-Mode Rejection Ratio vs Temperature

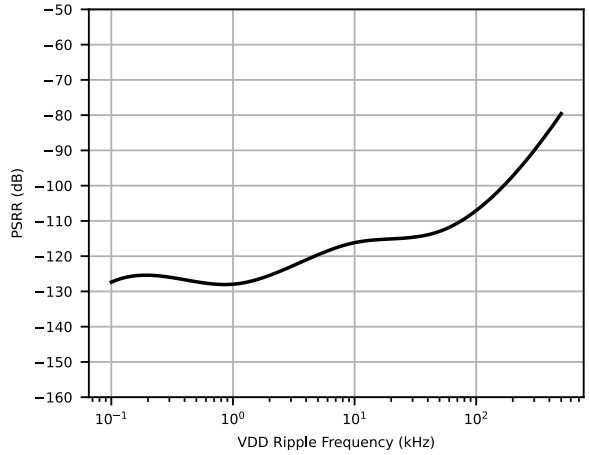


Figure 6.18 Power-Supply Rejection Ratio vs VDD Input Frequency

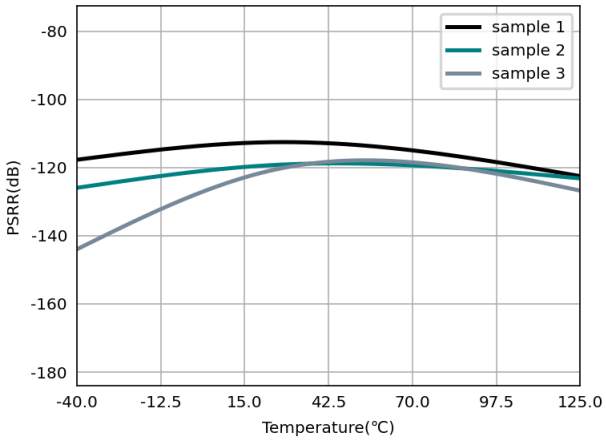


Figure 6.19 Power-Supply Rejection Ratio vs Temperature

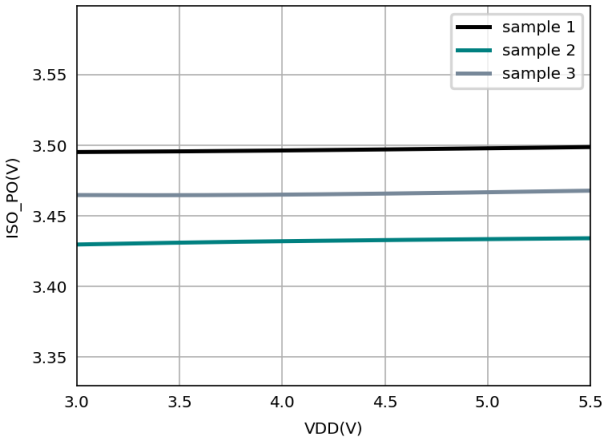


Figure 6.20 ISO-PO LDO Regulation

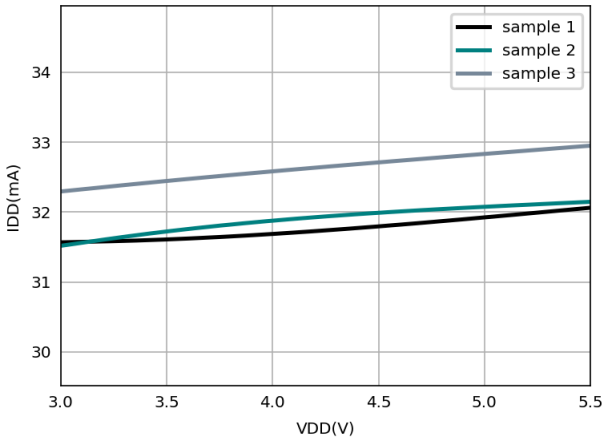


Figure 6.21 Input Supply Current vs Supply Voltage (IE=1mA)

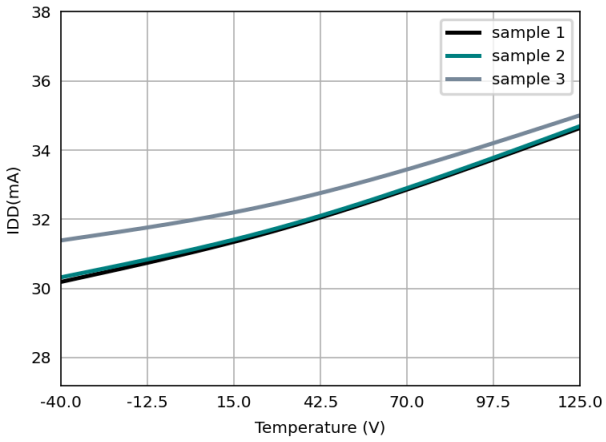


Figure 6.22 Input Supply Current vs Temperature (IE=1mA)

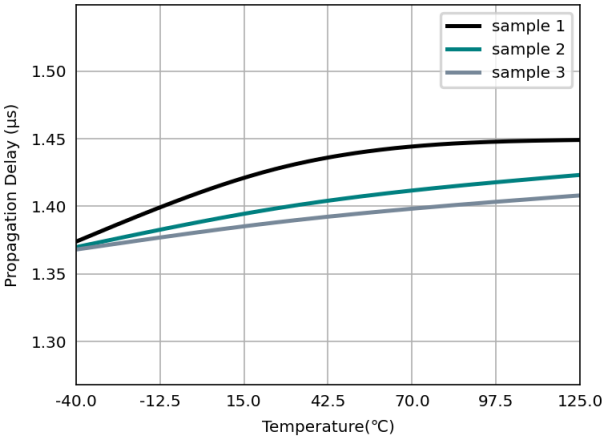


Figure 6.23 Input and Output Signal Delay time vs Temperature

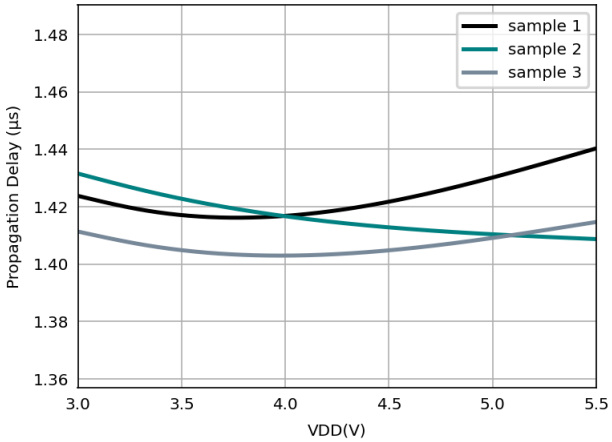


Figure 6.24 Input and Output Signal Delay time vs Supply Voltage

(1) According to the test results of 30 pcs samples.

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value	Unit	Comments
Minimum External Clearance	CLR	8	mm	IEC 60664-1:2007
Minimum External Creepage	CPG	8	mm	IEC 60664-1:2007
Distance Through Insulation	DTI	26	μm	Distance through insulation (internal clearance – capacitive signal isolation)
		75	μm	Distance through insulation (internal clearance – transformer power isolation)
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

Description	Test Condition	Value
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	I to IV
	For Rated Mains Voltage ≤ 300Vrms	I to IV
	For Rated Mains Voltage ≤ 600Vrms	I to IV
	For Rated Mains Voltage ≤ 1000Vrms	I to III
Climatic Classification		40/125/21
Pollution Degree per DIN VDE 0110		2

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value	Unit
DIN EN IEC 60747-17 (VDE 0884-17)				
Maximum repetitive isolation voltage		V_{IORM}	2121	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	1500	V_{RMS}
	DC Voltage		2121	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, t_{ini} = 60 s , $V_{pd(m)}=1.2*V_{IORM}$, t_m=10s.	q_{pd}	<5	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, t_{ini}=60s ,$V_{pd(m)}=1.6*V_{IORM}$, t_m=10s			pC
	Method b, $V_{ini}=1.2*V_{IOTM}$, t_{ini}=1s			pC

Description	Test Condition	Symbol	Value	Unit
	$V_{pd\ (m)}$=1.875*V_{IORM}, t_m=1s（method b1）or $V_{pd(m)}$=V_{ini}, t_m=t_{ini}(method b2)			
Maximum transient isolation voltage	t = 60sec	V_{IOTM}	8000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50μs waveform per IEC62368-1	V_{IMP}	6250	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50μs waveform, V_{IOSM}≥V_{IMP} × 1.3	V_{IOSM}	10000	V_{PEAK}
Isolation resistance	V_{IO} =500V, T_{amb}=25°C	R_{IO}	>10^{12}	Ω
	V_{IO} =500V, 100°C ≤ T_{amb} ≤ 125°C	R_{IO}	>10^{11}	Ω
	V_{IO} =500V, T_{amb}=T_s	R_{IO}	>10^{9}	Ω
Isolation capacitance	f = 1MHz	C_{IO}	0.8	pF
Safety total power dissipation	V_I = 5.5V, T_J = 150 °C, T_A = 25 °C	Ps	1524	mW
Safety input, output, or supply current	θ_{JA} = 82°C/W for SOW8, V_I = 5.5V, T_J = 150 °C, T_A = 25 °C	Is	277	mA
Maximum safety temperature		Ts	150	°C
UL1577				
Insulation voltage per UL	V_{TEST} = V_{ISO}, t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO}, t = 1 s	V_{ISO}	5000	V_{RMS}

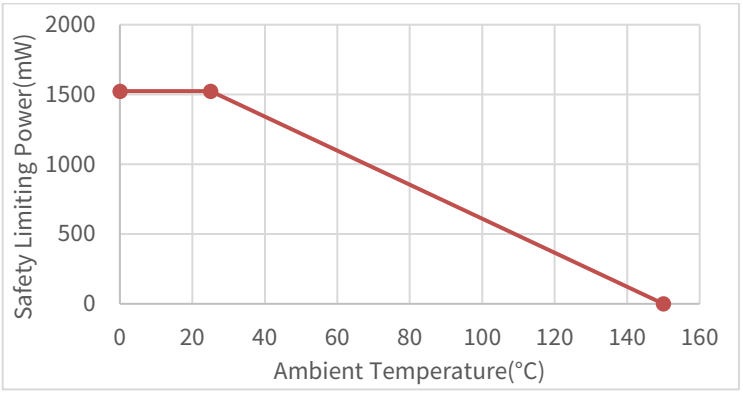


Figure 7.1 NSI3602D Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

7.3. Regulatory Information

The NSI3602D are approved or pending approval by the organizations listed in table.

UL		VDE	CQC	TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified According to EN IEC 62368-1	Certified According to EN IEC 62368-1

UL		VDE	CQC	TUV
Single Protection, 5000V_{rms} Isolation voltage	Single Protection, 5000V_{rms} Isolation voltage	Reinforce Insulation V_{IORM}=2121 V_{PEAK} V_{IOTM}=8000 V_{PEAK} V_{IOSM}=10000 V_{PEAK}	Reinforced insulation	5000Vrms for 1min
E500602	E500602	40052820	CQC20001264939	R50574061

8. Function Description

8.1. Overview

The NSI3602D is a high performance isolated amplifier with integrated isolated power supply that accept fully-differential input. The fully-differential input is ideally suited for shunt current monitoring in high voltage applications where isolation is required.

The low-side power supply VDD feeds power to the isolated power supply input through an LDO with external connection from the LDO pin to the ISO_PI pin. The output of the isolated power supply is regulated by an internal LDO with external connection from the ISO_PO pin to the LDO_IN pin, to power the high-side circuit. The integrated isolated power supply enables single-power operation on the low side of the device without the need for a separate isolated power supply for the high side, effectively reducing the board area.

The analog input is continuously sampled by a second-order Σ-Δ modulator in the device, which is driven by a pre-stage fully-differential amplifier in the device. With the internal voltage reference and clock generator, the modulator converts the analog input signal to a digital bitstream. The output of the modulator is transferred by the drivers (called TX in the Functional Block Diagram) across the isolation barrier that separates the isolated input and output side voltage. The received bitstream and clock are synchronized and processed, as shown in the Functional Block Diagram, by a fourth-order analog filter on the output side and has a differential output.

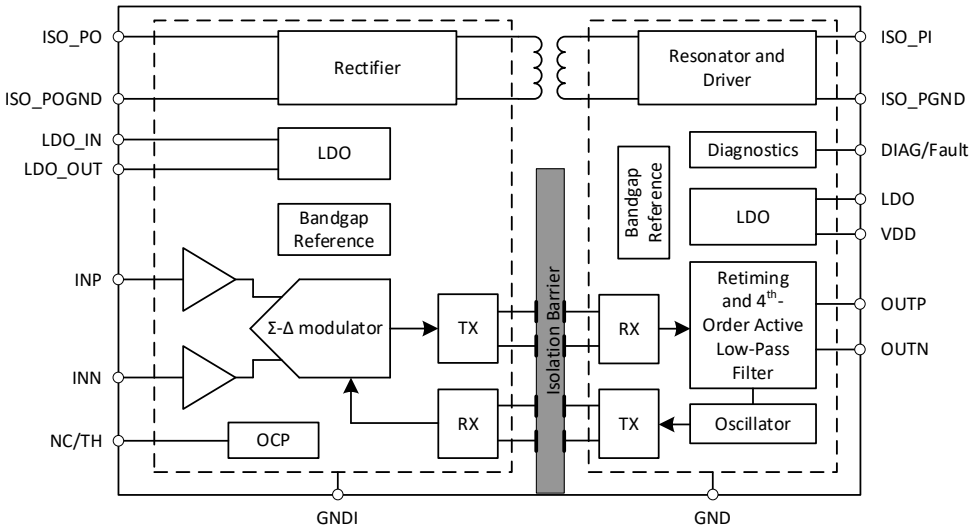


Figure 8.1 Function Block Diagram of NSI3602D

8.2. Analog Input and output

There are two restrictions on the analog input signals (VINP and VINN).

- If the input voltage exceeds the range GND1 – 6 V to VDD + 0.5 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on.
- The linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

For linear input range, the analog output of NSI3602D has a fixed gain of 41. If an input signal exceeding the clipping input range is applied to the NSI3602D ($V_{IN} \geq V_{Clipping}$), the analog output will be clipped (typically, 2.49V for positive clipping and -2.49V for negative clipping).

In addition, NSI3602D integrates some diagnostic measures and offers a fail-safe output to simplify system-level design. The fail-safe output is a negative differential output voltage that does not occur under normal device operation, and it will

only be activated when the undervoltage of the integrated isolated power supply output ISO_PO or the high-side LDO output LDO_OUT is detected. Use the maximum $V_{FAILSAFE}$ voltage -2.5V as a reference value for the fail-safe detection on the system level.

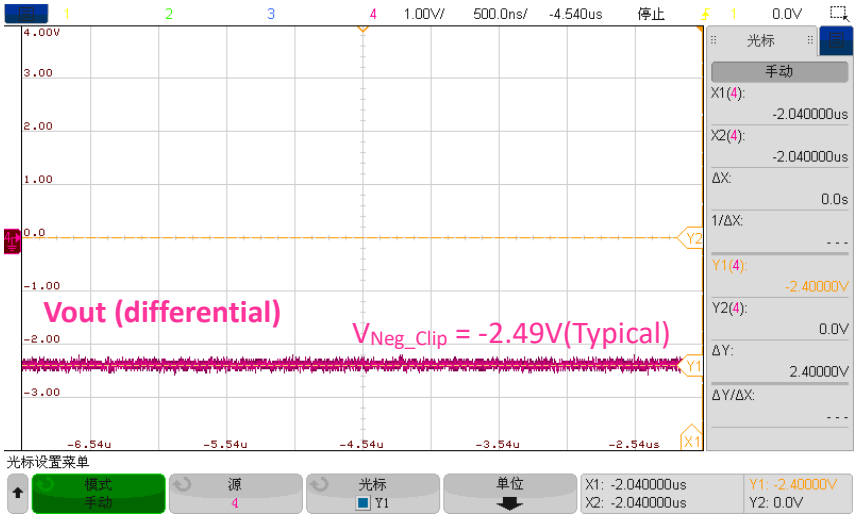


Figure 8.2 Typical negative clipping output

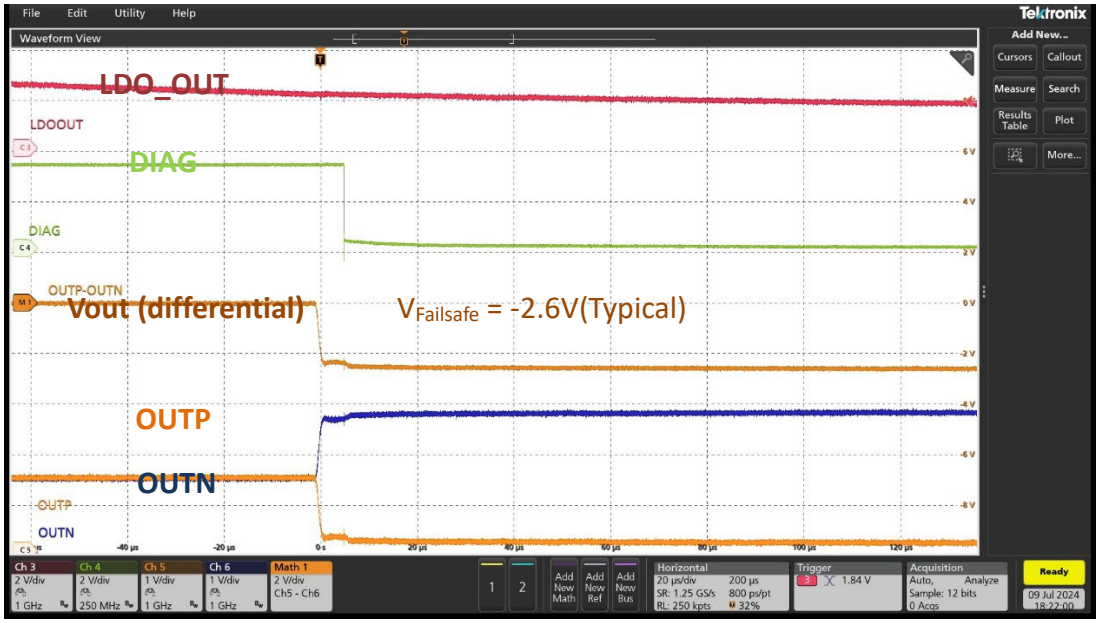


Figure 8.3 Typical Failsafe output

8.3. Accuracy Related Parameters

Parameters related to the accuracy performance are explained in this section, including Vos and its drift, EG and its drift, Nonlinearity. Other immunity parameters that affect accuracy like CMRR and PSRR are also included.

8.3.1.Input offset V_{OS} and Gain Error E_G

Vos and EG are the most significant factor influencing accuracy. The ideal curve and actual curve are shown in Figure 8.4.

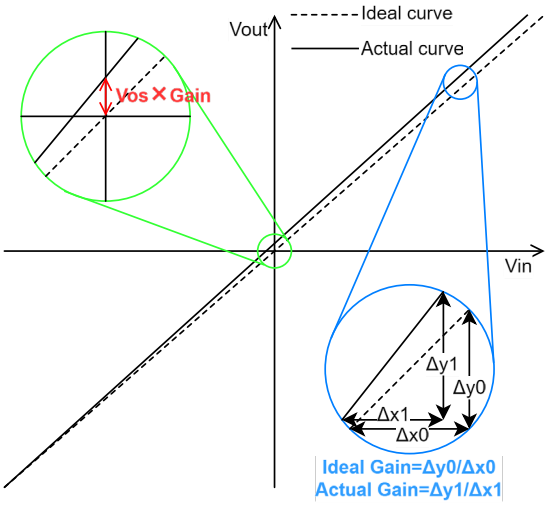


Figure 8.4 Vos and EG diagram

V_{OS} means the input offset voltage when input is 0V. The tested output should be divided by nominal gain as Vos is defined as the offset voltage referred to input (See Equation 1).

$$\text{Vos} = \text{Vo}/\text{Nominal Gain} \quad \text{Equation 1}$$

where

- Vo is the output voltage tested when input is 0V.
- Nominal Gain is 41 for NSI3602D.

Gain is the magnification of the amplifier, and the definition formula is shown in Equation 2. EG means the difference between actual and ideal slope. It should be noted that EG is tested across the whole input range to minimize test error (See Equation 3).

$$\text{Gain} = \frac{\Delta y1}{\Delta x1} = \frac{\text{Vo1} - \text{Vo2}}{\text{Vin1} - \text{Vin2}} \quad \text{Equation 2}$$

$$\text{E}_\text{G} = \frac{\text{Gain} - \text{Nominal Gain}}{\text{Nominal Gain}} \times 100\% \quad \text{Equation 3}$$

where Vin1 and Vin2 are the lower and upper limit of the input FSR separately, Vo1 and Vo2 are the output voltage corresponding to Vin1 and Vin2.

8.3.2.Input offset drift TCV_{OS} and Gain error thermal drift TCE_G

Input offset drift TCV_{OS} means the drift of V_{OS} over the whole operating temperature range, which is calculated as Equation 4.

$$\text{TCVos} = \frac{\text{Vos}_\text{max} - \text{Vos}_\text{min}}{\text{TempRange}} \quad \text{Equation 4}$$

where

- Vos_{max} and Vos_{min} is the maximum and minimum offset voltage over the whole operating ambient temperature range.
- TempRange covers the whole operating temperature, from -40°C to 125°C.

Gain error thermal drift TCE_G is the drift of E_G over the whole operating temperature range, which is calculated as Equation 5.

$$\text{TCE}_G = \frac{\text{E}_\text{Gmax} - \text{E}_\text{Gmin}}{\text{TempRange}} \quad \text{Equation 5}$$

where E_{Gmax} and E_{Gmin} is the maximum and minimum Gain Error over the whole temperature.

Both TCV_{OS} and TCE_G should be multiplied by the direction of temperature drift.

8.3.3.Nonlinearity

Nonlinearity describes the deviation between the actual output and the ideal linear output. Calculate the peak-to-peak value of the error between the actual output and the fitting curve, and nonlinearity is expressed as the ratio of half of the peak-to-peak error to the full-scale range of the output voltage (See Equation 6).

$$\text{Nonlinearity} = \frac{\text{Error\_pkpk}}{2 \times V_{OFSR}} \times 100\% \quad \text{Equation 6}$$

where

- Error_pkpk is the peak-to-peak value of the error between the actual output and the fitting curve.
- V_{OFSR} represents the full-scale range of the output voltage (4.1V for NSI3602D).

8.3.4.Power-Supply Rejection Ratio

Power-Supply Rejection Ratio (PSRR) describes the level of the output error (input inferred) which is affected by the variation of power supply. PSRR is defined in dB and calculated as Equation 7.

$$\text{PSRR} = 20 \times \log_{10}\left(\frac{V_{O\_var}}{\text{Nominal Gain} \times VDD_{var}}\right) \quad \text{Equation 7}$$

Where V_{O_var} and VDD_{var} are respectively the variation value of the output voltage and the supply voltage.

8.3.5.Common-Mode Rejection Ratio

Common-Mode Rejection Ratio (CMRR) quantifies the ability of a differential amplifier to suppress the variation of the common mode signals while amplifying the differential-mode signals. CMRR is calculated as:

$$\text{CMRR} = 20 \times \log_{10}\left(\frac{V_{O\_var}}{\text{Nominal Gain} \times V_{CM\_var}}\right) \quad \text{Equation 8}$$

where CMRR is the input-referred voltage variation in dB and V_{CM_var} is the variation value of the input common-mode voltage.

8.3.6.Total Error Calculation

The total error is contributed by parameters discussed above. It is helpful to know the respective contribution of all different parameters when something is wrong about system current sensing. This section will introduce the calculation method of total error.

Parameters which mainly affects sensing accuracy are Vos, EG and Nonlinearity and their drift. PSRR and CMRR are not a dominant factor in most case. However, PSRR can be a concern when the power supply has high-frequency ripple, in which case a larger decoupling capacitor and a better layout is highly recommended (Refer to Section 9.3).

The error introduce by Vos and its drift can be calculated as:

$$\text{Error\_Vos} = \frac{Vos_{max} + TCV_{os} \times \Delta T}{V_{IN}} \times 100\% \quad \text{Equation 9}$$

where

- Vos_{max} is the maximum value of input offset voltage at 25°C, which is ±0.05mV for NSI3602D.
- TCV_{os} is the maximum drift of input offset voltage over the whole working temperature, which is 0.6 uV/°C for 3602D
- ΔT is the range of temperature variation.
- V_{IN} is the input voltage in the application.

The error introduced by E_G and TCE_G can be calculated as：

$$\text{Error\_}E_G = E_G + TCE_G \times \Delta T \quad \text{Equation 10}$$

where

- E_G is the maximum value of Gain Error when the temperature is 25°C, which is ±0.25% for NSI3602D.
- TCE_G is the maximum drift of Gain Error over the whole temperature, which is ±50ppm/°C for NSI3602D.

The error introduced by Nonlinearity is $Nonlinearity_{max}$, the maximum value of Nonlinearity in the entire temperature range, - 40°C to 125°C, which is ±0.05% for NSI3602D. The total error sensing error is expressed as:

$$\text{Total\_Error} = \sqrt{\text{Error\_Vos}^2 + \text{Error\_E}_G{}^2 + \text{Nonlinearity}_{\max}{}^2} \quad \text{Equation 11}$$

For example, consider an NSI3602D with the sensing input voltage of ±50mV and a - 40°C to 85°C temperature range. The total error calculation is shown in Table 1.

Table 8.1 Total Error Calculation of NSI3602D (- 40°C to 85°C)

Error Component	Symbol	Equation	Error at Vin=±50mV	Error at Vin=±5mV
Input offset error	Error_Vos	$\text{Error\_Vos} = \frac{\text{Vos}_{\max} + \text{TCV}_{\text{os}} \times \Delta T}{V_{IN}} \times 100\% = \frac{\pm 0.05\text{mV} \pm 0.6\mu\text{V/°C} * 65°C}{V_{IN}} \times 100\%$	±0.178%	±1.78%
Gain error	Error_EG	$\text{Error\_E}_G = \text{E}_G + \text{TCE}_G \times \Delta T = \pm 0.25\% \pm 50\text{ppm/°C} \times 65°C$	±0.575%	±0.575%
Nonlinearity	$\text{Nonlinearity}_{\max}$	$\text{Nonlinearity}_{\max} = \pm 0.05\%$	±0.05%	±0.05%
Total error	Total_Error	$\text{Total\_Error} = \sqrt{\text{Error\_Vos}^2 + \text{Error\_E}_G{}^2 + \text{Nonlinearity}_{\max}{}^2}$	±0.604%	±1.871%

Since the input offset voltage is independent of input voltage, it becomes the dominant factor of the total error when the input voltage is low. To improve the system accuracy, especially under low-input applications, it is recommended to perform software zero-point calibration and gain error calibration. With system-level calibration, the total error can also be reduced significantly. The reduced error is calculated as Table 8.2.

Table 8.2 Total Error Calculation with Software Calibration (- 40°C to 85°C)

Error Component	Symbol	Equation	Error at Vin=±50mV	Error at Vin=±5mV
Input offset error	Error_Vos	$\text{Error\_Vos} = \frac{\text{TCV}_{\text{os}} \times \Delta T}{V_{IN}} \times 100\% = \frac{0.6\mu\text{V/°C} * 65°C}{V_{IN}} \times 100\%$	±0.078%	±0.78%
Gain error	Error_EG	$\text{Error\_E}_G = \text{TCE}_G \times \Delta T = \pm 50\text{ppm/°C} \times 65°C$	±0.325%	±0.325%
Nonlinearity	$\text{Nonlinearity}_{\max}$	$\text{Nonlinearity}_{\max} = \pm 0.05\%$	±0.05%	±0.05%
Total error	Total_Error	$\text{Total\_Error} = \sqrt{\text{Error\_Vos}^2 + \text{Error\_E}_G{}^2 + \text{Nonlinearity}_{\max}{}^2}$	±0.338%	±0.846%

The maximum total error with and without calibration is show in Figure 8.3, considering 50mV input as full load, NSI3602D can achieve <1% error at more than 10% load(Vin≥5mV) with software calibration, and <1% error at more than 30% load(Vin≥15mV) without software calibration.

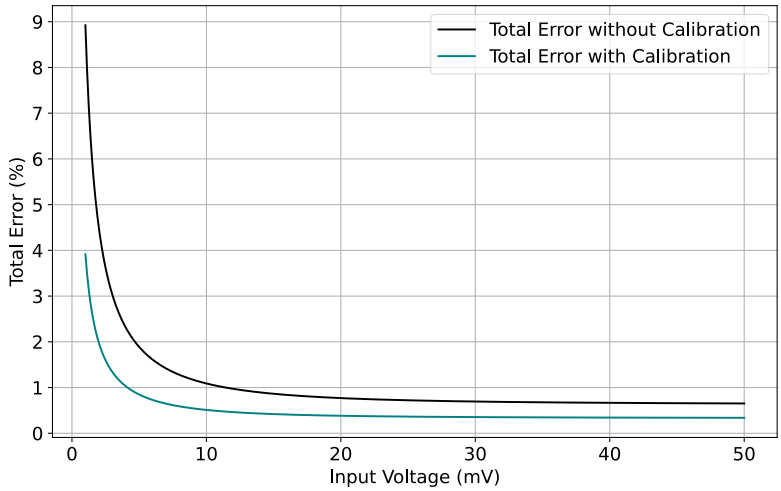


Figure 8.5 Total Error Over - 40°C to 85°C vs Input Voltage

8.4. Isolated power

The NSI3602D integrates an isolated DC/DC power supply that includes the following components as shown in Figure 8.1:

- Low-side low-dropout regulator (LDO) to provide stable voltage for the input of the isolated DC/DC converter.
- Isolated DC/DC converter with the primary resonator and driver, an air-core transformer, and the secondary rectifier. The converter does not output a constant voltage and it is not recommended to drive additional load.
- High-side LDO to convert the isolated DC/DC converter output to a stable voltage and supply for the high-side signal circuitry. The high-side LDO can provide a limited current of 1mA for external load.

The isolated DC/DC power supply uses a spread spectrum clocking technique and optimized transformer design to improve the electro-magnetic interference (EMI) performance.

8.5. Diagnostic Output

The open-drain diagnosis output DIAG helps confirm the device is in normal operation and simplifies system-level design and diagnostics. The DIAG pin need to be connected to the pull-up supply through a resister. If the device operates normally, the DIAG pin is in a high-impedance state and pulled up to high level externally. The DIAG pin is actively pulled low when the undervoltage of the integrated isolated power supply output ISO_PO or the high-side LDO output LDO_OUT is detected. The failsafe mode is activated correspondingly. The amplifier outputs a negative differential voltage $V_{FAILSAFE}$. The diagnostic output feature is only activated when the NSI3600D is properly powered on, which means the DIAG pin will not be pull down during power up procedure.

The DIAG pin can be floating if not used.

9. Application Note

9.1. Typical Application Circuit

The following key features make NSI3602D the ideal solution for high accuracy isolated current measurement.

- Reinforced isolation barrier supports a working voltage up to 1500Vrms, provide extremely high reliability for dangerous high voltage systems.
- Excellent common mode transient immunity(CMTI, 150kV/us typ) ensures the device to provide accurate and reliable measurements even in the presence of high-power switching.
- Isolated power supply integrated, reduces the need of external isolated high-side supply compared to traditional NSI1300-Q1, simplifies design and reduces area.

- Excellent DC accuracy and low drift, high linearity over FSR, limited sensitivity to external magnetic fields, make sure the device can provide extremely high sensing accuracy.

The typical application circuit is shown in Figure 9.1. The output of the low-side LDO (LDO pin) need to be connected to the isolated power supply input (ISO_PI pin). The isolated power supply output (ISO_PO pin) need to be connected to the input of the high-side LDO (LDO_IN pin). In this way, the high-side amplifier circuitry is powered by an isolated power supply. The necessary filter and bypass capacitors should be added to the device power supply, the isolated power supply input (ISO_PI pin) and output (ISO_PO pin), and the input of the high-side LDO (LDO_IN pin).The recommended capacitance can refer to Figure 9.1.

The voltage across the shunt resistor R_{sense} is applied to the differential input of the NSI3602D through a RC filter. The differential output of the isolated amplifier is converted to a single-ended analog output with an operational-amplifier-based circuit. Suggest to add >1kΩ resistor on the OUTP and OUTN pin to prevent output over-current. An analog-to-digital converter usually receives the analog output and converts to digital signal for controller processing.

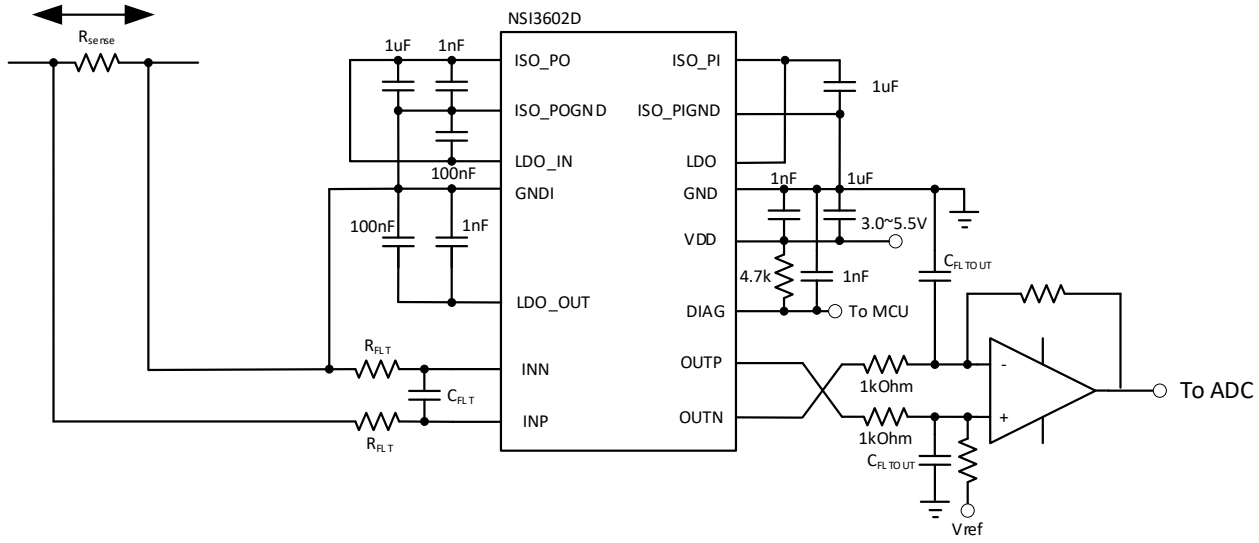


Figure 9.1 Typical application circuit

9.2. Shunt Resistor Selection

Choosing a particular shunt resistor is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller sense resistor decreases power dissipation, while larger sense resistor can improve measure accuracy by utilizing the full input range of isolated amplifier.

There are two other factors should be considered when selecting the shunt resistor:

- The voltage-drop caused by the rated current range must not exceed the recommended linear input voltage range: $V_{SHUNT} \leq FSR$.
- The voltage-drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $V_{SHUNT} \leq V_{Clipping}$.

9.3. PCB Layout

There are some key guidelines or considerations for optimizing performance in PCB layout:

- The filter and bypass capacitors of VDD, ISO_PO, ISO_PI and LDO_OUT pins should be placed as close as possible to the pins respectively. For multiple filter capacitors of the same pin, capacitors with smaller values should be placed closer to the pin to filter out high-frequency noise better. An additional 1~10μF capacitor may be used for the power supply pin VDD in noisy conditions.
- Kelvin rules is recommended for the connection between shunt resistor to NSI3602D. Because of the Kelvin connection, any voltage drops across the trace and leads should have no impact on the measured voltage.
- Place the shunt resistor close to the INP and INN inputs and keep the layout of both connections symmetrical and run very close to each other to the input of the NSI3602D. This minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal.

- To suppress radiation on the power lines, place Ferrite Beads respectively in series with the line of VDD and GND for filter. The ferrite Beads, together with decoupling capacitors, can filter and isolate noise well. In the layout area, the ferrite beads need to effectively separate the chip layout area from peripheral circuit without overlap in different PCB layers. Ferrite Beads can also be added in series with the differential input to suppress radiation on the input signal lines.
- Keep the trace lengths of the wiring as short as possible and don't place a ground plane in the high-voltage domain, which minimizes the antenna on this node to minimize radiated emissions.

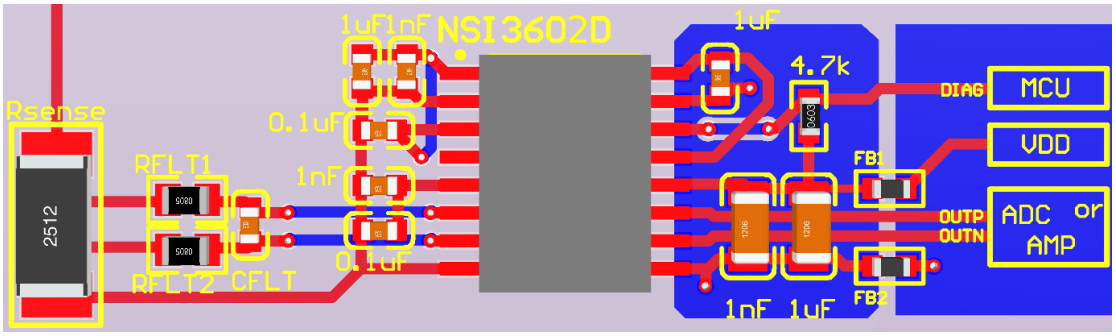
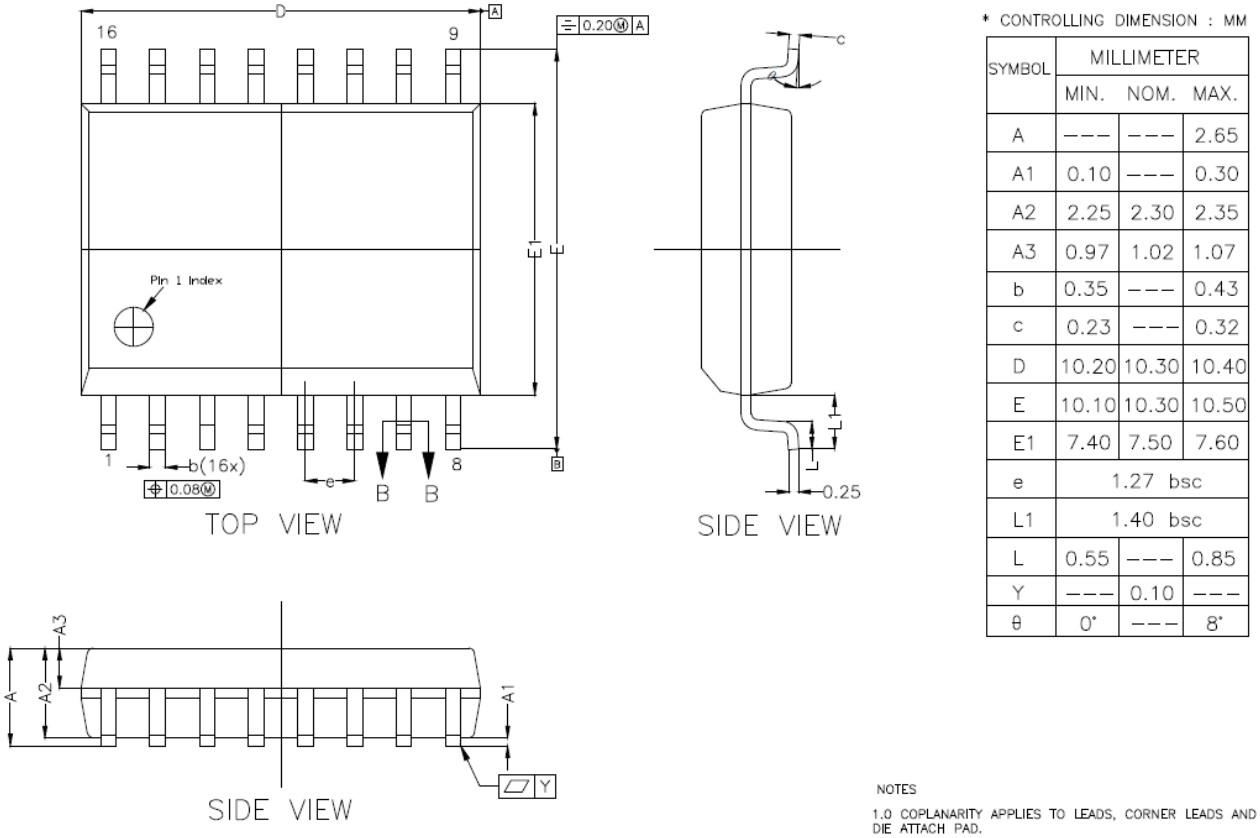


Figure 9.2 PCB layout example of NSI3602D

10. Package Information



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, perside.

Figure 10.1 SOW16 package shape and dimension in millimeters

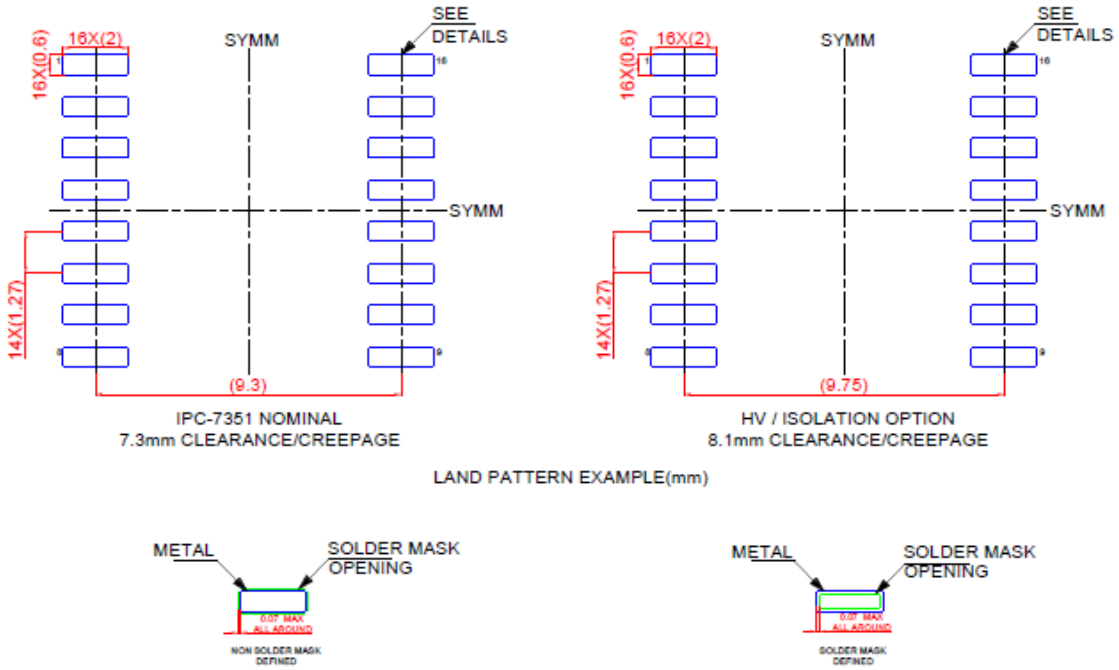


Figure 10.2 SOW16 Package Board Layout Example

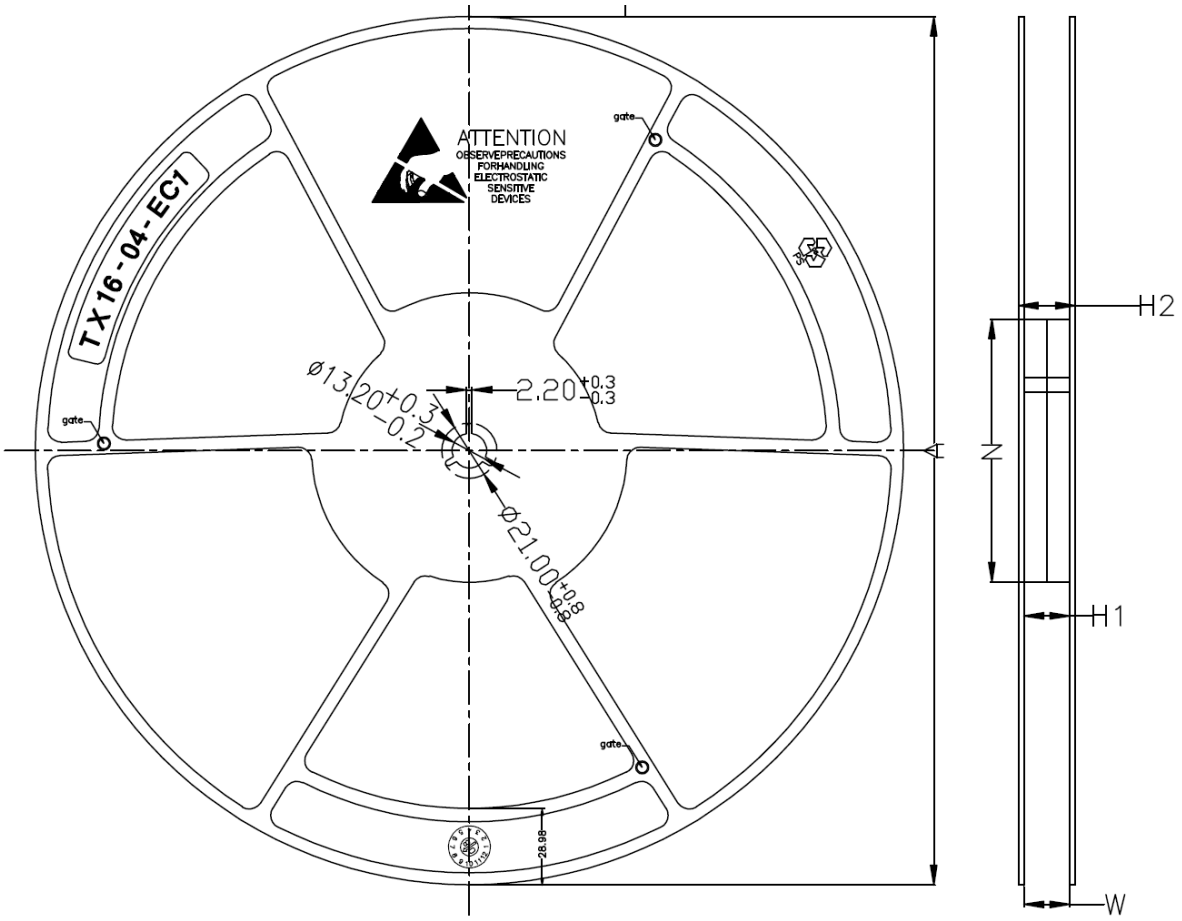
11. Ordering Information

Part No.	*Isolation Rating(kV)*	*Linear Input Range(mV)*	*Moisture Sensitivity Level*	*Temperature*	*Automotive*	*Package Type*	*Package Drawing*	*SPQ*
NSI3602D-Q1SWR	5	-0.05 ~ 0.05	Level-3	-40 to 125°C	YES	SOP16 (300mil)	SOW16	1500

12. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
NSI3602D-Q1	Click here	Click here	Click here	Click here

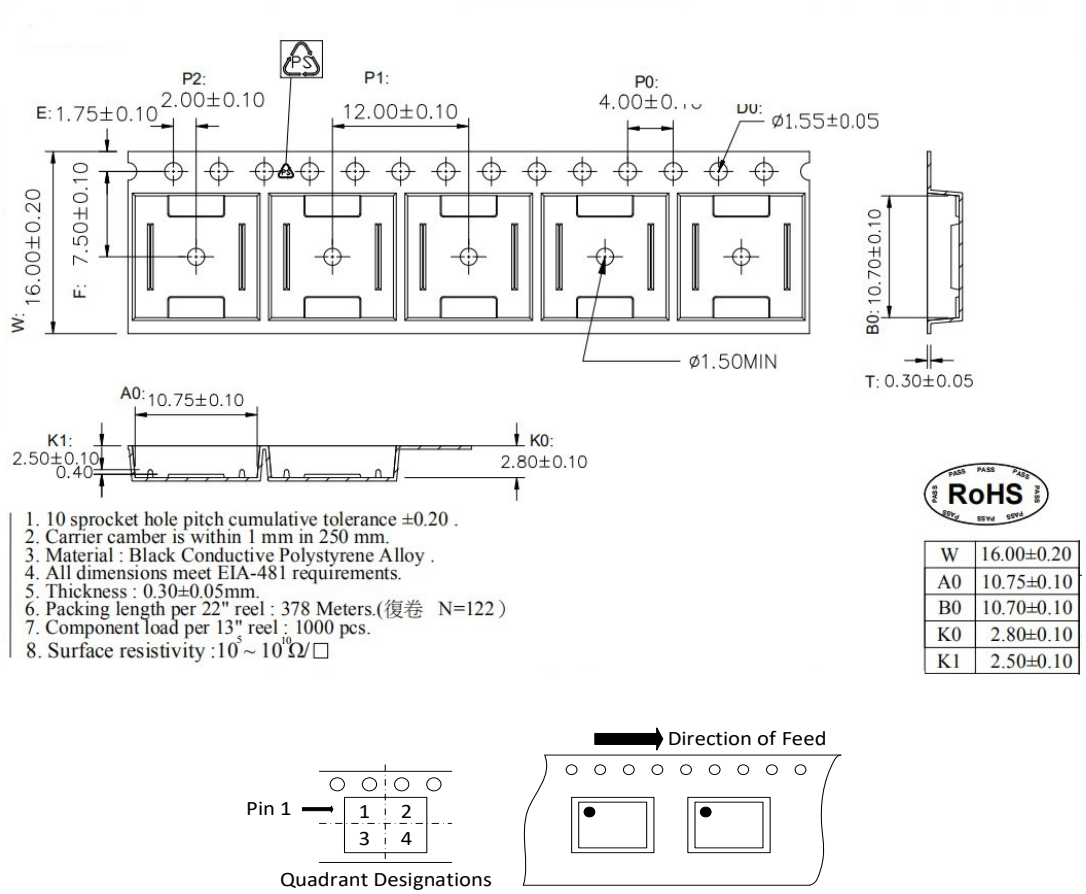
13. Tape and Reel Information



PRODUCT SPECIFICATIONS					
TAPE WIDTH	øA +2 −2	øN +2 −2	H1 +2 −0	H2 +1 −1	W +3.5 −0.2
16MM	330	100	16.4	20.6	16.4

NOTES:
1. MATERIAL:DISSIPATIVE(BLACK)
2. FLANGE WARPAGE:3 MM MAXIMUM 5
3. ALL DIMENSIONS ARE IN MM
4. ESD - SURFACE RESISTIVITY-10 TO 10 OHMS/SQ
5. GENERAL TOLERANCE: ±0.25 MM

Figure 13.1 Reel Information



W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

Figure 13.2 Tape Information of SOP16(300mil)

14. Revision History

Revision	Description	Date
1.0	Initial Release	2025/12/05

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