NOVOSENSE

NSR22601-Q1, NSR22602-Q1, NSR22603-Q1 NSR22604-Q1, NSR22605-Q1, NSR22606-Q1

Automotive Wide input Non-Synchronous Boost, SEPIC, Flyback Controller

Datasheet (EN) 1.2

Product Overview

The NSR2260x-Q1 is an adjustable output non-synchronous controller for switching regulators with low-side N-channel MOSFET. The device is used peak-current-mode control with internal slope compensation. It is suitable for topologies requiring a low-side MOSFET, such as boost, flyback, SEPIC, etc.

The NSR2260x-Q1 has built in features such as adjustable soft−start, VCC under-voltage lockout, cycle−by−cycle current limiting, short−circuit hiccup protection and thermal shutdown. DFN12 and HTSSOP14 packages are available.

Key Features

- AEC-Q100 Grade 1 Qualified
- Wide 4.5 V to 50 V Input Range
- Internal Driver With 1.5-A Peak Current Capability
- 1 V ±1.5% Accuracy Feedback Reference
- Low shutdown current: 1.28 μA (typ.)
- Low quiescent switching current: 323 μA (typ.)
- Peak Current Mode with Internal Slope Compensation
- Selectable frequency spread spectrum

  NSR22603-Q1, NSR22604-Q1, NSR22605-Q1, NSR22606-Q1
- Cycle-by-cycle Current Limit

  NSR22601-Q1, NSR22603-Q1, NSR22605-Q1
- Optional hiccup mode overload protection

  NSR22602-Q1, NSR22604-Q1, NSR22606-Q1
- Adjustable Soft-start
- Hiccup disabled during soft start
- Over-voltage Protection
- Over-temperature Protection
- Wettable flank 3.0-mm × 2.0-mm DFN12 package
- Lead Type 5.0-mm × 4.4-mm HTSSOP14 package
- RoHS-compliant package

Applications

- Automotive On-board Charger and DC-DC
- Automotive Traction Inverter
- Automotive Start-stop Applications
- Automotive ADAS Driver Information
- Boost for Audio Amplifiers

Device Information

Part Number	Package Info
NSR22601-Q1	3.0 mm x 2.0 mm DFN12-WF
NSR22602-Q1	3.0 mm x 2.0 mm DFN12-WF
NSR22603-Q1	3.0 mm x 2.0 mm DFN12-WF
NSR22604-Q1	3.0 mm x 2.0 mm DFN12-WF
NSR22605-Q1	5.0 mm x 4.4 mm HTSSOP14
NSR22606-Q1	5.0 mm x 4.4 mm HTSSOP14

Typical Circuits

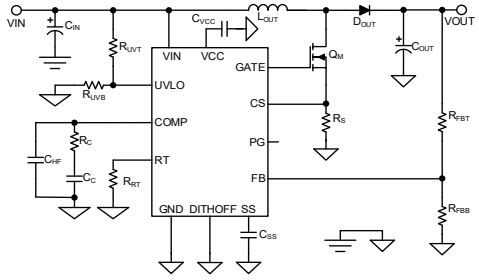

Figure 1 Typical Boost application circuits

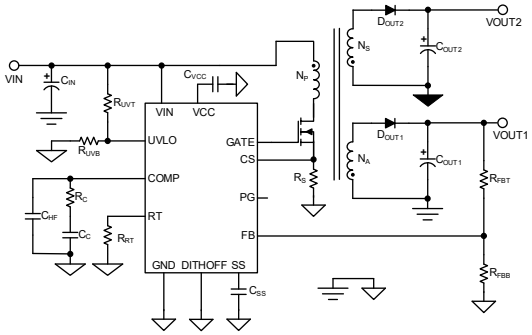

Figure 2 Typical Flyback application circuits

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1. Product Family Table

Part Number	Hiccup Protection	Selectable spread spectrum	Package
NSR22601-Q1	N	N	DFN12-WF
NSR22602-Q1	Y	N	DFN12-WF
NSR22603-Q1	N	Y	DFN12-WF
NSR22604-Q1	Y	Y	DFN12-WF
NSR22605-Q1	N	Y	HTSSOP14
NSR22606-Q1	Y	Y	HTSSOP14

2. Pin Configuration and Functions

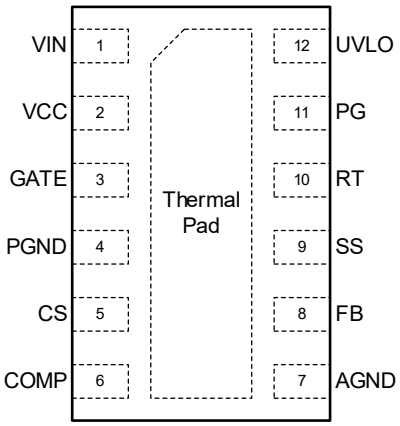


Figure 2.1 NSR22601-Q1 and NSR22602-Q1 Pin Configuration

PIN NO.	SYMBOL	FUNCTION
1	VIN	Power supply input.
2	VCC	Driver supply voltage output. Connect to a bypass 0.47μF to 4.7μF capacitor to GND.
3	GATE	Gate driver output. The gate of the external MOSFET should be connected to this pin.
4	PGND	Power ground reference for external power circuit.
5	CS	Current sense input. Connect this pin to a sense resistor which connected between source of external power MOSFET and GND.
6	COMP	Transconductance amplifier output. Connect to an external compensation network.
7	AGND	Analog ground reference for internal bias circuit.
8	FB	Feedback voltage input. Connect to an external resistor divider from output to GND to regulate output voltage.
9	SS	Soft start charging current output. Connect this pin to a soft start capacitor.
10	RT	Frequency adjust input. Connect to an external resistor to set switching frequency.
11	PG	Power good indication pin internally connected to the drain of a MOSFET. When used, connect to an external source with a proper pull-up resistor.
12	UVLO	Under voltage lockout input. The part is disabled into non-switching mode when this pin is set as low.

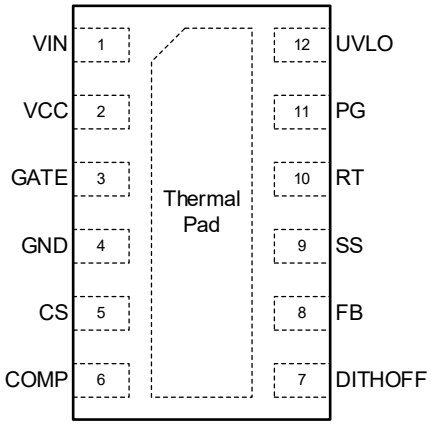


Figure 2.2 NSR22603-Q1 and NSR22604-Q1 Pin Configuration

PIN NO.	SYMBOL	FUNCTION
1	VIN	Power supply input.
2	VCC	Driver supply voltage output. Connect to a bypass 0.47μF to 4.7μF capacitor to GND.
3	GATE	Gate driver output. The gate of the external MOSFET should be connected to this pin.
4	GND	Ground reference.
5	CS	Current sense input. Connect this pin to a sense resistor which connected between source of external power MOSFET and GND.
6	COMP	Transconductance amplifier output. Connect to an external compensation network.
7	DITHOFF	Spread spectrum selection pin. Connect it to GND to enable spread spectrum. Connect it to the VCC pin to disable spread spectrum.
8	FB	Feedback voltage input. Connect to an external resistor divider from output to GND to regulate output voltage.
9	SS	Internal soft-start current source connection. Connect a capacitor from SS to GND.
10	RT	Frequency adjust input. Connect to an external resistor to set switching frequency.
11	PG	Power good indication pin internally connected to the drain of a MOSFET. When used, connect to an external source with a proper pull-up resistor.
12	UVLO	Under voltage lockout input. The part is disabled into non-switching mode when this pin is set as low.

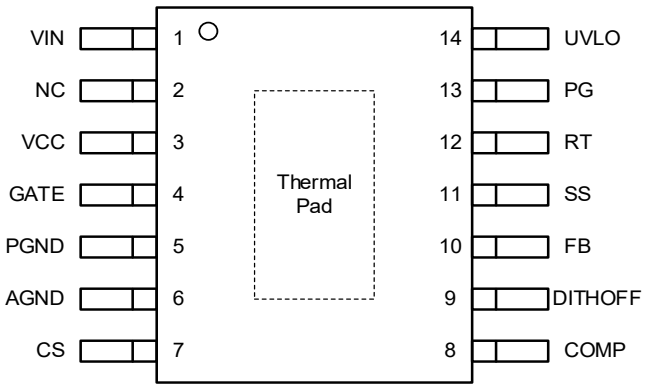


Figure 2.3 NSR22605-Q1 and NSR22606-Q1 Pin Configuration

PIN NO.	SYMBOL	FUNCTION
1	VIN	Power supply input.
2	NC	Not internally connected.
3	VCC	Driver supply voltage output. Connect to a bypass 0.47μF to 4.7μF capacitor to GND.
4	GATE	Gate driver output. The gate of the external MOSFET should be connected to this pin.
5	PGND	Power ground reference for external power circuit.
6	AGND	Analog ground reference for internal bias circuit.
7	CS	Current sense input. Connect this pin to a sense resistor which connected between source of external power MOSFET and GND.
8	COMP	Transconductance amplifier output. Connect to an external compensation network.
9	DITHOFF	Spread spectrum selection pin. Connect it to GND to enable spread spectrum. Connect it to the VCC pin to disable spread spectrum.
10	FB	Feedback voltage input. Connect to an external resistor divider from output to GND to regulate output voltage.
11	SS	Soft start charging current output. Connect this pin to a soft start capacitor.
12	RT	Frequency adjust input. Connect to an external resistor to set switching frequency.
13	PG	Power good indication pin internally connected to the drain of a MOSFET. When used, connect to an external source with a proper pull-up resistor.
14	UVLO	Under voltage lockout input. The part is disabled into non-switching mode when this pin is set as low.

3. Absolute Maximum Ratings

Description	Min	Max	Unit
VIN to GND	-0.3	55	V
VCC to GND	-0.3	18 or VIN + 0.3	V
GATE to GND (DC)	-0.3	18	V
GATE to GND (100ns)	-1		V
GATE to GND (50ns)	-2		V
CS to GND (DC)	-0.3	1	V
CS to GND (100ns)	-1		V
CS to GND (20ns)	-2		V
COMP to GND	-0.3		V
COMP Sink Current		5	mA
DITHOFF to GND	-0.3	18	V
FB to GNDs	-0.3	4	V
SS to GND	-0.3	3.8	V
RT to GND	-0.3	3.8	V
PG to GND	-0.3	18	V
PG Sink Current		1	mA
UVLO to GND	-0.3	VIN + 0.3	V
PGND to AGND	-0.3	0.3	V
Junction Temperature	-40	150	°C
Storage temperature	-55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to conditions on Absolute Maximum Ratings for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND terminal.

4. ESD Ratings

Parameters	Symbol	Value	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), per AEC-Q100-002-RevD	±2000	V
	Charged device model (CDM), per AEC-Q100-011-RevB	±750	V

5. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{IN}	4.5		50	V
VCC Voltage	V_{VCC}	4.5		16	V
DITHOFF Input	$V_{DITHOFF}$	0		16	V
UVLO Input	V_{UVLO}	0		50	V
FB Input	V_{FB}	0		4	V
Switching Frequency Range	f_{SW}	100		1000	kHz
Junction Temperature Range	T_J	-40		125	°C

6. Thermal Information

Parameters	Symbol	DFN12	HTSSOP14	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	64	44	°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	63	49	°C/W

The thermal data is based on the JEDEC standard high-K profile, JESD 51-7, four layers board.

7. Specifications

7.1. Electrical Characteristics

V_{IN} = 12 V, R_T = 19.1 kΩ, T_J = -40 °C to 125 °C. Unless otherwise noted, typical value is at T_J = 25 °C.

Parameters	Symbol	Min	Typ	Max	Unit	Conditions
Quiescent Current						
Quiescent current (shutdown mode)	I_{SD}		1.28	3.5	μA	V_{IN} = 12 V, V_{UVLO} = 0 V
Quiescent current (switching)	I_{Q_SW}		323	550	μA	V_{IN} = 12 V, V_{UVLO} = 2 V, V_{FB} = V_{REF}, RT = 220kΩ
VCC Regulator						
VCC Regulation	V_{VCC_NOL}	6.59	6.88	7.25	V	V_{IN} = 8 V, No load
VCC Regulation	V_{VCC_LOAD}	6.52			V	V_{IN} = 8 V, I_{VCC} = 35mA
VCC UVLO Threshold	V_{VCC_UVLO}	3.4	3.865	4.16	V	VCC rising
VCC UVLO Hysteresis	$V_{VCC\_UVLOHYS}$		0.656		V	
VCC sourcing current limit	I_{VCC_CL}	35	68		mA	V_{IN} = 10 V, V_{VCC} = 0 V
Clock dithering threshold	V_{DITH_R}	1.2	1.73	2.3	V	
Clock dithering threshold	V_{DITH_F}	0.8	1.18	1.6	V	
Clock dithering threshold hysteresis	V_{DITH_HYS}		0.55		V	
Frequency Timing						
Minimum pulse width	t_{ON_MIN}		106		ns	RT = 19.1 kΩ
Switching frequency	f_{SW1}	80	97	113	kHz	RT = 220 kΩ, V_{IN} = 4V
Switching frequency	f_{SW2}	980	1098	1250	kHz	RT = 19.1 kΩ, V_{IN} = 4V
Maximum duty cycle	D_{MAX1}	80	87	96	%	RT = 220 kΩ, V_{IN} = 4V
Maximum duty cycle	D_{MAX2}	80	87	96	%	RT = 19.1 kΩ, V_{IN} = 4V
Enable and UVLO						
Enable threshold rising	V_{EN_R}	0.55	0.77	1	V	
Enable threshold falling	V_{EN_F}	0.51	0.726	0.95	V	
Enable threshold hysteresis	V_{EN_HYS}		0.046		V	
UVLO threshold	V_{UVLO_R}	1.44	1.5	1.56	V	
UVLO threshold	V_{UVLO_F}	1.4	1.45	1.51	V	
UVLO threshold hysteresis	V_{UVLO_HYS}		0.05		V	
UVLO Source Current	I_{UVLO}	4	5	6	μA	V_{UVLO} = 1.6V
Soft Start						
Soft-start current	I_{SS}	8.5	10	11.5	μA	
SS pull-down switch RDSON	R_{SS}		5.9		Ω	
Current Sense						
CS output bias current	I_{SLOPE}	22.5	30	37.5	μA	RT = 220 kΩ
Current limit threshold voltage	V_{CL}	90	100	110	mV	
Internal slope compensation	V_{SL}		40		mV	
Error Amplifier						
Reference voltage	V_{REF}	0.985	1	1.015	V	
Transconductance	G_m		2.05		mA/V	
VEA maximum output voltage	V_{EAO_H}	2.5	2.8		V	
VEA minimum output voltage	V_{EAO_L}		1	1.1	V	
VEA sourcing current	I_{EAO_SRC}	170			μA	
Gate Driver						

Parameters	Symbol	Min	Typ	Max	Unit	Conditions
High-state voltage R_{DSON}	R_{DRVH_DRP} (1)		2.2		Ω	
Low-state voltage R_{DSON}	R_{DRVL_DRP} (1)		1.1		Ω	
Power Good						
Undervoltage threshold	P_{GL}	87	90	93	%	FB falling (reference to VREF)
Undervoltage threshold	P_{GH}		95		%	FB rising (reference to VREF)
PG pull-down switch R_{DSON}	R_{PG}		55		Ω	1mA sinking
Hiccup protection (NSR22602, NSR22604 and NSR22606 Only)						
Hiccup waiting period	t_{HCP_WAIT} (2)		64		Cycles	
In-hiccup period	t_{HCP_IN} (2)		32768		Cycles	
Hiccup timer reset cycles	t_{HCP_RST} (2)		8		Cycles	
Over-voltage protection						
Over-voltage protection threshold	V_{OVP_R}	106	110	113	%	FB rising (reference to VREF)
Over-Voltage protection threshold	V_{OVP_F}		105		%	FB falling (reference to VREF)
Thermal Shutdown						
Thermal shutdown threshold	T_{SD} (2)		175		°C	
Thermal shutdown hysteresis	T_{SD_HYS} (2)		15		°C	

(1) *Not test covered, guaranteed by characterization.*

(2) *Not test covered, guaranteed by design.*

8. Detailed Description

8.1. Overview

The NSR2260x-Q1 is an adjustable output non-synchronous controller for switching regulators with low-side N-channel MOSFET. The device is applied with peak current mode control with internal slope compensation. It is suitable for use in topologies requiring a low-side MOSFET, such as boost, flyback, SEPIC, etc.

The NSR2260x-Q1 has built in features such under-voltage lockout, cycle−by−cycle current limiting, short−circuit hiccup protection and thermal shutdown. The device is also optimized for EMC performance with internal spread-spectrum. DFN12 and HTSSOP14 packages are available.

8.2. Block Diagram

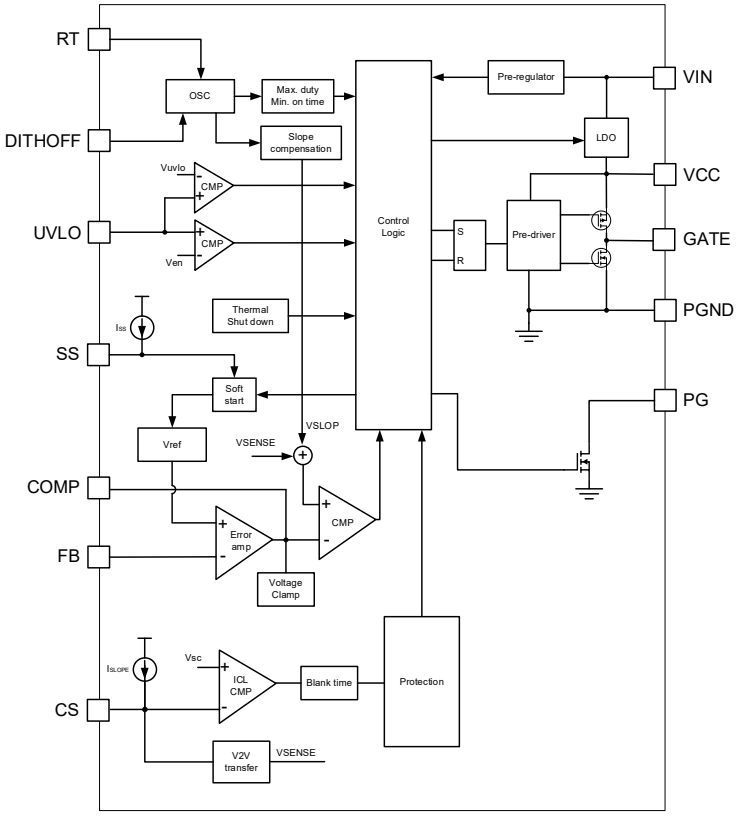


Figure 8.1 Block Diagram

8.3. Feature Description

8.3.1. Supply Voltage

The NSR2260x-Q1 series have a recommended input voltage up to 50V. When in low-voltage condition, the device integrates an under-voltage lock-out function to shut down the device when the VCC voltage falls below an internal threshold (V_{VCC_UVLO}). This function ensures a proper supply voltage for internal circuits. There is also a lock-out threshold hysteresis ($V_{VCC\_UVLOHYS}$) during under-voltage shutdown and re-start to avoid noise trigger for a well-designed system.

8.3.2. Quiescent Current

When pull UVLO pin low the device is on shutdown mode, VIN pin draws a low current (I_{SD}) with the result that power consumption is low in device. When the device is out of shutdown, VIN pin draws a higher current as internal circuits start to work without switching on driver output. When light-load condition, the efficiency is lower as internal driver works to charge and discharge external MOSFETs. Total VIN current is the sum of quiescent current and the average GATE output current. Knowing the operating frequency and the MOSFET gate charge (Q_g), average OUT current can be calculated from below equation:

$$I_{GATE} = Q_g \times f_{SW} \quad (1)$$

8.3.3. VCC Regulator

An internal VCC regulator converts VIN voltage to a typical 6.88V as the voltage rail for internal circuits and gate driver output when on both stand-by and run mode. A capacitor is needed in VCC pin with the value from 1 μF to 4.7 μF. VCC pin can also be supplied by an external bias between the typical 6.88V and Vin(within absolutemaximum rating) to get a higher gate driver output voltage of high state. This connection helps reduce internal power dissipation with an additional transformer winding for VCC.

8.3.4. Frequency Timing

8.3.4.1. Minimum On-time and Maximum Duty

In typical peak-current mode control, on-time period is terminated when CS pin voltage is higher than a certain voltage determined by close loop. To avoid any false triggering caused by spikes when turn-on transient, a blanking time is built which actually blocks the turn-off signal when normal operation. As a result, this blanking time act as a minimum on-time (t_{ON_MIN}) function. During minimum on-time, cycle-by-cycle current limit is disabled.

The NSR2260x-Q1 has a maximum duty (D_{MAX}) restriction in case short current happens in power MOSFET which may cause damage when start-up.

8.3.4.2. Switching Frequency Setting

The switching frequency can be set by a resistor connecting from RT pin to GND with a typical range from 100kHz to 1000kHz. The below equation can be used to get the resistor:

$$R_T = \frac{2.21 \times 10^{10}}{f_{SW}} - 955 \quad (2)$$

8.3.5. Enable and UVLO

When UVLO pin voltage is between enable threshold (V_{EN}) and the UVLO threshold (V_{UVLO}) for more than EN start-up deglitch time (~2.5μs), then after a EN start-up delay (~95μs) the device enters stand-by mode. In standby mode, there is no switching at the GATE output but VCC regulator are operational.

When UVLO pin voltage is above UVLO threshold (V_{UVLO}) and VCC pin voltage is above VCC UVLO Threshold (V_{VCC_UVLO}), the device enters run mode. A soft-start sequence starts with the entry of run mode.

8.3.6. Soft Start

When the device is powered, internal reference voltage is started from 0V, an internal soft-start current source (I_{SS}) turns on when VCC voltage is above VCC UVLO threshold (V_{VCC_UVLO}). The soft-start current source charges an external capacitor connected between SS pin and GND pin. The internal reference tracks on the voltage on soft-start capacitor when it's lower than feedback reference voltage (V_{REF}). The SS pin is pulled down to ground by an internal switch when the VCC is less than VCC UVLO threshold, the UVLO is less than the UVLO threshold, during hiccup mode off-time or thermal shutdown.

Soft-start time is calculated by

$$t_{SS} = \frac{C_{SS}}{I_{SS}} \quad (3)$$

8.3.7. Current Sense

Cycle-by-cycle current limit is built to limit MOSFET current when normal work. As out of blanking time, the driver output is off once the voltage on CS pin is higher than current limit threshold voltage (V_{CL}). When next cycle comes driver regularly outputs high and current limit continues working.

In peak current mode control, when duty cycle is higher than 50%, an internal slope compensation is needed to avoid sub-harmonic oscillation. There are fixed and programmable slope compensation designed to prevent the oscillation at high duty cycle. For fixed slope compensation an Internal ramp increases linearly from 0V to a fix level (V_{SL}). For programmable slope compensation, a saw-tooth current (source output bias current, I_{SLOPE}) flows out of the CS pin.

A RC low-pass filter is recommended on CS pin to GND to avoid unwanted spike when MOSFET switching especially on Flyback topology. The R_F and C_F values can be calculated:

$$3 \times R_F \times C_F < \frac{1-D}{f_{SW}} \quad (4)$$

8.3.8. Error Amplifier

The device has a trans-conductance error amplifier from FB pin to COMP pin. The internal trans-conductance error amplifier provides symmetrical sourcing and sinking capability during normal operation. A typical Type 2 loop compensation network with R_{COMP}, C_{COMP}, and optional C_{HF} loop compensation components is recommended connect COMP pin and GND to configure the error amplifier gain and phase characteristics to achieve a stable loop response.

The COMP pin features internal clamps. The maximum COMP clamp limits the maximum COMP pin voltage below its absolute maximum rating even in shutdown. The minimum COMP clamp limits the minimum COMP pin voltage in order to start switching as soon as possible during no load to heavy load transition. The minimum COMP clamp is disabled when FB is connected to ground in Flyback topology.

8.3.9. Gate Driver

Peak output current capability of NSR2260x-Q1 is up to 1.5A. High level driving voltage has a high-state voltage drop from VCC voltage while low level voltage has and low-state voltage bouncing from GND. There is a VCC sourcing current (I_{VCC_CL}) limit which limits average driving current:

$$Q_{G@VCC} \times f_{SW} < 35mA \quad (5)$$

An internal 1-MΩ resistor is connected between GATE and PGND to prevent a false turn on during shutdown. A small resistor is recommend connected between Gate and Source of external MOSFET to prevent a false-turn-on in high dV/dt conditions.

8.3.10. Power Good

PG pin is an open-drain output. When used, connect it to an external voltage source with a proper pull-up resistor. when the FB pin voltage is greater than the feedback undervoltage threshold, the VCC is greater than the VCC UVLO threshold and the UVLO is greater than the EN threshold, the internal MOSFET is in off-state and PG pin is set as high. There is a PG deglitch time(~22μs) to prevents any false pull-down of the internal MOSFET due to transients.

8.3.11. Hiccup Protection (NSR22602-Q1, NSR22604-Q1 and NSR22606-Q1 Only)

Hiccup protection is integrated to protect device from overload or short conditions. When the hiccup mode fault timer detects 64 cycles of current limiting the device to stop switching and SS is pulled down. The device keeps in switching-off state for 32768 cycles and then tries to start. The 64-cycles hiccup mode fault timer is reset if 8 consecutive switching cycles occur without exceeding the current limit threshold.

8.3.12. Thermal Shutdown

The device is protected from junction temperature higher than thermal shutdown threshold (T_{SD}). When the junction temperature falls below the thermal shutdown trigger point minus the hysteresis (T_{SD_HYS}), the output turns on again.

9. Typical Application

NSR2260x-Q1 series are designed for boost, flyback, SEPIC and other switching DC-DC topologies suitable for peak current mode control with low-side switches.

9.1. Boost Converter

9.1.1. Typical Circuits

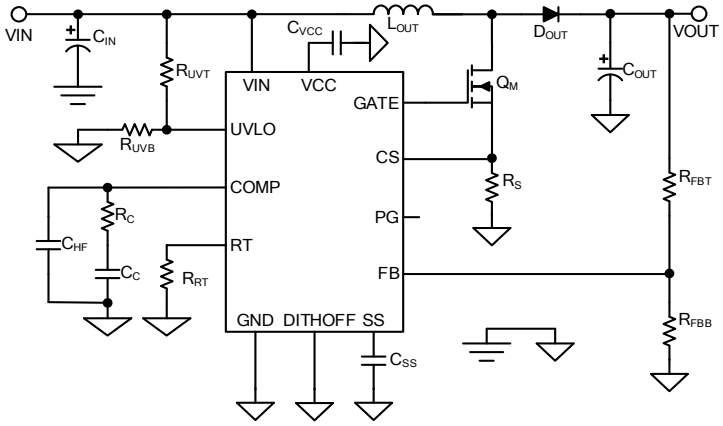


Figure 9.1 Typical Boost Converter Connection with NSR2260x-Q1

9.1.2. Loop Stability Analysis and Design

A Boost converter is a typical closed-loop control system which can be described as below flow chart:

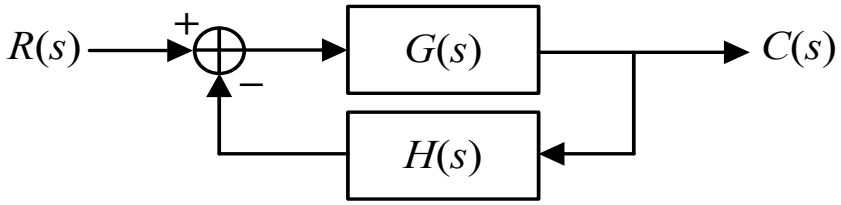


Figure 9.2 Closed-loop Control Flow Chart

Where G(s) can be considered as the transfer function of power stage while H(s) is the compensation section. As loop stability performance of small signal is directly determined by closed-loop transfer function expressed as below:

$$G_{\text{CLOSED}}(s) = \frac{G(s)}{1 + G(s)H(s)} \quad (6)$$

The most straightforward method to check response caused by certain distributing is calculation with closed-loop transfer function from s-domain to time-domain. Frequency stability criterion is a more simple way which is equivalent to Nyquist stability criterion. The frequency stability criterion checks gain and phase curves versus frequency, which is commonly called Bode plot of open-loop transfer function

$$G_{\text{OPEN}}(s) = G(s)H(s) \quad (7)$$

9.1.2.1. Transfer Function and Pole-zero Location of Power Stage

In a Boost converter with peak-current-mode control and an operational transconductance amplifier (OTA) as major control component, power stage transfer function can be derived as below:

$$G(s) = A_{VC} \frac{\left(1-\frac{s}{\omega_R}\right)\cdot\left(1+\frac{s}{\omega_{\text{ESR}}}\right)}{\left(1+\frac{s}{\omega_P}\right)\cdot\left(1+\frac{s}{Q_N\cdot\omega_N}+\frac{s^2}{\omega_N{}^2}\right)} \quad (8)$$

Where:

$$A_{VC} = \frac{R_{LOAD}}{R_S \cdot \left[2\frac{V_{OUT}}{V_{IN}} + \frac{R_{LOAD} \cdot {V_{IN}}^2}{f_{SW} \cdot L_{OUT} \cdot {V_{OUT}}^2} \cdot \left(0.5 + \frac{S_A}{S_N}\right)\right]} \quad (9)$$

S_A is voltage slope of internal compensation:

$$S_A = V_{SL} \cdot f_{SW} \quad (10)$$

S_N is voltage slope between current sense resistor when inductor current rises:

$$S_N = R_S \frac{V_{IN}}{L_{OUT}} \quad (11)$$

The angular frequency of pole from main power is:

$$\omega_P = \frac{\frac{2}{R_{LOAD}} + \frac{{V_{IN}}^3}{f_{SW} \cdot L_{OUT} \cdot {V_{OUT}}^3}\left(1 + \frac{S_A}{S_N}\right)}{C_{OUT}} \quad (12)$$

In a closed current-loop power stage transfer function, there is a pair of complex-conjugate pole at half the switching frequency with the below Q_N values:

$$\omega_N = \pi \cdot f_{SW} \quad (13)$$

$$Q_N = \frac{1}{\left[\pi \cdot (1 - Duty) \cdot \left(1 + \frac{S_A}{S_N}\right) - 0.5\right]} \quad (14)$$

When output capacitor has a equivalent series resistance (ESR), there is a zero lays at below angular frequency:

$$\omega_{ESR} = \frac{1}{C_{OUT} \cdot R_{ESR}} \quad (15)$$

There is also a right half plane zero (RHPZ) in a current-loop Boost:

$$\omega_R = \frac{R_{LOAD} \cdot (1 - Duty)^2}{L_{OUT}} \quad (16)$$

9.1.2.2. Transfer Function and Pole-zero Location of Compensation Stage

For transfer function of compensation section it can be expressed when C_C >> C_{HF} and output resistance of amplifier >> R_C:

$$H(s) = \frac{R_{FBB} \cdot G_{EA} \cdot R_{EAO}}{R_{FBB} + R_{FBT}} \cdot \frac{1 + \frac{s}{\omega_{COMPZ}}}{\left(1 + \frac{s}{\omega_{COMPP1}}\right) \cdot \left(1 + \frac{s}{\omega_{COMPP2}}\right)} \quad (17)$$

Where:

$$\omega_{COMPZ} = \frac{1}{R_C \cdot C_C} \quad (18)$$

$$\omega_{COMPP1} = \frac{1}{R_{EAO} \cdot C_C} \quad (19)$$

$$\omega_{COMPP2} = \frac{1}{R_C \cdot C_{HF}} \quad (20)$$

9.1.2.3. Loop Stability Analysis

From above equations, any change of some components could cause significant changes to loop stability. In a typically designed boost converter, when component changed, the influential changes on loop stability is summary in below table:

Component Changes	Influence on Transfer Function	Typical Influence on Bode Plot
Increase L_{OUT}	Lower ω_P	Lower phase margin
Increase C_{OUT}	Lower ω_P	Lower bandwidth
Increase ESR of C_{OUT}	Lower ω_{ESR}	Earlier boost on phase at high frequency
Increase R_S	Lower A_{VC}	Lower bandwidth
Increase R_C	Lower ω_{COMPZ} Lower ω_{COMPP2}	Earlier boost on gain and phase at low frequency Earlier drop on gain and phase at high frequency
Increase C_C	Lower ω_{COMPZ} Lower ω_{COMPP1}	Earlier boost on gain and phase at low frequency Earlier drop on gain and phase at medium frequency
Increase C_{HF}	Lower ω_{COMPP2}	Earlier drop on gain and phase at high frequency

9.2. Flyback Converter

9.2.1. Typical Circuits

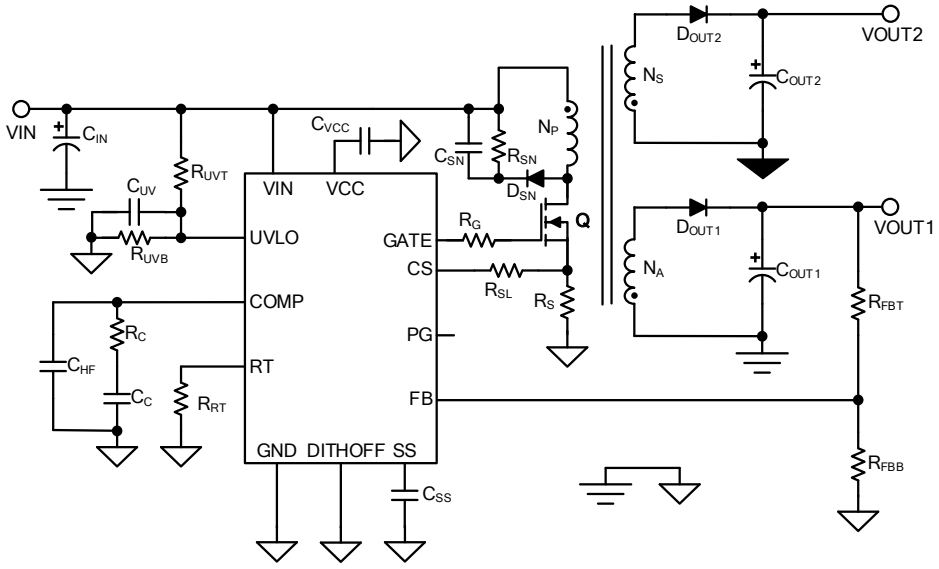


Figure 9.3 Typical Flyback Converter Connection with NSR2260x-Q1

9.2.2. Loop Stability Analysis and Design

9.2.2.1. Transfer Function and Pole-zero Location of Power Stage

In a CCM Flyback converter with peak-current-mode control and an operational transconductance amplifier (OTA) as major control component, when feedback signal come from resistance divider of auxiliary winding output which share common ground with primary winding, the power stage transfer function can be derived as below:

$$G(s) = A_{VC} \frac{\left(1 - \frac{s}{\omega_R}\right) \cdot \left(1 + \frac{s}{\omega_{ESR}}\right)}{\left(1 + \frac{s}{\omega_P}\right) \cdot \left(1 + \frac{s}{\omega_L}\right)} \quad (21)$$

Where:

$$A_{VC} = \frac{N_P \cdot R_{LOAD}}{N_S \cdot R_S} \cdot \frac{1}{\frac{(1-\text{Duty})^2}{t_L} \cdot \left(1 + 2\frac{S_A}{S_N}\right) + 2M_R + 1} \quad (22)$$

t_L is a time constant determined by power stage components and working condition:

$$t_L = \frac{2{N_S}^2 \cdot L_{PRI} \cdot f_{SW}}{{N_P}^2 \cdot R_{LOAD}} \quad (23)$$

M_R is voltage transition ratio from primary input voltage to secondary output voltage:

$$M_R = \frac{N_P \cdot V_{OUT}}{N_S \cdot V_{IN}} \quad (24)$$

S_A is voltage slope of internal compensation:

$$S_A = V_{SL} \cdot f_{SW} \quad (25)$$

S_N is voltage slope between current sense resistor when MOSFET is ON and primary current rises:

$$S_N = R_S \frac{V_{IN}}{L_{PRI}} \quad (26)$$

The angular frequency of pole from main power is:

$$\omega_P = \frac{\frac{(1-\text{Duty})^3}{t_L} \cdot \left(1 + 2\frac{S_A}{S_N}\right) + Duty + 1}{R_{LOAD} \cdot C_{OUT}} \quad (27)$$

In a CCM Flyback converter with PCM control, there is a high-frequency pole from primary inductance and Slope compensation:

$$\omega_L = \frac{\left(V_{IN} + \frac{N_P}{N_S} \cdot V_{OUT}\right) \cdot R_S \cdot f_{SW}}{S_A \cdot L_{PRI}} \quad (28)$$

When output capacitor has a equivalent series resistance (ESR), there is a zero lays at below angular frequency:

$$\omega_{ESR} = \frac{1}{C_{OUT} \cdot R_{ESR}} \quad (29)$$

There is also a right half plane zero (RHPZ) in a current-loop Flyback:

$$\omega_R = \frac{R_{LOAD} \cdot (1 - \text{Duty})^2 \cdot {N_P}^2}{\text{Duty} \cdot L_{PRI} \cdot {N_S}^2} \quad (30)$$

9.2.2.2. Transfer Function and Pole-zero Location of Compensation Stage

For transfer function of compensation section it can be expressed when C_C >> C_{HF} and output resistance of amplifier >> R_C:

$$H(s)=\frac{R_{FBB}\cdot G_{EA}\cdot R_{EAO}}{R_{FBB}+R_{FBT}}\cdot\frac{1+\frac{s}{\omega_{COMPZ}}}{\left(1+\frac{s}{\omega_{COMPP1}}\right)\cdot\left(1+\frac{s}{\omega_{COMPP2}}\right)} \quad (31)$$

Where:

$$\omega_{COMPZ}=\frac{1}{R_C\cdot C_C} \quad (32)$$

$$\omega_{COMPP1}=\frac{1}{R_{EAO}\cdot C_C} \quad (33)$$

$$\omega_{COMPP2}=\frac{1}{R_C\cdot C_{HF}} \quad (34)$$

9.2.2.3. Loop Stability Analysis

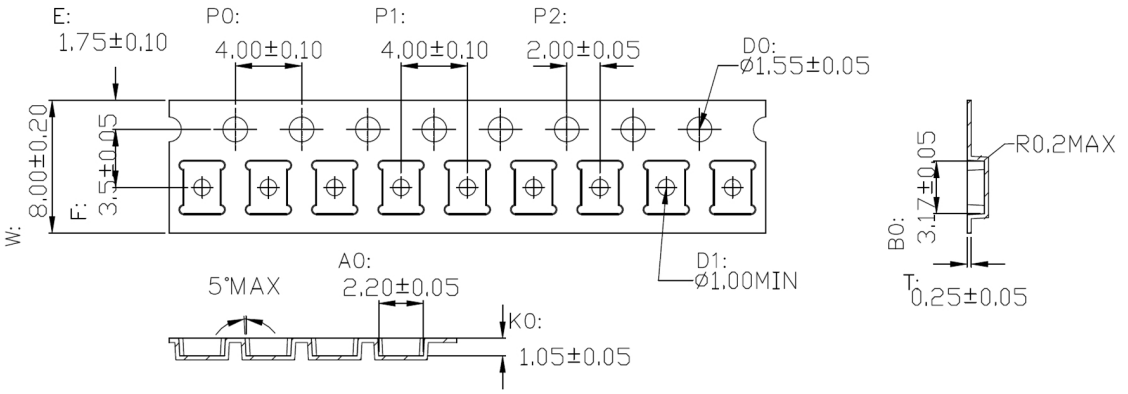
From above equations, any change of some components could cause significant changes to loop stability. In a typically designed CCM flyback converter, when component changed, the influential changes on loop stability is summary in below table:

Component Changes	Influence on Transfer Function	Typical Influence on Bode Plot
Increase L_{PRI}	Lower ω_P, Lowe ω_L	Lower phase margin
Increase C_{OUT}	Lower ω_P	Lower bandwidth
Increase ESR of C_{OUT}	Lower ω_{ESR}	Earlier boost on phase at high frequency
Increase R_S	Lower A_{VC}	Lower bandwidth
Increase R_C	Lower ω_{COMPZ} Lower ω_{COMPP2}	Earlier boost on gain and phase at low frequency Earlier drop on gain and phase at high frequency
Increase C_C	Lower ω_{COMPZ} Lower ω_{COMPP1}	Earlier boost on gain and phase at low frequency Earlier drop on gain and phase at medium frequency
Increase C_{HF}	Lower ω_{COMPP2}	Earlier drop on gain and phase at high frequency

10. Package Information

10.1. DFN12

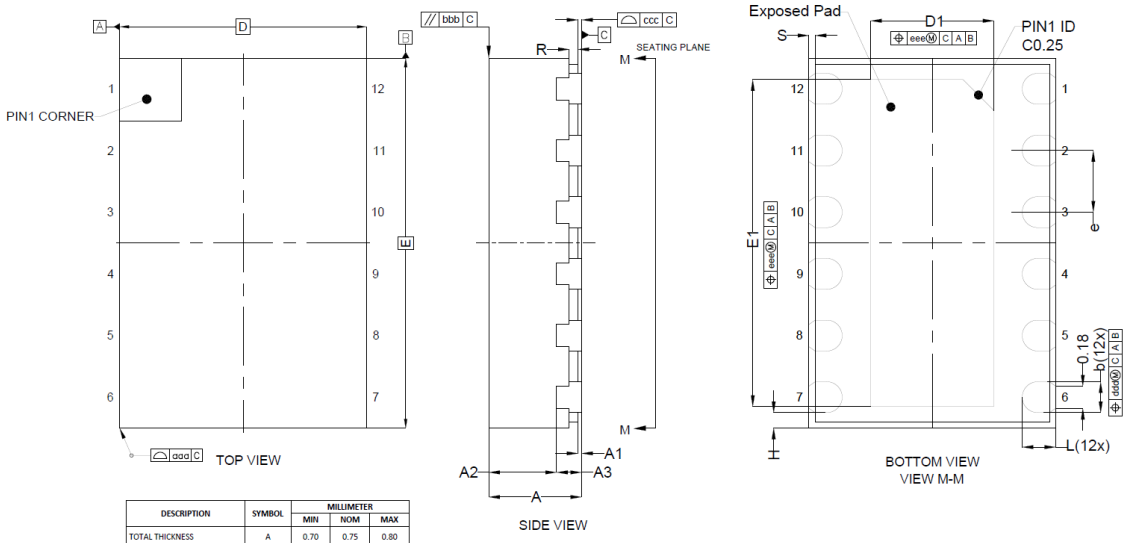
10.1.1. Tape and Reel



1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.25±0.05mm.
6. Packing length per 17" reel : 500 Meters.
7. Surface resistivity :10^{5}~ 10^{10}Ω/sq

W	8.00±0.20
A0	2.20±0.05
B0	3.17±0.05
K0	1.05±0.05

10.1.2. Mechanical Data



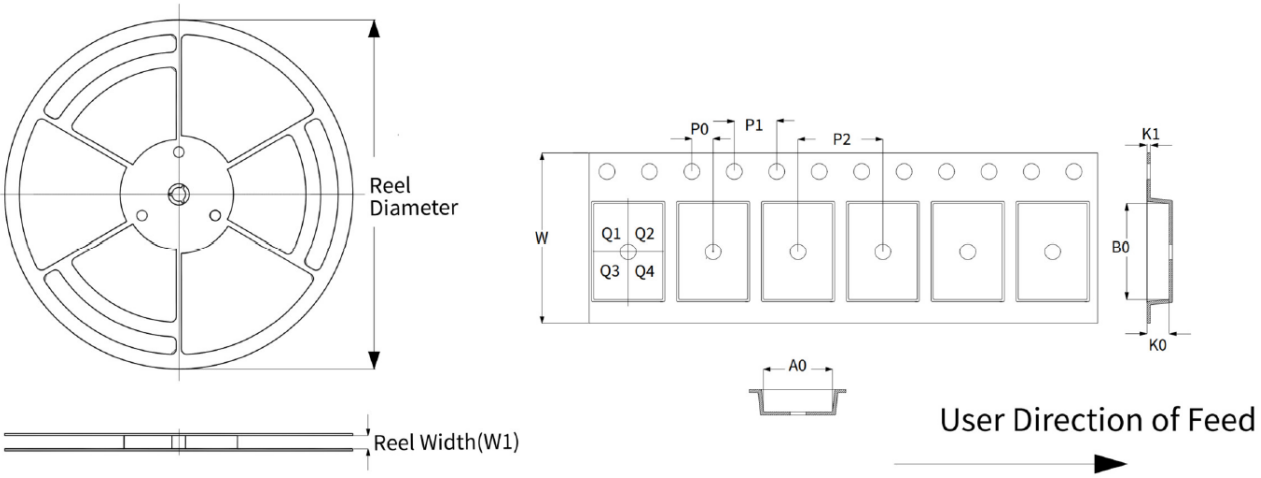
DESCRIPTION		SYMBOL	MILLIMETER MIN	NOM	MAX
TOTAL THICKNESS		A	0.70	0.75	0.80
STAND OFF		A1	0.00	---	0.05
MOLD THICKNESS		A2	0.50	0.55	0.60
L/F THICKNESS		A3		0.203 REF	
BODY SIZE	X	D	1.95	2.00	2.05
	Y	E	2.95	3.00	3.05
LEAD PITCH		e		0.50 BSC	
LEAD WIDTH		b	0.20	0.25	0.30
LEAD LENGTH		L	0.22	0.27	0.32
EP SIZE	X	D1	0.95	1.00	1.05
	Y	E1	2.60	2.65	2.70
STEP CUT WIDTH		S	0.001	0.05	0.09
STEP CUT HEIGHT		R	0.05	0.10	0.15
LEAD EDGD TO PKG EDGE		H		0.125	
TOLERANCE OF FORM AND POSITION					
GEOMETRIC TOLERANCE		aaa		0.05	
MOLD FLATNESS		bbb		0.10	
LEAD COPLANARITY		ccc		0.08	
LEAD POSITION OFFSET		ddd		0.10	
EXPOSED PAD OFFSET		eee		0.10	

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

10.2. HTSSOP14

10.2.1. Tape and Reel

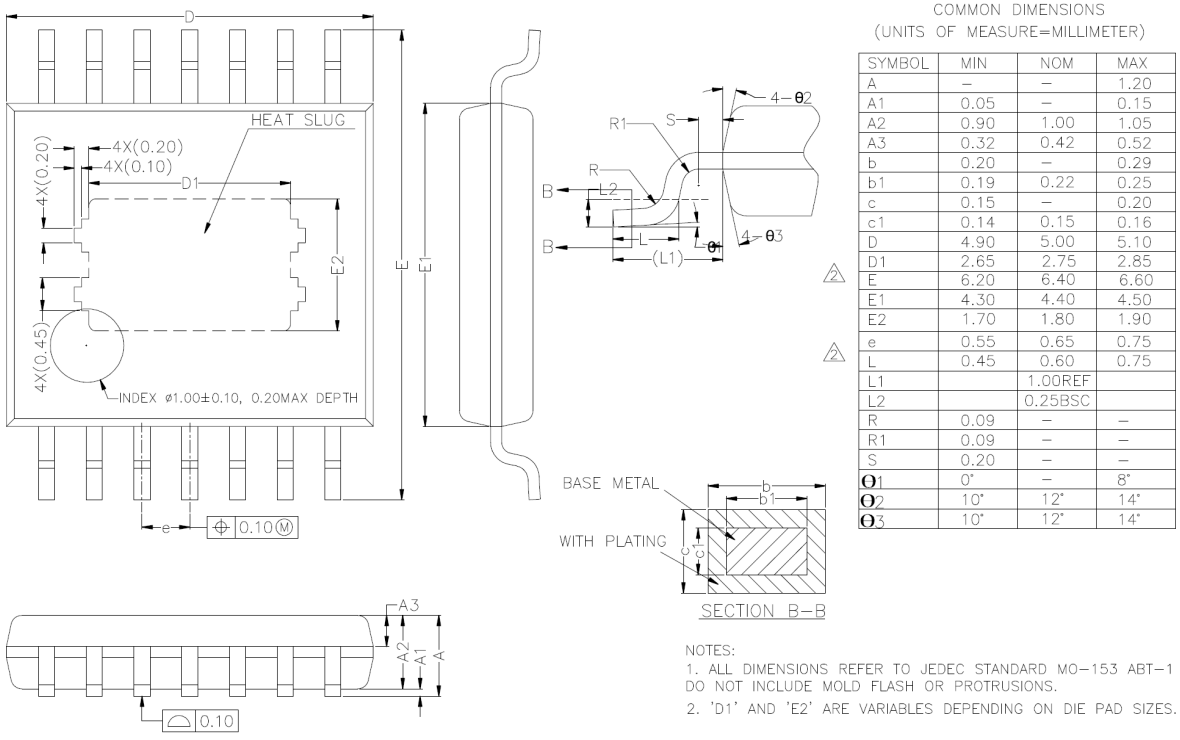


Reel Diameter	Reel Width(W1)	W	A0	B0	P0	P1	P2	K0	K1	PIN1 Quadrant
330	12.4	12.0	6.85	5.45	2.0	4.0	8.0	1.6	0.35	Q1

Note:

1. All dimensions are nominal.
2. The picture is only for reference. Please make the object as the standard.
3. Unit: mm.

10.2.2. Mechanical Data



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.90	1.00	1.05
A3	0.32	0.42	0.52
b	0.20	–	0.29
b1	0.19	0.22	0.25
c	0.15	–	0.20
c1	0.14	0.15	0.16
D	4.90	5.00	5.10
D1	2.65	2.75	2.85
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	1.70	1.80	1.90
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ1	0°	–	8°
θ2	10°	12°	14°
θ3	10°	12°	14°

NOTES:
1. ALL DIMENSIONS REFER TO JEDEC STANDARD MO-153 ABT-1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. 'D1' AND 'E2' ARE VARIABLES DEPENDING ON DIE PAD SIZES.

11. Order Information

Orderable Part	SPQ	MPQ	Package Type Pins	Operating Temp	MSL	Device Marking
NSR22601-Q1DBAR	3000	3000	DFN12-WF	-40 to 125°C	3	R22601
NSR22602-Q1DBAR	3000	3000	DFN12-WF	-40 to 125°C	3	R22602
NSR22603-Q1DBAR	3000	3000	DFN12-WF	-40 to 125°C	3	R22603
NSR22604-Q1DBAR	3000	3000	DFN12-WF	-40 to 125°C	3	R22604
NSR22605-Q1HTSKR	4000	4000	HTSSOP14	-40 to 125°C	3	NSR 22605Q
NSR22606-Q1HTSKR	4000	4000	HTSSOP14	-40 to 125°C	3	NSR 22606Q

12. Revision History

Revision	Description	Date
1.0	Initial version	2025/11
1.1	Change V_{EN_R} ,V_{EN_F} and I_{SLOPE} range in 7.1 Electrical Characteristics. Correct reel width in 10.2.1 Tape and Reel.	2025/12
1.2	Rearrange the title number of figures. Delete parameter R_{EAO} in 7.1 Electrical Characteristics. Add more annotation in 7.1 Electrical Characteristics. Correct HTSSOP14 package parameter E2 in 10.2.2 Mechanical Data. Add more information in 11. Order Information.	2026/05

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