NOVOSENSE

# NSI67x0-Q1

# Single-Channel Isolated Smart Gate Driver

Datasheet (EN) 1.2

## Product Overview

The NSI67x0 is a single-channel reinforced isolated smart gate driver to drive IGBT and SiC MOSFETs in many applications. It can source and sink 10A peak current. System robustness is supported by 150kV/us minimum common-mode transient immunity (CMTI). The NSI67x0 includes crucial protection features such as miller clamp, DESAT or OC, UVLO and soft turn off. UVLO and short circuit faults are reported through separate pins. It integrates the isolated analog to PWM sensor, which can be used for easier temperature or voltage sensing, further increasing the drivers' versatility and simplifying the system design effort, size, and cost.

## Key Features

- 5.7kV$_{RMS}$ withstand isolation voltage
- SiC MOSFETs and IGBTs up to 2121V$_{pk}$
- Driver side supply voltage: up to 33V with UVLO
- 10A peak source and sink output current
- High CMTI: ±150kV/us
- DESAT or OC option for protection
- Monitor status of device on FLT and RDY
- 80ns typical propagation delay
- 420mA or 900mA soft turn off current option
- 50ns maximum pulse width distortion
- Isolated analog sensor with PWM output for
  – Temperature sensing with NTC, PTC or thermal diode
  – High voltage DC-Link or phase voltage
- RoHS & REACH Compliant
- Lead-free component, suitable for lead-free soldering profile: 260°C, MSL3
- AEC-Q100 Qualified for Grade1: $T_A$ from -40°C to 125°C

## Safety Regulatory Approvals

- UL recognition: 5700V$_{RMS}$
- DIN EN IEC 60747-17(VDE 0884-17)
- CSA component notice 5A
- CQC certification per GB4943.1

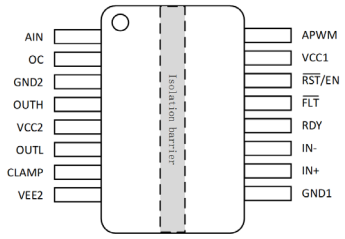
## Applications

- Traction Inverter for EVs
- On-board Charger and charging pile
- DC/DC Converter for HEV/EVs

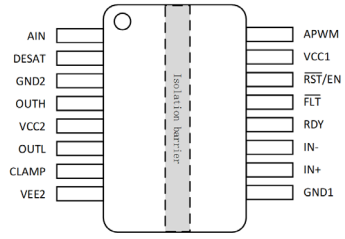
## Device Information

| *Part Number* | *AIN-Internal current source* | *Protection* |
|---|---|---|
| NSI6730ASA-Q1SWR | YES | OC, Detection Threshold=0.7V $I_{STO}$=420mA |
| NSI6730ASB-Q1SWR | YES | DESAT, Detection Threshold=6.5V, $I_{STO}$=420mA |
| NSI6730ASC-Q1SWR | YES | DESAT, Detection Threshold=9V $I_{STO}$=420mA |
| NSI6770ASC-Q1SWR | NO | DESAT, Detection Threshold=9V $I_{STO}$=420mA |
| NSI6770AHC-Q1SWR | NO | DESAT, Detection Threshold=9V $I_{STO}$=900mA |

## Pin Map




NSI6730ASA



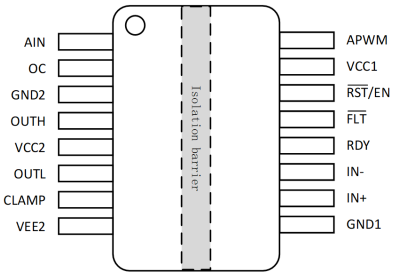

NSI6730ASB / NSI6730ASC
NSI6770ASC/NSI6770AHC

## Index

# 1. Pin Configuration and Functions

NSI6730ASA

Top View




NSI6730ASB / NSI6730ASC

NSI6770ASC / NSI6770AHC

Top View

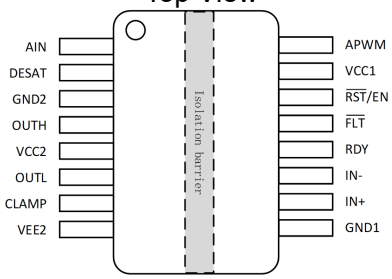



**Table 1.1 NSI67x0 Pin Configuration and Description**

| *Symbol* | *PIN No.* | | *Function* |
|---|---|---|---|
| | *NSI6730ASA* | *NSI6730ASB<br>NSI6730ASC<br>NSI6770ASC<br>NSI6770AHC* | |
| AIN | 1 | 1 | Isolated Analog sensing input |
| DESAT | / | 2 | DESAT for Fast overcurrent and short circuit protection |
| OC | 2 | / | OC for Fast overcurrent and short circuit protection |
| GND2 | 3 | 3 | Driver side ground pin |
| OUTH | 4 | 4 | Driver source output pin |
| $V_{CC2}$ | 5 | 5 | Driver side positive supply pin |
| OUTL | 6 | 6 | Driver sink output pin |
| CLAMP | 7 | 7 | Internal active miller clamp to prevent false turn-on |
| $V_{EE2}$ | 8 | 8 | Driver side negative supply pin |
| GND1 | 9 | 9 | Input-side ground pin |
| IN+ | 10 | 10 | Non-inverting gate driver control input |
| IN- | 11 | 11 | Inverting gate driver control input |
| RDY | 12 | 12 | Power good signal. Active low to report under voltage lock |
| $\overline{FLT}$ | 13 | 13 | Fault output pin. Active low to report overcurrent or short circuit |
| $\overline{RST}/EN$ | 14 | 14 | Enable the device if this pin is set to high, or set low to reset the fault signal under DESAT condition |
| $V_{CC1}$ | 15 | 15 | Input-side power supply |
| APWM | 16 | 16 | Isolated Analog Sensing PWM output |

## 2. Absolute Maximum Ratings

| Parameters | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Driver Side Supply Voltage | $V_{CC2}$-$V_{EE2}$ | -0.3 | 38 | V |
| Driver Side Supply Voltage | $V_{CC2}$-GND2 | -0.3 | 38 | V |
| Driver Side Supply Voltage | $V_{EE2}$-GND2 | -17.5 | 0.3 | V |
| Output Signal Voltage – DC | $V_{OUTH}$, $V_{OUTL}$, $V_{CLAMP}$ | $V_{EE2}$-0.3 | $V_{CC2}$ | V |
| Input Side Supply Voltage | $V_{CC1}$ | -0.3 | 6 | V |
| Input Signal Voltage – DC | $V_{IN+}$, $V_{IN-}$, $V_{RST}$ | GND1-0.3 | $V_{CC1}$+0.3 | V |
| RDY, FLT (Input Side) voltage | $V_{RDY}$, $V_{FLT}$ | GND1-0.3 | $V_{CC1}$ | V |
| DESAT or OC (Driver Side) input voltage | $V_{DESAT}$ | GND2-0.3 | $V_{CC2}$+0.3 | V |
| AIN input voltage | $V_{AIN}$ | GND2-0.3 | 6 | V |
| FLT and RDY input current | $I_{FLT}$, $I_{RDY}$ | | 20 | mA |
| APWM output current | $I_{APWM}$ | | 20 | mA |
| Operating Junction Temperature | $T_J$ | -40 | 150 | °C |
| Storage Temperature | $T_{stg}$ | -65 | 150 | °C |

## 3. ESD Ratings

| | | Symbol | Value | Unit |
|---|---|---|---|---|
| Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | $V_{ESD\_HBM}$ | ±3000 | V |
| | Charged-device model (CDM), per AEC Q100-011 | $V_{ESD\_CDM}$ | ±1500 | V |

1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 4. Recommended Operating Conditions

| Parameters | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Ambient Temperature | $T_A$ | -40 | 125 | °C |
| Input Side Supply Voltage | $V_{CC1}$-GND1 | 3 | 5.5 | V |
| Driver Side Supply Voltage | $V_{CC2}$-GND2 | 13 | 33 | V |
| Driver Side Supply Voltage | $V_{CC2}$-$V_{EE2}$ | - | 33 | V |
| AIN input voltage | $V_{AIN}$ | 0 | 5 | V |
| IN+, IN-,$\overline{RST}$/EN (Respect to GND1) | High level input voltage | 0.7×$V_{CC1}$ | $V_{CC1}$ | V |
| | Low level input voltage | 0 | 0.3×$V_{CC1}$ | |

# 5. Thermal Information

| *Parameters* | *Symbol* | *SOW16* | *Unit* |
|---|---|---|---|
| Junction–to-ambient thermal resistance | $R_{\theta JA}$ | 67.6 | °C/W |
| Junction–to-top characterization parameter | $\Psi_{JT}$ | 14.9 | °C/W |
| Junction–to-board characterization parameter | $\Psi_{JB}$ | 30.4 | °C/W |
| Junction–to-case(top) thermal resistance | $R_{JC(top)}$ | 29.7 | °C/W |

1) Standard JESD51-7 High Effective Thermal Conductivity Test Board (2S2P) in an environment described in JESD51-2a.

2) Standard JESD51-7 High Effective Thermal Conductivity Test Board (2S2P) by transient dual interface test method described in JESD51-14.

3) Obtained by Simulating in an environment described in JESD51-2a.

# 6. Specifications

## 6.1. DC Electrical Characteristics

All min and max specifications are at $T_A$=-40°C to 125°C. Typical values are tested at $V_{CC1}$=3.3V or 5V, $V_{CC2}$ =15V or 33V, $V_{EE2}$=GND2.

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| **Input Side Supply** | | | | | | |
| Input side Supply Quiescent Current | $I_{CC1\_ON}$ | 2.5 | 3.6 | 4.5 | mA | $V_{CC1}$=5V, OUT=High, $V_{AIN}$=2V |
| | $I_{CC1\_OFF}$ | 0.6 | 1.5 | 2.6 | | $V_{CC1}$=5V, OUT=Low, $V_{AIN}$=2V |
| $V_{CC1}$ UVLO Rising Threshold | $V_{CC1\_ON}$ | 2.5 | 2.72 | 2.95 | V | |
| $V_{CC1}$ UVLO Falling Threshold | $V_{CC1\_OFF}$ | 2.35 | 2.57 | 2.75 | V | |
| $V_{CC1}$ UVLO Hysteresis | $V_{CC1\_HYS}$ | | 0.15 | | V | |
| $V_{CC1}$ UVLO deglitch time | $t_{VCC1\_FIL}$(1) | | 7 | | μs | |
| $V_{CC1}$ UVLO on delay to output high | $t_{VCC1H\_OUT}$(1) | | 60 | | | IN+=$V_{CC1}$ IN-=GND1 |
| $V_{CC1}$ UVLO off delay to output low | $t_{VCC1L\_OUT}$(1) | | 5 | | | |
| $V_{CC1}$ UVLO on delay to RDY high | $t_{VCC1H\_RDY}$(1) | | 60 | | | $\overline{RST}$/EN=$V_{CC1}$ |
| $V_{CC1}$ UVLO off delay to RDY low | $t_{VCC1L\_RDY}$(1) | | 5 | | | |
| **Driver Side Supply** | | | | | | |
| Driver side Supply Quiescent Current | $I_{CC2\_ON}$ | 3.4 | 4.6 | 6 | mA | $V_{CC2}$=15V, $V_{EE2}$=GND2, OUT=High，$V_{AIN}$=2V |
| | $I_{CC2\_OFF}$ | 2 | 4 | 5.5 | | $V_{CC2}$=15V, $V_{EE2}$=GND2, OUT=Low，$V_{AIN}$=2V |
| $V_{CC2}$ UVLO Rising Threshold | $V_{CC2\_ON}$ | 10.5 | 12.1 | 13 | V | |
| $V_{CC2}$ UVLO Falling Threshold | $V_{CC2\_OFF}$ | 9.9 | 11.1 | 11.8 | V | |
| $V_{CC2}$ UVLO Hysteresis | $V_{CC2\_HYS}$ | | 1 | | V | |
| $V_{CC2}$ UVLO deglitch time | $t_{VCC2\_FIL}$(1) | | 4.9 | | μs | |
| $V_{CC2}$ UVLO on delay to output high | $t_{VCC2H\_OUT}$(1) | | 14 | | | IN+=$V_{CC1}$ IN-=GND1 |
| $V_{CC2}$ UVLO off delay to output low | $t_{VCC2L\_OUT}$(1) | | 5.5 | | | |
| $V_{CC2}$ UVLO on delay to RDY high | $t_{VCC2H\_RDY}$(1) | | 18 | | | $\overline{RST}$/EN=$V_{CC1}$, DESAT=GND2 |
| $V_{CC2}$ UVLO off delay to RDY low | $t_{VCC2L\_RDY}$(1) | | 10 | | | |
| **RDY Reporting** | | | | | | |
| $V_{CC2}$ UVLO RDY low minimum holding time | $t_{RDY\_HLD}$ | 0.55 | | 1 | ms | |

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Open drain low output voltage | $V_{RDY\_L}$ | | | 0.3 | V | $I_{SINK\_RDY}$=5mA |
| RDY open drain output on resistance | $R_{ODON\_RDY}$ | | 31 | | Ω | $I_{SINK\_RDY}$=5mA |
| **Input Pin Characteristic** | | | | | | |
| Logic High Input Threshold (IN+, IN-, RST) | $V_{INH}$ | 2.2 | 2.8 | 3.5 | V | $V_{CC1}$=5V |
| Logic Low Input Threshold (IN+, IN-, RST) | $V_{INL}$ | 1.5 | 2.2 | 2.9 | V | $V_{CC1}$=5V |
| Input Hysteresis Voltage (IN+, IN-, RST) | $V_{hys\_IN}$ | | 0.6 | | V | $V_{CC1}$=5V |
| IN+ Input Current | $I_{IN+\_H}$ | | 95 | | μA | $V_{IN+}$=5V |
| IN- Input Current | $I_{IN-\_L}$ | | -95 | | μA | $V_{IN-}$=GND1 |
| RST Input Current | $I_{RST\_H}$ | | 105 | | μA | $V_{RST}$=5V |
| IN+ pull down resistance | $R_{IN+}$ | | 55 | | kΩ | |
| IN- pull up resistance | $R_{IN-}$ | | 55 | | | |
| RST pull down resistance | $R_{RST}$ | | 50 | | | |
| RST deglitch filter time for Enable/Shutdown | $t_{min\_RST}$ | 28 | 40 | 60 | ns | |
| RST deglitch filter time for Resetting FLT | $t_{RST\_FIL}$ | 400 | 660 | 800 | ns | |
| **FLT Reporting** | | | | | | |
| Open drain low output voltage | $V_{FLT\_L}$ | | | 0.3 | V | $I_{SINK\_FLT}$=5mA |
| FLT mute time | $t_{FLT\_MUTE}$ | 0.55 | | 1 | ms | |
| FLT open drain output on resistance | $R_{ODON\_FLT}$ | | 31 | | Ω | $I_{SINK\_FLT}$=5mA |
| **Output Pin Characteristic** | | | | | | |
| High Level Output Voltage | $V_{OH}$ | | $V_{CC2}$-0.1 | | V | $I_{OUT}$=-100mA, $V_{IN+}$=High,$V_{IN-}$=Low |
| Low Level Output Voltage | $V_{OL}$ | | 40 | | mV | $I_{OUT}$=100mA, $V_{IN+}$=Low, $V_{IN-}$=Low |
| Output pull-up resistance | $R_{OH}$ | | 0.7 | | Ω | $I_{OUT}$=-100mA, $V_{IN+}$=High, $V_{IN-}$=Low |
| Output pull-down resistance | $R_{OL}$ | | 0.4 | | Ω | $I_{OUT}$=100mA, $V_{IN+}$=Low, $V_{IN-}$=High |
| High Level Peak Output Current | $I_{OUTH}$(1) | | 10 | | A | |
| Low Level Peak Output Current | $I_{OUTL}$(1) | | 10 | | A | |
| OUT Short Circuit Clamping Voltage | $V_{CLP\_OUT}$ | | $V_{CC2}$+1.35 | | V | $V_{IN+}$=High, $V_{IN-}$=Low, $I_{OUTL}$=0.5A, pulse width<10us |

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| OUT Active Pull-Down Voltage | $V_{SD\_OUT}$ | 1.5 | 2.4 | 3 | V | $V_{CC2}$=OPEN, $I_{OUTL}$=0.1×$I_{OUTL}$(typ) |
| **Internal miller clamp** | | | | | | |
| Clamp Threshold Voltage | $V_{CLAMP\_TH}$ | 1.5 | 2.1 | 2.5 | V | $V_{CLAMP}$ falling, $V_{IN+}$=Low, $V_{IN-}$=Low |
| Clamp Delay | $t_{DCLMP}$(2) | | 70 | | ns | |
| Miller clamp pull down resistance | $R_{clamp}$ | | 0.6 | | Ω | $I_{CLAMP}$=0.1A |
| Output low clamp voltage | $V_{clamp\_L}$ | | 60 | | mV | $I_{CLAMP}$=0.1A |
| Output low clamp current | $I_{clamp}$(1) | | 5.7 | | A | |
| CLAMP Short Circuit Clamping Voltage | $V_{CLP\_CLAMP}$ | | $V_{CC2}$+1.4 | | V | $V_{IN+}$=High, $V_{IN-}$=Low, $I_{OUTH}$=0.5A, pulse width<10us |
| | | | $V_{CC2}$+0.9 | | | $V_{IN+}$=High, $V_{IN-}$=Low, $I_{CLAMP}$=20mA |
| **AIN-APWM SENSING** | | | | | | |
| Analog sensing voltage range (Linear region) | $V_{AIN}$ | 0.3 | | 4.6 | V | |
| APWM output frequency | $f_{APWM}$ | 8 | 10 | 12 | kHz | |
| AIN-APWM bandwidth | $BW_{AIN}$(2) | | 5 | | kHz | |
| APWM Duty cycle (Linear region) | $D_{APWM}$ | 91.2 | 92 | 92.8 | % | $V_{AIN}$=0.4V |
| | | 74.2 | 75 | 75.8 | | $V_{AIN}$=1.25V |
| | | 48.9 | 50 | 51.1 | | $V_{AIN}$=2.5V |
| | | 8.5 | 10 | 11.5 | | $V_{AIN}$=4.5V |

## 6.2. Specialized Characteristics

All min and max specifications are at $T_A$=-40°C to 125°C. Typical values are tested at $V_{CC1}$=3.3V or 5V, $V_{CC2}$ =15V or 32V, $V_{EE2}$=GND2.

| *Parameter* | *Symbol* | *Min* | *Typ* | *Max* | *Unit* | *Condition* |
|---|---|---|---|---|---|---|
| **NSI6730ASA** | | | | | | |
| **OC PROTECTION** | | | | | | |
| Blanking Capacitor Discharge Current | $I_{DCHG}$ | | 40 | | mA | $V_{OC}$=6v |
| Detection Threshold | $V_{OCTH}$ | 0.63 | 0.69 | 0.77 | V | |
| OC deglitch filter time | $t_{oc\_FIL}$ | 120 | 170 | 220 | ns | |
| OC sense to OUT(L) 90% delay | $t_{oc\_OFF}$ | 150 | 230 | 400 | ns | |
| OC sense to FLT low delay | $t_{OC\_FLT}$ | | 1.5 | | µs | |
| **Soft turn off current** | | | | | | |
| Soft turn off current | $I_{STO}$ | 250 | 420 | 600 | mA | |
| **AIN-APWM SENSING** | | | | | | |
| Internal current source | $I_{AIN}$ | | 200 | | µA | |
| **NSI6730ASB** | | | | | | |
| **DESAT PROTECTION** | | | | | | |
| Blanking Capacitor Discharge Current | $I_{DCHG}$ | 20 | 43 | 60 | mA | $V_{DESAT}$=6V |
| Blanking Capacitor Charge Current | $I_{CHG}$ | 430 | 510 | 570 | µA | $V_{DESAT}$=2V |
| Leading edge blank time | $t_{DESAT\_LEB}$(1) | | 230 | | ns | |
| DESAT deglitch filter time | $t_{DESAT\_FIL}$ | 50 | 160 | 230 | ns | |
| DESAT sense to OUT(L) 90% delay | $t_{DESAT\_OFF}$ | 150 | 230 | 300 | ns | |
| DESAT sense to FLT low delay | $t_{DESAT\_FLT}$ | | 1.4 | | µs | |
| Detection Threshold | $V_{DESAT\_TH}$ | 6 | 6.4 | 7 | V | |
| **Soft turn off current** | | | | | | |
| Soft turn off current | $I_{STO}$ | 250 | 420 | 600 | mA | |
| **AIN-APWM SENSING** | | | | | | |
| Internal current source | $I_{AIN}$ | | 200 | | µA | |
| **NSI6730ASC** | | | | | | |
| **DESAT PROTECTION** | | | | | | |
| Blanking Capacitor Discharge Current | $I_{DCHG}$ | 20 | 43 | 60 | mA | $V_{DESAT}$=6V |
| Blanking Capacitor Charge Current | $I_{CHG}$ | 430 | 510 | 570 | µA | $V_{DESAT}$=2V |
| Leading edge blank time | $t_{DESAT\_LEB}$(1) | | 230 | | ns | |
| DESAT deglitch filter time | $t_{DESAT\_FIL}$ | 50 | 160 | 230 | ns | |

| | | | | | | |
|---|---|---|---|---|---|---|
| DESAT sense to OUT(L) 90% delay | $t_{DESAT\_OFF}$ | 150 | 230 | 300 | ns | |
| DESAT sense to FLT low delay | $t_{DESAT\_FLT}$ | | 1.4 | | μs | |
| Detection Threshold | $V_{DESAT\_TH}$ | 8.5 | 9.1 | 10 | V | |
| **Soft turn off current** | | | | | | |
| Soft turn off current | $I_{STO}$ | 250 | 420 | 600 | mA | |
| **AIN-APWM SENSING** | | | | | | |
| Internal current source | $I_{AIN}$ | | 200 | | μA | |
| **NSI6770ASC** | | | | | | |
| **DESAT PROTECTION** | | | | | | |
| Blanking Capacitor Discharge Current | $I_{DCHG}$ | 20 | 43 | 60 | mA | $V_{DESAT}$=6V |
| Blanking Capacitor Charge Current | $I_{CHG}$ | 430 | 510 | 570 | μA | $V_{DESAT}$=2V |
| Leading edge blank time | $t_{DESAT\_LEB}$(1) | | 230 | | ns | |
| DESAT deglitch filter time | $t_{DESAT\_FIL}$ | 50 | 160 | 230 | ns | |
| DESAT sense to OUT(L) 90% delay | $t_{DESAT\_OFF}$ | 150 | 230 | 300 | ns | |
| DESAT sense to FLT low delay | $t_{DESAT\_FLT}$ | | 1.4 | | μs | |
| Detection Threshold | $V_{DESAT\_TH}$ | 8.5 | 9.1 | 10 | V | |
| **Soft turn off current** | | | | | | |
| Soft turn off current | $I_{STO}$ | 250 | 420 | 600 | mA | |
| **NSI6770AHC** | | | | | | |
| **DESAT PROTECTION** | | | | | | |
| Blanking Capacitor Discharge Current | $I_{DCHG}$ | 20 | 43 | 60 | mA | $V_{DESAT}$=6V |
| Blanking Capacitor Charge Current | $I_{CHG}$ | 430 | 510 | 570 | μA | $V_{DESAT}$=2V |
| Leading edge blank time | $t_{DESAT\_LEB}$(1) | | 230 | | ns | |
| DESAT deglitch filter time | $t_{DESAT\_FIL}$ | 50 | 160 | 230 | ns | |
| DESAT sense to OUT(L) 90% delay | $t_{DESAT\_OFF}$ | 150 | 230 | 300 | ns | |
| DESAT sense to FLT low delay | $t_{DESAT\_FLT}$ | | 1.4 | | μs | |
| Detection Threshold | $V_{DESAT\_TH}$ | 8.5 | 9.1 | 10 | V | |
| **Soft turn off current** | | | | | | |
| Soft turn off current | $I_{STO}$ | 600 | 900 | 1200 | mA | |

(1) *Not test covered, guaranteed by characterization.*

(2) *Not test covered, guaranteed by design.*

## 6.3. Switching Electrical Characteristics

Typical values are at $V_{CC1}$=5V, $V_{CC2}$ =15V, $V_{EE2}$=GND2. All min and max specifications are at $T_A$=-40°C to 125°C. If not mentioned, $C_L$=0.1nF.

| *Parameter* | *Symbol* | *Min* | *Typ* | *Max* | *Unit* | *Condition* |
|---|---|---|---|---|---|---|
| Minimum Pulse Width | $t_{PWmin\_IN+}$ | 10 | 30 | 60 | ns | |
| Output Rise Time | $t_R$ | | 45 | | ns | $C_{LOAD}$=10nF |
| Output Fall Time | $t_F$ | | 47 | | ns | |
| Propagation Delay | $t_{pLH\_IN+}$ | 50 | 80 | 140 | ns | $C_{LOAD}$=0.1nF |
| | $t_{pHL\_IN+}$ | 50 | 90 | 140 | ns | |
| Pulse Width Distortion $\lvert t_{PHL}-t_{PLH}\rvert$ | $t_{PWD}$ | | | 50 | ns | |
| Common Mode Transient Immunity | CMTI(1) | 150 | | | kV/μs | |

(1) *Not test covered, guaranteed by characterization.*

(2) *Not test covered, guaranteed by design.*

# 7. High Voltage Feature Description

## 7.1. Insulation and Safety Related Specifications

| *Parameter* | *Symbol* | *SOW16* | *Unit* | *Comments* |
|---|---|---|---|---|
| Minimum External Clearance | CLR | 8.0 | mm | IEC 60664-1:2007 |
| Minimum External Creepage | CPG | 8.0 | mm | IEC 60664-1:2007 |
| Distance Through Insulation | DTI | 20 | μm | Minimum internal gap |
| Tracking Resistance (Comparative Tracking Index) | CTI | >600 | V | DIN EN 60112 (VDE 0303-11); IEC 60112 |
| Material Group | | I | | |

| *Description* | *Test Condition* | *Value* |
|---|---|---|
| Overvoltage Category per IEC60664-1 | For Rated Mains Voltage ≤ 150Vrms | I to IV |
| | For Rated Mains Voltage ≤ 300Vrms | I to IV |
| | For Rated Mains Voltage ≤ 600Vrms | I to IV |
| | For Rated Mains Voltage ≤ 1000Vrms | I to III |
| Climatic Classification | | 40/125/21 |
| Pollution Degree per DIN VDE 0110 | | 2 |

## 7.2. Insulation Characteristics for SOW16 Package

| Description | Test Condition | Symbol | Value | Unit |
|---|---|---|---|---|
| Maximum Working Isolation Voltage | AC voltage (sine wave) Time dependent dielectric breakdown (TDDB)test | $V_{IOWM}$ | 1500 | $V_{RMS}$ |
| | DC voltage | | 2121 | $V_{DC}$ |
| Maximum Repetitive Peak Isolation Voltage | AC voltage(bipolar) | $V_{IORM}$ | 2121 | $V_{PEAK}$ |
| Apparent Charge | Method a, after Input/output safety test subgroup 2/3, Vini=VIOTM, tini = 60s , Vpd(m)=1.2*VIORM, tm=10s. | $q_{pd}$ | ＜5 | pC |
| | Method a, after environmental tests subgroup 1, Vini=VIOTM, tini=60s ,Vpd(m)=1.6*VIORM, tm=10s | | | |
| | Method b, routine test (100% production) and preconditioning (type test);Vini=1.2*VIOTM, tini=1s Vpd (m)=1.875*VIORM, tm=1s （method b1）or Vpd(m)=Vini, tm=tini(method b2) | | | |
| Maximum Transient Isolation Voltage | t = 60s | $V_{IOTM}$ | 8000 | $V_{PEAK}$ |
| Maximum impulse voltage | Tested in air, 1.2/50-us waveform per IEC62368-1 | $V_{IMP}$ | 6250 | $V_{PEAK}$ |
| Maximum Surge Isolation Voltage | Test method per IEC60065,1.2/50us waveform, $V_{TEST}=V_{IOSM}\times1.6$ | $V_{IOSM}$ | 10000 | $V_{PEAK}$ |
| Isolation Resistance | $V_{IO}$ =500V at $T_A=T_S$ | $R_{IO}$ | $>10^9$ | Ω |
| | $V_{IO}$ =500V at 100°C≤$T_A$≤125°C | | $>10^{11}$ | Ω |
| | $V_{IO}$ =500V ,$T_A$=25°C | | $>10^{12}$ | Ω |
| Isolation Capacitance | f = 1MHz | $C_{IO}$ | 0.8 | pF |
| **UL1577** | | | | |
| Maximum Withstanding Isolation Voltage | $V_{TEST}$= $V_{ISO}$, t = 60s (qualification); $V_{TEST}$= 1.2 ×$V_{ISO}$, t = 1s (100%production) | $V_{ISO}$ | 5700 | $V_{RMS}$ |

## 7.3. Safety Limiting Values for SOW16 Package

| Description | Test Condition | Symbol | Value | | Unit |
|---|---|---|---|---|---|
| Maximum Safety Temperature | | $T_S$ | 150 | | °C |
| Maximum Safety Power Dissipation | $R_{\theta JA}$=67.6°C/W, $T_J$=150°C, $V_{CC2}$=20V, $V_{EE2}$=-5V $T_A$=25°C | $P_S$ | Total | 1270 | mW |
| Maximum Safety Current | $R_{\theta JA}$=67.6°C/W, $V_{CC2}$=15V, $V_{EE2}$ =-5V $T_J$=150°C, $T_A$=25°C | $I_S$ | Driver side | 62 | mA |
| | $R_{\theta JA}$=67.6°C/W, $V_{CC2}$=20V, $V_{EE2}$ =-5V $T_J$=150°C, $T_A$=25°C | | Driver side | 49.6 | |

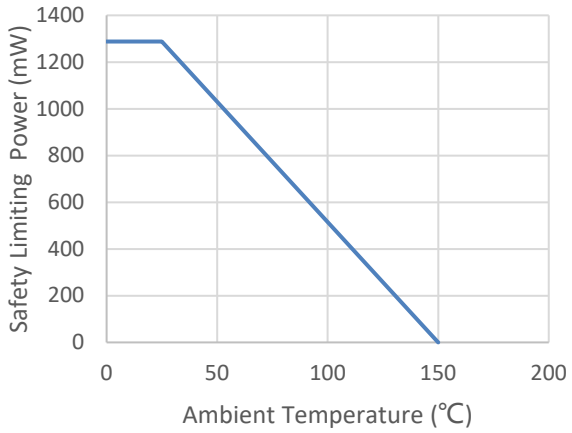



Figure 7.1 Thermal Derating Curve for Limiting Power per DIN VDE V 0884-17 for SOW16 Package

## 7.4. Regulatory Information for SOW16 Package

| *UL* | | *TUV* | *CQC* |
|---|---|---|---|
| UL 1577 Component Recognition Program | Approved under CSA Component Acceptance Notice 5A | DIN EN IEC 60747-17 (VDE 0884-17) | Certified according to GB4943.1 |
| Single Protection, 5700$V_{RMS}$ Isolation Voltage | Single Protection, 5700$V_{RMS}$ Isolation voltage | Reinforced Insulation $V_{IORM}$=2121$V_{PEAK}$, $V_{IOTM}$=8000$V_{PEAK}$ | Reinforced Insulation |
| E500602 | | R 50574061 | CQC20001264939 |

# 8. Typical Characteristics

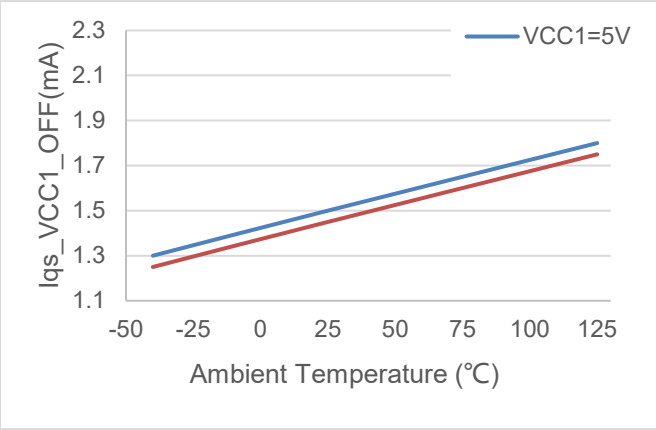



Figure 8.1 VCC1 OFF supply current vs temperature

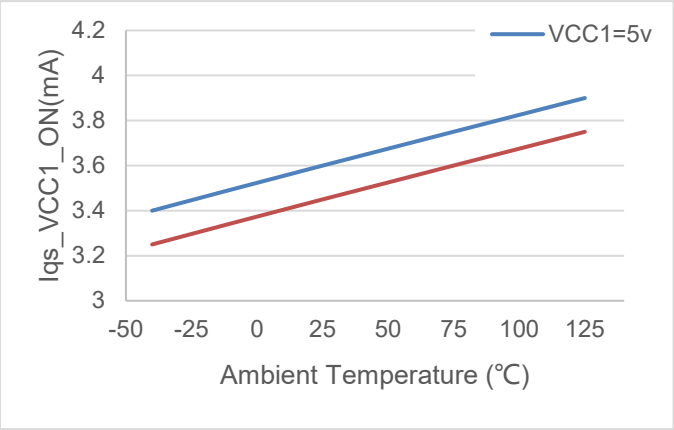



Figure 8.2 VCC1 ON supply current vs temperature

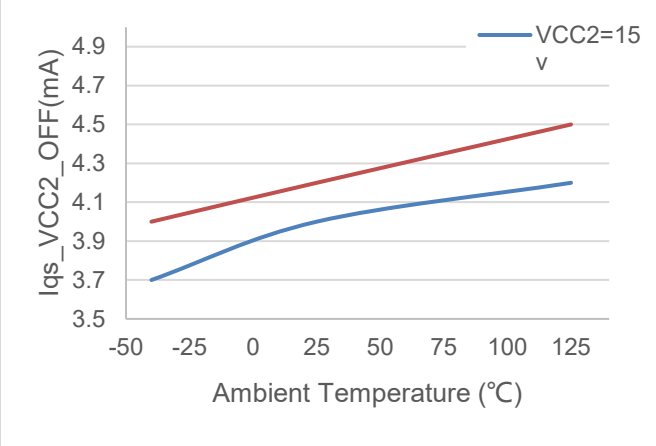



Figure 8.3 VCC2 OFF supply current vs temperature

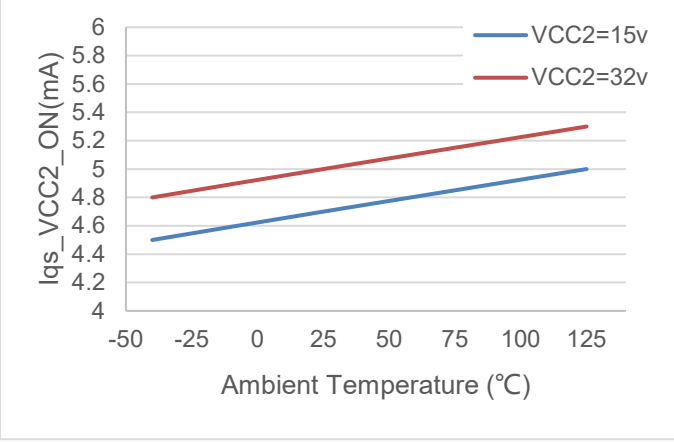



Figure 8.4 VCC2 ON supply current vs temperature

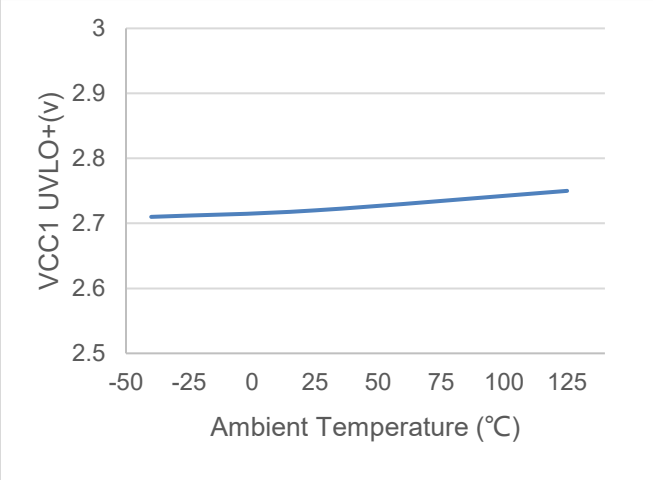



Figure 8.5 VCC1 UVLO+ vs temperature

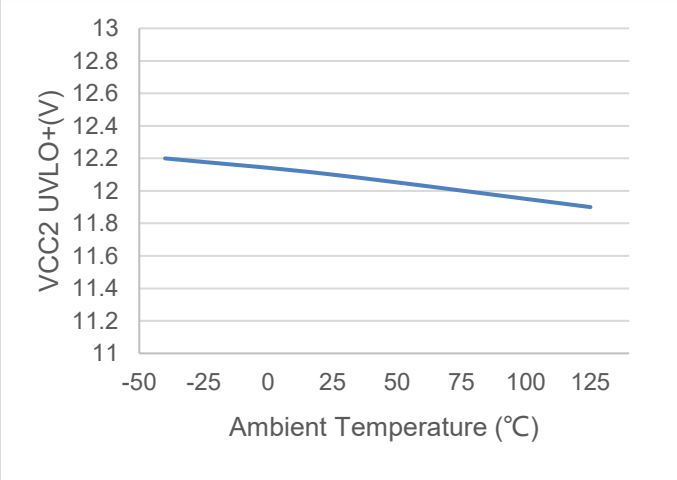



Figure 8.6 VCC2 UVLO+ vs temperature

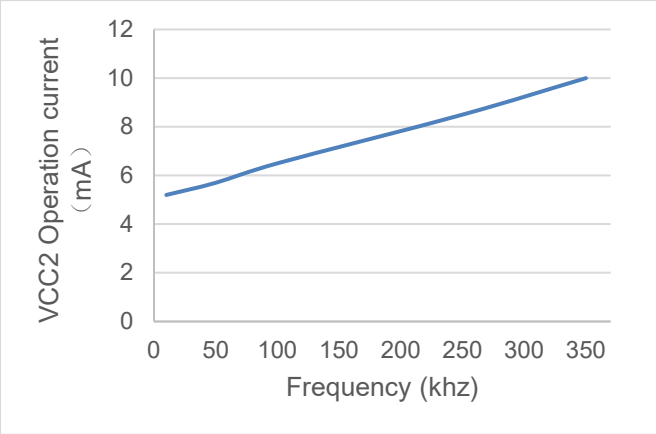



Figure 8.7 VCC2 operation current vs temperature

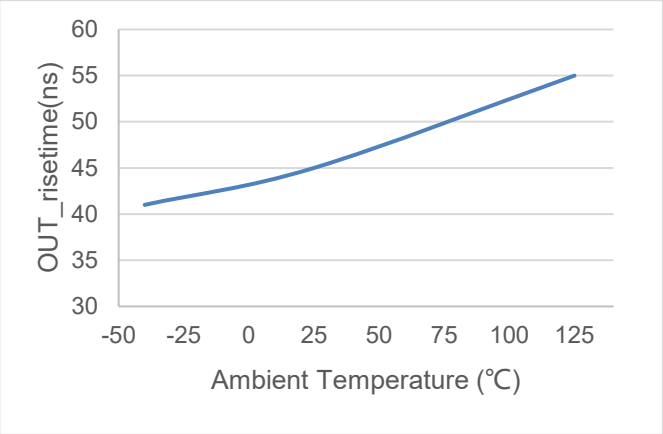



Figure 8.8 risetime vs temperature

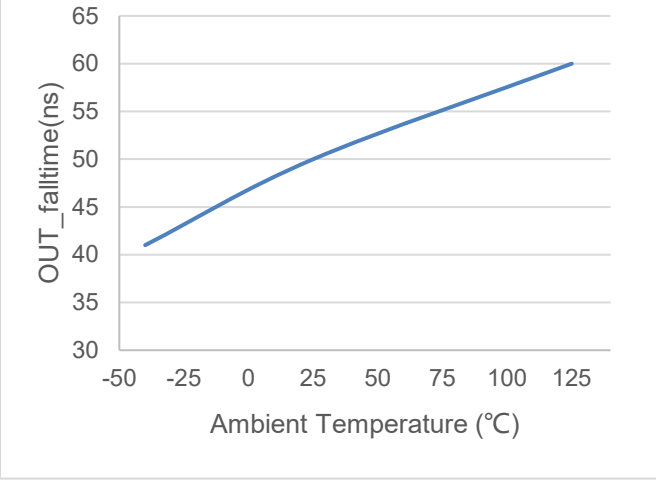



Figure 8.9 fall time vs temperature

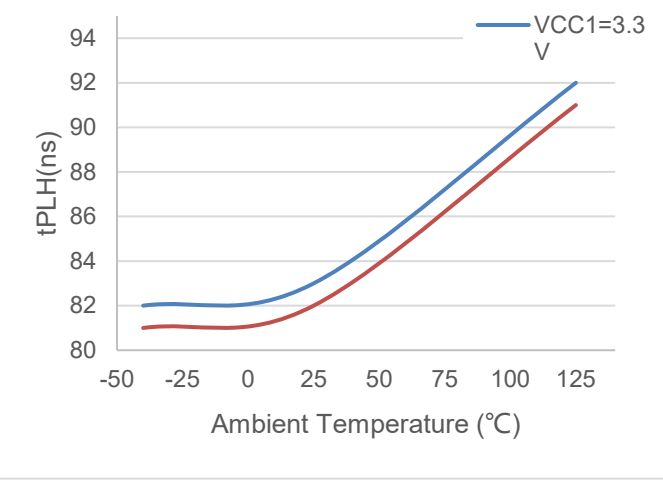



Figure 8.10 $t_{PLH\_IN+}$ vs temperature

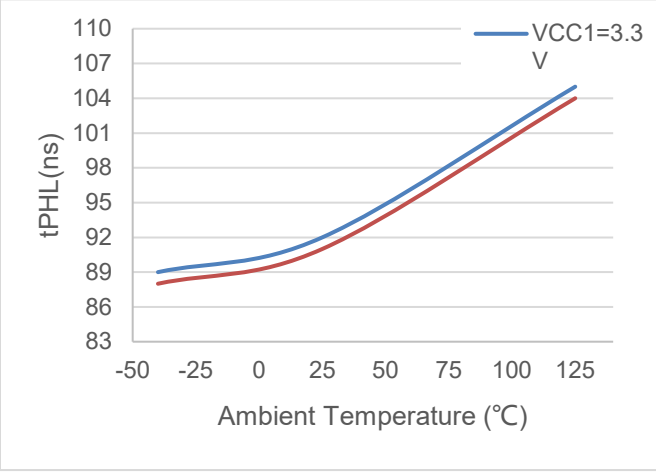



Figure 8.11 $t_{PHL\_IN+}$ vs temperature

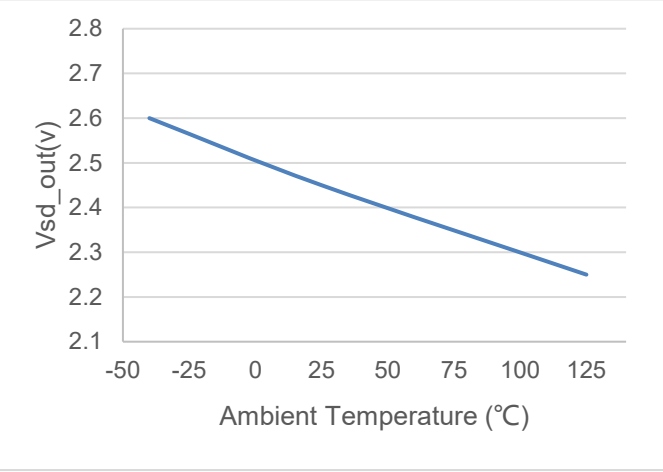



Figure 8.12 Active pulldown voltage vs temperature

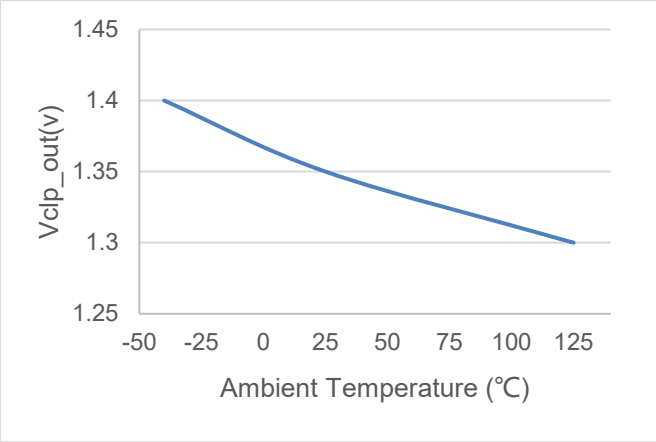



Figure 8.13 short circuit clamp vs temperature

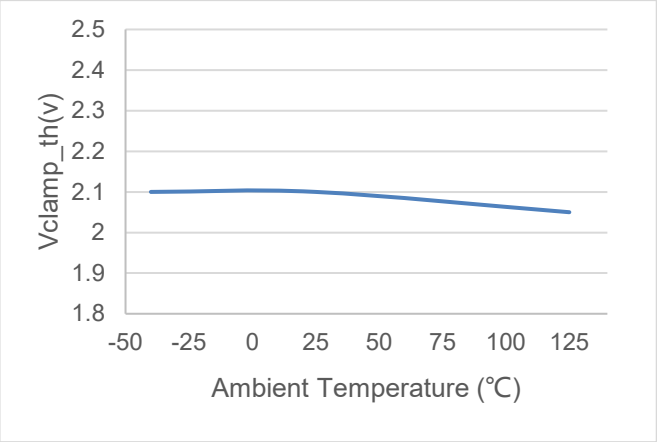



Figure 8.14 miller clamp threshold vs temperature

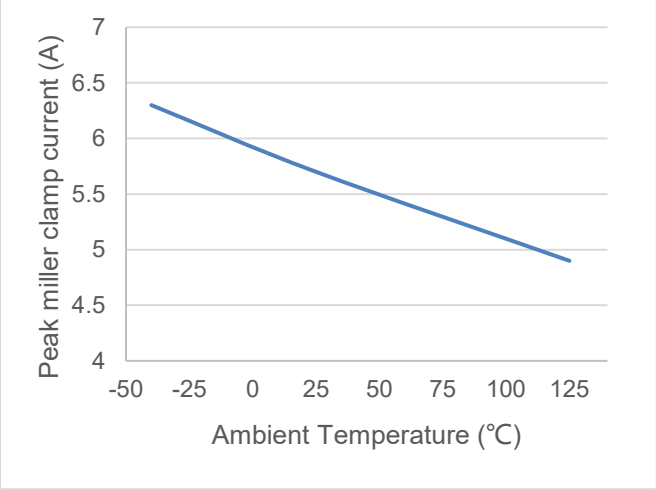



Figure 8.15 peak miller clamp current vs temperature

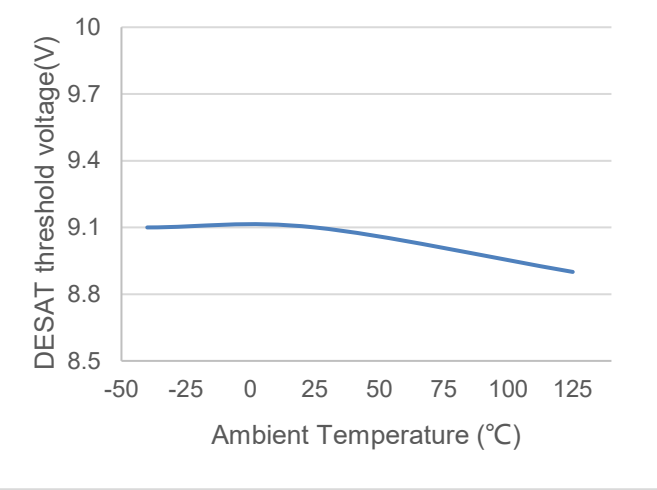



Figure 8.16 DESAT threshold vs temperature

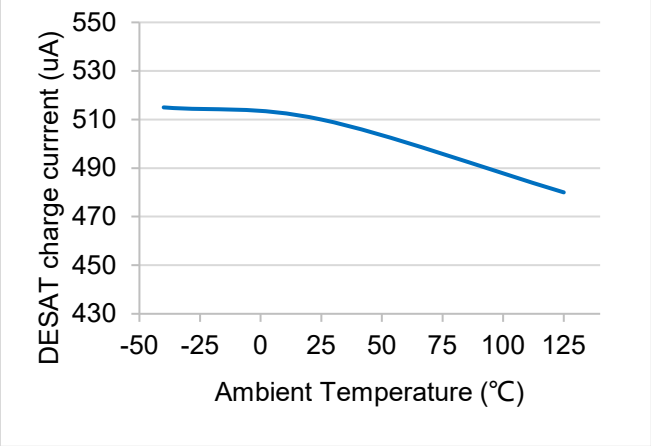



Figure 8.17 DESAT charge current vs temperature

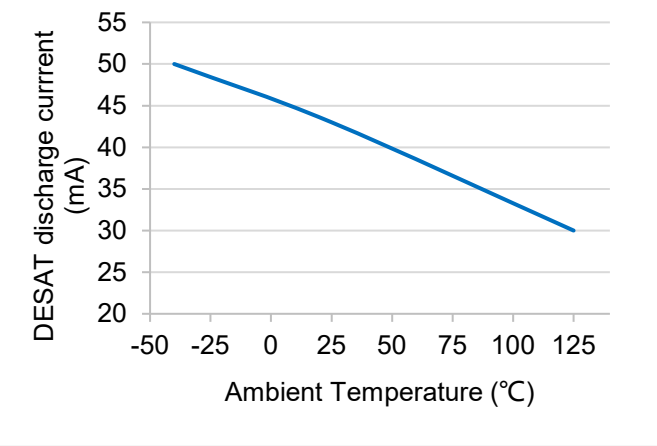



Figure 8.18 DESAT discharge current vs temperature

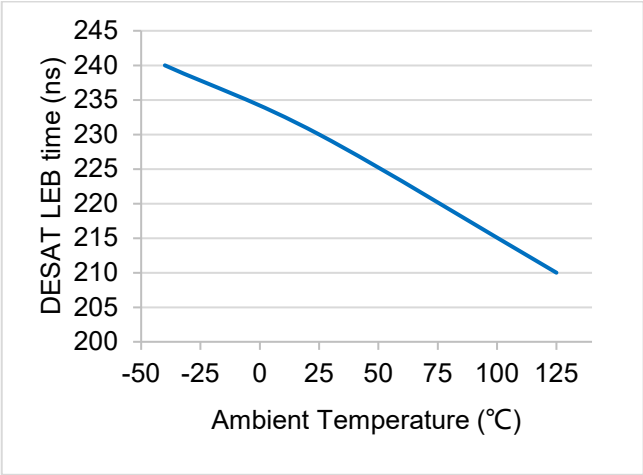



Figure 8.19 DESAT LEB time vs temperature

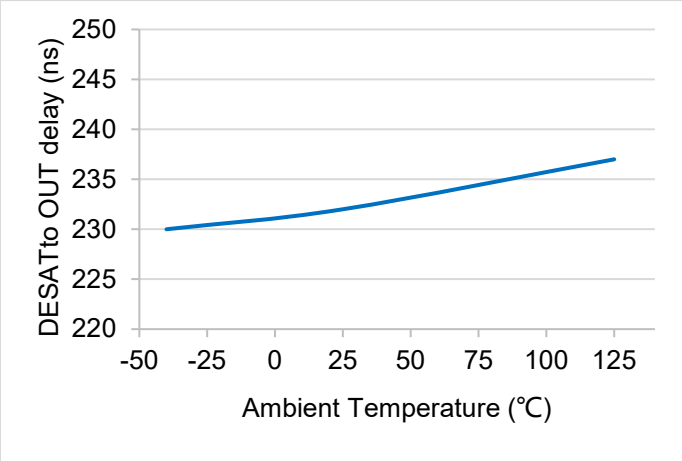



Figure 8.20 DESAT to OUT delay vs temperature

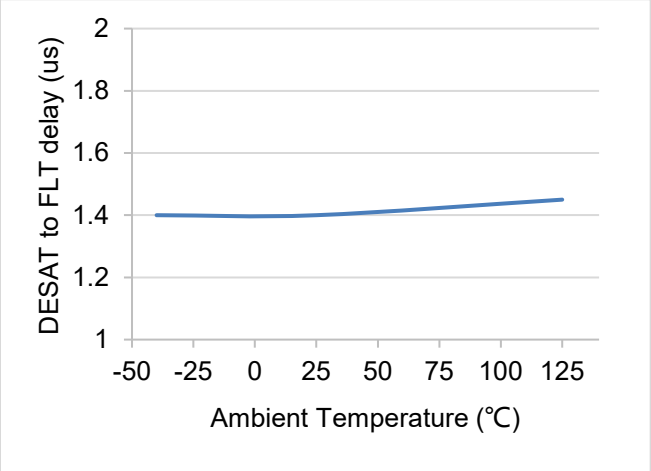



Figure 8.21 DESAT to FLT delay vs temperature

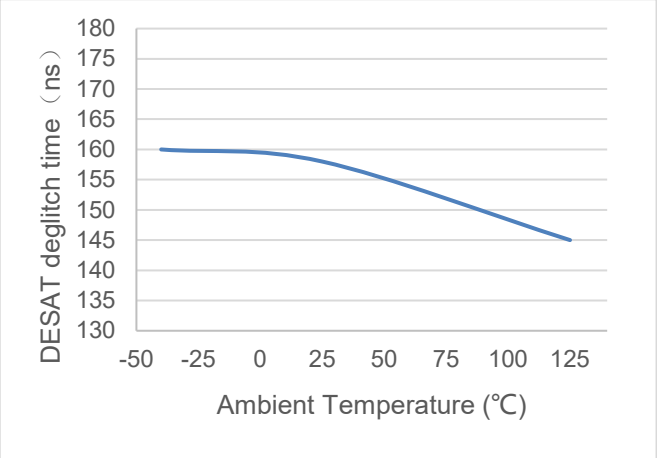



Figure 8.22 DESAT deglitch time vs temperature

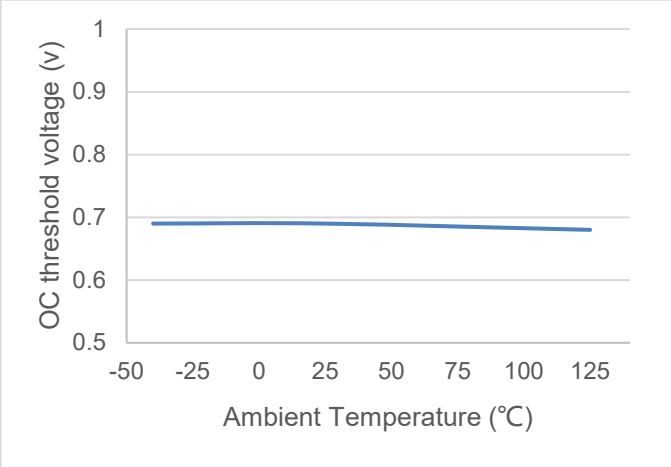



Figure 8.23 OC threshold voltage vs temperature

# 9. Function Description

## 9.1. Overview

The NSI67x0 is a highly reliable power transistor gate driver. It can source and sink 10A peak current, which is suitable for driving MOSFET, IGBT, or SiC MOSFET. The NSI67x0 is available in SOW16 package, which can support 5700$V_{RMS}$ isolation per UL1577. System robustness is supported by 150kV/us minimum common-mode transient immunity (CMTI).

Besides, the NSI67x0 includes crucial protection features such as miller clamp, DESAT short circuit detection and soft turn off. UVLO and short circuit fault are reported through separate pins.

The isolation barrier inside NSI67x0 is based on the capacitive isolation. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI. The digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side.

The functional block diagram of NSI67x0 is shown below. Two input pins with non-inverting and inverting logic support interlock and shoot through protection. Low resistance of high side and low side MOSFET in the output stage ensures high driving capability. Split outputs can control the rise and fall time individually. Active pull-down and short circuit clamping features are implemented to protect power transistor.

In summary, the NSI67x0 is suitable to replace source and sink reinforced gate driver in high reliability, power density and efficiency switching power system.

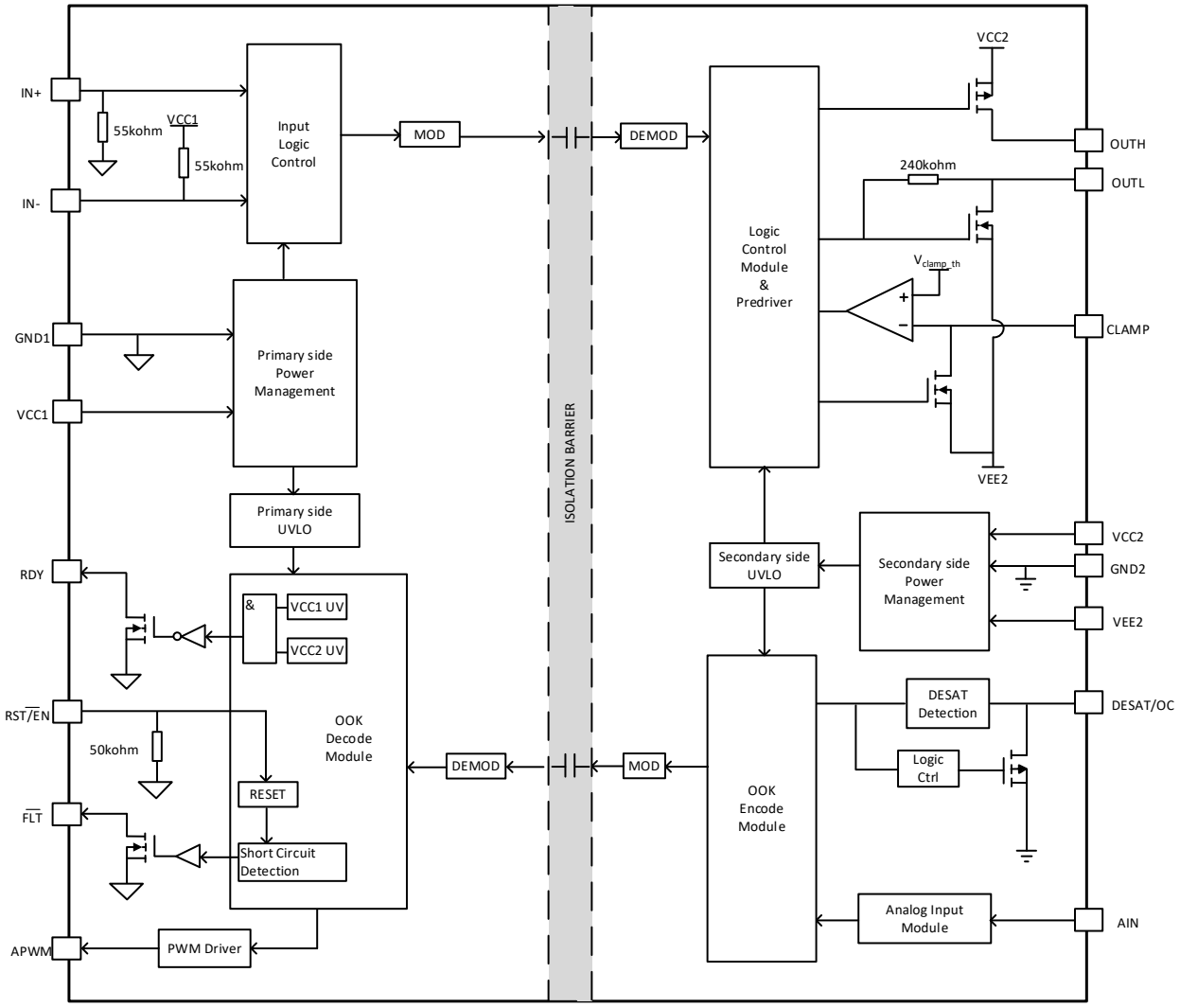



Figure 9.1 Function Blocks

## 9.2. Power Supply

Power supply $V_{CC1}$ is able to support from 3.3V to 5.5V. Power supply $V_{CC2}$ is able to support from 13V to 32V. To be mentioned, NSI67x0 also supports bipolar power supply mode on the driver side. In the case of fast switching speed, the negative power supply is crucial to prevent false turn on from parasitic Miller capacitor.

## 9.3. Output Stage

NSI67x0 supports the split output, which means the rising time and falling time can be adjusted independently. The output voltage is switched between VCC2 and VEE2. It can be controlled by IN+, IN- and $\overline{RST}$/EN. The NSI67x0 has a P-channel MOSFET pulled up the OUTH pin when turning on external power transistor. The measurement result $R_{OH}$ represents the on-resistance of P-channel MOSFET. The voltage and current of external power transistor drain to source or collector to emitter change during turn on. The pull-down structure of NSI67x0 is simply composed of an N-channel MOSFET with on-resistance of $R_{OL}$. The result is quite small, indicating the strong driving capability of NSI67x0.

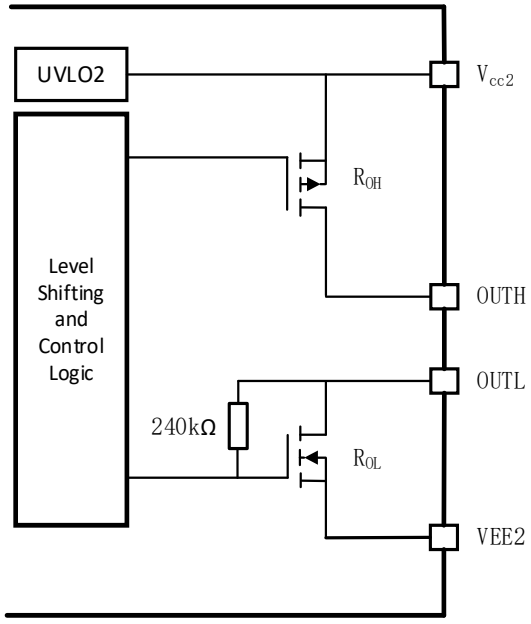



Figure 9.2 NSI67x0 output stage

## 9.4. Active Pull-Down

The Active Pull-Down feature ensures a safe IGBT or MOSFET off-state if $V_{CC2}$ is not connected to the power supply. When $V_{CC2}$ is floating, the driver output is still able to be held low.

## 9.5. Internal Active Miller Clamp

Active miller clamp is used to prevent false turn on. After the external power transistor is turned off, the other one of the phase leg is turned on. The voltage of the drain-source or collector-emitter rises instantly. The dv/dt will cause a high current on miller parasitic capacitor. The voltage drops on the gate resistor possibly turn on the external power transistor unintentionally, which will cause a catastrophic damage. To deal with that, NSI67x0 is equipped with a miller clamp pin. The clamp pin detects the gate voltage of IGBT or MOSFET. When the gate voltage is decreasing and reaches the $V_{CLAMP\_TH}$, the clamp pin will be pulled down by the internal MOSFET, providing a low impedance path to avoid the false turn on.

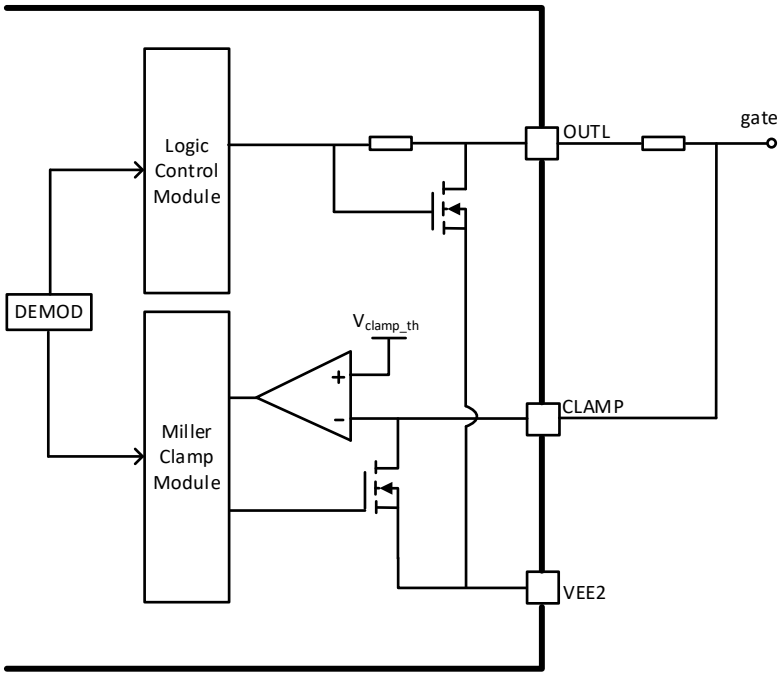



Figure 9.3 Active Miller Clamp

## 9.6. Short Circuit Clamping

During a short circuit the gate voltage of IGBT or MOSFET tends to rise because of the feedback via the miller capacitance. The diode between OUTH/OUTL/CLAMP and $V_{CC2}$ pins inside the driver limits this voltage when the output voltage is higher than the supply voltage. A maximum current of 500mA may be fed back to the supply through this path for 10μs. If higher currents are expected or tighter clamping is desired ,external Schottky diodes may be added.

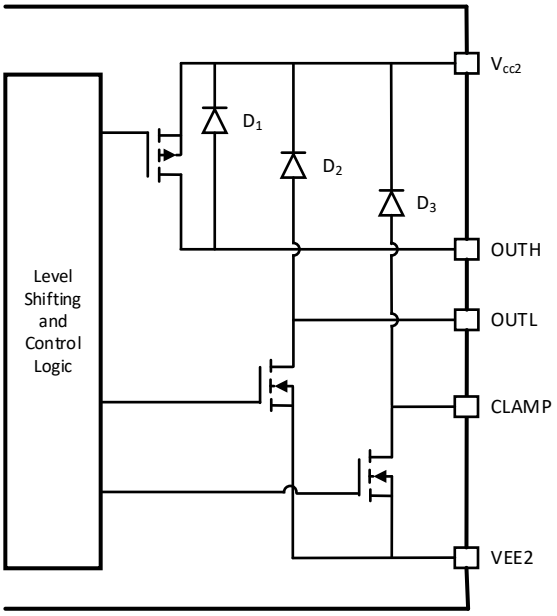



Figure 9.4 Short circuit Clamping

## 9.7. VCC1 and VCC2 Undervoltage Lock Out (UVLO)

To ensure correct switching, NSI67x0 is equipped with an under-voltage lockout for input and output power supply independently. $V_{CC1}$ voltage should not fall below the UVLO threshold for normal operation, or the gate-driver output can become clamped low. Output supply UVLO is referred to GND2 pin. If $V_{CC2}$-GND2 falls below the UVLO threshold, OUTL of the gate-driver will be clamped low.

Local bypass capacitors should be placed between the $V_{CC2}$ and GND2 pins, as well as the $V_{CC1}$ and GND1 pins. A Capacitor of 220nF to 10μF is recommended for device biasing. Additional 100nF capacitor in parallel with the device biasing capacitor is recommended for high frequency filtering. The capacitors should be positioned as close to the device as possible for better noise filtering. Low-ESR, ceramic surface-mount capacitors are recommended. The RDY pin will report a power good signal if the device is out of UVLO condition.

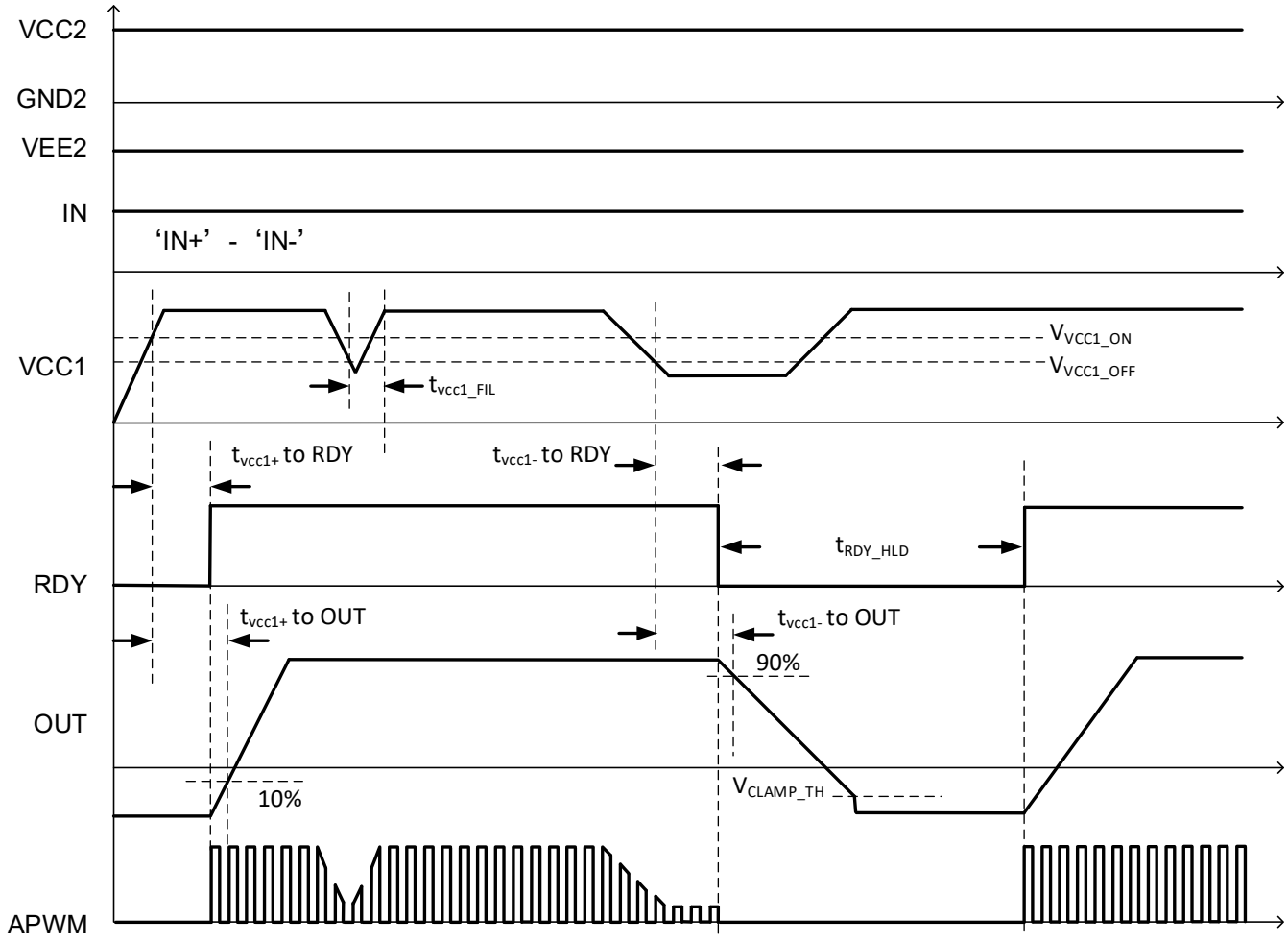



Figure 9.5 RDY vs $V_{CC1}$ timing Diagram

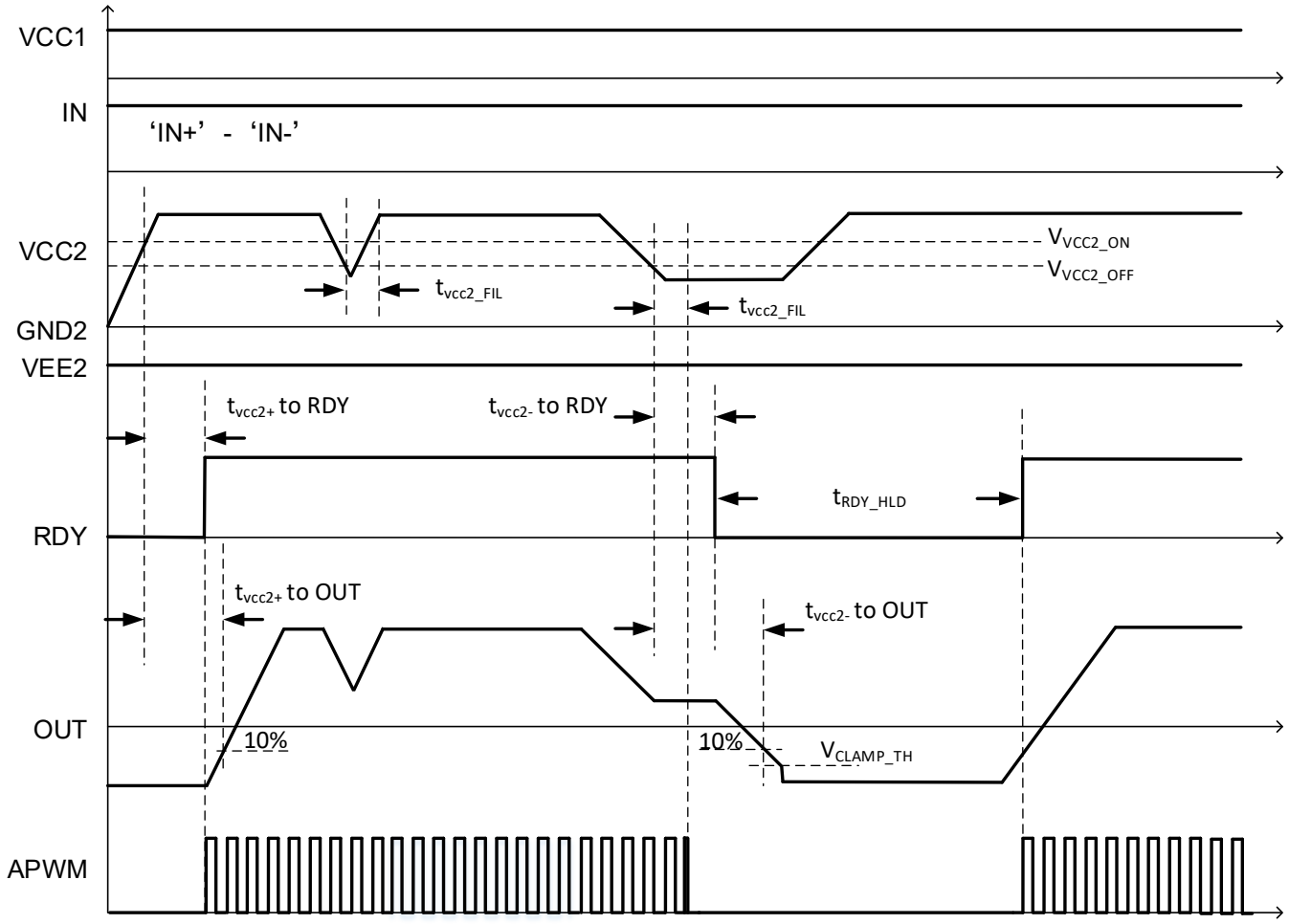



Figure 9.6 RDY vs $V_{CC2}$ timing Diagram

## 9.8. Desaturation (DESAT) Protection

Desaturation protection is used to prevent the power transistor from a short circuit. The DESAT pin has a typical threshold voltage, which means the output will be driven low if DESAT pin reaches threshold voltage. By default, the DESAT pin is pulled down by an internal MOSFET. The internal current source is designed to work only when the output is high level. There is a leading-edge blanking time to filter the overshoot when the external power transistor is turned on. The current source begins to charge after the internal leading-edge blanking time.

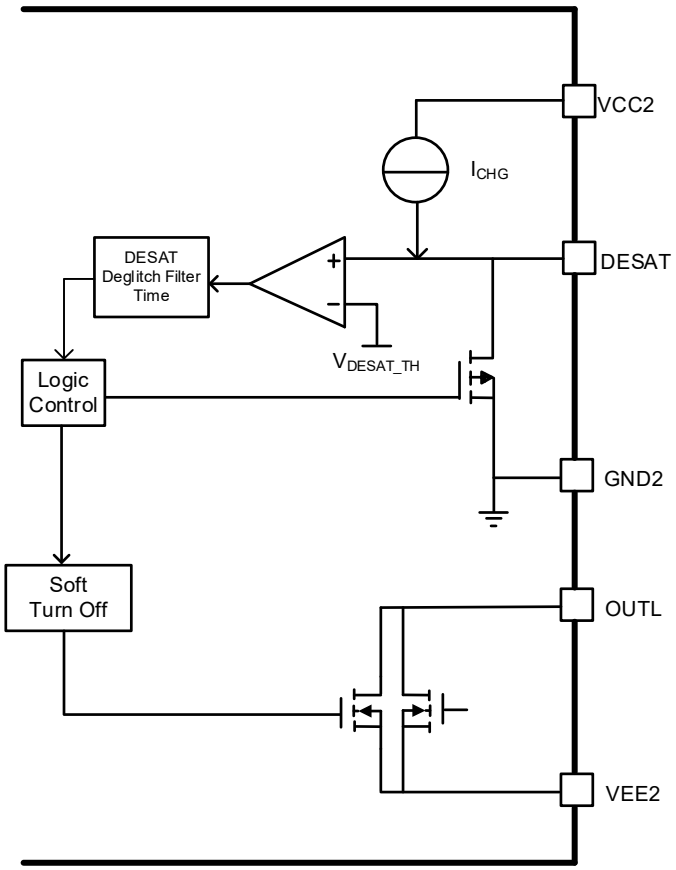



Figure 9.7 DESAT Protection

## 9.9. Overcurrent (OC) Protection

The Overcurrent protection is used to implement a fast overcurrent and short circuit protection feature to protect the SiC MOSFET or IGBT from catastrophic breakdown during fault. The OC threshold voltage is respected to GND2. When the input is in floating condition, or the output is held in low state, the OC pin is pulled down by an internal MOSFET and held in LOW state, which prevents the overcurrent and short circuit fault from false triggering. The OC pin is in high-impedance state when the output is in high state, which means the overcurrent and short circuit protection feature only works when the power semiconductor is in on state. The internal pulldown MOSFET helps to discharge the voltage of OC pin when the power semiconductor is turned off.

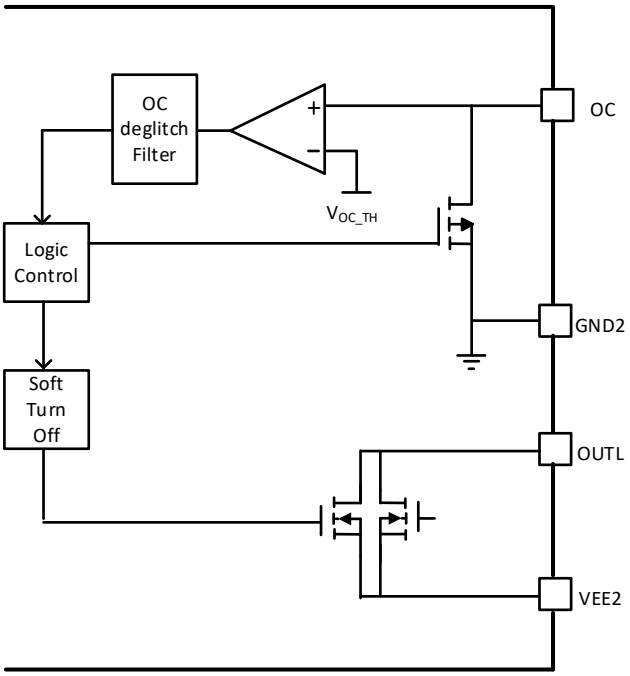



Figure 9.8 OC Protection

## 9.10. Soft Turn-Off

The soft turn-off is designed to prevent the overshoot breakdown when DESAT protection is triggered. When the short circuit fault occurs, the external power transistor transits from the active region to ohmic region very quickly. The high di/dt may result in the overshoot voltage on the parasitic inductance of the emitter. Therefore, the device should be turned off in a soft manner. But the turn off speed should not be too slow. There is a balance between the overshoot and large energy dissipation. Soft turn off current is a compromising choice.

## 9.11. Fault ($\overline{\text{FLT}}$ and $\overline{\text{RST}}$/EN)

The $\overline{\text{FLT}}$ pin of NSI67x0 is used to report a warning signal if the fault is detected on DESAT. If the fault occurs, the $\overline{\text{FLT}}$ pin will be pulled down and held in low state for a mute time. During the mute time, NSI67x0 ignores any reset signal. After that, the $\overline{\text{FLT}}$ pin will be reset to high impedance status if the reset signal is checked. The $\overline{\text{RST}}$/EN pin is pulled down to GND1 by an internal resistor, which means the device is disabled by default. Therefore, the $\overline{\text{RST}}$/EN pin must be pulled up externally to enable the device. Timing diagram of fault report is shown below.

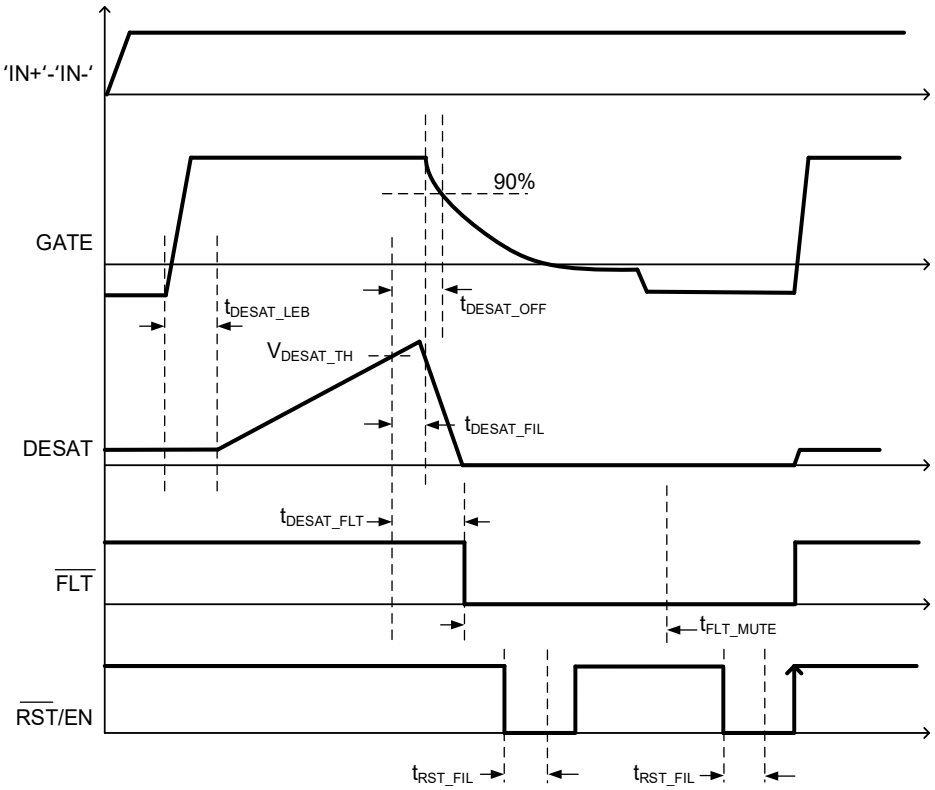



Figure 9.9 DESAT protection Timing Diagram

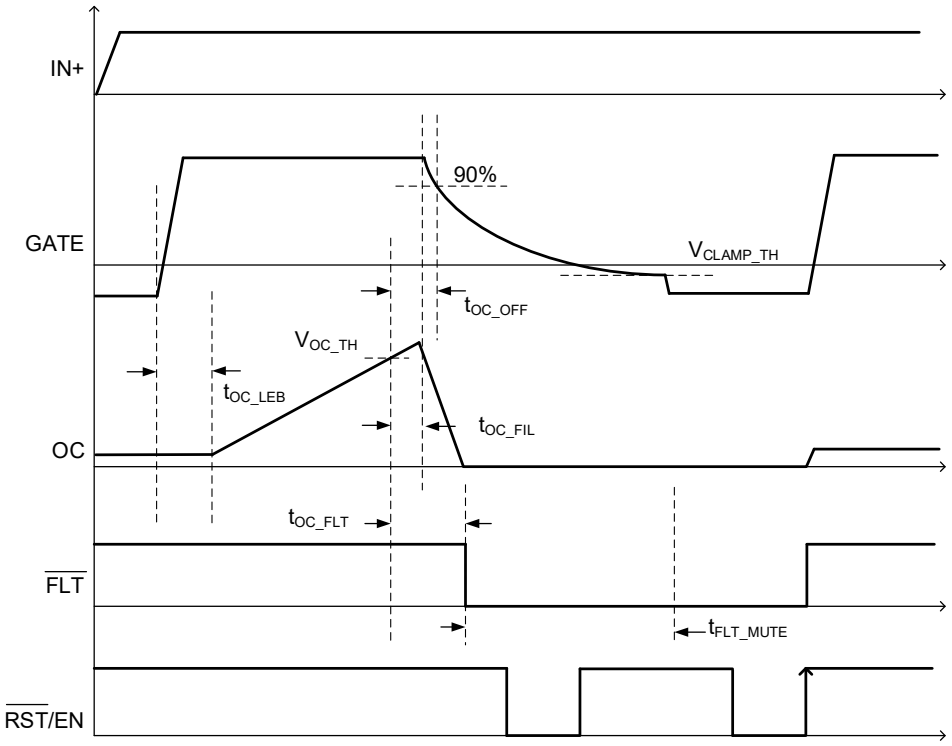



Figure 9.10 OC protection Timing Diagram

## 9.12. Isolated Analog Signal Sensing Function

NSI67x0 provides an AIN pin on the output side and an APWM pin on the input side. NSI67x0 can transfer the AIN voltage to the corresponding duty cycle of the APWM pin. NSI6730 integrated current source in AIN pin is used to bias the external thermal diode or thermal sensing resistor while NSI6770 does not have the current source. Therefore, AIN pin can be used to detect the HVDC bus voltage or IPM temperature. The duty cycle of output PWM signal can be directly calculated by MCU. Otherwise, the output signal can be transferred to an analog signal by a RC filter.

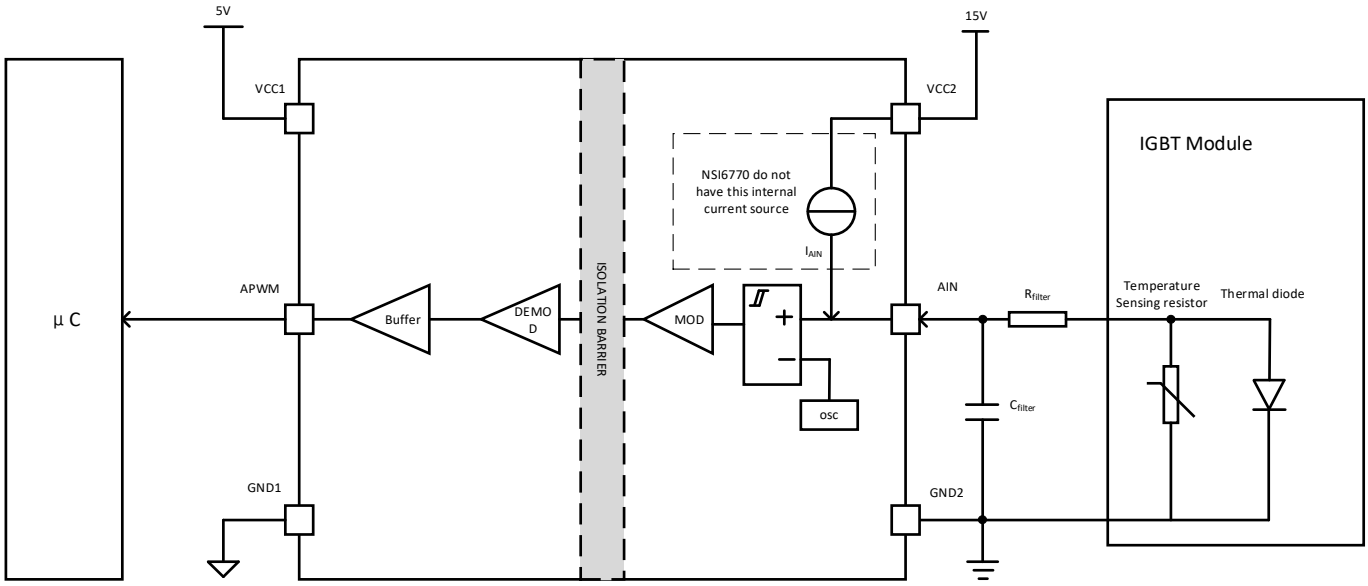



Figure 9.11 Isolated Analog signal sensing

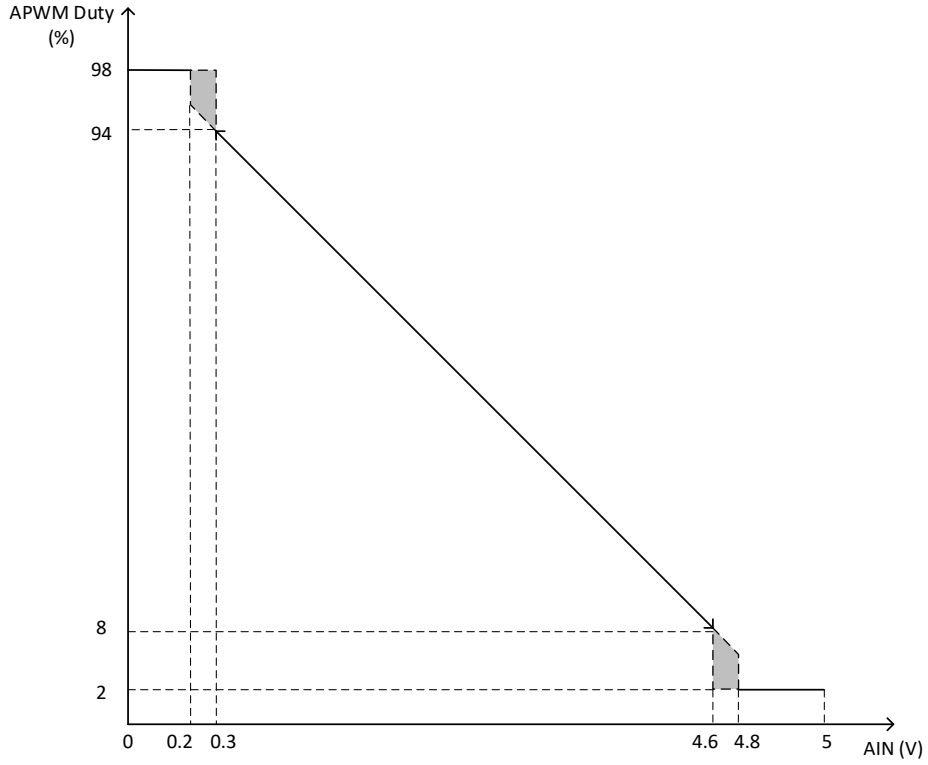



Figure 9.12 APWM duty vs analog input voltage

Note：In the gray region, the duty cycle of the APWM output is uncertain.

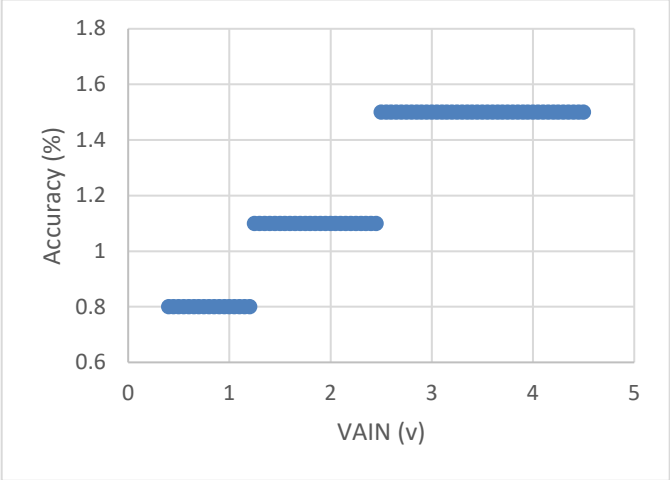



Figure 9.13 Duty accuracy of APWM

## 9.13. Device Functional Modes

Table lists the common functional modes of the device.

| Input | | | | | | Output | | | |
|---|---|---|---|---|---|---|---|---|---|
| $V_{CC1}$ | $V_{CC2}$ | IN+ | IN- | EN/RST | DESAT or OC | RDY | FLT | OUTH/OUTL | CLAMP |
| PU | PD/OPEN | X | X | X | X | LOW | HIZ | LOW | LOW |
| PD | PU | X | X | X | X | LOW | HIZ | LOW | LOW |
| OPEN | X | X | X | X | X | HIZ | HIZ | LOW | LOW |
| PU | PU | X | X | LOW | X | HIZ | HIZ | LOW | LOW |
| PU | PU | LOW | X | HIGH | X | HIZ | HIZ | LOW | LOW |
| PU | PU | HIGH | LOW | HIGH | HIGH | HIZ | LOW | LOW | LOW |
| PU | PU | HIGH | LOW | HIGH | LOW | HIZ | HIZ | HIGH | HIZ |
| PU | PU | HIGH | HIGH | HIGH | X | HIZ | HIZ | LOW | LOW |

Open: VCC <POR; PU: VCC>VCC UVLO; PD: POR < VCC <VCC UVLO; X: Irrelevant; HIZ: High impedance

POR is around 1.8V.

# 10. Application Note

## 10.1. Typical Application Circuit

Bypassing capacitors for $V_{CC1}$ and $V_{CC2}$ supplies are needed to achieve reliable performance. To filter noise, 0.1μF/50V ceramic capacitor is recommended to be placed as close as possible to NSI67x0, both at $V_{CC1}$ and $V_{CC2}$ side. For $V_{CC2}$ supply, additional 10μF/50V ceramic capacitor is recommended, to support high peak currents when turning on external power transistor. If the $V_{CC1}$ or $V_{CC2}$ power supply is located long distance from the IC, bigger capacitance is essential.

The input filter composed by $R_{in}$ and $C_{in}$ can be used if input PWM has ring due to long traces or bad PCB layout. However, it will introduce longer propagation delay.

A 4.7kΩ resistor can be used as pull-up resistor for $\overline{FLT}$,RDY and $\overline{RST}/EN$ pins.

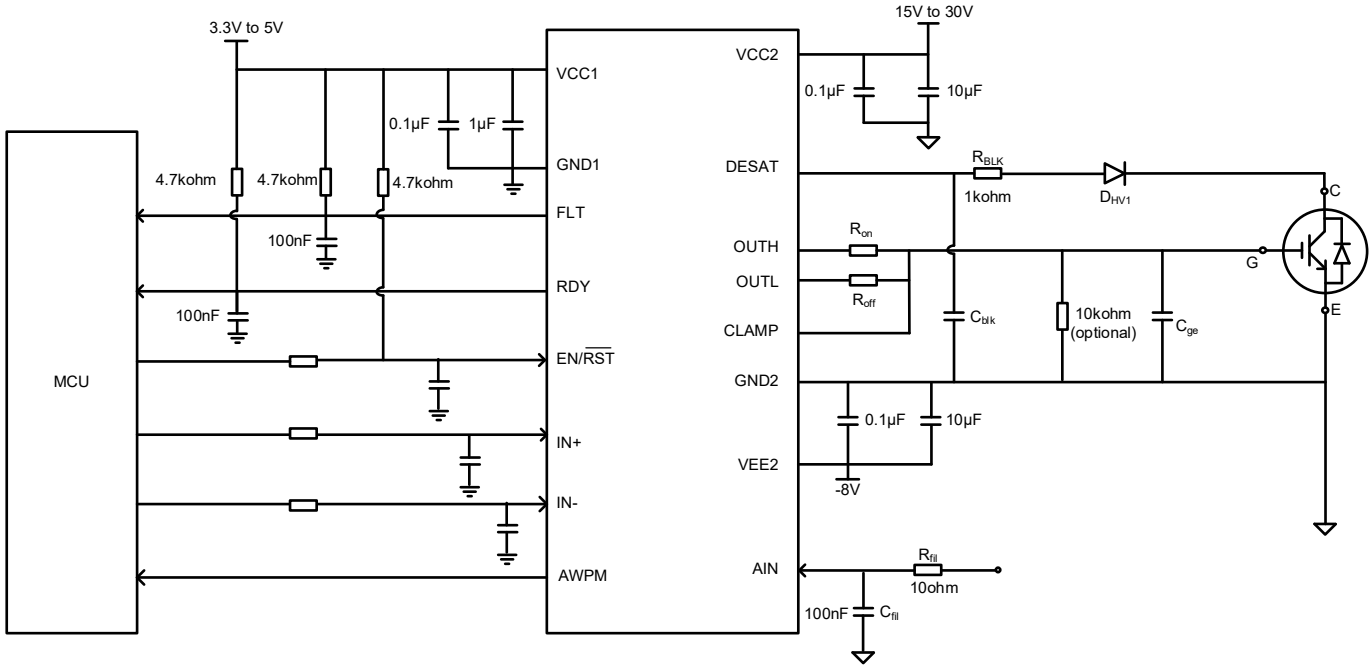



Figure10.1 Typical Application

## 10.2. Design for IN+, IN- and $\overline{RST}$/EN

In the application with NSI67x0, the noise from parasitic inductance and coupled capacitance cannot be ignored any more. To filter the noise, NSI67x0 is designed with a 40ns deglitch filter. Besides, the external low pass filter can also be placed near the input pins. Low pass filter will increase the noise immunity and delay time, so it should be based on the requirements.

## 10.3. Design for EN/$\overline{RST}$ ,RDY and $\overline{FLT}$

EN/$\overline{RST}$pin is used to enable the device and reset the fault signal. It is pulled down by default. $\overline{FLT}$and RDY pin are open-drain output, which means they cannot work without externally pull-up resistor. In this application, a 4.7kΩ pull-up resistor is recommended for RDY, $\overline{FLT}$and EN/$\overline{RST}$ pin. A 100nF capacitor can be placed near the device if it is necessary.

## 10.4. Design for Automatic Reset Control

$\overline{RST}$/EN pin has two functions. It is used to enable the device and reset the fault signal after DESAT is detected. The $\overline{RST}$/EN pin is pulled down to GND by an internal resistor, so the $\overline{RST}$/EN pin must be pulled up externally to enable the device.

After DESAT is detected, the FLT pin will be pulled down until the rising edge of the $\overline{RST}$/EN pin is coming. To be mentioned, there is a FLT mute time, which means the reset signal must be held for at least $t_{FLT\_MUTE}$.

NSI67x0 can be designed for automatic reset mode. $\overline{RST}$/EN pin can be connected to IN+ directly when the PWM is applied to the IN+. Besides, $\overline{RST}$/EN pin can be connected with IN- through a NOT logic if the PWM is applied to the IN-. Whichever mode is used, the PWM off time should be longer than the $t_{FLT\_MUTE}$.

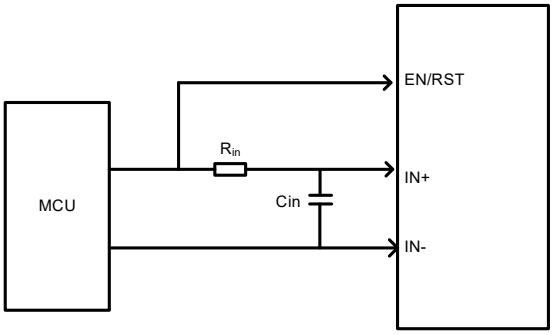



Figure10.2 Auto-reset control

## 10.5. PWM Interlock Protection

For applications to drive power transistors in half bridge configuration, two NSI67x0 can be used. NSI67x0 supports interlock protection. If the controller has some mistakes, leading to negative dead time, the output PWM of NSI67x0 is adjusted to avoid power transistor shoot through.

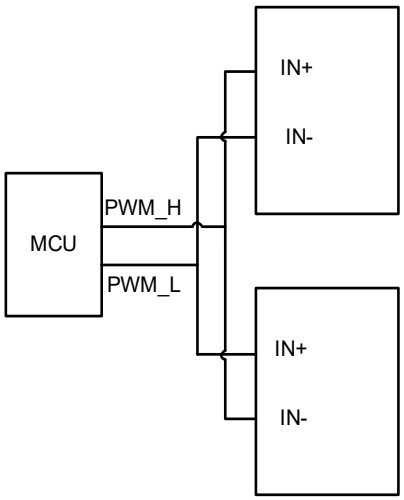



Figure10.3 Interlock Protection

## 10.6. Design for $R_{on}$ and $R_{off}$

NSI67x0 features split output, so the turn on and turn off switching speed can be independently controlled. The turn on and turn off resistance determine the peak source and sink current, which can be estimated by the formula:

$$I_{SOURCE} = \min(\frac{VCC2 - VEE2}{R_{ON} + R_{OH} + R_{Gint}}, 10A)$$

$$I_{SINK} = \min(\frac{VCC2 - VEE2}{R_{OFF} + R_{OL} + R_{Gint}}, 10A)$$

Where

$R_{Gint}$ is the internal resistance of the SiC or IGBT.

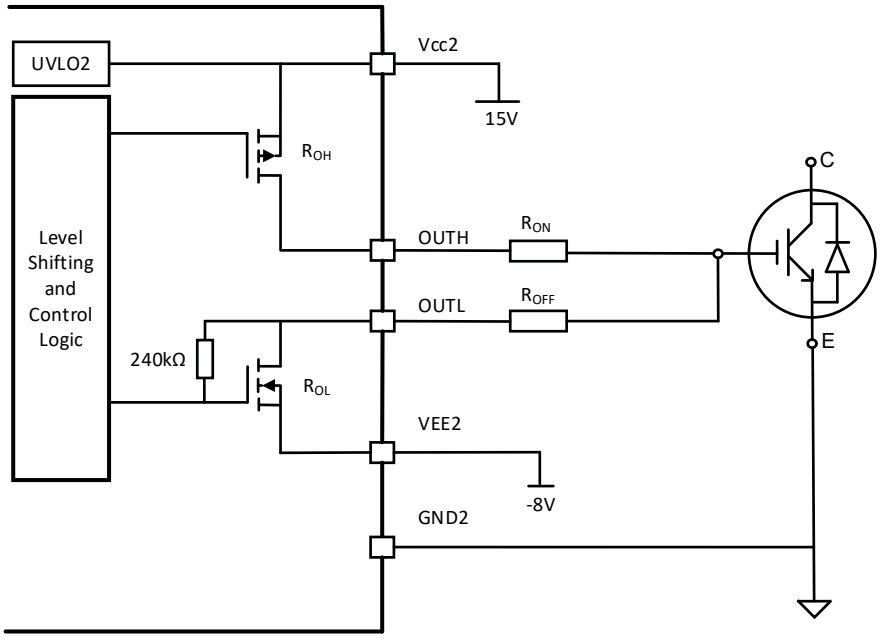



Figure10.4 Gate resistor design

## 10.7. Design for DESAT Protection

DESAT is used to protect the power semiconductor from overcurrent. When the voltage of DESAT is over the $V_{DESAT\_TH}$, the block of soft turn off will be activated and the fault pin will be pulled down. For typical application, the crucial components required to build the DESAT circuit are the DESAT diode, DESAT resistor and the blank capacitor.

The DESAT diode function is to conduct forward current. In order to avoid the false detection caused by the reverse recovery spikes, a very fast reverse recovery time diode with small reverse parasitic capacitance is recommended. The DESAT detection threshold voltage of 9V can be reduced by the DESAT diode, which can be calculated as:

$$V_{DESAT} = V_{DESAT\_TH} - n \times V_F$$

The anti-parallel diode of IGBT has a large transient forward voltage of the diode, which may result in a large negative voltage spike on the DESAT pin, then it may draw a large current from driver. DESAT resistor is used to limit the current. From 100Ω to 1kohm resistor is recommended to be added in series with the DESAT diode.

The DESAT fault detection should remain a short blanking time so that the collector voltage can fall below the $V_{DESAT\_TH}$. This blanking time can make sure that there is no nuisance tripping during the IGBT turn-on. It is based on the blank capacitor, which can be estimated as:

$$t_{BLK} = \frac{C_{BLK} \times V_{DESAT\_TH}}{I_{CHG}}$$

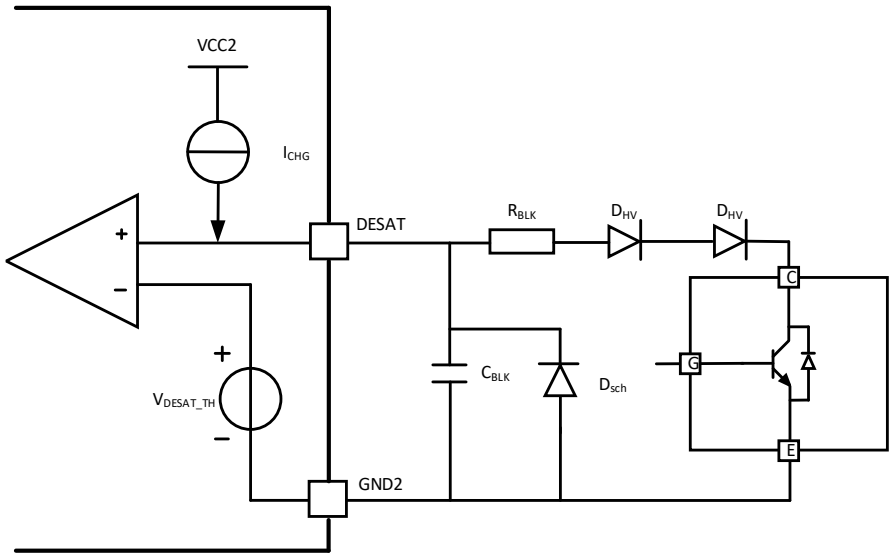



Figure10.5 DESAT protection

## 10.8. Design for OC Protection

A suitable overcurrent and short circuit protection is important to prevent the SiC MOSFET and IGBT modules from catastrophic break down. Because the output characteristics of SiC MOSFET and IGBT are different. Compared to the IGBT, SiC MOSFET has a larger linear region. The transition point from linear region to saturation region is far higher than the IGBT's. The drain current keeps increasing with the increasing drain to source voltage, which means it may be destroyed before the transition point. So, the OC protection is more suitable in the SiC application.

The SiC/IGBT module with mirror current source is preferred in OC protection because of the smaller noise and lower power dissipation. The mirror current source is used to scale down the device current. The scaled-down the current can be measured by an external high precision shunt resistor $R_s$ and the device current can be calculated based on the ratio. To further improve the noise immunity, a low pass filter can be added. A 100pF to 10nF filter capacitor and a 10ohm to 100ohm resistor can be added. The typical application circuit is shown below.

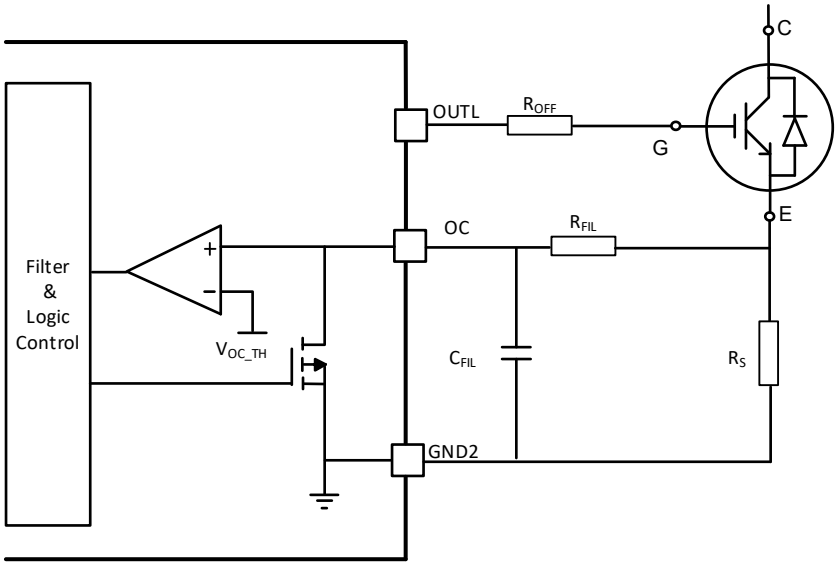



Figure10.6 OC protection

## 10.9. Design for AIN and APWM

The analog input pin is used to detect analog signals on the secondary side like temperature, bus voltage and so on. The voltage detected in the AIN pin can be transformed to the PWM duty at the APWM pin. NSI6730 provides an internal current source, which is used to forward bias the thermal diode or create a voltage drop on a temperature sensing resistor. To be mentioned, the NSI6770 does not have the internal current source therefore requires add external current source to NTC or Thermal diode in the system. The duty cycle of the PWM changes linearly from 8% to 94% when the voltage of AIN pin changes from 4.6v to 0.3v. The relationship between voltage and duty refer to the Equation below.

$$D_{APWM}(\%) = -20 \times V_{AIN} + 100$$

There is a low pass filter recommended in the AIN pin to filter the noise caused by the switching of the external power transistor. The APWM pin can be connected to the MCU directly and the AIN voltage can be calculated by the PWM duty cycle. A typical application is shown below.

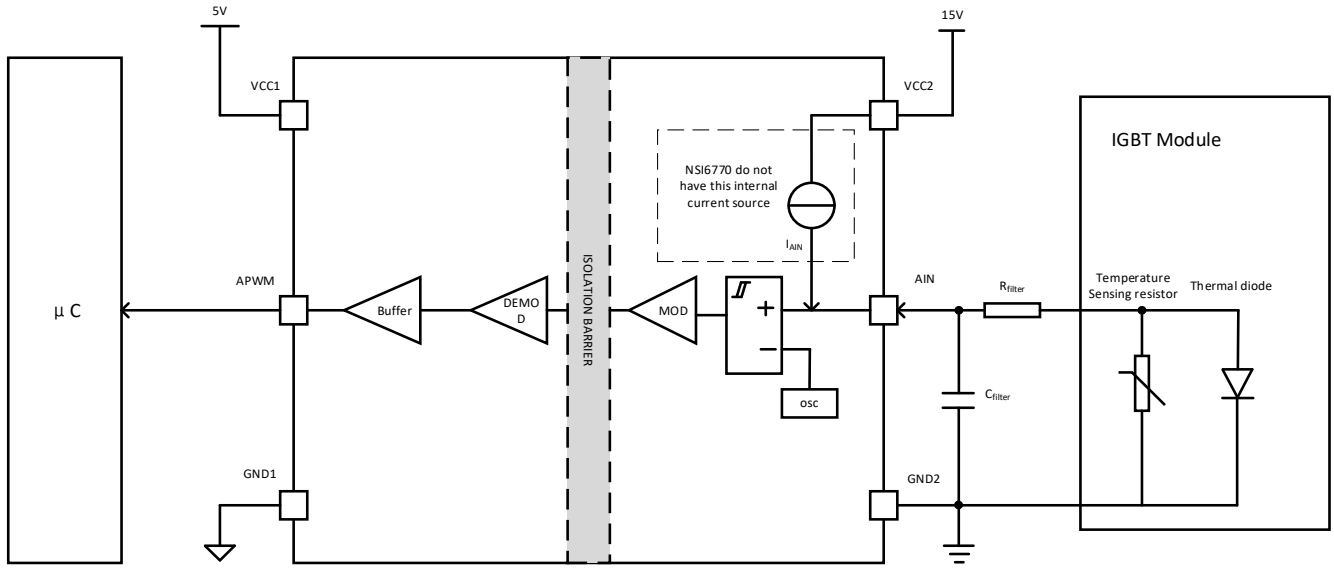


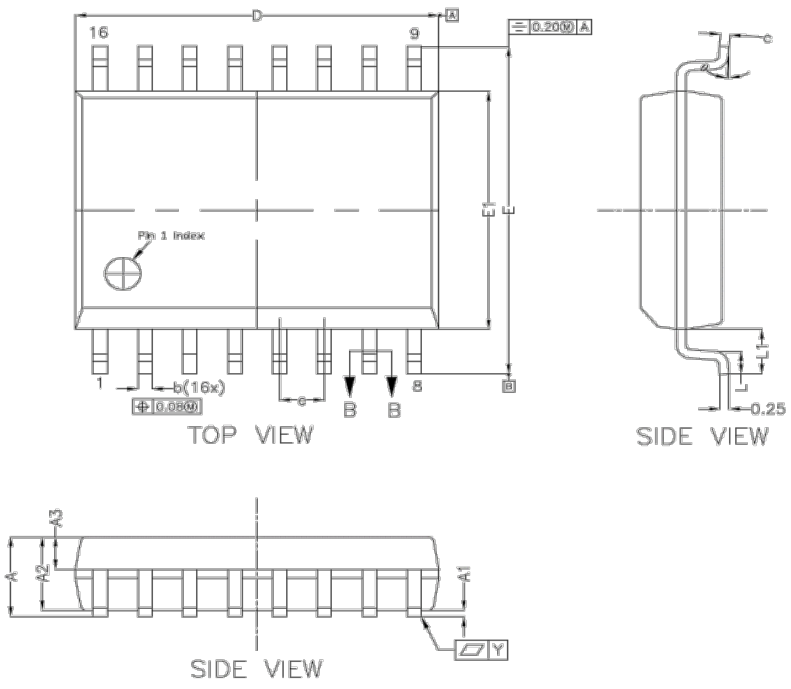

Figure10.7 Design for the IGBT temperature sensing

## 10.10. PCB Layout

Careful PCB layout is essential for optimal performance. Some key guidelines are:

- The bypass capacitors should be placed close to NSI67x0, between $V_{CC1}$ to GND1, $V_{CC2}$ to GND2 and $V_{EE2}$ to GND2.
- The decoupling capacitors of the input power supply should be connected to pin15 and pin9 through a dependent trace. The voltage spike on the parasitic inductance may affect the internal control logic.
- There is high switching current that charges and discharges the gate of external power transistor, leading to EMI and ring issues. The parasitic inductance of this loop should be minimized, by decreasing loop area and placing NSI67x0 close to power transistor.
- Place a large amount of copper connecting to $V_{EE2}$ pin and $V_{CC2}$ pin for thermal dissipation, with priority on $V_{EE2}$ pin. If the system has multi-layers of $V_{EE2}$ or $V_{CC2}$, use multiple vias of adequate size for connection.
- To ensure isolation performance between primary and secondary side, the space under the chip should keep free from planes, traces, pads or via.

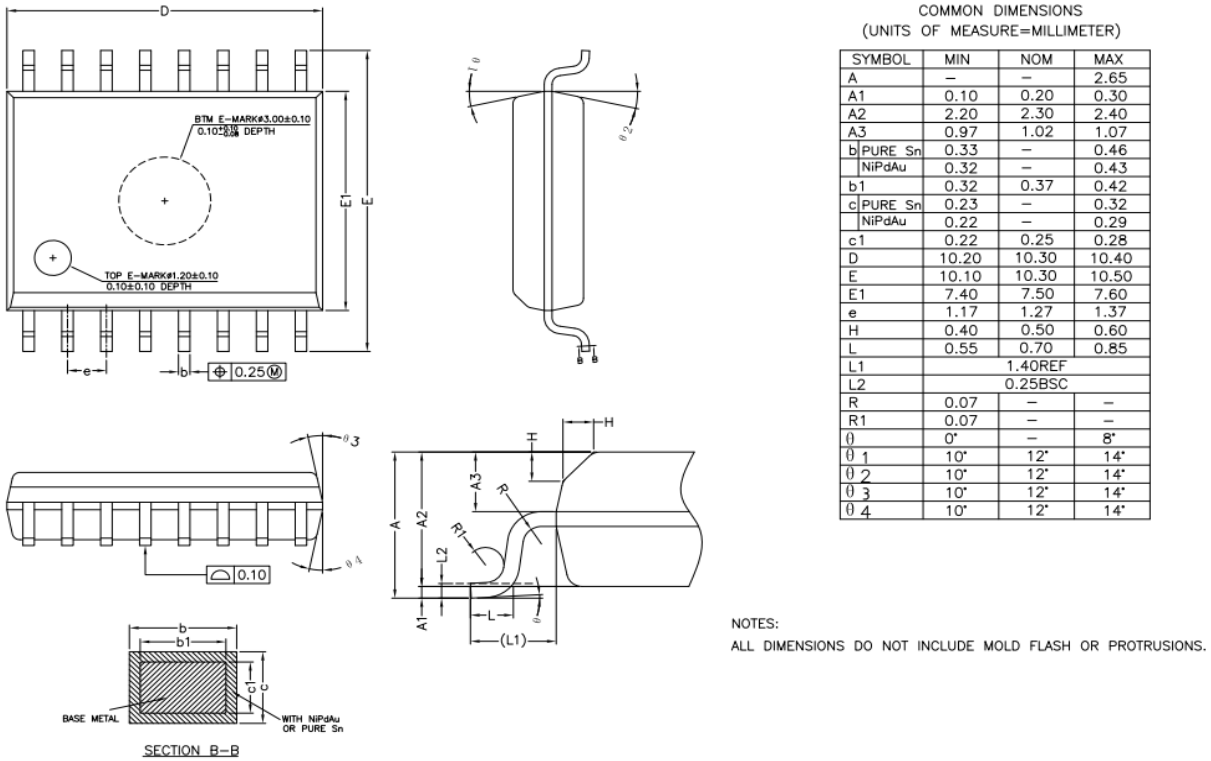
# 11. Package Information




* CONTROLLING DIMENSION : MM

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | --- | --- | 2.65 |
| A1 | 0.10 | --- | 0.30 |
| A2 | 2.25 | 2.30 | 2.35 |
| A3 | 0.97 | 1.02 | 1.07 |
| b | 0.35 | --- | 0.43 |
| c | 0.23 | --- | 0.32 |
| D | 10.20 | 10.30 | 10.40 |
| E | 10.10 | 10.30 | 10.50 |
| E1 | 7.40 | 7.50 | 7.60 |
| e | 1.27 bsc | | |
| L1 | 1.40 bsc | | |
| L | 0.55 | --- | 0.85 |
| Y | --- | 0.10 | --- |
| θ | 0° | --- | 8° |

Figure 11.1 SOW16 Package Shape and Dimension (ATX)




COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

| SYMBOL | | MIN | NOM | MAX |
|---|---|---|---|---|
| A | | – | – | 2.65 |
| A1 | | 0.10 | 0.20 | 0.30 |
| A2 | | 2.20 | 2.30 | 2.40 |
| A3 | | 0.97 | 1.02 | 1.07 |
| b | PURE Sn | 0.33 | – | 0.46 |
| | NiPdAu | 0.32 | – | 0.43 |
| b1 | | 0.32 | 0.37 | 0.42 |
| c | PURE Sn | 0.23 | – | 0.32 |
| | NiPdAu | 0.22 | – | 0.29 |
| c1 | | 0.22 | 0.25 | 0.28 |
| D | | 10.20 | 10.30 | 10.40 |
| E | | 10.10 | 10.30 | 10.50 |
| E1 | | 7.40 | 7.50 | 7.60 |
| e | | 1.17 | 1.27 | 1.37 |
| H | | 0.40 | 0.50 | 0.60 |
| L | | 0.55 | 0.70 | 0.85 |
| L1 | | 1.40REF | | |
| L2 | | 0.25BSC | | |
| R | | 0.07 | – | – |
| R1 | | 0.07 | – | – |
| θ | | 0° | – | 8° |
| θ 1 | | 10° | 12° | 14° |
| θ 2 | | 10° | 12° | 14° |
| θ 3 | | 10° | 12° | 14° |
| θ 4 | | 10° | 12° | 14° |

Figure 11.2 SOW16 Package Shape and Dimension (TongFu)

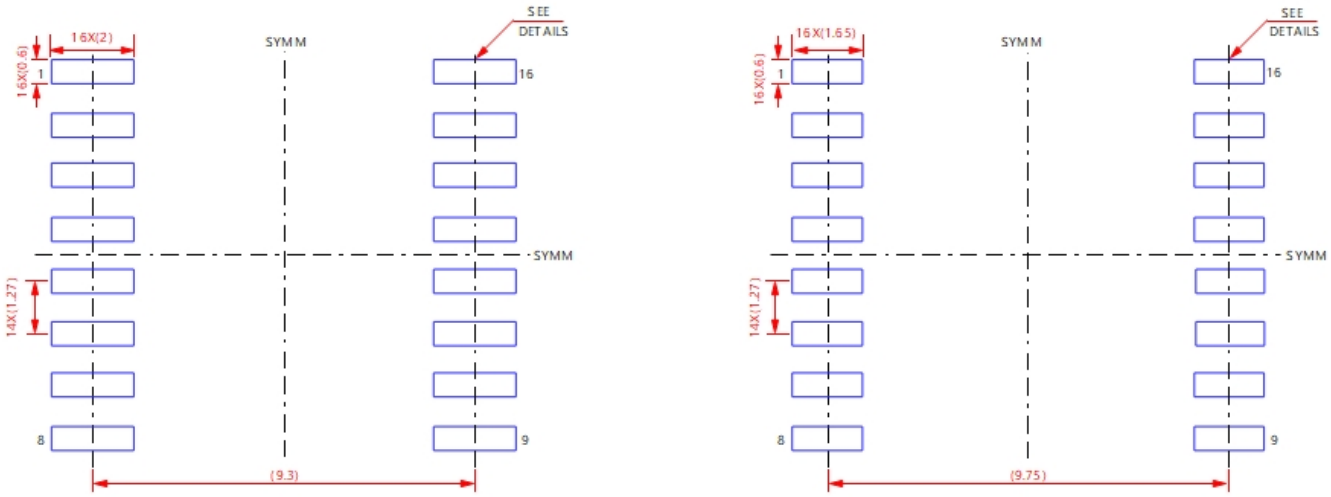



Figure 11.3 Footprint example

## 12. Ordering Information

| *Part Number* | *Protection* | Internal Current Source (AIN) | *STO Current* | *MSL* | *Category* | Ambient Temperature | *MPQ* | *SPQ* | *Package Type* |
|---|---|---|---|---|---|---|---|---|---|
| NSI6770ASC-Q1SWR | DESAT, 9V | NO | 420mA | 3 | Automotive | -40°C to 125°C | 1000 | 1000 | SOW16 |
| NSI6730ASC-Q1SWR | DESAT, 9V | YES | 420mA | 3 | Automotive | -40°C to 125°C | 1000 | 1000 | SOW16 |
| NSI6730ASB-Q1SWR | DESAT, 6.5V | YES | 420mA | 3 | Automotive | -40°C to 125°C | 1000 | 1000 | SOW16 |
| NSI6730ASA-Q1SWR | OC, 0.7V | YES | 420mA | 3 | Automotive | -40°C to 125°C | 1000 | 1000 | SOW16 |
| NSI6770AHC-Q1SWR | DESAT, 9V | NO | 900mA | 3 | Automotive | -40°C to 125°C | 1000 | 1000 | SOW16 |

# 13. Tape and Reel Information

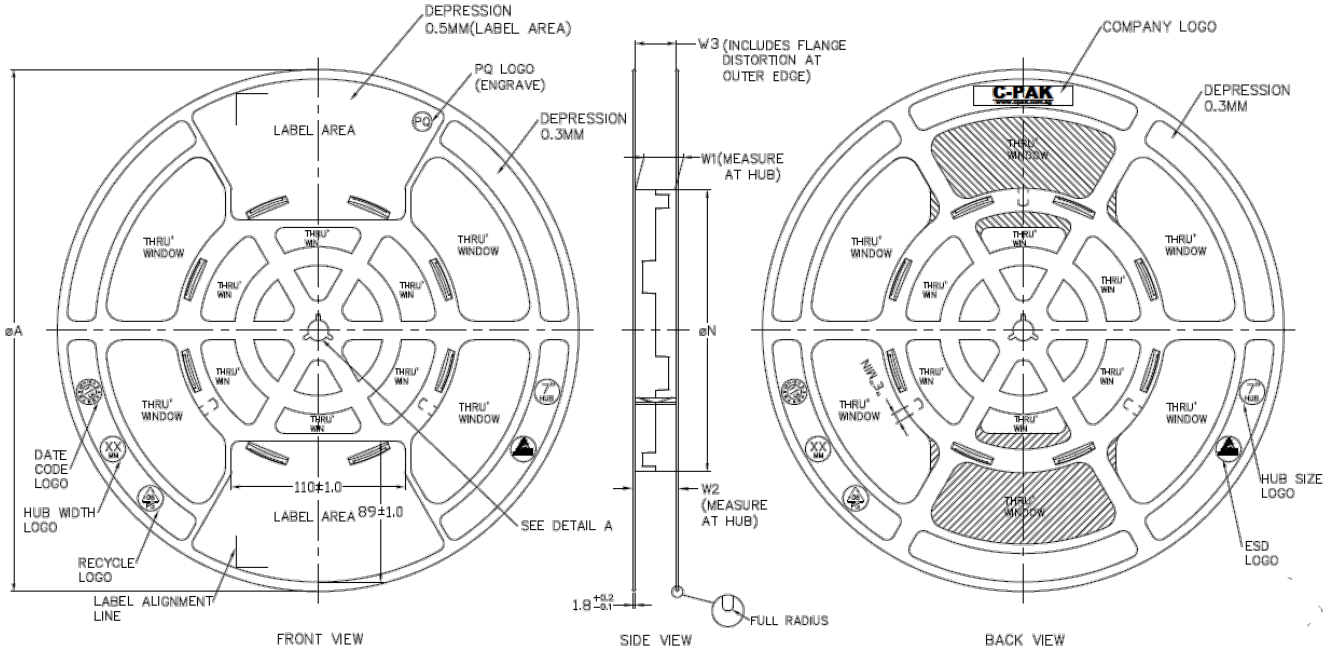
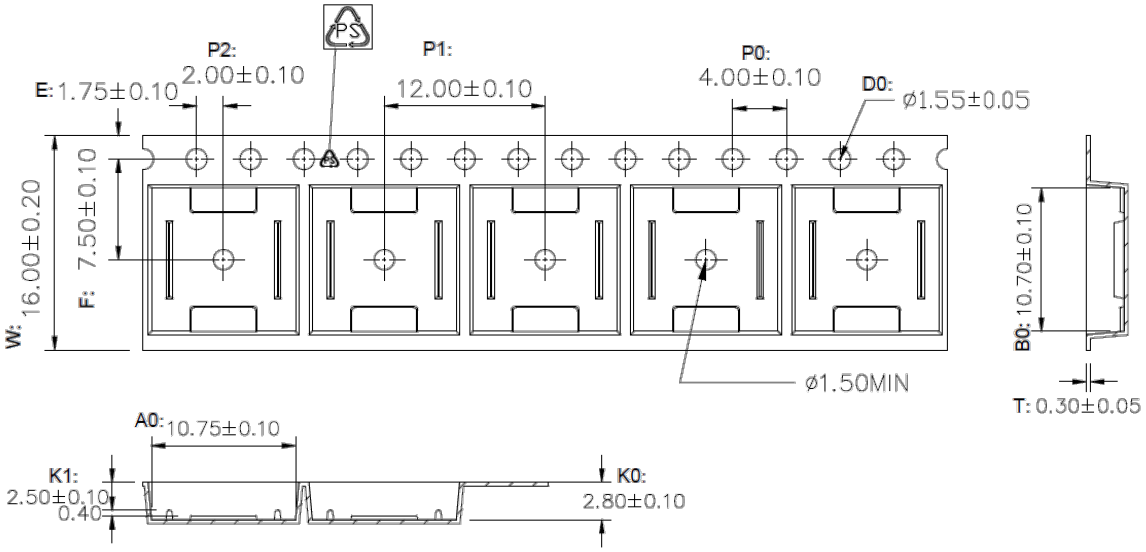
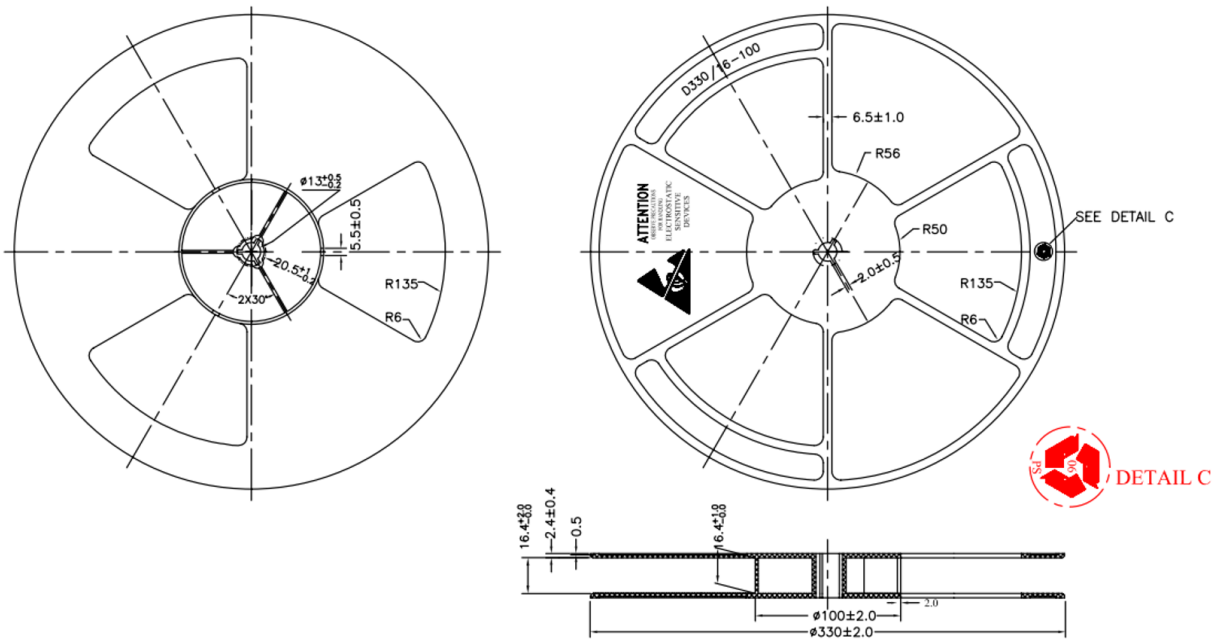



Figure 13.1 Reel Information (ATX)




1. 10 sprocket hole pitch cumulative tolerance ±0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy .
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 378 Meters.(N=122 )
7. Component load per 13" reel : 1000 pcs.

Figure 13.2 SOW16 Tape Information (ATX)




Notes:

Material: Polystyrene (Black);

Flatness: Maximum allowable deviation: 3 mm;

Units: All dimensions are in millimeters (mm);

Surface Resistance: $10^5$ to $10^{11}$ ohms per square (Ω/sq);

Unspecified Tolerances: ±0.25 mm.

Figure 13.3 Reel Information (TongFu)

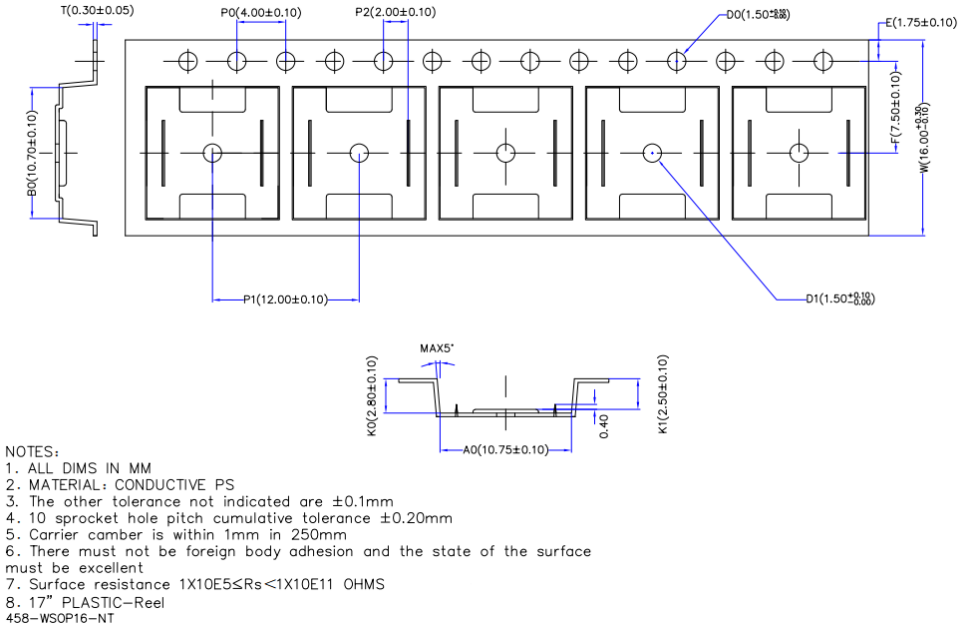



Figure 13.4 SOW16 Tape Information (TongFu)

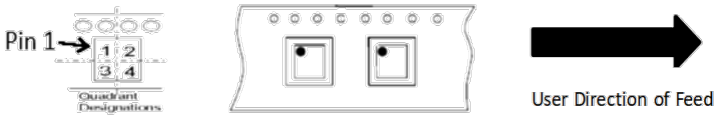



Figure 13.5 Quadrant Designation for Pin1 Orientation in Tape

# 14. Revision History

| Revision | Description | Date |
|---|---|---|
| 1.0 | Initial version | 2025/03/28 |
| 1.1 | 1) Added AIN=1.25V and optimized the precision of APWM<br>2) Updated the certificate of the CQC<br>3) Updated the maximum value of RST deglitch time | 2025/11/26 |
| 1.2 | 1）Updated ordering information, which modified the moisture sensitivity level of the SOW16 package from MSL2 to MSL 3 because a new package supplier with MSL3 is added.<br>2）Updated the CQC certificate | 2026/3/11 |

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