

Product Overview

The NSUC1602 is an ARM MCU with integrated 3 half-bridge Pre-Driver to control BLDC motors. It can use FOC or Six-Step commutation to control BLDC both for sensed and sensor-less mode. And it is widely used in the automotive water pump and cooling fan. This chip conforms to the AEC-Q100 standard, and its junction temperature can support up to 175°C. Also, it is integrated with over-voltage protection function, and the LIN port can support -40V~40V, BVDD pin can support -0.3~40V. The core of the chip is Cortex-M3 based on the ARM instruction set. The core adopts Harvard structure and uses independent data bus and address bus, which can improve the efficiency of getting address and data.

Key Features

- ARM Cortex-M3 32bit core
- 64KBytes Flash, 4KBytes SRAM, 1.5KBytes NVRAM
- 48MHz high precision oscillator
- 35KHz Low power and low speed clock
- Operating voltage 5.5V~28V
- One 12-bit high precision ADC with 2MSPS
- One 8-bit DAC and Comparator for hardware overcurrent protection
- Three rapid reverse voltage comparators (BEMFC)
- One SPI communication support 3 line / 4 line
- Two LINUART peripherals
- LIN PHY module support LIN2.2 communication
- Two 16-bit timers
- One window watchdog
- One digital watchdog
- Three phase Pre-Driver output (GDU)
- Six channels enhanced EPWM output
- One high voltage GPIO with PWMIO

- One 5V output ALDO
- Two temperature sensors
- Four working modes: active, retention, idle and sleep mode
- Sleeping power consumption is less than 75μA with full range of temperature
- AEC - Q100 Grade 0 reliability standard
- ROHS

Applications

- Automotive water pump
- Automotive cooling fan
- Automotive HVAC Blower
- Automotive oil pump
- BLDC motor control
- BDC motor control

Device Information

Part Number	Package	Body Size
NSUC1602-Q0QAERC	QFN40	5mm × 5mm

Functional Block Diagrams

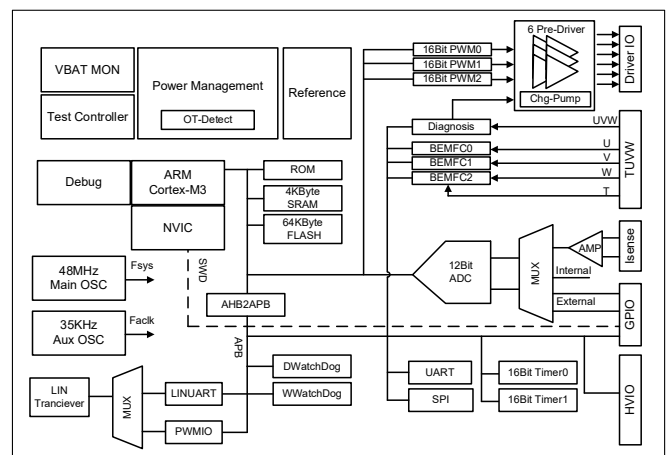


Figure 1. NSUC1602 Block Diagram

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1. Pin Configuration and Functions

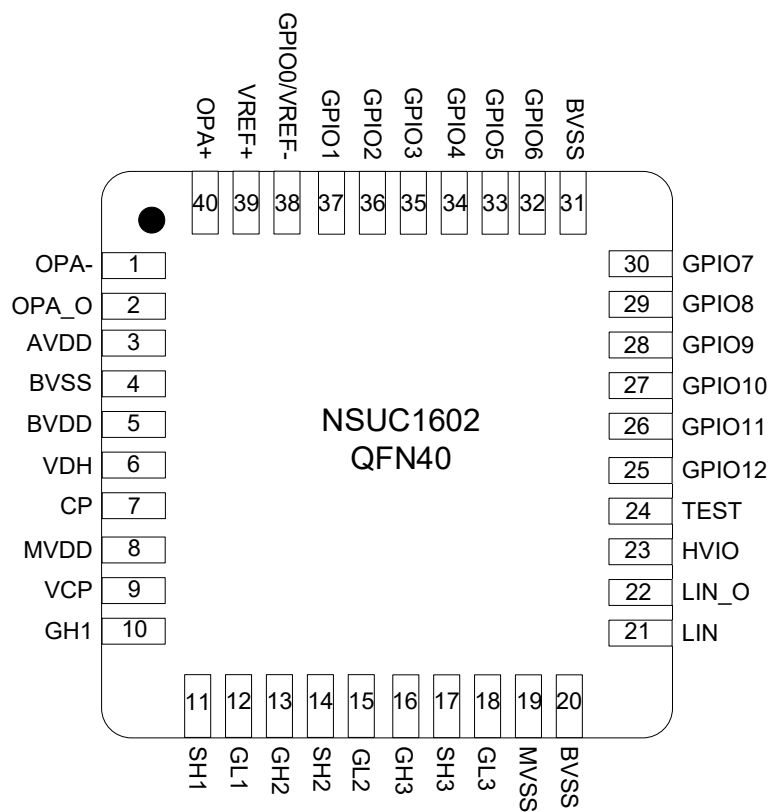


Figure 1.1 NSUC1602 Pin Out

Table 1.1 NSUC1602 Pin Configuration and Description

PIN NO.	SYMBOL	FUNCTION
1	OPA-	OPA Negative Input
2	OPA_O	OPA Output
3	AVDD	5V voltage output
4	BVSS	Battery Ground
5	BVDD	Battery Supply
6	VDH	MVDD with external RC filter Input
7	CP	ChargePump Driver Pin
8	MVDD	Pre-driver Power Supply
9	VCP	ChargePump Voltage Output
10	GH1	Gate driver High side MOSFET Gate output1
11	SH1	Gate driver High side MOSFET Source input1
12	GL1	Gate driver Low side MOSFET Gate output1

PIN NO.	SYMBOL	FUNCTION
13	GH2	Gate driver High side MOSFET Gate output2
14	SH2	Gate driver High side MOSFET Source input2
15	GL2	Gate driver Low side MOSFET Gate output2
16	GH3	Gate driver High side MOSFET Gate output3
17	SH3	Gate driver High side MOSFET Source input3
18	GL3	Gate driver Low side MOSFET Gate output3
19	MVSS	Pre-driver Ground
20	BVSS	Battery Ground
21	LIN	LIN Input
22	LIN_O	LIN Output
23	HVIO	High Voltage I/O
24	TEST	Test Pin
25	GPIO12	Generic I/O 12
26	GPIO11	Generic I/O 11
27	GPIO10	Generic I/O 10
28	GPIO9	Generic I/O 9
29	GPIO8	Generic I/O 8
30	GPIO7	Generic I/O 7
31	BVSS	Battery Ground
32	GPIO6	Generic I/O 6
33	GPIO5	Generic I/O 5
34	GPIO4	Generic I/O 4
35	GPIO3	Generic I/O 3
36	GPIO2	Generic I/O 2
37	GPIO1	Generic I/O 1
38	GPIO0/VREF-	Generic I/O 0/ VREF- Input
39	VREF+	VREF+ Input/ Internal VREF+ Output
40	OPA+	OPA Positive Input
41	EPAD	Exposed pad needs to be connected to GND

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
BVDD voltage	V_{SUP}	-0.3		40	V	
Ground voltage	V_{SS}	-0.3		+0.3	V	
LIN pin voltage	V_{LIN}	-40		40	V	
FET-PreDriver HS Drain	$MVDD$	-0.3		42	V	
FET-PreDriver HS Drain Sense	V_{DH}	-2		42	V	Target -5V, Negative limit for pulsed operation only
FET-PreDriver HS Gate	V_{HG}	-2		42	V	Target -5V, Negative limit for pulsed operation only
FET-PreDriver HS Source	V_{HS}	-2		42	V	Target -5V, Negative limit for pulsed operation only
FET-PreDriver HS Source negative pulse of up to 1us	V_{HS}	-7			V	
FET-PreDriver LS Gate	V_{LG}	-2		42	V	Target -5V, Negative limit for pulsed operation only
FET-PreDriver LS Source	$MVSS$	-2		42	V	Target -5V, Negative limit for pulsed operation only
Voltage range HS Gate vs Source	V_{HG} vs HS	-0.3		14	V	
Voltage range LS Gate vs Source	V_{LG} vs LS	-0.3		14	V	
CP	V_{CP}	-0.3		40	V	
VCP	V_{VCP}	-0.3		55	V	
HVIO	V_{HVIO}	-0.3		40	V	
AVDD	$AVDD$	-0.3		6	V	
GPIO	V_{GPIO}	-0.3		6	V	
OPA+/OPA-/OPA_O	$V_{OPA-PIN}$	-0.3		$AVDD+0.3$	V	
Storage temperature	$T_{STORAGE}$	-40		150	°C	
Operating temperature	$T_{OPERATION}$	-40		150	°C	
Junction temperature	T_J	-40		175	°C	
Latch up current	I_{Latch}		200		mA	$T_J=150^{\circ}C$
			200		mA	$T_J=25^{\circ}C$

3. ESD Ratings

Ratings		Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD		
	● LIN pins	±8.0	kV
	● Other pins	±2.0	kV
	Charged device model (CDM), per AEC-Q100-011-RevB		
	● All pins	±1000	V
	● Corner pins	±1000	V

4. Transient Supply Voltage

Parameters	Symbol	Min	Typ	Max	Unit	Comments
ISO 7637-2:2004 pulse 1	BVDD	-100			V	1),2)
ISO 7637-2:2004 pulse 2a	BVDD			75	V	3),7)
ISO 7637-2:2004 pulse 2b	BVDD			10	V	
ISO 7637-2:2004 pulse 3a	BVDD	-150			V	1),4)
ISO 7637-2:2004 pulse 3b	BVDD			100	V	4),5),7)
ISO 16750-2:2012	BVDD			-	V	6)
ISO 16750-2:2012	BVDD			40 400	V ms	

- 1) With reverse polarity diode.
2) Reverse polarity diode and 1 uF blocking capacitor with low ESR.
3) According to OEM requirement
4) 4.7 kΩ minimum series resistance for I/O ports.
5) The sum of the whole clamping currents must not exceed 100 mA.
6) Values according to OEM specifications.
7) With TVS diode.

5. Specifications

5.1 Recommended Operating Conditions and Characteristics, Note: (TA= -40°C to 150°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Ambient temperature	TA	-40		150	°C	
Junction temperature	TJ	-40		175	°C	
Thermal resistance (junction to housing)	RthJC		9.4		K/W	θJC-top Surface Temperature contours (JEDEC2S2P) 3)
Thermal resistance (junction to the environment)	RthJA		34		K/W	θJA Surface Temperature contours (JEDEC2S2P) 3)
Operating voltage range	BVDD	8		28	V	Power supply mode
		5.5		40	V	The performance of analog circuit drops and the motor operation cannot be guaranteed
RETENTION MODE Operating voltage	BVDD	2.5			V	
Half-bridge high-side power supply voltage	MVDD	8		28	V	
Operating current	Isy		10	15	mA	Active Mode, all IO input
			3.2		mA	Idle Mode Tj<=150°C
				50	μA	Sleep Mode Tj<=150°C
				75	μA	Sleep Mode, HVIO Wakeup Enabled Tj<=150°C
5V output capacitor	CAVDD			1	μF	AVDD pin
ChargePump Tank capacitor	CPTank		1		μF	
ChargePump Fly capacitor	CPFly		220		nF	
CP UV Vtrip+ (refer to MVDD)		4.9 5.9 6.8 7.8	5.25 6.25 7.25 8.25	5.6 6.6 7.7 8.7	V	
CP UV Vtrip- (refer to MVDD)		4.7 5.7 6.6 7.6	5 6 7 8	5.3 6.3 7.4 8.4	V	
CP UV Vtrip hysteresis		0.2	0.25	0.3	V	
CP OV Vtrip+ (refer to MVDD)		10.5	11	11.5	V	
CP OV Vtrip- (refer to MVDD)		10.2	10.75	11.3	V	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
CP OV Vtrip hysteresis		0.2	0.25	0.3	V	
VBAT capacitor	CVBVDD		10		uF	BVDD pin
Low level of I/O input	VIL			0.4	AVDD	GPIO, TEST, SWD
I/O input high level	VIH	0.6			AVDD	GPIO, TEST, SWD
I/O trigger hysteresis voltage	VHYST		0.5		V	
I/O weak up/down resistance	Rpull		10000		Ω	
I/O input weak pull-down current	IIWPD		50		μA	
I/O input low-level current	ILOW	-5		5	μA	IO_VIN=0
I/O input weak pull-up current	IIWPU		50		μA	
I/O input high-level current	IHIGH	-5		5	μA	IO_VIN=AVDD
I/O output low level	VOL			0.4	V	GPIO, TEST, SWD
I/O output high level	VOH	AVDD -0.4			V	GPIO, TEST, SWD
Output current	IOUT	-4		4	mA	GPIO
			20		mA	Pre-driver OUT (I _{CURRENT} = 1)
			300		mA	Pre-driver OUT (I _{CURRENT} = 15)
LIN bus voltage	VBUS	-2.7		20.7	V	
LIN wakeup high-level time	TWHI	1			1/FAUX	
LIN output low level	VBUSOL		0.8	1.2	V	
LIN output high level	VBUSOH	0.8		1	VBVDD	
LIN Internal pull-up resistance	RLIN_UP		30	60	KΩ	
LIN Driver dominant state current shutdown threshold	IBUS_LIM	40		200	mA	VBUS =18V
Input leakage current state 1	IBUS_LEA K_1	-1			mA	VBUS =0V, VBAT=12V
Input leakage current state 2	IBUS_LEA K_2			20	μA	VBUS>VBAT, 8<VBUS<18, 8<VBAT<18
Input leakage current state 3	IBUS_LEA K_3	-1		1	mA	VGND=VBVDD, 0<VBUS<18, VBAT=12V
Input leakage current state 4	IBUS_LEA K_4			30	μA	VBVDD=VGND, 0<VBUS<18, VBAT=disconnected

Parameters	Symbol	Min	Typ	Max	Unit	Comments
LIN receiver dominant state	VBUSdom			0.4	VBVDD	
LIN receiver recessive state	VBUSrec	0.6			VBVDD	
Center of LIN receiver threshold	VBUScent	0.475	0.5	0.525	VBVDD	
LIN receiving hysteresis threshold	VBUShyst			0.175	VBVDD	
LIN Duty Cycle 1	D1	39.6			%	Speed=20.0 kbps, THREC (max)=0.744x VBVDD; THDOM (max)=0.581xVBVDD VBVDD = 7.0 V to 18 V; D1 = tBUS_rec(min) / (2 x Tbit)
LIN Duty Cycle 2	D2			58.1	%	Speed=20.0 kbps, THREC (max)=0.422x VBVDD; THDOM (max)=0.284xVBVDD VBVDD = 7.6 V to 18 V; D2 = tBUS_rec(min) / (2 x Tbit)
LIN Duty Cycle 3	D3	41.7			%	Speed=10.4 kbps, THREC (max)=0.778x VBVDD THDOM (max)=0.616xVBVDD VBVDD = 7.0 V to 18 V; D3 = tBUS_rec(min) / (2 x Tbit)
LIN Duty Cycle 4	D4			59.0	%	Speed=10.4 kbps, THREC (max)=0.389x VBVDD THDOM (max)=0.251xVBVDD VBVDD = 7.6V to 18 V; D4 = tBUS_rec(min) / (2 x Tbit)
LIN receiver propagation delay	TRX_PD			6	μs	
Symmetry of LIN receiver propagation delay	RXD_SYM	-2		2	μs	
LIN slave capacitor	CSLAVE			30	pF	
LIN Falling slew rate	dV/dTfall		1.5		V/μs	SR=0, Cbus=1nF, Rbus = 1Kohm
			1			SR=1, Cbus=1nF, Rbus = 1Kohm
			2			SR=2, Cbus=1nF, Rbus = 1Kohm
			20			SR=3, Cbus=1nF, Rbus = 500 ohm
LIN Rising slew rate	dV/dTRise		1.5		V/μs	SR=0, Cbus=1nF, Rbus = 1Kohm

Parameters	Symbol	Min	Typ	Max	Unit	Comments
			1			SR=1, Cbus=1nF, Rbus = 1Kohm
			2			SR=2, Cbus=1nF, Rbus = 1Kohm
			20			SR=3, Cbus=1nF, Rbus = 500 ohm
Low pulse for LIN wake up	TWLO	28		150	μs	VBUS<VBVDD/2-360mv
LIN auto-addressing current	IAUTO_C	1.85	2.05	2.25	mA	SWC2
		1.0	1.12	1.24	mA	SWC1
		3.15	3.50	3.85	mA	SWC3
LIN shunt resistor	RSHUNT		1		Ω	
Comparator delay	BEMFCdelay		500	550	ns	
Comparator offset	BEMFCoffset		±5	±15	mV	
Comparator hysteresis voltage	BEMFChyst		0		mV	
		5	10	15	mV	
		10	20	30	mV	
		20	40	50	mV	
Comparator input voltage range	BEMFCVin	AVSS		AVDD	V	
Comparator startup time	BEMFCTon			5	μs	
DAC Gain error.	DAC_GE	-1.5		1.5	%	
DAC Zero point error	DAC_ZE	-2		2	mV	
Difference nonlinearity	DAC_DNL	-1		1	LSB	
Nonlinear integration	DAC_INL	-2		2	LSB	
ADC Resolution	ADC_RES		12		BIT	
ADC Difference nonlinearity	ADC_DNL	-1		1	LSB	
ADC Nonlinear integration	ADC_INL	-4		4	LSB	
ADC Zero error with buf	ADC_ZE	-10		10	LSB	
ADC Zero error without buf		-5		5	LSB	
ADC Gain error (Internal-ref)	ADC_GE	-0.5		0.5	%	
ADC Gain error (External-ref)		-0.5		0.5	%	
ADC clock frequency	Fadc		48		MHz	
ADC startup time				10	μs	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
ADC Conversion time	Ctime		0.5		μs	
Internal used ADC reference voltage	VREF		2.5		V	Full Temperature
		2.475	2.5	2.525	V	25°C
Reference Output Voltage 1.25	VREFO0		1.25		V	REF_SEL=0 ; Load capacity ±1mA ;
Reference Output Voltage 2.5	VREFO1		2.5		V	REF_SEL=1 ; Load capacity ±1mA ;
Reference temperature drift				30	ppm/C	
Reference Output Cload			1		μF	
Reference startup time			0.5		ms	
OPA Input voltage range	Vin	0		AVDD-1.2	V	
OPA Input Offset w/o Cal	Vos.raw	-7		7	mV	
OPA Input Offset w/i Cal	Vos.cal	-3		3	mV	
OPA Input bias current	IB			100	nA	
OPA Output load capacitance	CL	0		50	pF	
OPA Output load resistance	RL	10k			ohm	
OPA Output voltage swing	Vout	0.2		AVDD-0.2	V	
OPA Slew rate	SR		6		V/μs	CL= 50pF
OPA Unity gain bandwidth	GBW		15		MHz	
GDU Maximum total charge driver capability				100	nC	4)
GDU Charge current - High Side Driver	I_charge_H_15	200	300	450	mA	
GDU Discharge current - High Side Driver	I_discharg_e_H_15	200	300	450	mA	
GDU Charge current - Low Side Driver	I_charge_L_15	200	300	450	mA	
GDU Discharge current - Low Side Driver	I_discharg_e_L_15	200	300	450	mA	
GDU Charge current - High Side Driver	I_charge_H_1		15		mA	
GDU Discharge current - High Side Driver	I_discharg_e_H_1		25		mA	
GDU Charge current - Low Side Driver	I_charge_L_1		15		mA	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
GDU Discharge current - Low Side Driver	I_discharge_L_1		25		mA	
GDU FET gate drive voltage (Gxx vs. Sxx/MVSS)	VGL1/2/3_MVDD_xV VGH1/2/3_MVDD_xV	7.8	9	10	V	
GDU FET gate drive voltage (Gxx vs. Sxx/MVSS)	VGL1/2/3_MVDD_xV VGH1/2/3_MVDD_xV	6.3	MVDD-1	9.5	V	
GDU FET gate drive voltage (Gxx vs. Sxx/MVSS)	VGL1/2/3_MVDD_xV VGH1/2/3_MVDD_xV	3	MVDD-1	7.5	V	
GDU Rise time	t_rise_15	100	250	450	ns	
GDU Fall time	t_fall_15	100	250	450	ns	
GDU Rise time	t_rise_1	1.25	2.5	5	μs	
GDU Fall time	t_fall_1	1.25	2.5	5	μs	
GDU Low-side rising propagation delay	t_delay_L S_rise_15		200		ns	
GDU Low-side falling propagation delay	t_delay_L S_fall_15		200		ns	
GDU High-side rising propagation delay			200		ns	
GDU High-side falling propagation delay			200		ns	
GDU Low-side rising propagation delay	t_delay_L S_rise_1		1.5		μs	
GDU Low-side falling propagation delay	t_delay_L S_fall_1		1.5		μs	
GDU High-side rising propagation delay			1.5		μs	
GDU High-side falling propagation delay			1.5		μs	
GDU Inherent dead-time		100		500	ns	
GDU Boosted discharge mode Ron			8	12	Ω	
GDU FET gate pull-down resistor	Rpd_GH/GL_x	40	60	90	KΩ	
GDU SHx pull-down resistor		55	80	120	KΩ	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
GDU Low-side VDS threshold voltage	Vds_LS_t hreshold_ x	0.14 0.35 0.55 0.65 0.90 1.00 1.20 1.40	0.25 0.50 0.75 1.00 1.25 1.5 1.75 2.00	0.35 0.65 0.90 1.25 1.45 1.80 2.10 2.40	V	
GDU High-side VDS threshold voltage	Vds_HS_t hreshold_ x	0.15 0.35 0.55 0.65 0.90 1.00 1.20 1.40	0.25 0.50 0.75 1.00 1.25 1.5 1.75 2.00	0.35 0.65 0.90 1.25 1.45 1.80 2.10 2.40	V	
Temperature Errors	TEMPerr	-10		10	°C	
Thermal shut down temperature	TSD	185	195	210	°C	
Thermal shut down return temperature	TSDR	160	175	190	°C	
Main clock	Fmain1		48		MHz	ERM off
Auxiliary clock	Faux	14	35	56	KHz	
Analog power supply	AVDD	4.5	5	5.5	V	Load capacity 15mA ;
Digital power supply	DVDD	1.35	1.5	1.65	V	
BVDD undervoltage threshold	VBVDDup		6.5	7	V	threshold=00
			7.5	8	V	threshold=01
			8.5	9	V	threshold=10
			9.5	10	V	threshold=11
BVDD undervoltage threshold	VBVDDun	5.5	6		V	threshold=00
		6.5	7		V	threshold=01
		7.5	8		V	threshold=10
		8.5	9		V	threshold=11
BVDD undervoltage hysteresis	VBVDDhys	0.5		1	V	
BVDD overvoltage threshold	VBVDDOv0		19		V	BOV=0
BVDD overvoltage threshold	VBVDDOv1		28		V	BOV=1
Active mode POR threshold	VPOR			5.5	V	BVDD pin voltage
Sleep mode POR threshold	VPOR_Sleep	0.5			V	BVDD pin voltage

<i>Parameters</i>	<i>Symbol</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Unit</i>	<i>Comments</i>
Retent mode POR threshold	VPOR_Re tent			2.5	V	BVDD pin voltage
Retent mode voltage	VRETENT			5.5	V	BVDD pin voltage
NVR sector erasure time	T _{NVR_ERS}	10		12.5	ms	
NVR program time	T _{NVR_PGM}	40			μs	
NVR read cycle	T _{NVR_READ}	50			ns	
Number of NVR burns	NTIMES	20K			Cycles	Tj=165°C, each word
		20K			Cycles	Tj=125°C, each word
		20K			Cycles	Tj=25°C, each word
Number of Flash burns	NTIMES	20K			Cycles	
Data retention time	TRETENT	20			years	Tj=85°C

- 1) Parameter is derived from design characterization on a small sample size (mini-char data).
- 2) Using the checkpoint method for testing minimum or maximum parameter.
- 3) Parameter is simulated with model of 2s2p board according JEDEC. Values are only valid if the exposed pad is soldered onto the PCB.
- 4) Total gate charge specification is only a recommendation. FETs with higher gate charge can be used when resulting slew rates are tolerable by the application and resulting power dissipation does not lead to thermal overload.

6. Function Description

6.1. Power Supply

NSUC1602 can support the direct use of the 12V power supply on the automotive. The chip is integrated with a high voltage LDO. The on-chip analog module uses 5V LDO(AVDD) for power supply, the digital module uses 1.5V LDO(DVDD) for power supply, and the chip can also support Load-Dump and Cold-Crank in a low power consumption mode. When NSUC1602 is cold started, and if the supply voltage drops to retention voltage, and then the data can still be saved to SRAM. In this mode, the digital power supply 1.5V still works normally, all peripherals and cores of the processor are in reset state, and the program cannot be executed. When the power supply voltage returns to the normal voltage, the CPU resets the PC pointer, and starts running from scratch, and records the retention flag in the PMU status register. When the power supply voltage drops below the POR voltage, a POR signal will be generated first, and the chip will return to the normal power on startup mode. At this time, the data in the SRAM area cannot be saved.

6.2. Operating Mode

NSUC1602 provides flexible operation modes according to system requirements, including active mode, retention mode, idle mode, sleep mode, TSD mode, and OV/UV mode.

- Active mode: all modules can be used. The CPU can choose 48MHz or 32MHz
- Retention mode: the CPU and all peripherals are in reset state, and SRAM data will be saved
- Idle mode: the CPU is in reset state, other modules remain in the original state, and can be waked up by LINPORT and WWDG
- Sleep mode: the CPU and all modules are in power down state (except LIN port, low-speed clock, and low-power LDO that work normally), and it can be waked up by LINPORT & HVIO pin
- TSD mode: when the junction temperature exceeds 185 ° C, the system will enter the over temperature mode. Only some digital modules are in the active state, and other modules will be turned off. Reduce the power consumption to prevent the chip from overheating
- OV/UV mode: when the BVDD voltage exceeds the over voltage threshold, the system will enter the over voltage mode, and the charge pump will be turned off. The software can turn off other modules to reduce the current consumption. When the BVDD voltage is lower than the under-voltage threshold, the system will enter the under-voltage mode. The software can also turn off other modules for on-site protection

6.3. Temperature Detection

The NSUC1602 is internally integrated with two temperature sensors, one of which is used to monitor the over temperature of the whole chip. It is used for the system to judge whether to enter the thermal shutdown mode (TSD). When the temperature exceeds the threshold, it will enter the PMUHandler interrupt function. The customer can define the software to shut down some modules. When the temperature returns to normal, the TSD flag will be cleared by the hardware. Another temperature sensor is connected to ADC, and the temperature with high accuracy can be obtained through ADC conversion. Customer can use the software method to set a software temperature shutdown threshold and close the module with high power consumption before reaching the hardware thermal shutdown. The temperature sensor can achieve $\pm 10^{\circ}\text{C}$ accuracy within full temperature range.

6.4. Processor Core Architecture

NSUC1602 is a processor chip based on ARM Cortex-M3 core, which is a 32bit processor based on RISC instruction set and is widely used in automotive systems. The chip architecture is designed based on the Harvard architecture. The data bus and address bus are independent of each other and have three-level pipeline to improve the system operation efficiency, so that the performance can be achieved about 1.25DMIPS/MHz.

The kernel of NSUC1602 is mainly included the following modules:

- NVIC: 10 system interrupts, 20 user interrupts, which can be configured into 4 group interrupts, each group has 8 levels of priority
- DAP: AHB-AP&SWD Serial Line Monitoring
- 3 data breakpoints
- 8 Flash patch breakpoints

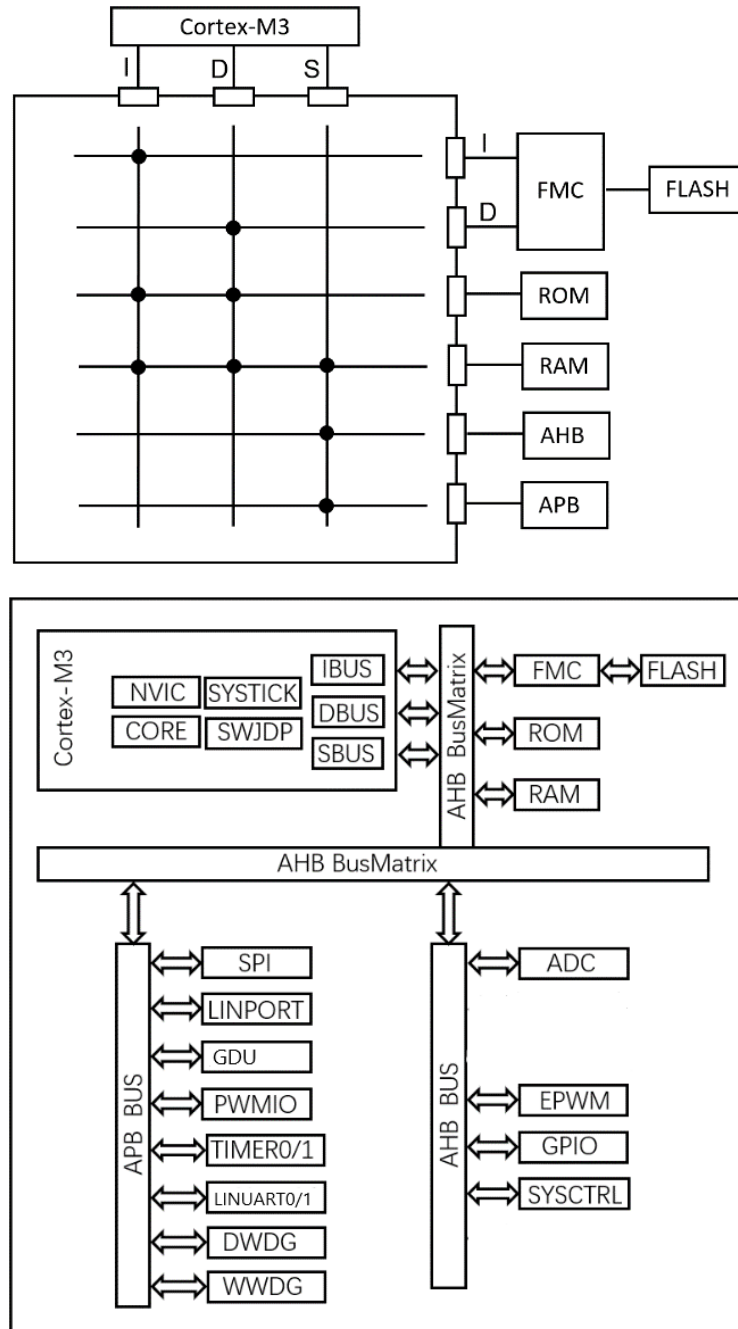
NSUC1602 supports SWD serial debugging function and communicates through SWCLK and SWIO (the two Pins are not allowed to be reused into any other function), The SWD port can be locked by burning the SWD protection bit of NVR, so that the program in Flash cannot be read through the SWD port, thus protecting the chip.

6.5. Clock System

The NSUC1602 has three clocks. The main clock can be 48MHz or 32MHz. This clock mainly provides the core and digital peripherals with an operating clock (excluding the window watchdog). The secondary clock is 35KHz. This clock mainly provides the window watchdog, the wake-up timer, and the LIN port wake-up module with a clock. When the CPU enters IDLE modes, it can wake up through the wake-up timer module and LIN port; When CPU enter SLEEP mode, it can wake up through LIN port and HVIO pin. These three clocks are generated by using the RC oscillator. Also, the 48MHz and 32MHz all have frequency EMI reduction modules and when it is enabled, the system EMI of the main frequency can be reduced.

6.6. Bus System

NSUC1602 integrated bus matrix is mainly composed of AHB bus and APB bus. The core can access Flash, ROM and RAM through I bus and D bus, and access AHB and APB peripherals through S bus. The APB bus is equipped with SPI, LINPORT, LINUART, UART1, PWMIO, TIMER0/1, DWDG, WWDG, GDU and other peripherals, and the AHB bus is equipped with ADC, DAC, BEMFC, EPWM, SYSCTRL, as shown in the figure below:



6.7. Memory Address Mapping

Program memory, data memory, registers and I/O ports are arranged in a 4GB address space. Each byte is encoded in the memory according to the little-endian format. The byte with the lowest number in the word is regarded as the least significant byte of the word, while the byte with the highest number is regarded as the most significant byte. Follow ARM® Cortex™-M3 has the following basic organizational structure for storage as Table 6.1.

Table 6.1 Basic Organization Structure of Memory

Classification	Boundary address	Capacity
ROM	0x0100 0000 - 0x0100 13FF	5KB
RAM (ID mapping)	0x1000 0000 - 0x1000 0FFF	4KB
FLASH	0x0800 0000 - 0x0800 FFFF	64KB
FLSAH Controller	0x4003 0000 - 0x4003 0FFF	4KB
RAM (S mapping)	0x2000 0000 - 0x2000 0FFF	4KB

All storage areas that are not allocated to on-chip memory and peripherals are considered "reserved areas". For details about peripheral register mapping, see the following table.

Table 6.2 Chip Peripheral Address Mapping Table

Classification	Boundary address	Peripheral
Reserved	0xE010 0000 - 0xFFFF FFFF	Reserved
Cortex™-M3	0xE000 0000 - 0xE00F FFFF	Cortex™-M3 internal peripherals
Reserved	0x4003 0FFF - 0xDFFF FFFF	Reserved
AHB	0x4002 5000 - 0x4002 5FFF	GPIO
	0x4002 4000 - 0x4002 4FFF	APMU
	0x4002 3000 - 0x4002 3FFF	Reserved
	0x4002 2000 - 0x4002 2FFF	ADC
	0x4002 1000 - 0x4002 1FFF	EPWM
	0x4002 0000 - 0x4002 0FFF	SYSCTRL
	0x4000 9000 - 0x4000 9FFF	UART1
APB	0x4000 8000 - 0x4000 8FFF	DWDG
	0x4000 7000 - 0x4000 7FFF	WWDG
	0x4000 6000 - 0x4000 6FFF	TIMER1
	0x4000 5000 - 0x4000 5FFF	TIMER0
	0x4000 4000 - 0x4000 4FFF	PWMIO
	0x4000 3000 - 0x4000 3FFF	LINUART
	0x4000 2000 - 0x4000 2FFF	LINPORT
	0x4000 1000 - 0x4000 1FFF	SPI
	0x4000 A000 - 0x4000 AFFF	SSI(SPI_SLAVE)
	0x4000 0000 - 0x4000 0FFF	GDU (Including DAC & CMP &BEMFC)

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NVR IF0,1,2 are used for customer to store their application data. The total size is 1.5KB.

NVR_IF0 address: 0x0801_0000 to 0x0801_01FF;

NVR_IF1 address: 0x0801_0200 to 0x0801_03FF;

NVR_IF2 address: 0x0801_0400 to 0x0801_05FF.

Note: NVR0,1,2 are not included in the 64KB flash area, it's additional memory.

6.8. Bootstrap Configuration

In the chip, different bootstrap modes can be selected through TEST pin, as shown in Table 6.3.

Table 6.3 Bootstrap Mode

Bootstrap mode selection pin	Bootstrap mode	Bootstrap space
TEST/IO9/IO10		
0/x/x	FLASH	Select FLASH as bootstrap space
1/0/0	SRAM	Select SRAM as bootstrap space

6.9. SYSCTRL Module

The SYSCTRL module of NSUC1602 includes system clock control logic, reset logic, system wake-up logic, power control logic, low power consumption control logic, analog configuration logic, chip key lock logic, and chip ID number. It can configure CPU clock, ERM module, clock settings and peripherals in debugging mode through the system control (SYSCTRL) module. In addition, the SYSCTRL module also provides control registers for calling power saving modes (IDLE, SLEEP), and reports status registers for resetting or awakening sources, and also provides status interrupt registers (BVDDUV, BVDDOV) related to BVDD and the flag from returning idle mode events (RFI).

6.10. GPIO Module

The GPIO of NSUC1602 is a programmable general purpose I/O peripheral, which contains one group of GPIOs, and a total of 13 I/Os. In input mode, each port can enable weak pull-up or weak pull-down resistors. The input of the port will be selected through the deglitch filter circuit and function multiplexing. The filtered input signal is stored in the data input register (GPIOx_DI). The input signal can also be used to generate GPIO interrupts on the rising or falling edge. In output mode, each port can be configured with push-pull or open drain mode and driven by data output register (GPIOx_DO). Some of the GPIO ports can be used as analog functions. In this mode, the input signals applied to the GPIO ports are sent to the ADC input multiplexer. Note that the range of analog input signals is limited from AVSS to AVDD. In the analog input mode, the digital function of the port is disabled, and the digital input signal is driven to "0". When the pin is configured as output, the value written to the output data register (DO) will be output on the I/O pin. When the pin is configured as input, the input data register (DI) captures the data of the I/O pin every 1 CPU clock cycle (FCLK). All GPIO pins have internal weak pull-up and pull-down resistance, which can be determined according to the setting of GPIOx_PUR/GPIOx_PDR. The specific pin definition abbreviations are shown in Table 6.4, and the multiplexing functions are shown in Table 6.4:

Table 6.4 Abbreviations of pin definitions

Name	Abbreviation	Definition
Pin Name	The pin functions during and after reset are the same as the actual pin names, unless otherwise specified in parentheses under the pin names.	
Pin type	S	Power supply pin
	SO	Power output pin
	I	Input pin only
	I/O	Input/output pin

Pin architecture	TT	5V tolerance I/O
Notes	Unless otherwise specified by notes, all I/Os are set to be suspended during and after reset	
Reuse function	Through GPIOx_MUX register selection function	

Table 6.5 Pin Function Reuse Table

No	PAD Name	PAD Type	I/O Type	Pin Function Description							
				AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7 (Reset)
38	GPIO0	I/O	TT	-	-	UART1_RX_I	TIM0_OUT	SPI_CS_O	TIM0_IN	TRIG0_O	ADC0
37	GPIO1	I/O	TT	-	-	UART1_TX_O	TIM1_OUT	SPI_CK_O	TIM1_IN	TRIG3_O	ADC1
36	GPIO2	I/O	TT	-	-	TIM0_OUT	SWO	SPI_MOSI_IO	LINUART_RX_I	Reload_O	ADC2
35	GPIO3	I/O	TT	-	-	TIM1_OUT	LINUART_TX_O	SPI_MISO_I	TIM0_IN	PWMIO_OUT	ADC3
34	GPIO4	I/O	TT	-	-	SPI_MISO_SLAVE	-	SWO	TIM1_IN	PWMIO_IN	ADC4
33	GPIO5	I/O	TT	-	-	SPI_MOSI_SLAVE	-	TIM0_IN	PWMIO_IN		ADC5
32	GPIO6	I/O	TT	-	-	SPI_CLK_SLAVE	SPI_MOSI_IO	TIM1_IN	PWMIO_IN		
30	GPIO7	I/O	TT	-	-	-	TIM0_OUT	UART1_TX_O	TIM0_IN		SWIO
29	GPIO8	I/O	TT		-	-	TIM1_OUT	UART1_RX_I	TIM1_IN		SWCLK
28	GPIO9	I/O	TT	-	-	UART1_RX_I	SPI_MISO_I	PWMIO_OUT	LINUART_RX_I	SWO	-
27	GPIO10	I/O	TT	-	-	SPI_CSN_SLAVE	SPI_CK_O	TIM0_OUT	TIM0_IN	BEMFC0_O	-
26	GPIO11	I/O	TT	-	-	UART1_RX_I	SPI_CS_O	TIM1_OUT	TIM1_IN	BEMFC1_O	-
25	GPIO12	I/O	TT	-	-	TIM0_OUT	SWO	UART1_TX_O	PWMIO_IN	BEMFC2_O	-
23	HVIO	I/O	TT	-	-	PWMIO_OUT	TIM1_OUT	-	PWMIO_IN		-
21	LIN	I/O	-	-	-	PWMIO_OUT	TIM0_OUT	LIN_DO	PWMIO_IN	LIN_DI	-
22	LIN_O	I/O	-	-	-	-	-	-	-	-	-

6.11. LIN Port Module

NSUC1602 integrates high-voltage LIN port, supports LIN protocol communication and PWM input/output functions, and has the following characteristics:

- supports LIN 2. X protocol
- supports LIN auto-addressing
- supports overcurrent protection
- multiple input source multiplexing (PWMIO, UART, LIN_DO, TIMER)
- IDLE and SLEEP wake-up function

- supports LIN TX timeout shutdown

6.12. ADC Module

The NSUC1602 integrates a high-precision 12 Bit ADC, which can convert analog voltage from - VREFADC to VREFADC into digital signals. VREF-ADC is derived from internal Bandgap voltage. ADC module mainly has the following characteristics:

- 12-bit A/D converter
- 0.5 μ s fast conversion time for 2 MSPS sampling rate
- input multiplexer with 15 analog channels (GPIO0 to GPIO5 single ended, GPIO4/5 differential, internal temperature sensor VTEMP, motor current detection through the shunt resistor on MVSS, differential inputs for LIN auto-addressing, etc.)
- The internal reference voltage VREFADC is from the internal Bandgap
- supports the acquisition queue of automatic sequential conversion with up to eight channels
- Amplifier for external resistor to config gain
- Event driven or time related start trigger source of the optional acquisition queue (software, timer, and EPWM)
- supports the end of conversion (EOC) interrupt and conflict of conversion event interrupt
- supports single sequence conversion, continuous sequence conversion, single channel conversion, continuous single channel conversion

6.13. Enhanced PWM module

The NSUC1602 integrates enhanced pulse width modulation (EPWM) module. The EPWM can generate control signals for the half bridges and synchronize signals for the ADC module and BEMFC module. It is optimized for BLDC, brush DC (BDC). EPWM mainly has the following features:

- Supports BLDC and BDC motor control
- Critical registers are controlled by protected registers
- Two time-base counting modes: edge-aligned counting and center-aligned counting
- Two waveform output modes: complementary mode and independent mode
- Provides interrupts for PWM period match, zero match, and duty cycle compare match
- 3 complementary PWM outputs or 6 independent PWM outputs with selectable output polarity mode
- Provides a register reload enable bit to ensure register reload synchronization
- 16-bit prescaler and 8-stage postscaler
- Switchable manual control of PWM output
- Ability to trigger ADC at any point during the PWM time-base period
- Supports four independently programmable PWM control modules for period, duty cycle, and ADC trigger events

6.14. PWMIO Module

NSUC1602 integrated PWMIO module supports bidirectional communication through PWM protocol, with minimum CPU interaction. It can generate PWM output signal (PWM out) and measure the high and low time of applied PWM input signal (PWM in). The input and output signals of the PWMIO module are multiplexed to the LIN port and the GPIO port. PWMIO mainly has the following characteristics:

- Periodic input signal measurement (1Hz to 10kHz)
- Interruption generated at the falling and rising edges of the input signal, overflow of the input counter and the end of the output cycle
- High and low level counter measurement
- Optional input deglitch filter with 3 μ s filtering time
- LINPORT or GPIO can both use PWMIO to send single pulse or periodic pulse out
- Two independent 14-bit counters for input capture and output comparison

6.15. SPI Module

The NSUC1602 integrated serial bus interface provides a SPI communication interface with bit rates ranging from 125kHz to 16MHz. The clock polarity, clock phase and data order (MSB or LSB first) can be configured, and the data width can be set as 8, 16, 24 or 32 bits. SPI module mainly has the following characteristics:

- Serial input and output are connected to external hardware

- 4-wire interface (CS, CK, MISO, MOSI), full duplex
- 3-wire interface (CS, CK, MOSI), Half duplex
- master operation only
- bit rate from 125kHz to 16MHz - programmable clock phase and polarity
- 8-, 16-, 24- and 32-bit data frames supported by hardware chip selection (CSN)
- chip selection managed by hardware or software (CS)
- programmable data sequence (MSB/LSB priority)
- one receive and one transmit FIFO, each 8×8 -bit, organized according to data frame width
- RX/TX events or FIFO flags generate interrupts
- can be used to connect external devices, such as EEPROM, external ADC or display

6.16. SSI Module

The NSUC1602 integrated serial bus interface provides an SSI communication interface with bit rates ranging from 125kHz to 4MHz. The clock polarity, clock phase and data order (MSB or LSB first) can be configured, and the data width can be set as 8, 16, 24 or 32 bits. SPI module mainly has the following characteristics:

- Serial input and output are connected to external hardware
- 4-wire interface (CS, CK, MISO, MOSI), full duplex
- 3-wire interface (CS, CK, MOSI), Half duplex
- Slave SPI operation only
- bit rate from 125kHz to 4MHz - programmable clock phase and polarity
- 8-, 16-, 24- and 32-bit data frames supported by hardware chip selection (CSN)
- chip selection managed by hardware or software (CS)
- programmable data sequence (MSB/LSB priority)
- one receive and one transmit FIFO, each 8×8 -bit, organized according to data frame width

6.17. Timer Module

The NSUC1602 integrated universal timer has two instances of the timer module (TIM0, TIM1), which have the same implementation mode and operate independently of each other. The timer module is based on a 16-bit input clock prescaler and a 16-bit timer counter. The Timer module mainly has the following characteristics:

- Optional input clock: internal or external
- 16-bit input clock predivider
- 16-bit timer counter
- Optional operation mode: timer, compare or capture
- Optional buffer for reloading and capturing values
- Optional output signal: static value, PWM signal or timer input signal
- Interrupt triggered by update, compare, capture, and capture overcurrent events

6.18. DWDG Module

The NSUC1602 integrated digital watchdog has the characteristics of high security and flexible use. It can be used to detect and solve faults caused by software errors, and trigger the system reset when the timer reaches the specified timeout value. DWDG mainly has the following features:

- 16bit down counter
- clock supports 4 to 512 frequency division
- reset when down counter value reaches 0x0 (if watchdog is activated)

6.19. WWDG Module

The NSUC1602 integrated window watchdog (WWDG) clock is provided by the APB clock after pre frequency division. The window watchdog is usually used to monitor the abnormal late or early operation of the application through a configurable time window. Software failure caused by external interference or unpredictable logic conditions that cause the application program to deviate from the normal operation sequence. Unless the value of the up counter is refreshed when it is greater than the window value, a system reset will be generated when the preset time period is reached. If the up counter is smaller

than the window register value, a reset will also be generated. This means that the counters must be refreshed within a limited time window. WWDG mainly has the following characteristics:

- Free running 8-bit up-counter
- Reset when the up-counter value counts to 0x0 (if the watchdog is activated)
- Reset when the up counter is overloaded in the window (if the watchdog is activated)

6.20. UART Module

The NSUC1602 integrated full duplex universal UART module can process 8-bit data with parity or not, and one or two stop bits. The bit timing logic allows the necessary bit rate to be adjusted in the bit stream to synchronize to the LIN bit rate with the minimum residual error. The module has two 8-byte FIFO for data reception and transmission. The bit rate adjustment logic can be used to automatically synchronize the UART bit rate to the LIN master bit rate. The enhanced features are optimized for the LIN slave mode. The UART module has the following features:

- 8bit frame
- parity check
- baud rate automatic adjustment
- support TX, RX, FIFO empty, FIFO full, frame error, TX and RX loop error, break and sync interrupt
- break and sync automatic detection of two independent transmit receive FIFO
- LIN modes
- automatic LIN packet header reception

6.21. Flash Module

NSUC1602 integrated FLASH has 64KB storage space for storing application code and data. Read access to FLASH supports zero wait execution. The default programming mode of FLASH is to operate by page, while the default erasing mode is to execute by sector. During the erase and programming process of FLASH, interrupts must be disabled; otherwise, unexpected errors may occur. The Flash module has the following features:

- 64KB storage space
- supports ECC correction, one bit check and two bits error report from interrupt
- supports zero wait fast read access

6.22. NVR Module

The NSUC1602 integrated NVR is used to store non-volatile application data. During the erase and programming process of NVR, interrupts must be disabled; otherwise, unexpected errors may occur. the 1.5K bytes of the NVR are the client area (address is 0x0801_0000 to 0x0801_05FF), The NVR module has the following characteristics:

- 64*64bit (512 Bytes) for each sector
- totally customer can use 3 sectors (all size is about 1.5KBytes)

6.23. GDU Module

NSUC1602 integrated PreDriver port for driving external MOSFET, it can drive DC motors such as brush DC motor or brushless DC motor. Each driver output is composed of two n-channel power FETs, which can respectively use as high side and low side driver. The PreDriver module has the following characteristics:

- internal integrated over-current protection monitoring
- the high side is driven by charge pump, and supports 100% duty cycle conduction
- integrated resistance network and three back EMF comparators, Support sensorless BLDC control
- integrated 8-bit current limiting DAC, support 255 grades of current limiting
- integrated OPA which can support for current amplify
- support low side single resistance, it can be used for ADC sampling current
- support automatic shutdown in sleep, retention, TSD modes

In GDU module, there is a BEMFC module has three identical channels for processing the output signal of the BEMF comparator. BEMFC mainly has the following characteristics:

- supports parallel processing of three channels
- supports BEMF voltage zero crossing detection in BLDC motor applications
- Each channel's input polarity is programmable

- Each channel's deglitch filter is programmable
- Each channel's blanking filter is programmable and synchronized with the EPWM output signal
- All channels are shared an interrupt source to CPU, and which is triggered by the rising edge or falling edge of the zero-crossing detection logic output

7. Application Note

7.1. Typical Application Circuit of BLDC Motor Controlling

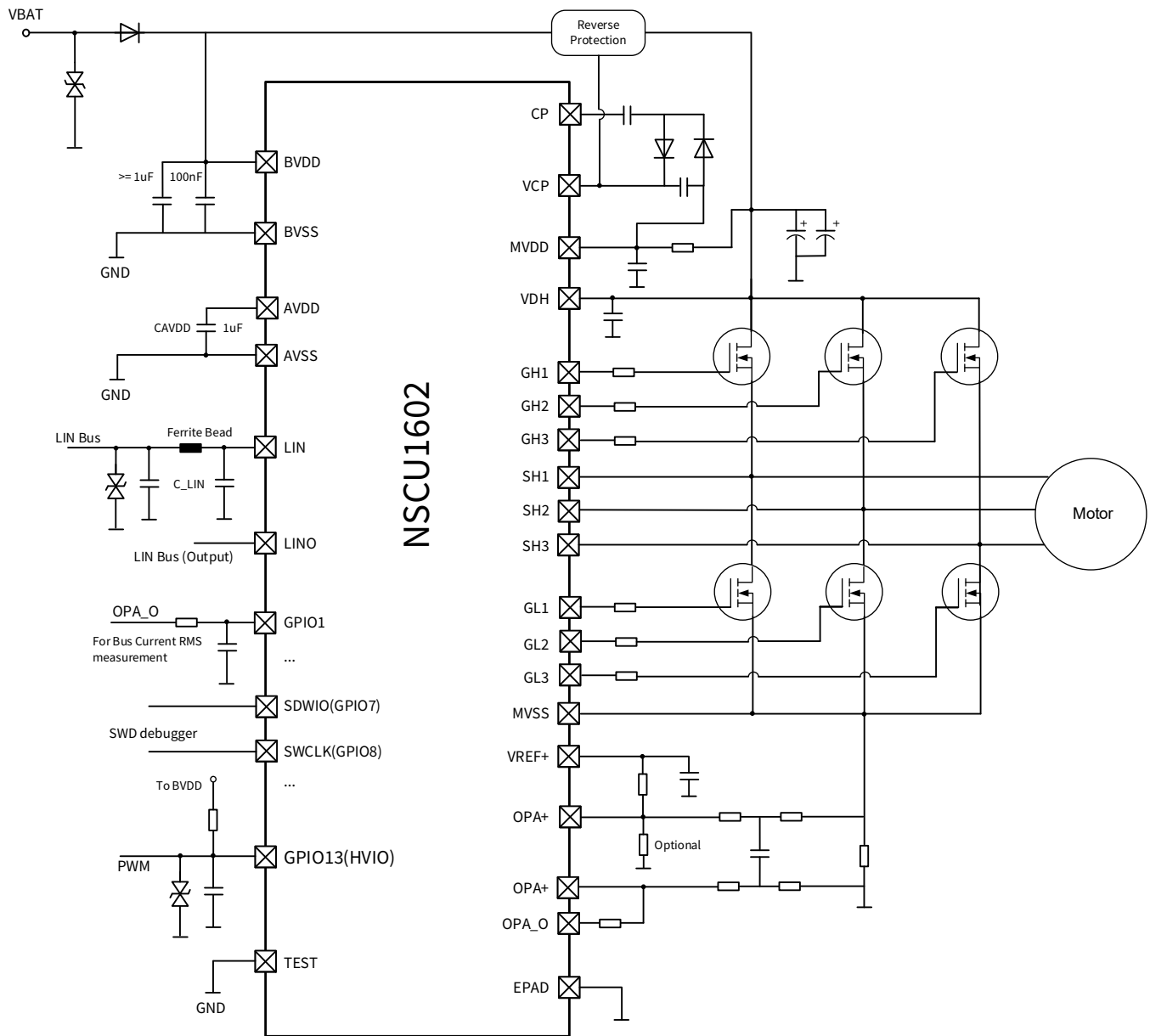


Figure 7.1 Typical application diagram

Note: This is a very simplified example of a BLDC application circuit. It shall not be regarded as a warranty of a certain functionality, condition, or quality of the device. The function must be verified in the actual application.

8. Function Safety

The NSUC1602 are ASSPs and developed as SEooC [ISO 26262] with assumed technical safety requirements with ASIL-B capability targets. The technical safety concept is described in the Safety manual.

9. Package Information

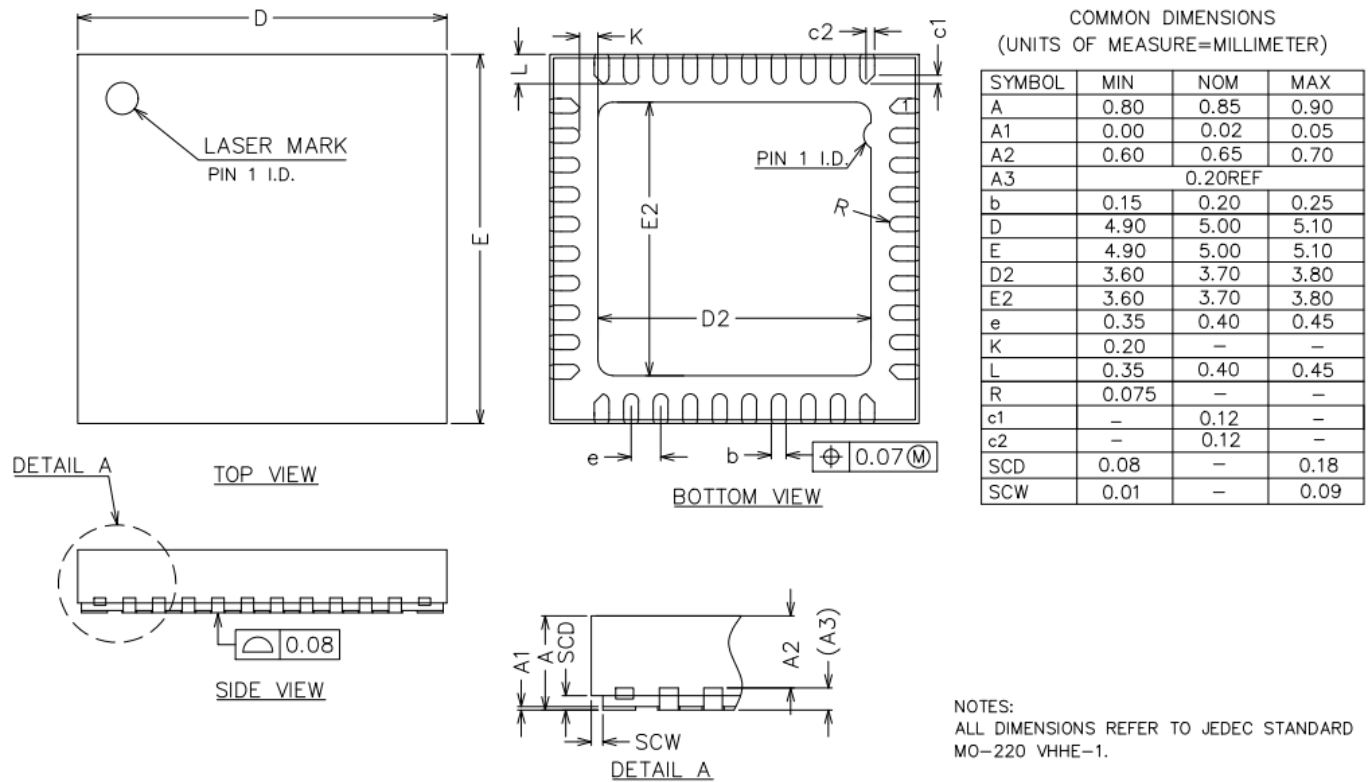


Figure 9.1 QFN40(5*5) Package Shape and Dimension in millimeters and (inches)

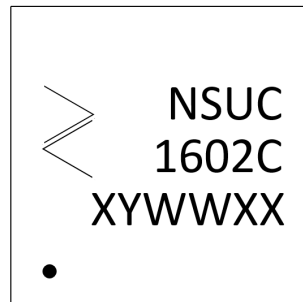
10. Ordering Information

Standard Ordering Item No.:

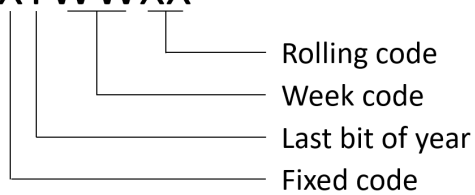
Part Number	Temperature	Flash Size (KB)	SRAM Size (KB)	Power Supply Voltage (V)	Package	MSL	SPQ	MPQ
NSUC1602-Q0QAERC	-40~150°C	64	4	12	QFN40(5*5)	MSL2	5000	5000

*Other order part numbers are acceptable. If you need other specifications, please contact NOVOSENSE for special support.

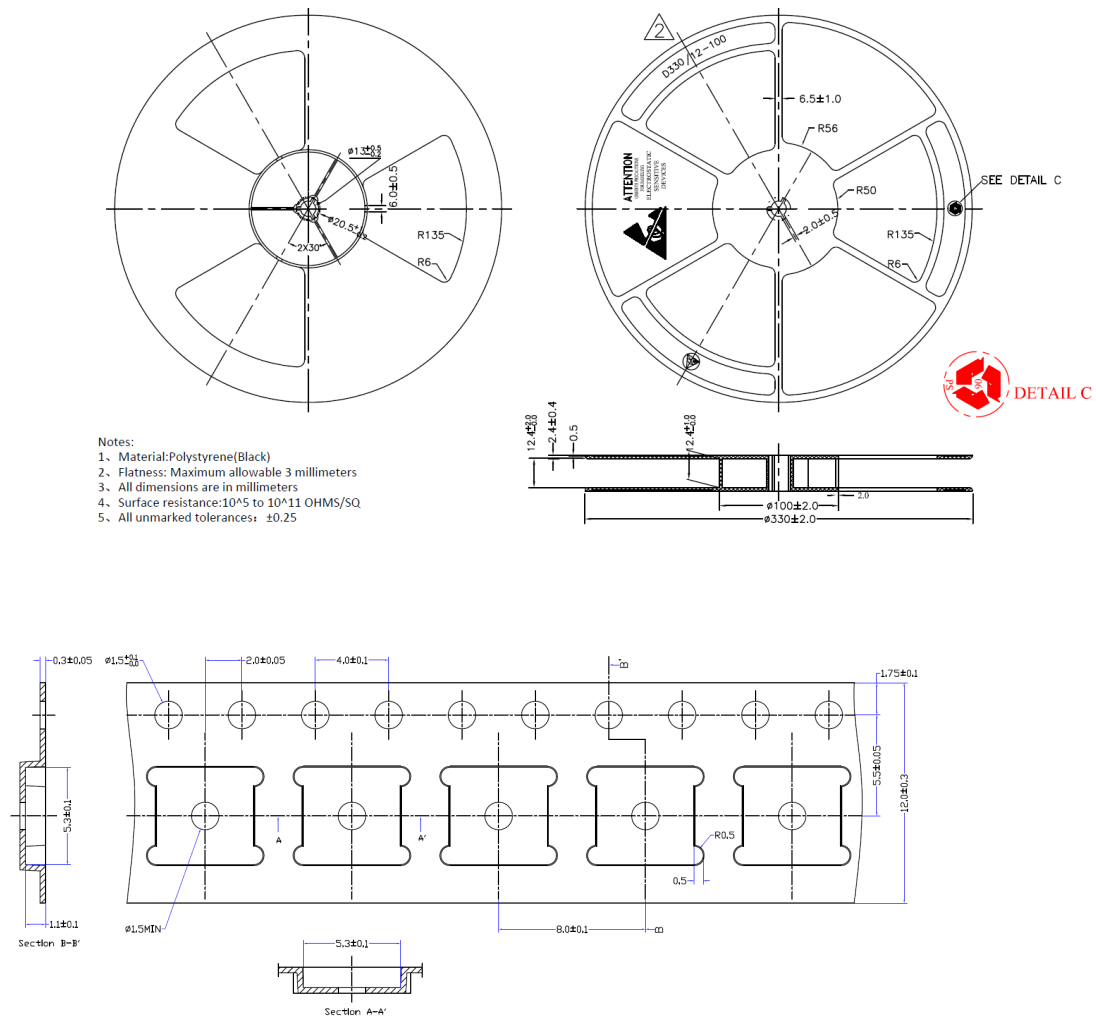
Marking rules:



XYWWXX



11. Tape and Reel Information



12. Revision History

Revision	Description	Date
1.0	Initial Version.	2025/04/29
1.1	ADD spec 'Symmetry of receiver propagation delay'	2026/02/04
1.2	ADD AVDD&VREF Load capacity	2026/05/14
1.3	1. Corrected errors in Figure 1 2. Optimized parameter naming conventions for spec table 3. Fixed ADC address mapping error and duplicate EPWM addresses 4. Format optimization for partial contents 5. Updated Figure 1.1 chip pin-out diagram 6. Add function safety description	2026/08/28

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