

Product Overview

The NSR2240x-Q1 is an adjustable output non-synchronous controller for switching regulators with low-side N-channel MOSFET. The device is applied with peak current mode control with internal slope compensation. It is suitable for topologies requiring a low-side MOSFET, such as boost, flyback, SEPIC, etc.

The NSR2240x-Q1 has built in features such as internal soft-start, under-voltage lockout, cycle-by-cycle current limiting, short-circuit protection and thermal shutdown. MSOP8 and MSOP10 packages are available.

Key Features

- AEC-Q100 Grade1 Qualified
- Wide 4 V to 44 V Input Range
- Internal Push-pull Driver With 1A Peak Current Capability
- 1.26 V Reference Voltage for NSR22401-Q1
- 1.275 V Reference Voltage for NSR22402-Q1
- Peak Current Mode with Internal Slope Compensation
- Internal Soft-start
- Adjustable Under-voltage Lockout (NSR22402-Q1)
- Cycle-by-cycle Current Limit
- Short Circuit Protection
- Over-voltage Protection
- Over-temperature Protection
- RoHS-compliant package

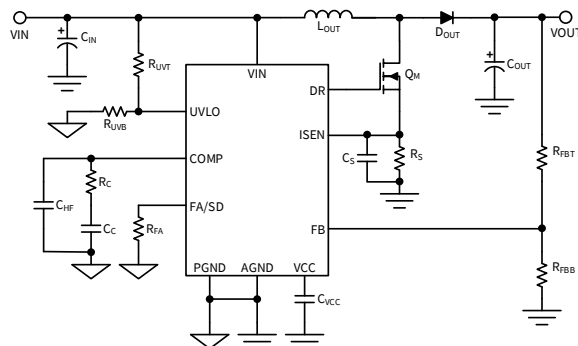
Applications

- Automotive On-board Charger
- Automotive DC-DC Converter
- Automotive Start-stop Applications
- Automotive ADAS Driver Information
- Boost for Audio Amplifiers

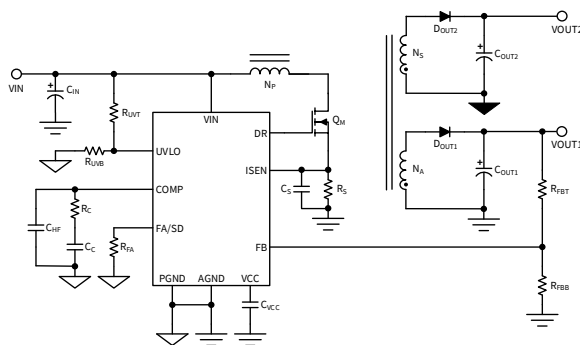
Device Information

Part Number	Package Info
NSR22401-Q1	3.00 mm x 3.00 mm MSOP8
NSR22402-Q1	3.00 mm x 3.00 mm MSOP10

Typical Circuits



NSR2240x Typical Boost Application Circuits



NSR2240x Typical Flyback Application Circuits

INDEX

1. PIN CONFIGURATION AND FUNCTIONS	3
2. ABSOLUTE MAXIMUM RATINGS	5
3. ESD RATINGS	5
4. RECOMMENDED OPERATING CONDITIONS	5
5. THERMAL INFORMATION	5
6. SPECIFICATIONS	6
6.1. ELECTRICAL CHARACTERISTICS	6
6.2. TYPICAL PERFORMANCE CHARACTERISTICS	8
7. DETAILED DESCRIPTION	9
7.1. OVERVIEW	9
7.2. BLOCK DIAGRAM	9
7.3. FEATURE DESCRIPTION	9
7.3.1. SUPPLY VOLTAGE	9
7.3.2. QUIESCENT CURRENT	9
7.3.3. FREQUENCY TIMING	10
7.3.4. UVLO AND SHUTDOWN	10
7.3.5. CURRENT SENSE	10
7.3.6. ERROR AMPLIFIER	11
7.3.7. DRIVER OUTPUT	11
7.3.8. OVER-VOLTAGE PROTECTION	11
7.3.9. THERMAL SHUTDOWN	11
8. TYPICAL APPLICATION	11
8.1. BOOST CONVERTER	11
8.1.1. TYPICAL CIRCUITS	11
8.1.2. LOOP STABILITY ANALYSIS AND DESIGN	12
8.2. FLYBACK CONVERTER	15
8.2.1. TYPICAL CIRCUITS	15
8.2.2. LOOP STABILITY ANALYSIS AND DESIGN	16
9. PACKAGE INFORMATION	18
9.1. MSOP8	18
9.1.1. TAPE AND REEL	18
9.1.2. MECHANICAL DATA	19
9.2. MSOP10	19
9.2.1. TAPE AND REEL	19
9.2.2. MECHANICAL DATA	21
10. ORDER INFORMATION	22
11. REVISION HISTORY	23

1. Pin Configuration and Functions

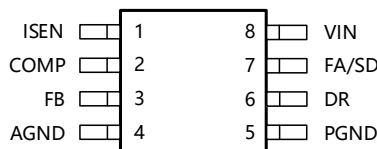


Figure 1 NSR22401-Q1 Pin Configuration

PIN NO.	SYMBOL	FUNCTION
1	ISEN	Current sense amplifier input. Connect this pin to a sense resistor which connected between source of external power MOSFET and GND.
2	COMP	Transconductance amplifier output. Connect to an external compensation network.
3	FB	Feedback voltage input. Connect to an external resistor divider from output to GND to regulate output voltage.
4	AGND	Analog ground reference for internal bias circuit.
5	PGND	Power ground reference for external power circuit.
6	DR	Gate driver output. The gate of the external MOSFET should be connected to this pin.
7	FA/SD	Frequency adjust and shutdown input. Connect to an external resistor to set switching frequency. The device is disabled when the pin is set as high.
8	VIN	Power supply input.

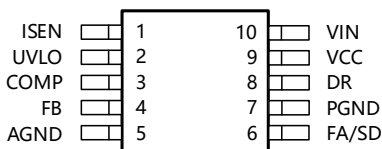


Figure 2 NSR22402-Q1 Pin Configuration

PIN NO.	SYMBOL	FUNCTION
1	ISEN	Current sense amplifier input. Connect this pin to a sense resistor which connected between source of external power MOSFET and GND.
2	UVLO	Under voltage lockout input. The part is disabled into non-switching mode when this pin is set as low.
3	COMP	Transconductance amplifier output. Connect to an external compensation network.
4	FB	Feedback voltage input. Connect to an external resistor divider from output to GND to regulate output voltage.
5	AGND	Analog ground reference for internal bias circuit.
6	FA/SD	Frequency adjust and shutdown input. Connect to an external resistor to set switching frequency. The device is disabled when the pin is set as high.
7	PGND	Power ground reference for external power circuit.

<i>PIN NO.</i>	<i>SYMBOL</i>	<i>FUNCTION</i>
8	DR	Gate driver output. The gate of the external MOSFET should be connected to this pin.
9	VCC	Driver supply voltage output. Connect to a bypass 0.47μF to 4.7uF capacitor to GND. Do not connect to external sources.
10	VIN	Power supply input.

2. Absolute Maximum Ratings

Description	Min	Max	Units
VIN	-0.4	48	V
COMP	-0.4	6	V
DR	-0.4	13	V
FB	-0.4	6	V
FA/SD	-0.4	6	V
ISEN	-0.4	6	V
UVLO (NSR22402-Q1)	-0.4	6	V
VCC (NSR22402-Q1)	-0.4	13	V
Junction Temperature	-40	150	°C
Lead Temperature		260	°C
Storage Temperature	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to conditions on Absolute Maximum Ratings for extended periods may affect device reliability.

3. ESD Ratings

Parameters	Symbol	Value	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), per AEC-Q100-002-RevD	±2000	V
	Charged device model (CDM), per AEC-Q100-011-RevB	±750	V

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V _{IN}	4		44	V

5. Thermal Information

Parameters	Symbol	MSOP8	MSOP10	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	156.8	157.1	°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	49.8	51.0	°C/W

The thermal data is based on the JEDEC standard high-K profile, JESD 51-7, four layer board.

6. Specifications

6.1. Electrical Characteristics

$V_{IN}=12V$, $R_{FA} = 40k\Omega$, $T_A=-40^{\circ}C$ to $125^{\circ}C$. Unless otherwise noted, typical value is at $T_A = 25^{\circ}C$.

Parameters	Symbol	Min	Typ	Max	Unit	Conditions
Supply Voltage						
Input under-voltage lock-out threshold	$V_{IN_UVLO_F}$		3.25	3.95	V	
Input under-voltage lock-out hysteresis	$V_{IN_UVLO_HYS}$		170		mV	
Quiescent Current						
Quiescent current (shutdown mode)	I_{SHDN}		9	15	μA	$V_{SD} = 3V$, $V_{IN} = 12V$
Quiescent current (non-switching)	I_{Q_NSW}		2.1	2.5	mA	
Quiescent current (switching)	I_{Q_SW}		2.5	3.1	mA	
Frequency Timing						
Minimum pulse width	t_{ON_MIN}	150	200	280	ns	
Maximum duty cycle	D_{MAX}		85		%	
Switching frequency (NSR22401-Q1)	f_{SW}	350	400	440	kHz	$R_{FA} = 40k\Omega$
Switching frequency (NSR22402-Q1)	f_{SW}	400	475	550	kHz	$R_{FA} = 40k\Omega$
Internal soft-start time (NSR22401-Q1)	t_{SS}	3	4	7	ms	$25^{\circ}C$
Internal soft-start time (NSR22402-Q1)	t_{SS}	8.7	15	21.3	ms	$25^{\circ}C$
Slope compensating ramp	V_{SL}		90		mV	Internal Compensation Ramp Voltage
UVLO and Shutdown						
UVLO source current (NSR22402-Q1)	I_{UVLO}	3	4	6	μA	
UVLO threshold (NSR22402-Q1)	V_{UVLO_F}	1.34	1.4	1.54	V	UVLO voltage ramping down
Shutdown threshold high	V_{SD_H}		1.35	1.7	V	
SD pin source current	I_{SDP_SRC}		-1		μA	$V_{SD} = 5V$, $25^{\circ}C$
Current Sense						
Cycle-by-cycle current limit threshold	V_{CL}	140	160	190	mV	$V_{IN} = 5V$
Over-current protection threshold	V_{SC}	290	350	380	mV	$V_{IN} = 5V$
ISEN output bias current	I_{SEN_BIAS}		40		μA	
Error Amplifier						
Transconductance (NSR22401-Q1)	G_m	600	815	1000	μS	$V_{COMP} = 1.4V$, $I_{EAO} = 100\mu A$
Transconductance (NSR22402-Q1)	G_m	385	450	580	μS	$V_{COMP} = 1.4V$, $I_{EAO} = 100\mu A$
VFB input bias current	I_{FB}		15		nA	
Reference voltage (NSR22401-Q1)	V_{REF}	1.228	1.26	1.292	V	$4V \leq V_{IN} \leq 40V$
Reference voltage (NSR22402-Q1)	V_{REF}	1.244	1.275	1.305	V	$4V \leq V_{IN} \leq 40V$
Feedback voltage line regulation			0.001		%/V	$2.97 \leq V_{IN} \leq 40V$, $25^{\circ}C$
VEA maximum output voltage	V_{EA_MAX}	2.1	2.5	2.7	V	$V_{FB} = 0V$, COMP pin floating

Parameters	Symbol	Min	Typ	Max	Unit	Conditions
VEA minimum output voltage	V_{EA_MIN}	0.2	0.3	0.6	V	$V_{FB} = 1.4V$
VEA sourcing current (NSR22401-Q1)	I_{EA_SRC}	110	160	220	μA	$V_{COMP} = 1.4V, V_{FB} = 0V$
VEA sourcing current (NSR22402-Q1)	I_{EA_SRC}	70	105	140	μA	$V_{COMP} = 1.4V, V_{FB} = 0V$
VEA sinking current (NSR22401-Q1)	I_{EA_SNK}	50	105	150	μA	$V_{COMP} = 1.4V, V_{FB} = 1.4V$
VEA sinking current (NSR22402-Q1)	I_{EA_SNK}	40	60	80	μA	$V_{COMP} = 1.4V, V_{FB} = 1.4V$
Gate Driver						
Driving voltage	V_{DRV}		V_{IN}		V	$V_{IN} < 7.5V, 25^{\circ}C$
			7.5		V	$V_{IN} \geq 7.5V, 25^{\circ}C$
Driver Switch On Resistance (top)	$R_{DRV_{T}}$		5		Ω	$I_{DR} = 0.2A, V_{IN} = 5V$
Driver Switch On Resistance (bottom)	$R_{DRV_{B}}$		1.7		Ω	$I_{DR} = 0.2A$
Drive Pin Rise Time	$T_{DRV_{R}}$		21		ns	$C_{GS} = 3000pF, V_{DR} = 0 \text{ to } 3V, 25^{\circ}C$
Drive Pin Fall Time	$T_{DRV_{F}}$		40		ns	$C_{GS} = 3000pF, V_{DR} = 3 \text{ to } 0V, 25^{\circ}C$
Over-voltage protection						
Over-voltage protection threshold	V_{OVP}	26	80	135	mV	
Over-Voltage protection hysteresis	V_{OVP_HYS}		75		mV	
Thermal Shutdown						
Thermal shutdown threshold	T_{SD}		175		$^{\circ}C$	
Thermal shutdown hysteresis	T_{SD_HYS}		20		$^{\circ}C$	

6.2. Typical Performance Characteristics

Unless otherwise specified, $V_{IN} = 12\text{ V}$, $T_J = 25^\circ\text{C}$.

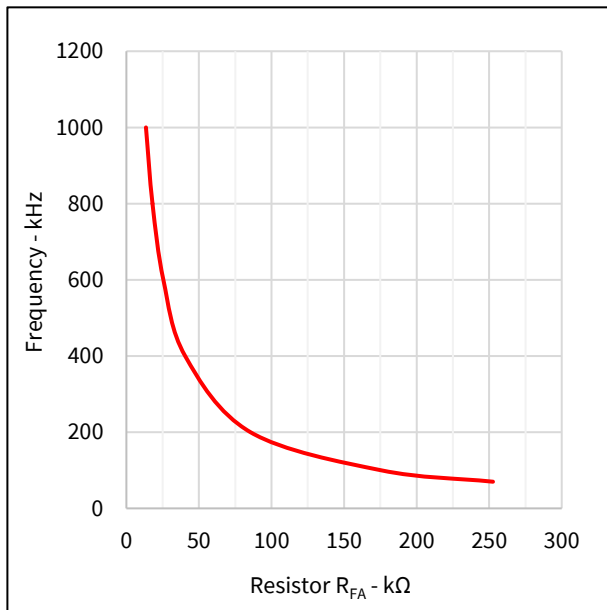


Figure 3 Switching Frequency vs RFA of NSR22401-Q1

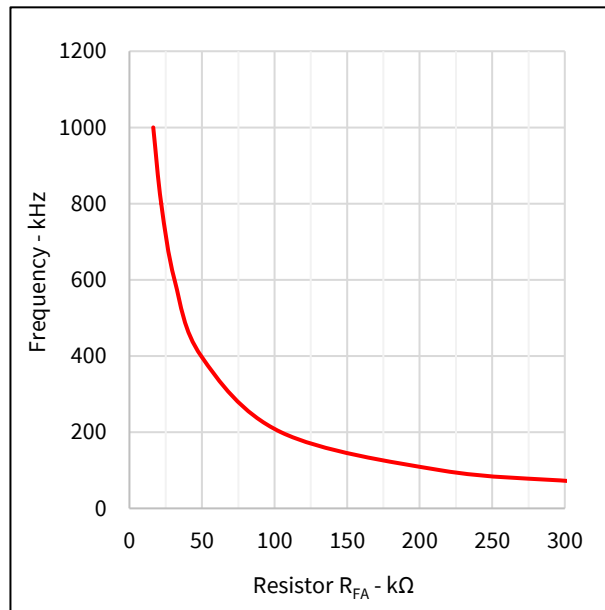


Figure 5 Switching Frequency vs RFA of NSR22402-Q1

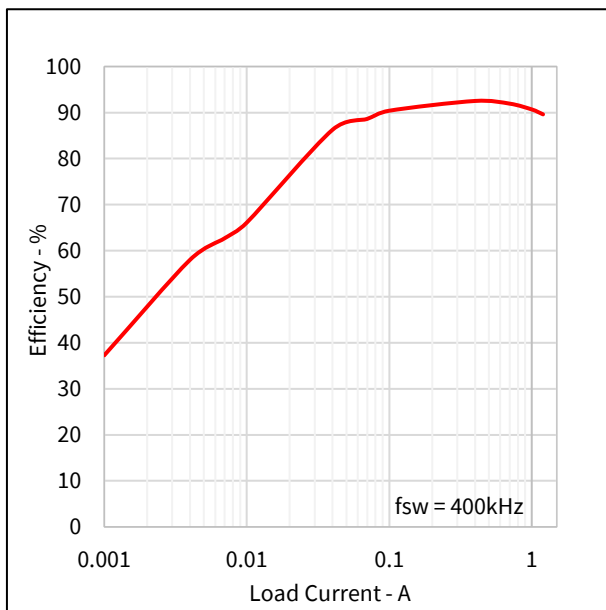


Figure 4 Efficiency Performance

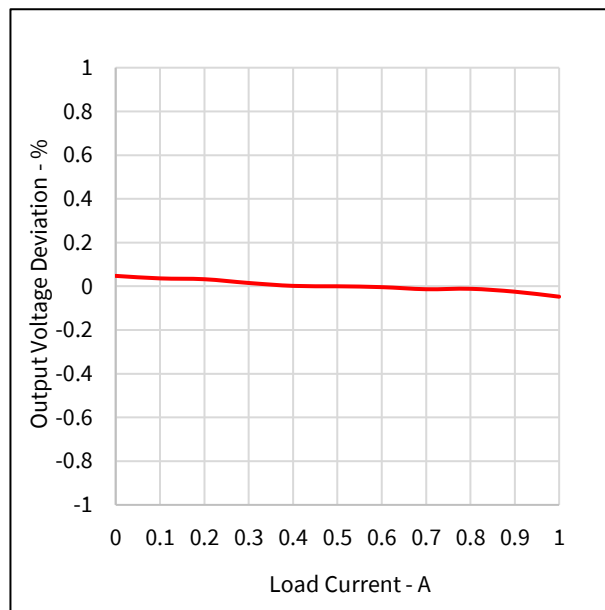


Figure 6 Load Regulation

7. Detailed Description

7.1. Overview

The NSR2240x-Q1 is an adjustable output non-synchronous controller for switching regulators with low-side N-channel MOSFET. The device is applied with peak current mode control with internal slope compensation. It is suitable for use in topologies requiring a low-side MOSFET, such as boost, flyback, SEPIC, etc.

The NSR2240x-Q1 has built in features such as internal soft-start, under-voltage lockout, cycle-by-cycle current limiting, short-circuit protection and thermal shutdown. MSOP8 and MSOP10 packages are available.

7.2. Block Diagram

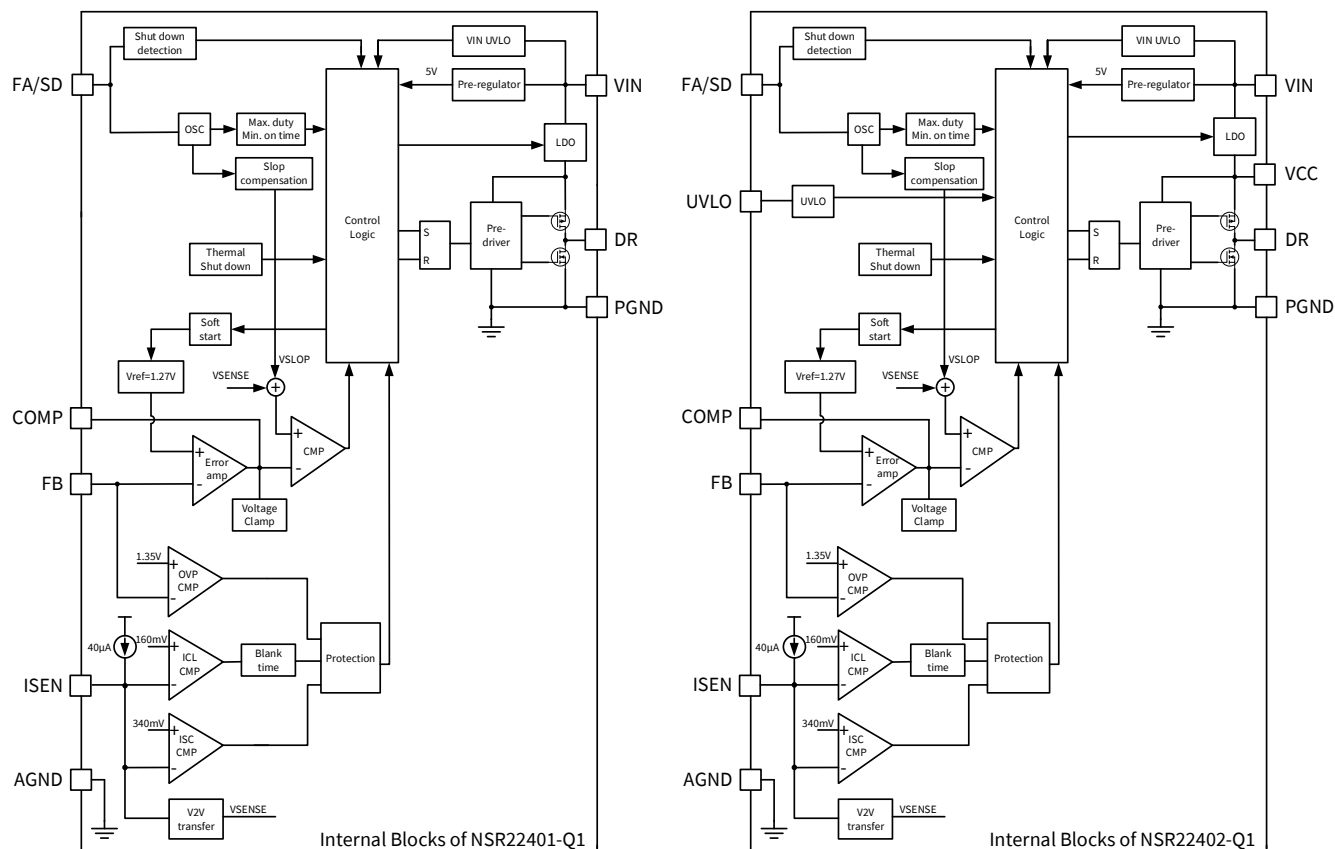


Figure 7 Block Diagram

7.3. Feature Description

7.3.1. Supply Voltage

The NSR22401-Q1 and NSR22402-Q1 have a recommended input voltage up to 40V. When in low-voltage condition, the device integrates an under-voltage lock-out function to shut down the device when the input voltage falls below an internal threshold ($V_{IN_UVLO_F}$). This function ensures a proper supply voltage for internal circuits. There is also a lock-out threshold hysteresis ($V_{IN_UVLO_HYS}$) during under-voltage shutdown and re-start to avoid noise trigger for a well-designed system.

7.3.2. Quiescent Current

When pull FA/SD pin high the device enters shutdown mode, VIN pin draws a low current (I_{SHDN}) with the result that power consumption is low in device. When the device is out of shutdown, VIN pin draws a higher current as internal circuits start to work without switching on driver output. Under light-load condition, the supply current is higher as internal driver works to charge and discharge external MOSFETs. Total VIN current is the sum of quiescent current and the average DR output current. Knowing the operating frequency and the MOSFET gate charge (Qg), average output current can be calculated from below equation:

$$I_{DR} = Q_g \times f_{SW} \quad (1)$$

7.3.3. Frequency Timing

7.3.3.1. Minimum On-time and Maximum Duty

In typical peak-current mode control, on-time period is terminated when ISEN pin voltage is higher than a certain voltage determined by close loop. To avoid any false triggering caused by spikes when turn-on transient, a blanking time is built which actually blocks the turn-off signal when normal operation. As a result, this blanking time behaviors as a minimum on-time (t_{ON_MIN}) function. During minimum on-time, cycle-by-cycle current limit is disabled while short circuit protection works which protects power converter from a serious over-load or short-to-ground conditions.

The NSR22401 and NSR22402 have a maximum duty (D_{MAX}) restriction in case short current happens in power MOSFET which may cause damage when start-up.

7.3.3.2. Switching Frequency Setting

The switching frequency can be set by a resistor connecting from FA/SD pin to GND with a typical range from 70kHz to 475kHz.

In additional, for NSR22401, the below equation can be used to get the resistor:

$$R_{FA} = \frac{18 \times 10^3}{f_{SW}} - 4.5 \quad (2)$$

For NSR22402, refer to below equation:

$$R_{FA} = \frac{22 \times 10^3}{f_{SW}} - 5.6 \quad (3)$$

In both above equations, f_{sw} is in kHz and R_{FA} in k Ω .

7.3.3.3. Soft Start

When the device is powered, internal reference voltage is started from 0V. After a soft-start time (t_{ss}) internal reference reaches feedback reference voltage (V_{REF}) and then internal reference voltage is switched to feedback reference voltage as soft start is finished.

7.3.3.4. Slope Compensation

In peak current mode control, when duty cycle is higher than 50%, an internal slope compensation is needed to avoid sub-harmonic oscillation. NSR22401 and NSR22402 have a cycle-by-cycle slope ramp integration which has a fixed voltage (V_{SL}) when each cycle ends. As frequency goes higher the compensation slope goes higher following below equation:

$$S_a = V_{SL} \times f_{SW} \quad (4)$$

7.3.4. UVLO and Shutdown

For NSR22401 and NSR22402, FA/SD pin also offers shutdown function for low current assumption application. When voltage applied on this pin is higher than shutdown threshold (V_{SD_H}), device entries into shutdown mode.

For NSR22402, an under-voltage lock-out function is integrated with a UVLO pin. Different from shutdown threshold, when voltage applied on this pin is lower than UVLO input low voltage (V_{UVLO_F}) device entries into under-voltage lock-out mode.

7.3.5. Current Sense

Cycle-by-cycle current limit is built to limit inductor and MOSFET current when normal work. As out of blanking time, the driver output is off once the voltage on ISEN pin is higher than current limit threshold voltage (V_{CL}). When next cycle comes driver regularly outputs high and current limit continues working.

For serious heavy load and short-to-ground condition, a higher threshold (V_{SC}) is integrated to protect from large current in-rush even within blanking time. When V_{SC} is triggered continuously in 7 cycles, working frequency will scale down by 7 for a lower free-wheeling current and power loss.

7.3.6. Error Amplifier

The device has a transconductance error amplifier from FB pin to COMP pin while transconductance specifications of NSR22401 and NSR22402 are different. Refer to block diagrams to get the internal connections for slope compensation, current sense and error amplifier.

7.3.7. Driver Output

Peak output current capability of NSR22401 and NSR22402 is up to 1A. The internal driver resistance for both high-side and low-side is low to offer a quick transition for external MOSFET which helps with lower switching power loss. When input voltage of device is below 7.2V (typical), the high voltage driver output follows input. When input voltage is higher than 7.2V (typical), driver output keeps a constant 7.2V (typical) as high.

7.3.8. Over-voltage Protection

When voltage on FB pin is higher than reference voltage (V_{REF}) plus over-voltage protection threshold (V_{OVP}), driver output is off. There is a hysteresis voltage (V_{OVP_HYS}) for recovery from over-voltage condition.

7.3.9. Thermal Shutdown

The device is protected from junction temperature higher than thermal shutdown threshold (T_{SD}). When the junction temperature falls below the thermal shutdown trigger point minus the hysteresis (T_{SD_HYS}), the output turns on again.

8. Typical Application

NSR22401 and NSR22402 are designed for boost, flyback and other switching DC-DC topologies suitable for peak current mode control with low-side switches.

8.1. Boost Converter

8.1.1. Typical Circuits

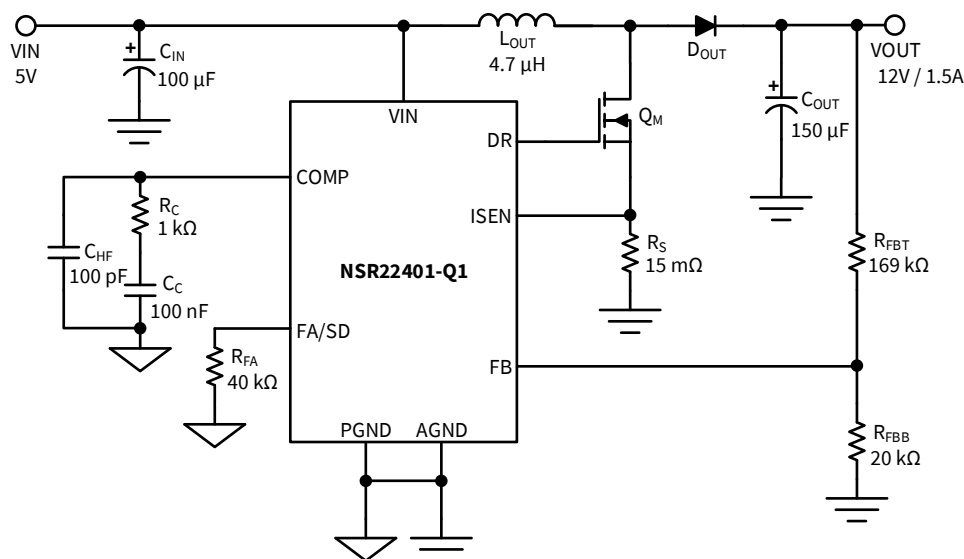


Figure 8 Typical Boost Converter Connection with NSR22401-Q1

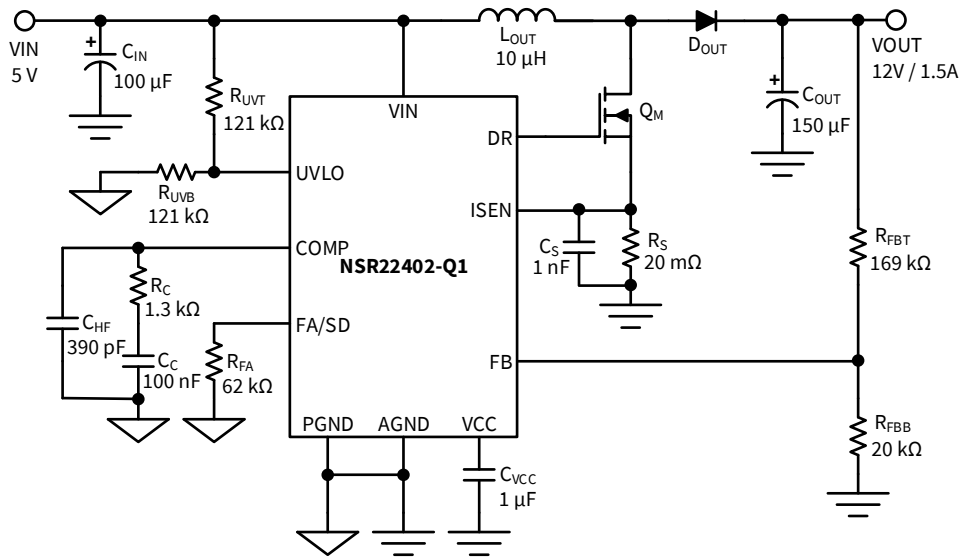


Figure 9 Typical Boost Converter Connection with NSR22402-Q1

8.1.2. Loop Stability Analysis and Design

A Boost converter is a typical closed-loop control system which can be described as below flow chart:

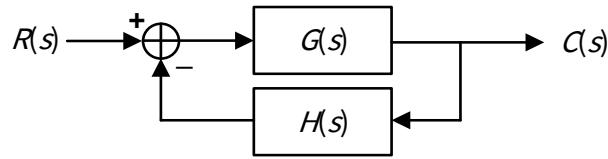


Figure 10 Closed-loop Control Flow Chart

Where $G(s)$ can be considered as the transfer function of power stage while $H(s)$ is the compensation section. As loop stability performance of small signal is directly determined by closed-loop transfer function expressed as below:

$$G_{CLOSED}(s) = \frac{G(s)}{1 + G(s)H(s)} \quad (5)$$

The most straightforward method to check response caused by certain distributing is calculation with closed-loop transfer function from s-domain to time-domain. Frequency stability criterion is a more simple way which is equivalent to Nyquist stability criterion. The frequency stability criterion checks gain and phase curves versus frequency, which is commonly called Bode plot of open-loop transfer function

$$G_{OPEN}(s) = G(s)H(s) \quad (6)$$

8.1.2.1. Transfer Function and Pole-zero Location of Power Stage

In a Boost converter with peak-current-mode control and an operational transconductance amplifier (OTA) as major control component, power stage transfer function can be derived as below:

$$G(s) = A_{VC} \frac{\left(1 - \frac{s}{\omega_R}\right) \cdot \left(1 + \frac{s}{\omega_{ESR}}\right)}{\left(1 + \frac{s}{\omega_P}\right) \cdot \left(1 + \frac{s}{Q_N \cdot \omega_N} + \frac{s^2}{\omega_N^2}\right)} \quad (7)$$

Where:

$$A_{VC} = \frac{R_{LOAD}}{R_S \cdot \left[2 \frac{V_{OUT}}{V_{IN}} + \frac{R_{LOAD} \cdot V_{IN}^2}{f_{SW} \cdot L_{OUT} \cdot V_{OUT}^2} \cdot \left(0.5 + \frac{S_A}{S_N} \right) \right]} \quad (8)$$

S_A is voltage slope of internal compensation:

$$S_A = V_{SL} \cdot f_{SW} \quad (9)$$

S_N is voltage slope between current sense resistor when inductor current rises:

$$S_N = R_S \frac{V_{IN}}{L_{OUT}} \quad (10)$$

The angular frequency of pole from main power is:

$$\omega_P = \frac{\frac{2}{R_{LOAD}} + \frac{V_{IN}^3}{f_{SW} \cdot L_{OUT} \cdot V_{OUT}^3} \left(1 + \frac{S_A}{S_N} \right)}{C_{OUT}} \quad (11)$$

In a closed current-loop power stage transfer function, there is a pair of complex-conjugate pole at half the switching frequency with the below Q_N values:

$$\omega_N = \pi \cdot f_{SW} \quad (12)$$

$$Q_N = \frac{1}{\left[\pi \cdot (1 - Duty) \cdot \left(1 + \frac{S_A}{S_N} \right) - 0.5 \right]} \quad (13)$$

When output capacitor has a equivalent series resistance (ESR), there is a zero lays at below angular frequency:

$$\omega_{ESR} = \frac{1}{C_{OUT} \cdot R_{ESR}} \quad (14)$$

There is also a right half plane zero (RHPZ) in a current-loop Boost:

$$\omega_R = \frac{R_{LOAD} \cdot (1 - Duty)^2}{L_{OUT}} \quad (15)$$

8.1.2.2. Transfer Function and Pole-zero Location of Compensation Stage

For transfer function of compensation section it can be expressed when $C_C \gg C_{HF}$ and output resistance of amplifier $\gg R_C$:

$$H(s) = \frac{R_{FBB} \cdot G_{EA} \cdot R_{EAO}}{R_{FBB} + R_{FBT}} \cdot \frac{1 + \frac{s}{\omega_{COMPZ}}}{\left(1 + \frac{s}{\omega_{COMP1}} \right) \cdot \left(1 + \frac{s}{\omega_{COMP2}} \right)} \quad (16)$$

Where:

$$\omega_{COMPZ} = \frac{1}{R_C \cdot C_C} \quad (17)$$

$$\omega_{COMP1} = \frac{1}{R_{EAO} \cdot C_C} \quad (18)$$

$$\omega_{COMP2} = \frac{1}{R_C \cdot C_{HF}} \quad (19)$$

8.1.2.3. Loop Stability Analysis

From above equations, any change of some components could cause significant changes to loop stability. In a typically designed boost converter, when component changed, influential changes on loop stability is summary in below table:

Component Changes	Influence on Transfer Function	Typical Influence on Bode Plot
Increase L_{OUT}	Lower ω_P	Lower phase margin
Increase C_{OUT}	Lower ω_P	Lower bandwidth
Increase ESR of C_{OUT}	Lower ω_{ESR}	Earlier boost on phase at high frequency
Increase R_S	Lower A_{VC}	Lower bandwidth
Increase R_C	Lower ω_{COMP2} Lower ω_{COMP2}	Earlier boost on gain and phase at low frequency Earlier drop on gain and phase at high frequency
Increase C_C	Lower ω_{COMP2} Lower ω_{COMP1}	Earlier boost on gain and phase at low frequency Earlier drop on gain and phase at medium frequency
Increase C_{HF}	Lower ω_{COMP2}	Earlier drop on gain and phase at high frequency

8.2. Flyback Converter

8.2.1. Typical Circuits

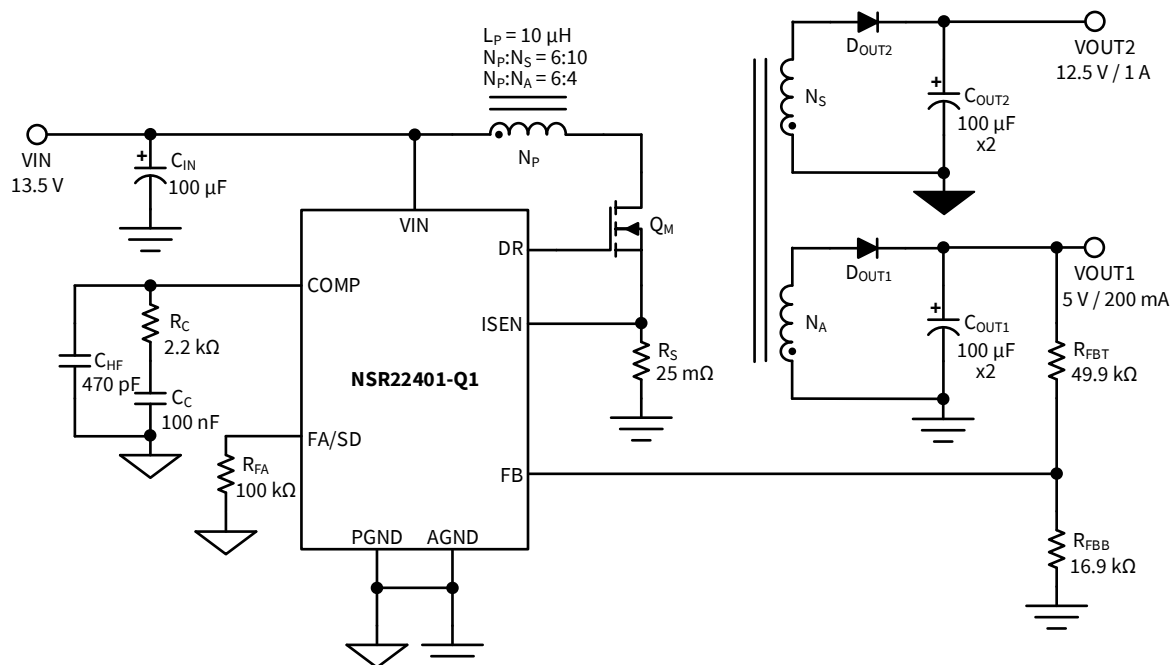


Figure 11 Typical Flyback Converter Connection with NSR22401-Q1

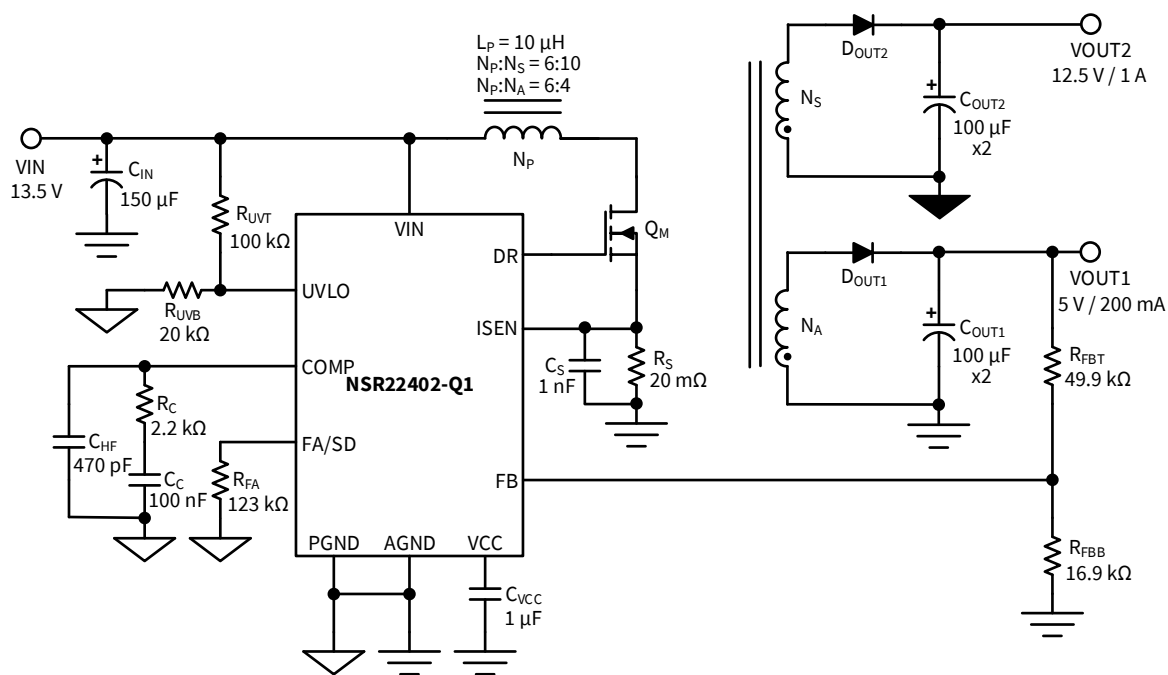


Figure 12 Typical Flyback Converter Connection with NSR22402-Q1

8.2.2. Loop Stability Analysis and Design

8.2.2.1. Transfer Function and Pole-zero Location of Power Stage

In a CCM Flyback converter with peak-current-mode control and an operational transconductance amplifier (OTA) as major control component, when feedback signal come from resistance divider of auxiliary winding output which share common ground with primary winding, the power stage transfer function can be derived as below:

$$G(s) = A_{VC} \frac{\left(1 - \frac{s}{\omega_R}\right) \cdot \left(1 + \frac{s}{\omega_{ESR}}\right)}{\left(1 + \frac{s}{\omega_P}\right) \cdot \left(1 + \frac{s}{\omega_L}\right)} \quad (20)$$

Where:

$$A_{VC} = \frac{N_P \cdot R_{LOAD}}{N_S \cdot R_S} \cdot \frac{1}{\frac{(1-Duty)^2}{t_L} \cdot \left(1 + 2 \frac{S_A}{S_N}\right) + 2M_R + 1} \quad (21)$$

t_L is a time constant determined by power stage components and working condition:

$$t_L = \frac{2N_S^2 \cdot L_{PRI} \cdot f_{SW}}{N_P^2 \cdot R_{LOAD}} \quad (22)$$

M_R is voltage transition ratio from primary input voltage to secondary output voltage:

$$M_R = \frac{N_P \cdot V_{OUT}}{N_S \cdot V_{IN}} \quad (23)$$

S_A is voltage slope of internal compensation:

$$S_A = V_{SL} \cdot f_{SW} \quad (24)$$

S_N is voltage slope between current sense resistor when MOSFET is ON and primary current rises:

$$S_N = R_S \frac{V_{IN}}{L_{PRI}} \quad (25)$$

The angular frequency of pole from main power is:

$$\omega_P = \frac{\frac{(1-Duty)^3}{t_L} \cdot \left(1 + 2 \frac{S_A}{S_N}\right) + Duty + 1}{R_{LOAD} \cdot C_{OUT}} \quad (26)$$

In a CCM Flyback converter with PCM control, there is a high-frequency pole from primary inductance and slop compensation:

$$\omega_L = \frac{\left(V_{IN} + \frac{N_P}{N_S} \cdot V_{OUT}\right) \cdot R_S \cdot f_{SW}}{S_A \cdot L_{PRI}} \quad (27)$$

When output capacitor has a equivalent series resistance (ESR), there is a zero lays at below angular frequency:

$$\omega_{ESR} = \frac{1}{C_{OUT} \cdot R_{ESR}} \quad (28)$$

There is also a right half plane zero (RHPZ) in a current-loop Flyback:

$$\omega_R = \frac{R_{LOAD} \cdot (1 - Duty)^2 \cdot N_p^2}{Duty \cdot L_{PRI} \cdot N_s^2} \quad (29)$$

8.2.2.2. Transfer Function and Pole-zero Location of Compensation Stage

For transfer function of compensation section it can be expressed when $C_C \gg C_{HF}$ and output resistance of amplifier $\gg R_C$:

$$H(s) = \frac{R_{FBB} \cdot G_{EA} \cdot R_{EAO}}{R_{FBB} + R_{FBT}} \cdot \frac{1 + \frac{s}{\omega_{COMPZ}}}{\left(1 + \frac{s}{\omega_{COMPP1}}\right) \cdot \left(1 + \frac{s}{\omega_{COMPP2}}\right)} \quad (30)$$

Where:

$$\omega_{COMPZ} = \frac{1}{R_C \cdot C_C} \quad (31)$$

$$\omega_{COMPP1} = \frac{1}{R_{EAO} \cdot C_C} \quad (32)$$

$$\omega_{COMPP2} = \frac{1}{R_C \cdot C_{HF}} \quad (33)$$

8.2.2.3. Loop Stability Analysis

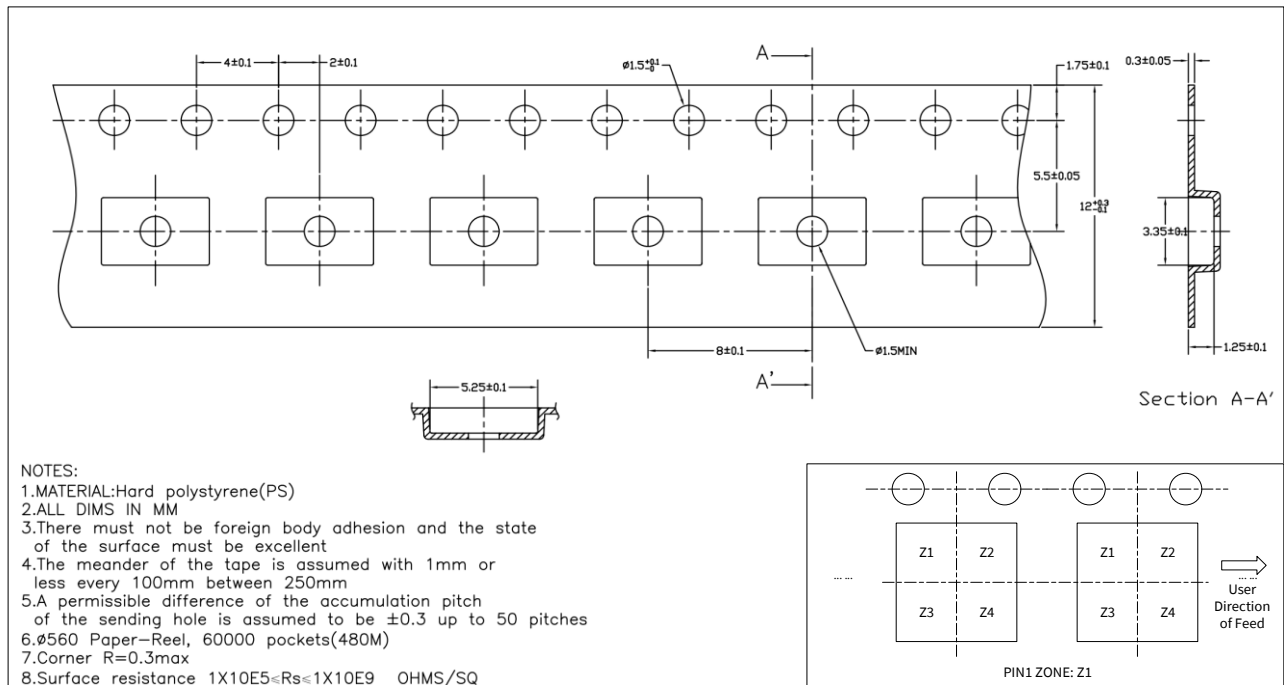
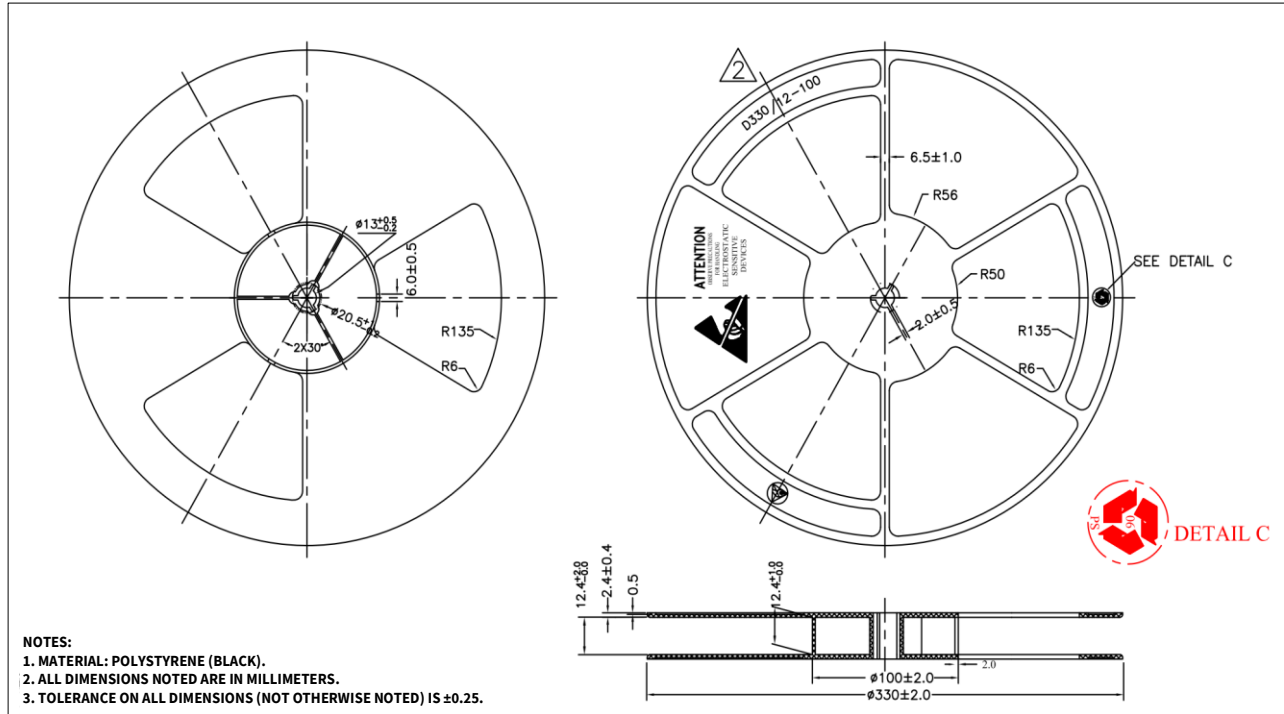
From above equations, any change of some components could cause significant changes to loop stability. In a typically designed CCM flyback converter, when component changed, influential changes on loop stability is summary in below table:

Component Changes	Influence on Transfer Function	Typical Influence on Bode Plot
Increase L_{PRI}	Lower ω_P , Lower ω_L	Lower phase margin
Increase C_{OUT}	Lower ω_P	Lower bandwidth
Increase ESR of C_{OUT}	Lower ω_{ESR}	Earlier boost on phase at high frequency
Increase R_s	Lower A_{VC}	Lower bandwidth
Increase R_C	Lower ω_{COMPZ} Lower ω_{COMPP2}	Earlier boost on gain and phase at low frequency Earlier drop on gain and phase at high frequency
Increase C_C	Lower ω_{COMPZ} Lower ω_{COMPP1}	Earlier boost on gain and phase at low frequency Earlier drop on gain and phase at medium frequency
Increase C_{HF}	Lower ω_{COMPP2}	Earlier drop on gain and phase at high frequency

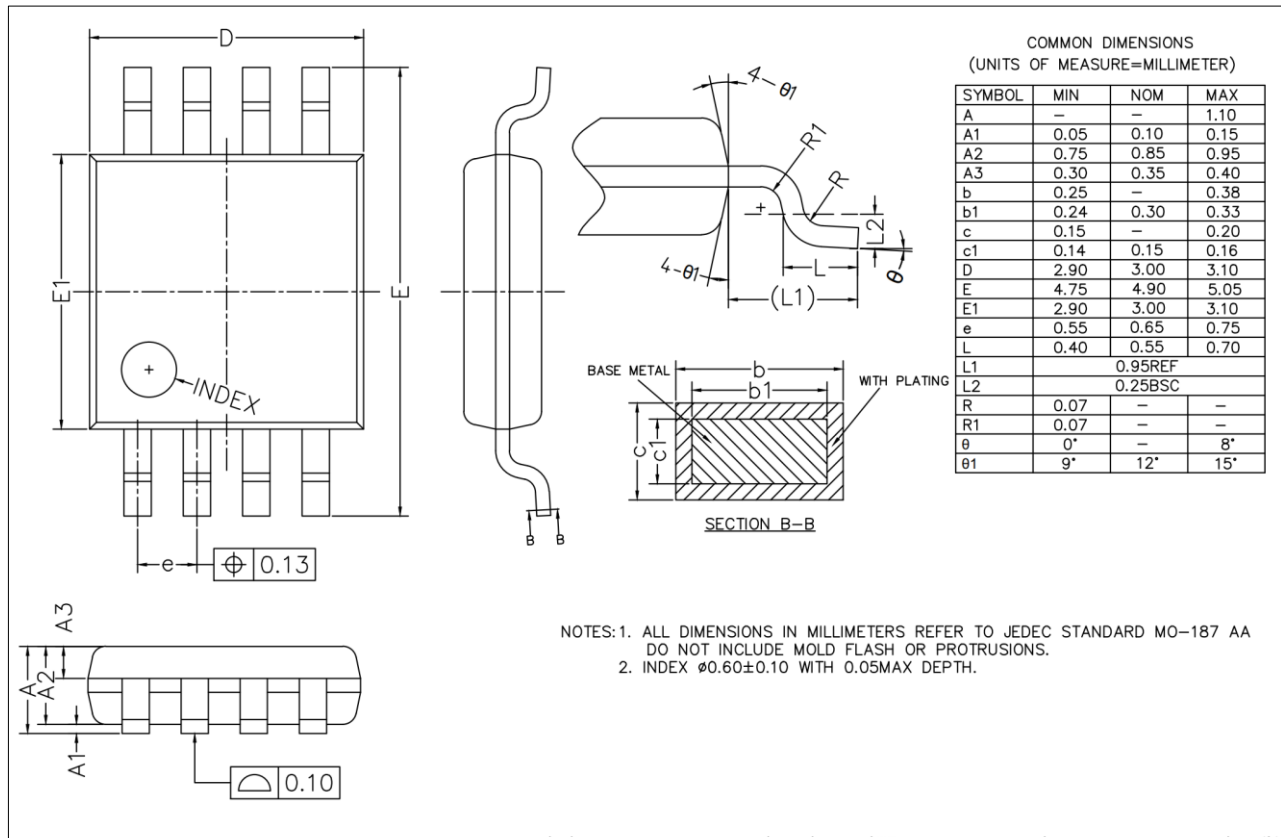
9. Package Information

9.1. MSOP8

9.1.1. Tape and Reel

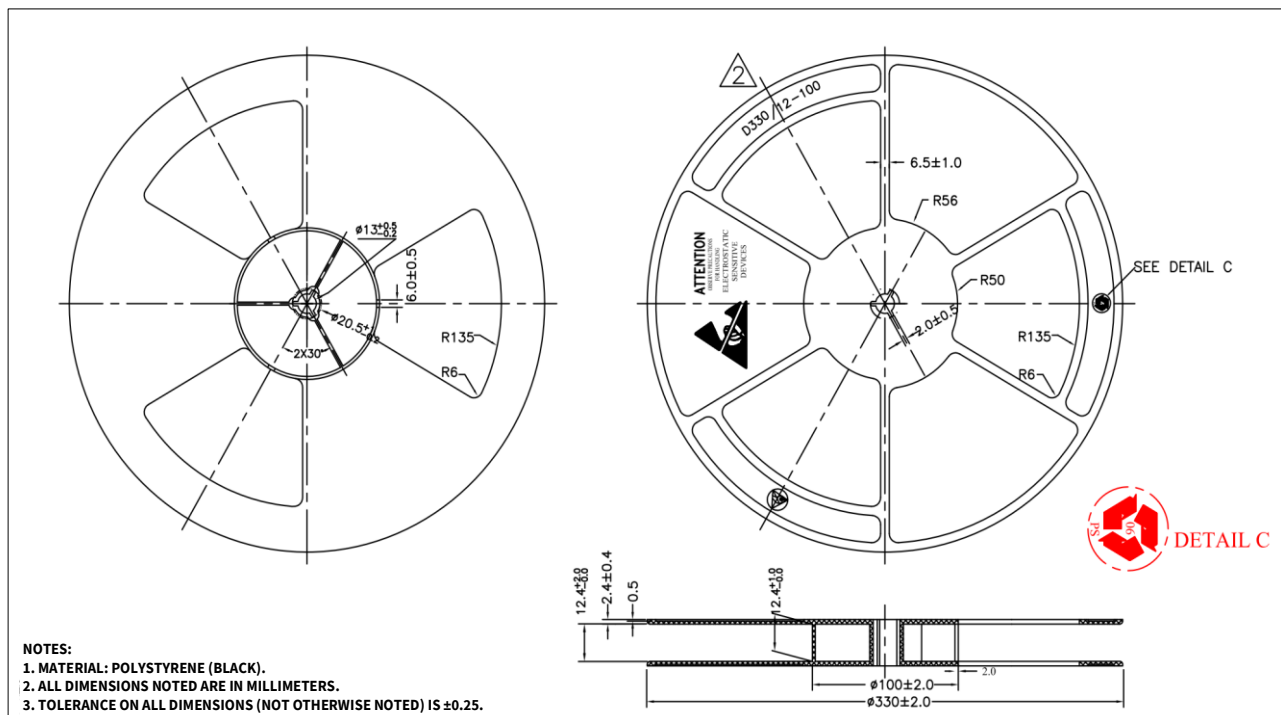


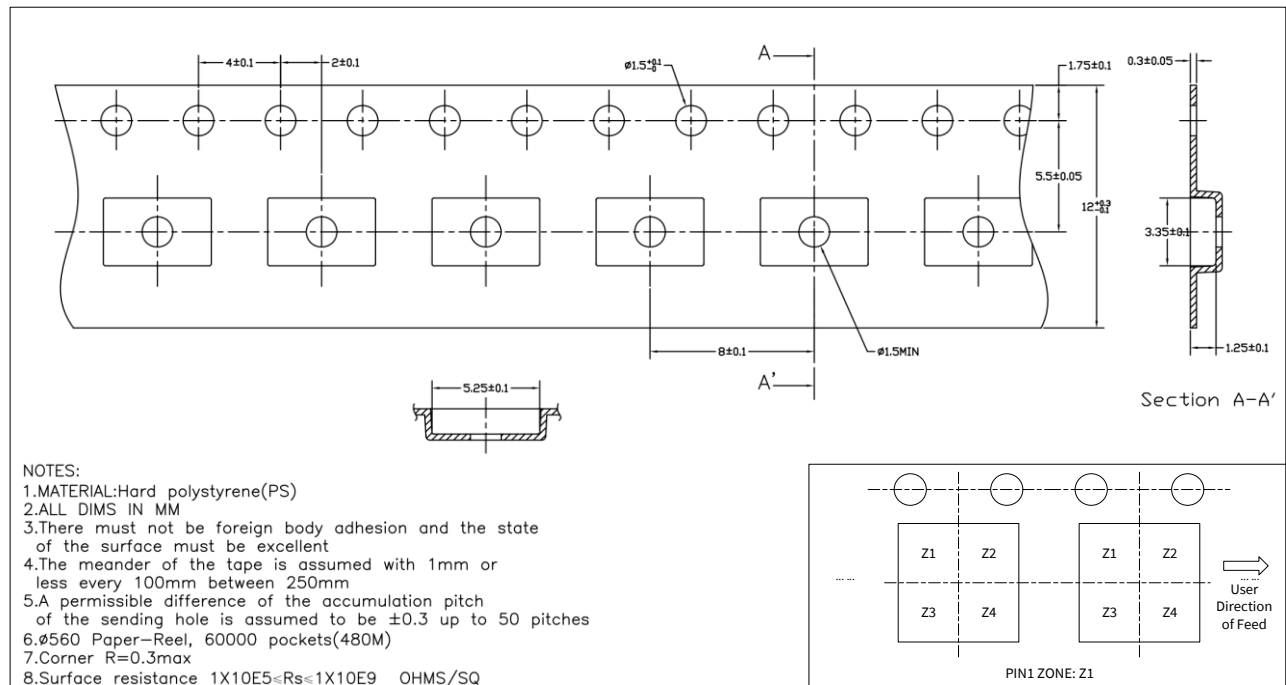
9.1.2. Mechanical Data



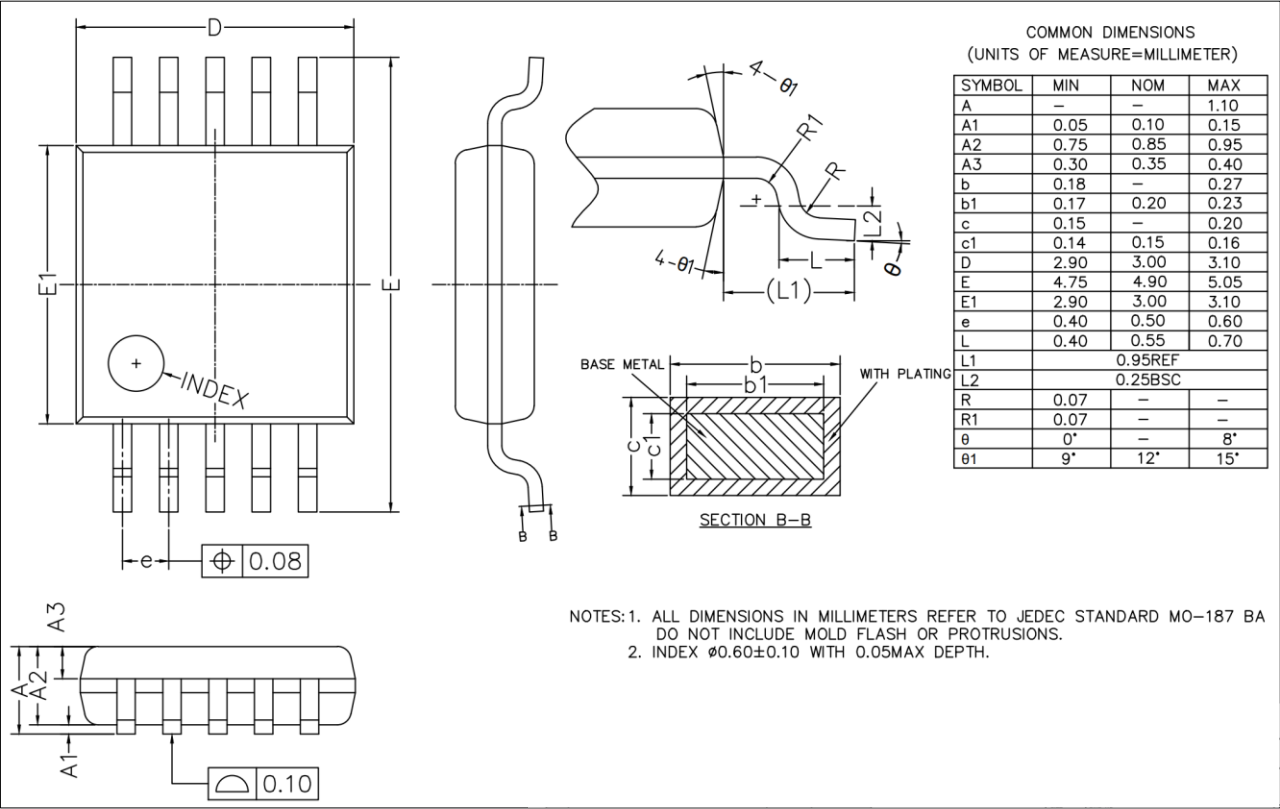
9.2. MSOP10

9.2.1. Tape and Reel





9.2.2. Mechanical Data



10. Order Information

Orderable Part Number	MSL	Package	SPQ	Marking
NSR22401-Q1MSR	1	MSOP8	2500	F401
NSR22402-Q1MSJR	1	MSOP10	2500	F402

11. Revision History

Revision	Description	Date
1.0	Initial version	2024/06
1.1	Update format, delete description “the device is also optimized for EMC performance with internal spread-spectrum”, add title for typical circuits at page1, revise name to NSR22402-Q1 in EC table error amplifier section at page6	2025/11

IMPORTANT NOTICE

The information given in this document (the “Document”) shall in no event be regarded as any warranty or authorization of, express or implied, including but not limited to accuracy, completeness, merchantability, fitness for a particular purpose or infringement of any third party’s intellectual property rights.

Users of this Document shall be solely responsible for the use of NOVOSENSE’s products and applications, and for the safety thereof. Users shall comply with all laws, regulations and requirements related to NOVOSENSE’s products and applications, although information or support related to any application may still be provided by NOVOSENSE.

This Document is provided on an “AS IS” basis, and is intended only for skilled developers designing with NOVOSENSE’s products. NOVOSENSE reserves the rights to make corrections, modifications, enhancements, improvements or other changes to the products and services provided without notice. NOVOSENSE authorizes users to use this Document exclusively for the development of relevant applications or systems designed to integrate NOVOSENSE’s products. No license to any intellectual property rights of NOVOSENSE is granted by implication or otherwise. Using this Document for any other purpose, or any unauthorized reproduction or display of this Document is strictly prohibited. In no event shall NOVOSENSE be liable for any claims, damages, costs, losses or liabilities arising out of or in connection with this Document or the use of this Document.

For further information on applications, products and technologies, please contact NOVOSENSE (www.novosns.com).

Suzhou NOVOSENSE Microelectronics Co., Ltd