NOVOSENSE

NSIP984x

Quad-Channel Digital Isolators with Integrated DC to DC Converter

Datasheet (EN) 1.0

Product Overview

The NSIP984x devices are quad-channel digital isolators with integrated isolated DC-DC converter. The isolated DC-DC converter provides up to 500mW output power using on chip transformer. The feedback PWM signal is sent to primary side by a digital isolator based on Novosense capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The NSIP984x devices are safety certified by UL1577, supporting 5.0kVrms withstand voltage while providing high electromagnetic immunity and low emissions. The data rate of the NSIP984x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 100kV/us. The NSIP984x devices provide 5V to 5V, 5V to 3.3V, 3.3V to 3.3V conversion mode, the output voltage can be set by SEL pin.

Key Features

- Emission optimized to meet CISPR 32 and EN 55032 Class B with >5 dB margin on 2 layers board
- Up to 5000Vrms Insulation voltage
- Power supply voltage:

  V_{DD}: 3V to 5.25V V_{DDL}: 1.8V to 5.5V
- 5V to 5V, 5V to 3.3V, support 100mA load current
- 3.3V to 3.3V, support 60mA load current
- Over current and over temperature protection
- Data rate: DC to 150Mbps
- High CMTI: 100kV/us Typ
- High system level EMC performance:

  Enhanced system level ESD, EFT, Surge immunity
- Operation temperature: -40℃~125℃
- RoHS-compliant packages: SOW16

Safety Regulatory Approvals

- UL recognition: up to 5000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN VDE V 0884-17

Applications

- Solar inverter & Energy storage
- EV charging piles
- Grid infrastructure & smart meter
- Heat pump
- Medical & Measurement

Device Information

Part Number	*Package*	*Body Size*
NSIP984x-DSWR	SOW16	10.30mm × 7.50mm

Functional Block Diagrams

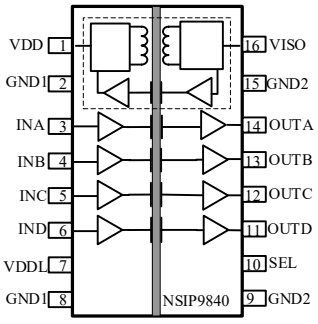

Figure 1. NSIP984x Block Diagram[1]

[1] The isolation channel direction can be either depend on different part number.

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1. Pin Configuration And Functions

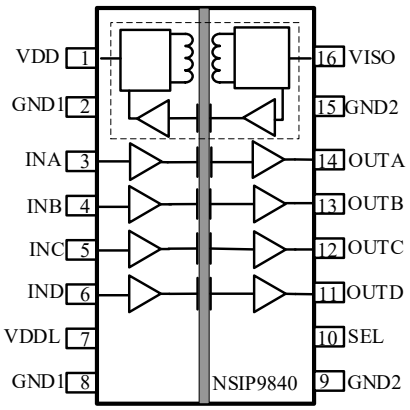


Figure 1.1 NSIP9840 Package

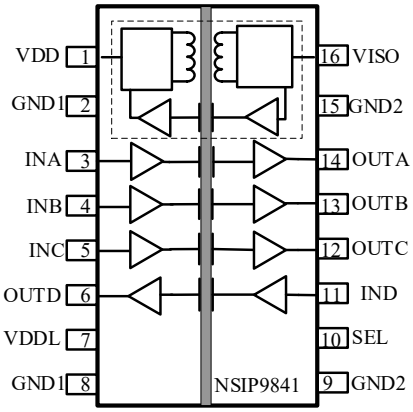


Figure 1.2 NSIP9841 Package

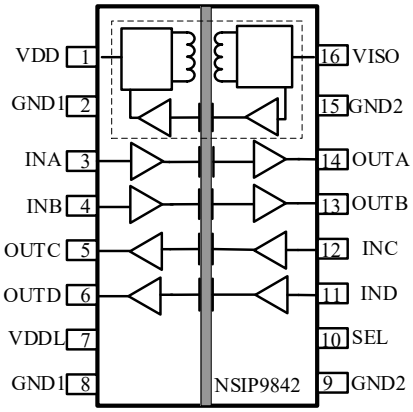


Figure 1.3 NSIP9842 Package

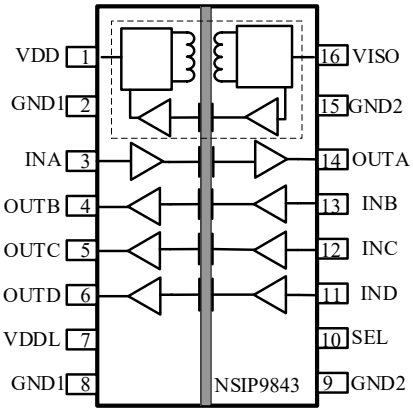


Figure 1.4 NSIP9843 Package

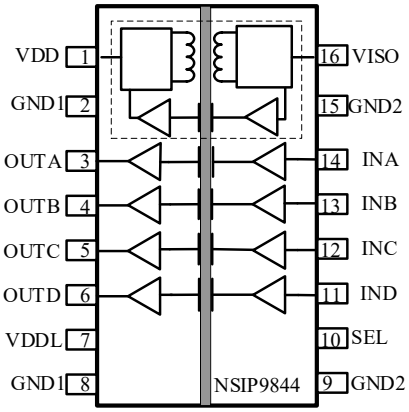


Figure 1.5 NSIP9844 Package

Table1.1 NSIP9840/ NSIP9841/ NSIP9842/ NSIP9843/NSIP9844 Pin Configuration and Description

NSIP9840 PIN NO.	NSIP9841 PIN NO.	NSIP9842 PIN NO.	NSIP9843 PIN NO.	NSIP9844 PIN NO.	SYMBOL	FUNCTION
1	1	1	1	1	VDD	Primary Supply Voltage.
2	2	2	2	2	GND1	Ground 1. Ground reference for Isolator Side primary. Pin 2 and Pin 8 are not internally connected. It is required that pin2 and pin8 be connected to a common ground.
3	3	3	3	14	INA	Logic Input A.
4	4	4	13	13	INB	Logic Input B.
5	5	12	12	12	INC	Logic Input C.
6	11	11	11	11	IND	Logic Input D.
7	7	7	7	7	VDDL	Side1 I/O logic level. When VDDL is not powered, the chip will shut down
8	8	8	8	8	GND1	Ground 1. Ground reference for Isolator Side primary. Pin 2 and Pin 8 are not internally connected. It is required that pin2 and pin8 be connected to a common ground.
9	9	9	9	9	GND2	Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected. It is recommended that pin9 and pin16 be connected to a common ground.
10	10	10	10	10	SEL	VISO output voltage selection. VISO=5V when SEL short to VISO, VISO=3.3V when SEL short to GND2 or floating.
11	6	6	6	6	OUTD	Logic Output D.
12	12	5	5	5	OUTC	Logic Output C.
13	13	13	4	4	OUTB	Logic Output B.
14	14	14	14	3	OUTA	Logic Output A.
15	15	15	15	15	GND2	Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected. It is recommended that pin9 and pin16 be connected to a common ground.
16	16	16	16	16	VISO	Secondary Supply Voltage Output for External Loads.

2. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage[2]	V_{DD}, V_{ISO}	-0.5		6	V	
Side1 I/O logic level[2]	V_{DDL}	-0.5		6	V	
Voltage at INx, OUTx, SEL pins[2]	V_{INA}, V_{INB} V_{INC}, V_{IND}, V_{OUTA}, V_{OUTB} V_{OUTC}, V_{OUTD} V_{SEL}	-0.5		V_{DDL}+0.5 V_{ISO}+0.5[3]	V	
Logic output current	Io	-15		15	mA	
Junction Temperature	T_J	-40		150	°C	
Storage Temperature	T_{stg}	-40		150	°C	

[1]Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2]All voltage values are with respect to the local ground pin (GND1 or GND2) and are peak voltage values.

[3]This value depends on whether the pin is located on the VDDL or VISO side. The maximum voltage at the I/O pins should not exceed 6 V.

3. ESD Ratings

Ratings		Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD	±8.0	kV
	Charged device model (CDM), per AEC-Q100-011-RevB	±2.0	kV

4. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit
Power Supply Voltage	V_{DD} @ V_{SEL} = 0V/Floating	3		5.25	V
	V_{DD} @ V_{SEL} = V_{ISO}	4.5		5.25	V
Side1 I/O logic level	V_{DDL}	1.8		5.5	V
High level output current	I_{OH} @ V_{DO}[1] = 5V	-4			mA
	I_{OH} @ V_{DO}[1] = 3.3V	-2			mA
Low level output current	I_{OL} @ V_{DO}[1] = 5V			4	mA

Parameters	Symbol	min	typ	max	unit
	I_{OL} @ V_{DO}[1] = 3.3V			2	mA
High Level Input Voltage	V_{IH}	0.7* V_{DI}[1]		V_{DI}[1]	V
Low Level Input Voltage	V_{IL}	0		0.3*V_{DI}[1]	V
Data rate	DR			150	Mbps
Ambient temperature	T_a	-40		125	°C

[1]V_{DI} is the input side supply, V_{DO} is the output side supply. This value depends on whether the pin is located on the VDDL or VISO side.

5. Thermal Characteristics

Parameters	Symbol	SOW16	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	59.2	°C/W
Junction-to-case (top) thermal resistance	ψ_{JT}	8.7	°C/W
Junction-to-board thermal resistance	ψ_{JB}	23	°C/W

6. Specifications

6.1. Isolated DC/DC Converter Static Specifications

(V_{DD}=4.5V~5.25V, V_{DDL}=1.8V~ 5.5V, SEL=V_{ISO}, T_a=-40°C to 125°C. Unless otherwise noted, Typical values are at V_{DD} = V_{DDL} = 5V, T_a = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Isolated Supply Voltage	V_{ISO}	4.6	5	5.25	V	I_{ISO} = 0 to 100mA
Positive-going UVLO threshold on V_{DD}	$V_{DD+(UVLO)}$		2.7	3	V	
Negative-going UVLO threshold on V_{DD}	$V_{DD-(UVLO)}$	2.1	2.5		V	
UVLO threshold hysteresis on V_{DD}	$V_{HYS(UVLO)}$		0.2		V	
Line Regulation	$V_{ISO(LINE)}$		2		mV/V	I_{ISO} = 50mA, VDD= 4.5V to 5.25V
Load Regulation	$V_{ISO(LOAD)}$		0.5		%	I_{ISO}= 10 to 90mA
Output Ripple	$V_{ISO(RIP)}$		70		mVpp	20MHz bandwidth, C_{LOAD} = 0.1 µF || 10 µF, I_{ISO} = 100 mA
Efficiency at maximum load current	EFF		49		%	I_{ISO} = 100mA, C_{LOAD} = 0.1µF|| 10µF
Current available to isolated supply	I_{ISO}	100			mA	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
VDD supply current without digital isolator	I_{VDD_POWER}		36	60	mA	No VISO Load
			200	265	mA	I_{ISO}=100mA

(V_{DD}=4.5V~5.25V, V_{DDL}=1.8V~ 5.5V, SEL=0V, T_a=-40°C to 125°C. Unless otherwise noted, Typical values are at V_{DD} = V_{DDL} = 5V, T_a = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Isolated Supply Voltage	V_{ISO}	3	3.3	3.5	V	I_{ISO} = 0 to 100mA
Positive-going UVLO threshold on V_{DD}	$V_{DD+(UVLO)}$		2.7	3	V	
Negative-going UVLO threshold on V_{DD}	$V_{DD-(UVLO)}$	2.1	2.5		V	
UVLO threshold hysteresis on V_{DD}	$V_{HYS(UVLO)}$		0.2		V	
Line Regulation	$V_{ISO(LINE)}$		2		mV/V	I_{ISO} = 50mA, VDD= 4.5V to 5.25V
Load Regulation	$V_{ISO(LOAD)}$		0.5		%	I_{ISO}= 10 to 90mA
Output Ripple	$V_{ISO(RIP)}$		70		mVpp	20MHz bandwidth, C_{LOAD} = 0.1 μF || 10 μF, I_{ISO} = 100 mA
Efficiency at maximum load current	EFF		40		%	I_{ISO} = 100mA, C_{LOAD} = 0.1μF|| 10μF
Current available to isolated supply	I_{ISO}	100			mA	
VDD supply current without digital isolator	I_{VDD_POWER}		32	55	mA	No VISO Load
			165	230	mA	I_{ISO}=100mA

(V_{DD}=3V~3.6V, V_{DDL}=1.8V~ 5.5V, SEL=0V, T_a=-40°C to 125°C. Unless otherwise noted, Typical values are at V_{DD} = V_{DDL} = 3.3V, T_a = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Isolated Supply Voltage	V_{ISO}	3	3.3	3.5	V	I_{ISO} = 0 to 60mA
Positive-going UVLO threshold on V_{DD}	$V_{DD+(UVLO)}$		2.7	3	V	
Negative-going UVLO threshold on V_{DD}	$V_{DD-(UVLO)}$	2.1	2.5		V	
UVLO threshold hysteresis on V_{DD}	$V_{HYS(UVLO)}$		0.2		V	
Line Regulation	$V_{ISO(LINE)}$		3		mV/V	I_{ISO} = 30mA, VDD= 3V to 3.6V
Load Regulation	$V_{ISO(LOAD)}$		1		%	I_{ISO}= 10 to 54mA

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Output Ripple	$V_{ISO(RIP)}$		45		mVpp	20MHz bandwidth, C_{LOAD} = 0.1 µF || 10 µF, I_{ISO} = 60 mA
Efficiency at maximum load current	EFF		48		%	I_{ISO} = 60mA, C_{LOAD} = 0.1µF|| 10µF
Current available to isolated supply	I_{ISO}	60			mA	
VDD supply current without digital isolator	I_{VDD_POWER}		35	60	mA	No VISO Load
			131	170	mA	I_{ISO}=60mA

6.2. Digital Isolator Electrical Characteristics

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Input pin rising threshold	V_{ITH}	0.7*V_{DI}[1]			V	
Input pin falling threshold	V_{ITL}			0.3*V_{DI}[1]	V	
Input pin threshold hysteresis	$V_{I(UVLO)}$	0.1*V_{DI}[1]			V	
High level input current	I_{IH}		8	15	µA	V_I = V_{DI}[1] at INx or SEL
Low level input current	I_{IL}	-15	-8		µA	V_I = 0 at INx or SEL
High Level Output Voltage	V_{OH}	V_{DO}[1]-0.4			V	V_{DO}[1] = 5V, I_{OH} ≥- 4mA
		V_{DO}[1]-0.3			V	V_{DO}[1] = 3.3V, I_{OH} ≥- 2mA
Low Level Output Voltage	V_{OL}			0.4	V	V_{DO}[1] = 5V, I_{OL} ≤ 4mA
				0.3	V	V_{DO}[1] = 3.3V, I_{OL} ≤ 2mA
Output Impedance	R_{out}		50		ohm	
Common Mode Transient Immunity	CMTI	100	150		kV/µs	V_I = V_{DI}[1]or 0 V
Thermal Shutdown Temperature			165		°C	

[1]V_{DI} is the input side supply, V_{DO} is the output side supply. This value depends on whether the pin is located on the VDDL or VISO side.

(V_{DD}=4.5V~5.25V, V_{DDL}=1.8V~ 5.5V, SEL=V_{ISO}, T_a=-40℃ to 125°C. Unless otherwise noted, Typical values are at V_{DD} = V_{DDL} = 5V, T_a = 25°C)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply Current	NSIP9840					
	$I_{DD(Q0)}$		35		mA	All Input 0V for NSIP9840W0 or All Input at supply for NSIP9840W1
	$I_{DD(Q1)}$		38		mA	All Input at supply for NSIP9840W0 or All Input 0V for NSIP9840W1
	$I_{DD(1M)}$		35		mA	All Input with 1Mbps square wave, C_L=15pF
	$I_{DD(10M)}$		39		mA	All Input with 10Mbps square wave, C_L=15pF
	$I_{DD(100M)}$		70		mA	All Input with 100Mbps square wave, C_L=15pF
	NSIP9841					
	$I_{DD(Q0)}$		36		mA	All Input 0V for NSIP9841W0 or All Input at supply for NSIP9841W1
	$I_{DD(Q1)}$		40		mA	All Input at supply for NSIP9841W0 or All Input 0V for NSIP9841W1
	$I_{DD(1M)}$		38		mA	All Input with 1Mbps square wave, C_L=15pF
	$I_{DD(10M)}$		42		mA	All Input with 10Mbps square wave, C_L=15pF
	$I_{DD(100M)}$		74		mA	All Input with 100Mbps square wave, C_L=15pF
	NSIP9842					
	$I_{DD(Q0)}$		37		mA	All Input 0V for NSIP9842W0 or All Input at supply for NSIP9842W1
	$I_{DD(Q1)}$		42		mA	All Input at supply for NSIP9842W0 or All Input 0V for NSIP9842W1
	$I_{DD(1M)}$		41		mA	All Input with 1Mbps square wave, C_L=15pF
	$I_{DD(10M)}$		45		mA	All Input with 10Mbps square wave, C_L=15pF
	$I_{DD(100M)}$		78		mA	All Input with 100Mbps square wave, C_L=15pF

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Current	NSIP9843					
	$I_{DD(Q0)}$		38		mA	All Input 0V for NSIP9843W0 or All Input at supply for NSIP9843W1
	$I_{DD(Q1)}$		44		mA	All Input at supply for NSIP9843W0 or All Input 0V for NSIP9843W1
	$I_{DD(1M)}$		44		mA	All Input with 1Mbps square wave, C_L=15pF
	$I_{DD(10M)}$		48		mA	All Input with 10Mbps square wave, C_L=15pF
	$I_{DD(100M)}$		82		mA	All Input with 100Mbps square wave, C_L=15pF
	NSIP9844					
	$I_{DD(Q0)}$		39		mA	All Input 0V for NSIP9844W0 or All Input at supply for NSIP9844W1
	$I_{DD(Q1)}$		46		mA	All Input at supply for NSIP9844W0 or All Input 0V for NSIP9844W1
	$I_{DD(1M)}$		47		mA	All Input with 1Mbps square wave, C_L=15pF
	$I_{DD(10M)}$		51		mA	All Input with 10Mbps square wave, C_L=15pF
	$I_{DD(100M)}$		86		mA	All Input with 100Mbps square wave, C_L=15pF
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5	ns	
Propagation Delay	t_{PLH}		10	25	ns	
	t_{PHL}		10	25	ns	
Pulse Width Distortion	PWD			5	ns	$\lvert t_{PHL} - t_{PLH} \rvert$
Rising Time	t_r			5	ns	C_L = 15pF
Falling Time	t_f			5	ns	C_L = 15pF
Channel-to-Channel Delay Skew	$t_{SK(c2c)}$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK(p2p)}$			5	ns	

(V_{DD}=4.5V~5.25V, V_{DDL}=1.8V~ 5.5V, SEL=0V, T_a=-40°C to 125°C. Unless otherwise noted, Typical values are at V_{DD} = V_{DDL} = 5V, T_a = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Current	NSIP9840					
	$I_{DD(Q0)}$		32		mA	All Input 0V for NSIP9840W0 or All Input at supply for NSIP9840W1
	$I_{DD(Q1)}$		36		mA	All Input at supply for NSIP9840W0 or All Input 0V for NSIP9840W1
	$I_{DD(1M)}$		35		mA	All Input with 1Mbps square wave, C_L=15pF
	$I_{DD(10M)}$		34		mA	All Input with 10Mbps square wave, C_L=15pF
	$I_{DD(100M)}$		50		mA	All Input with 100Mbps square wave, C_L=15pF
	NSIP9841					
	$I_{DD(Q0)}$		32		mA	All Input 0V for NSIP9841W0 or All Input at supply for NSIP9841W1
	$I_{DD(Q1)}$		36		mA	All Input at supply for NSIP9841W0 or All Input 0V for NSIP9841W1
	$I_{DD(1M)}$		35		mA	All Input with 1Mbps square wave, C_L=15pF
	$I_{DD(10M)}$		36		mA	All Input with 10Mbps square wave, C_L=15pF
	$I_{DD(100M)}$		53		mA	All Input with 100Mbps square wave, C_L=15pF
	NSIP9842					
	$I_{DD(Q0)}$		32		mA	All Input 0V for NSIP9842W0 or All Input at supply for NSIP9842W1
	$I_{DD(Q1)}$		36		mA	All Input at supply for NSIP9842W0 or All Input 0V for NSIP9842W1
	$I_{DD(1M)}$		35		mA	All Input with 1Mbps square wave, C_L=15pF
	$I_{DD(10M)}$		38		mA	All Input with 10Mbps square wave, C_L=15pF
	$I_{DD(100M)}$		56		mA	All Input with 100Mbps square wave, C_L=15pF

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Current	NSIP9843					
	$I_{DD(Q0)}$		32		mA	All Input 0V for NSIP9843W0 or All Input at supply for NSIP9843W1
	$I_{DD(Q1)}$		36		mA	All Input at supply for NSIP9843W0 or All Input 0V for NSIP9843W1
	$I_{DD(1M)}$		35		mA	All Input with 1Mbps square wave, C_L=15pF
	$I_{DD(10M)}$		40		mA	All Input with 10Mbps square wave, C_L=15pF
	$I_{DD(100M)}$		59		mA	All Input with 100Mbps square wave, C_L=15pF
	NSIP9844					
	$I_{DD(Q0)}$		32		mA	All Input 0V for NSIP9844W0 or All Input at supply for NSIP9844W1
	$I_{DD(Q1)}$		36		mA	All Input at supply for NSIP9844W0 or All Input 0V for NSIP9844W1
	$I_{DD(1M)}$		35		mA	All Input with 1Mbps square wave, C_L=15pF
	$I_{DD(10M)}$		42		mA	All Input with 10Mbps square wave, C_L=15pF
	$I_{DD(100M)}$		62		mA	All Input with 100Mbps square wave, C_L=15pF
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5	ns	
Propagation Delay	t_{PLH}		10	25	ns	
	t_{PHL}		10	25	ns	
Pulse Width Distortion	PWD			5	ns	$\lvert t_{PHL} - t_{PLH} \rvert$
Rising Time	t_r			5	ns	C_L = 15pF
Falling Time	t_f			5	ns	C_L = 15pF
Channel-to-Channel Delay Skew	$t_{SK(c2c)}$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK(p2p)}$			5	ns	

(V_{DD}=3V~3.6V, V_{DDL}=1.8V~ 5.5V, SEL=0V, T_a=-40°C to 125°C. Unless otherwise noted, Typical values are at V_{DD} = V_{DDL} = 3.3V, T_a = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSIP9840					
	$I_{DD(Q0)}$		35		mA	All Input 0V for NSIP9840W0 or All Input at supply for NSIP9840W1
	$I_{DD(Q1)}$		40		mA	All Input at supply for NSIP9840W0 or All Input 0V for NSIP9840W1
	$I_{DD(1M)}$		38		mA	All Input with 1Mbps square wave, C_L=15pF
	$I_{DD(10M)}$		40		mA	All Input with 10Mbps square wave, C_L=15pF
	$I_{DD(100M)}$		55		mA	All Input with 100Mbps square wave, C_L=15pF
	NSIP9841					
	$I_{DD(Q0)}$		36		mA	All Input 0V for NSIP9841W0 or All Input at supply for NSIP9841W1
	$I_{DD(Q1)}$		41		mA	All Input at supply for NSIP9841W0 or All Input 0V for NSIP9841W1
	$I_{DD(1M)}$		39		mA	All Input with 1Mbps square wave, C_L=15pF
	$I_{DD(10M)}$		41		mA	All Input with 10Mbps square wave, C_L=15pF
	$I_{DD(100M)}$		59		mA	All Input with 100Mbps square wave, C_L=15pF
	NSIP9842					
	$I_{DD(Q0)}$		37		mA	All Input 0V for NSIP9842W0 or All Input at supply for NSIP9842W1
	$I_{DD(Q1)}$		42		mA	All Input at supply for NSIP9842W0 or All Input 0V for NSIP9842W1
	$I_{DD(1M)}$		40		mA	All Input with 1Mbps square wave, C_L=15pF
	$I_{DD(10M)}$		42		mA	All Input with 10Mbps square wave, C_L=15pF
	$I_{DD(100M)}$		63		mA	All Input with 100Mbps square wave, C_L=15pF

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Current	NSIP9843					
	$I_{DD(Q0)}$		38		mA	All Input 0V for NSIP9843W0 or All Input at supply for NSIP9843W1
	$I_{DD(Q1)}$		43		mA	All Input at supply for NSIP9843W0 or All Input 0V for NSIP9843W1
	$I_{DD(1M)}$		41		mA	All Input with 1Mbps square wave, C_L=15pF
	$I_{DD(10M)}$		43		mA	All Input with 10Mbps square wave, C_L=15pF
	$I_{DD(100M)}$		67		mA	All Input with 100Mbps square wave, C_L=15pF
	NSIP9844					
	$I_{DD(Q0)}$		39		mA	All Input 0V for NSIP9844W0 or All Input at supply for NSIP9844W1
	$I_{DD(Q1)}$		44		mA	All Input at supply for NSIP9844W0 or All Input 0V for NSIP9844W1
	$I_{DD(1M)}$		42		mA	All Input with 1Mbps square wave, C_L=15pF
	$I_{DD(10M)}$		44		mA	All Input with 10Mbps square wave, C_L=15pF
	$I_{DD(100M)}$		71		mA	All Input with 100Mbps square wave, C_L=15pF
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5	ns	
Propagation Delay	t_{PLH}		10	25	ns	
	t_{PHL}		10	25	ns	
Pulse Width Distortion	PWD			5	ns	$\lvert t_{PHL} - t_{PLH} \rvert$
Rising Time	t_r			5	ns	C_L = 15pF
Falling Time	t_f			5	ns	C_L = 15pF
Channel-to-Channel Delay Skew	$t_{SK(c2c)}$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK(p2p)}$			5	ns	

6.3. Typical Performance Characteristics

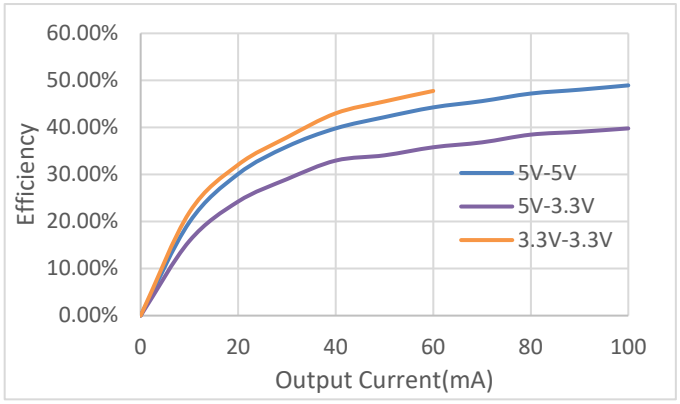


Figure 6.1 Output Current vs Efficiency

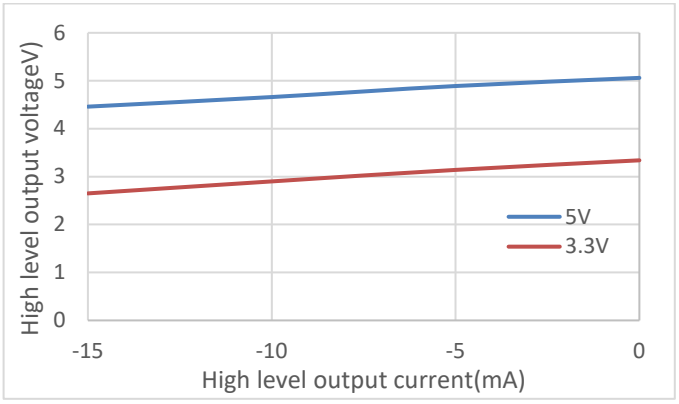


Figure 6.2 High-level Output Voltage vs Output Current

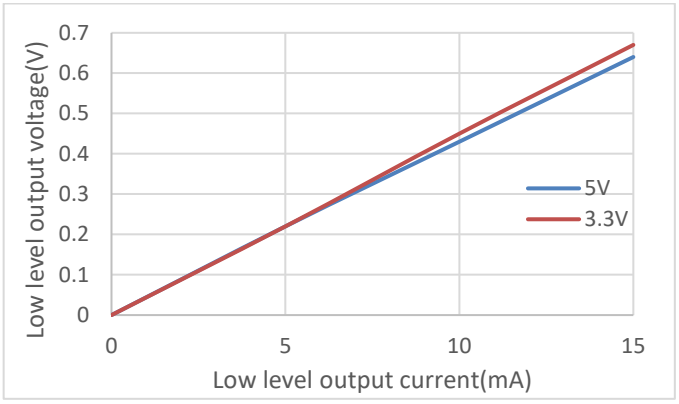


Figure 6.3 Low-level Output Voltage vs Output Current

6.4. Parameter Measurement Information

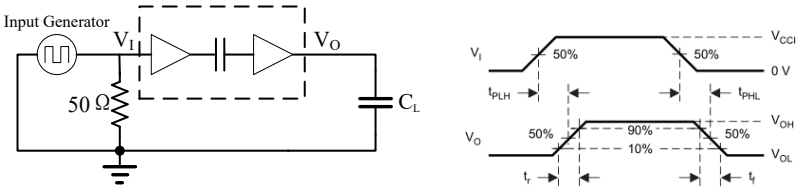


Figure 6.4 Switching Characteristics Test Circuit and Waveform

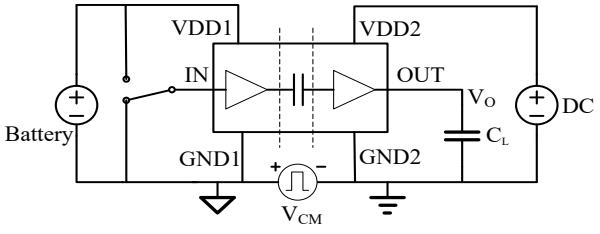


Figure 6.5 Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

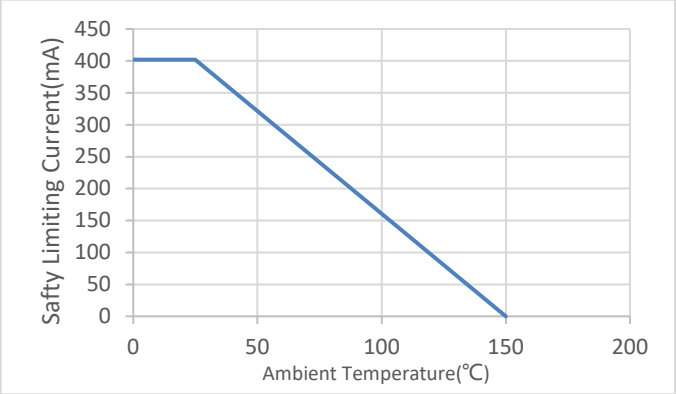
Parameters	*Symbol*	*Value*	*Unit*	*Comments*
Minimum External Air Gap (Clearance)	CLR	8.15	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	CPG	8.15	mm	Shortest terminal-to-terminal distance across the package surface
Distance Through Insulation	DTI	26	μm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

Description	*Test Condition*	*Value*
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	I to IV
	For Rated Mains Voltage ≤ 300Vrms	I to IV
	For Rated Mains Voltage ≤ 600Vrms	I to III
Climatic Classification		40/125/21
Pollution Degree per DIN VDE 0110,		2

7.2. Insulation Characteristics

Description	*Test Condition*	*Symbol*	*Value*	*Unit*
Maximum repetitive isolation voltage		V_{IORM}	1500	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	1061	V_{RMS}
	DC Voltage		1500	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, Vini=V_{IOTM}, t_{ini} = 60 s , $V_{pd(m)}$=1.2*V_{IORM}, t_m=10s.	q_{pd}	<5	pC
	Method a, after environmental tests subgroup 1, Vini=V_{IOTM}, t_{ini}=60s ,$V_{pd(m)}$=1.6*V_{IORM}, t_m=10s			pC
	Method b, routine test (100% production) and preconditioning (type test);V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd\ (m)}$=1.875*V_{IORM}, t_m=1s （method b1）or $V_{pd(m)}$=Vini, t_m=t_{ini}(method b2)			pC
Maximum transient isolation voltage	t = 60 sec	V_{IOTM}	7070	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50-us waveform per IEC62368-1	V_{IMP}	7600	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, V_{IOSM}≥V_{IMP} × 1.3	V_{IOSM}	10000	V_{PEAK}
Isolation resistance	V_{IO} =500V, T_{amb}=25℃	R_{IO}	>10^{12}	Ω
	V_{IO} =500V, 100℃ ≤ T_{amb} ≤ 125℃	R_{IO}	>10^{11}	Ω
	V_{IO} =500V, T_{amb}=T_s	R_{IO}	>10^9	Ω
Isolation capacitance	f = 1MHz	C_{IO}	~4	pF
Safety total power dissipation	θ_{JA} = 59.2 °C/W, V_I = 5.25V, T_J = 150 ℃, T_A = 25 ℃	Ps	2111	mW

Description	*Test Condition*	*Symbol*	*Value*	*Unit*
Safety input, output, or supply current	θ_{JA} = 59.2 °C/W, V_I = 5.25 V, T_J = 150 °C, T_A = 25 °C	Is	402	mA
Maximum safety temperature		Ts	150	°C
UL1577				
Insulation voltage per UL	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	V_{ISO}	5000	V_{RMS}



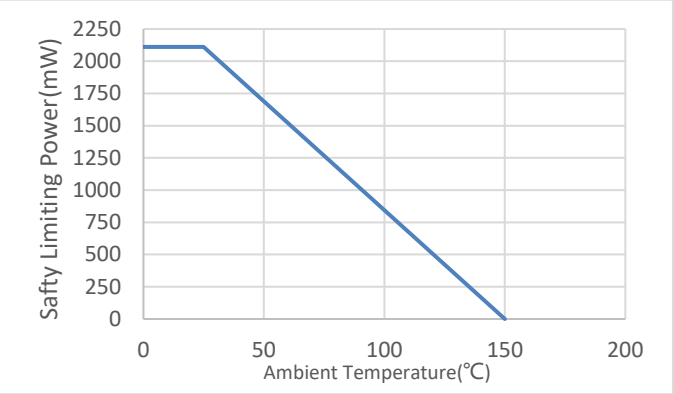


Figure 7.1 NSIP984x Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17

7.3. Regulatory Information

The NSIP984xWx-DSWR are certified with UL1577, VDE0884-17, GB4943.1, EN IEC 62368-1.

UL1577 & CSA Component Acceptance Notice 5A		DIN EN IEC 60747-17 ***(VDE 0884-17)***	***EN IEC62368-1***	***GB4943.1***
Single Protection, 5000V_{rms} Isolation voltage	Single Protection, 5000V_{rms} Isolation voltage	Reinforced Insulation V_{IORM}=1500Vpeak V_{IOTM}=7070Vpeak	5000Vrms for 1min	Certified according to GB4943.1
Certified by UL		Certified by TUV		Certified by CQC
E500602	E500602	R50632560	R50574061	CQC20001264939

8. Function Description

8.1. Overview

The NSIP984x devices are quad-channel digital isolators with integrated isolated DC-DC converter. The digital isolators are based on Novosense capacity isolation barrier technique. The isolated DC-DC converter provides up to 500mW output power using on chip transformer. The feedback PWM signal is sent to primary side by a digital isolator based on capacity isolation technology. The NSIP984x devices are safety certified by UL1577, supporting 5kVrms insulation withstand voltage, while providing high electromagnetic immunity and low emissions. The data rate of the NSIP984x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 100kV/us.

The high integrated solution can help to simplify system design and improve reliability. The NSIP984x devices are suitable for the limited PCB space applications. The devices are also suitable for wide temperature application which the most the power module can not support.

8.2. Device Functional Modes

The NSIP984x devices provide 5V to 5V, 5V to 3.3V, 3.3V to 3.3V conversion mode, the output voltage can be set by SEL pin. Supply configuration table showed below.

SEL PIN	*VDD*	*VISO*
Shorted to VISO	5V	5V
Shorted to GND2 or floating	5V	3.3V
Shorted to GND2 or floating	3.3V	3.3V

The NSIP984x devices provide four channel digital isolators. The digital isolators have default weak pull up or pull down input status when input is floating as shown in below table.

Input	*VDD1 status*	*VDDOUT status*	*Output*	*Comment*
H	Ready	Ready	H	Normal operation.
L	Ready	Ready	L	
floating	Ready	Ready	L(NSIP984xW0) H(NSIP984xW1)	Floating input status

8.3. Output Short And Over Temperature Protection

The NSIP984x devices are protected against output short. When the devices detect the output is short, the device will be in Hiccup mode and the transfer power will be limited. So the temperature of the device will be low, and the device is protected.

The NSIP984x devices are also protected against over temperature. When the devices detect the chip is over 165°C, the device will be shut down until the temperature of the device is below 145°C.

9. Application Note

9.1. Typical Application

The NSIP984x requires 0.1 μF and 10uF bypass capacitors between VDD and GND1, VISO and GND2. The capacitors should be placed as close as possible to the package. This is very important for the performance of the device.

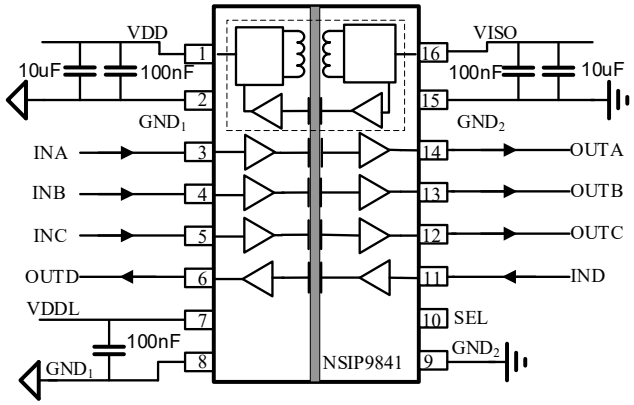


Figure 9.1 Basic schematic of NSIP984x

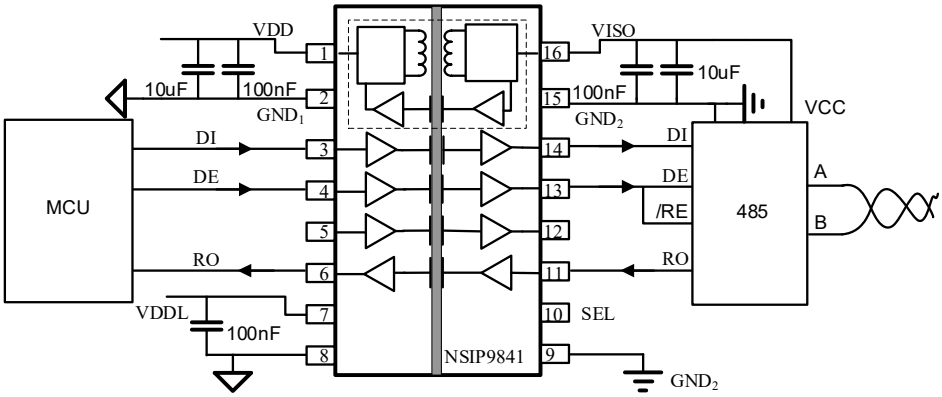


Figure 9.2 Half-Duplex RS-485 schematic using NSIP984x

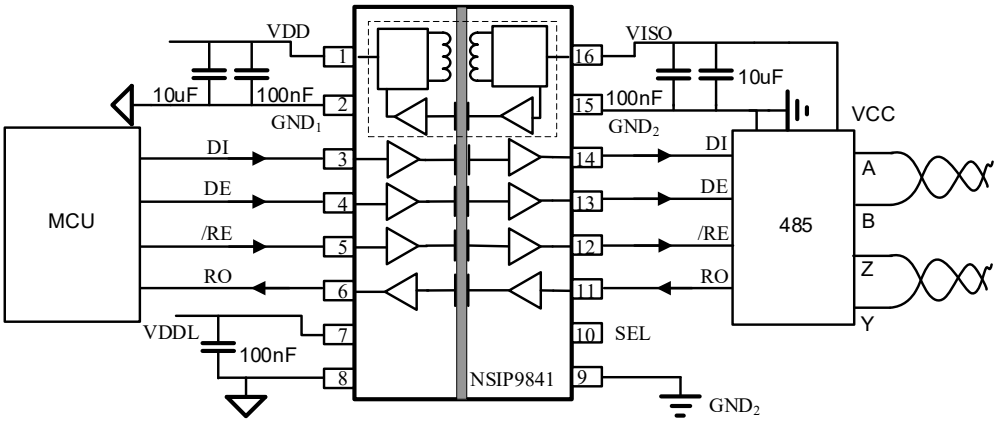


Figure 9.3 full-Duplex RS-485 schematic using NSIP984x

9.2. PCB Layout

The recommended PCB layout shown below. The low ESR capacitor C1 should be closed to PIN1 and PIN2, the distance should be less than 1mm. The low ESR capacitor C3 should be closed to PIN15 and PIN16, the distance should be less than 1mm. It is recommended that C1=C3=100nF and C2=C4=10uF.

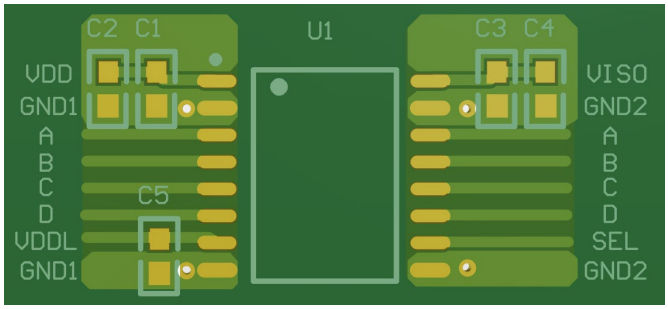


Figure 9.4 SOW16 Recommended PCB Layout — Top Layer

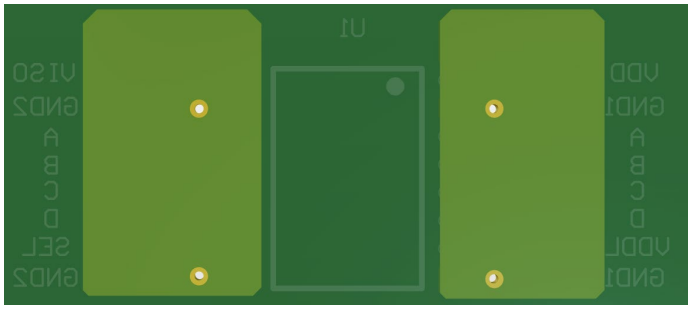
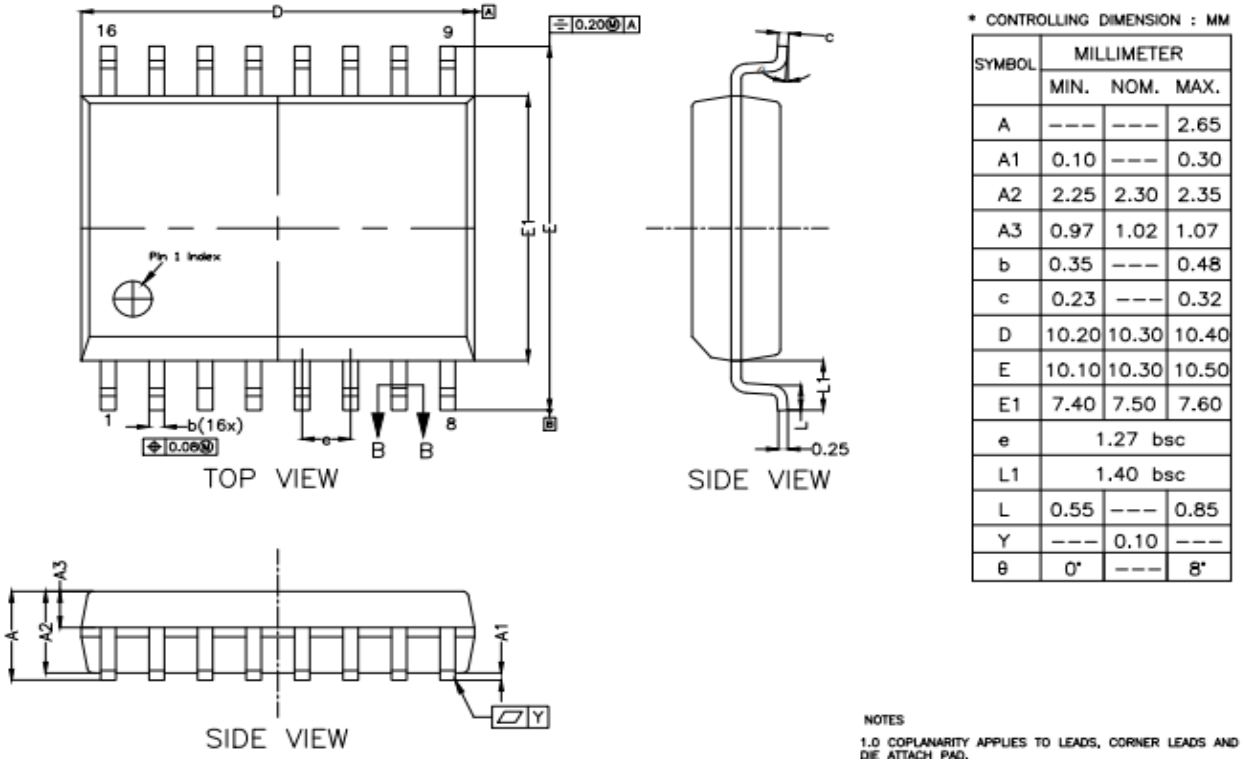


Figure 9.5 SOW16 Recommended PCB Layout — Bottom Layer

10. Package Information



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.48
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

NOTES

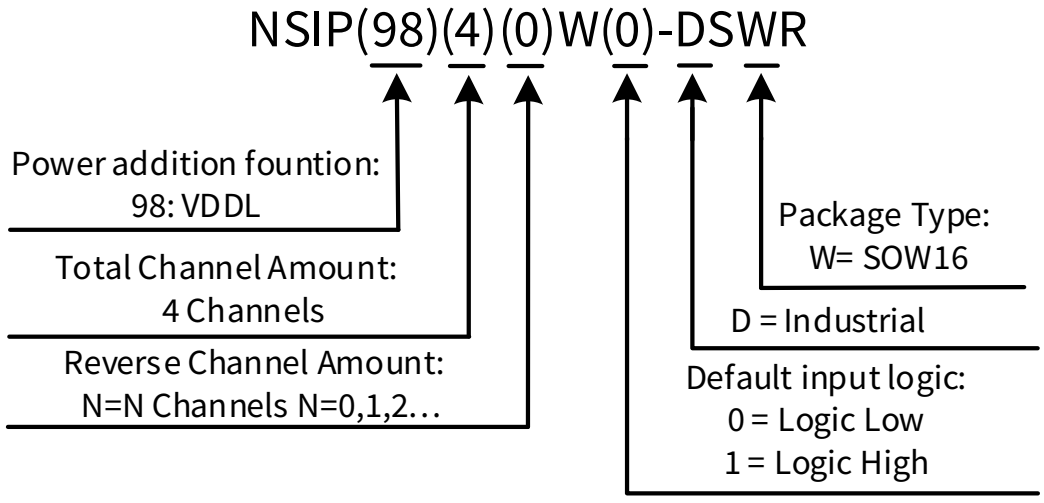
1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 10.1 SOW16 Package Shape and Dimension in millimeters

11. Order Information

Part Number	Isolation Rating (kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default input logic	Temperature	MSL	Package Type	Package Drawing	SPQ
NSIP9840W0-DSWR	5	4	0	150	Low	-40 to 125°C	3	SOP16 (300mil)	SOW16	1500
NSIP9840W1-DSWR	5	4	0	150	High	-40 to 125°C	3	SOP16 (300mil)	SOW16	1500
NSIP9841W0-DSWR	5	3	1	150	Low	-40 to 125°C	3	SOP16 (300mil)	SOW16	1500
NSIP9841W1-DSWR	5	3	1	150	High	-40 to 125°C	3	SOP16 (300mil)	SOW16	1500
NSIP9842W0-DSWR	5	2	2	150	Low	-40 to 125°C	3	SOP16 (300mil)	SOW16	1500
NSIP9842W1-DSWR	5	2	2	150	High	-40 to 125°C	3	SOP16 (300mil)	SOW16	1500
NSIP9843W0-DSWR	5	1	3	150	Low	-40 to 125°C	3	SOP16 (300mil)	SOW16	1500
NSIP9843W1-DSWR	5	1	3	150	High	-40 to 125°C	3	SOP16 (300mil)	SOW16	1500
NSIP9844W0-DSWR	5	0	4	150	Low	-40 to 125°C	3	SOP16 (300mil)	SOW16	1500
NSIP9844W1-DSWR	5	0	4	150	High	-40 to 125°C	3	SOP16 (300mil)	SOW16	1500

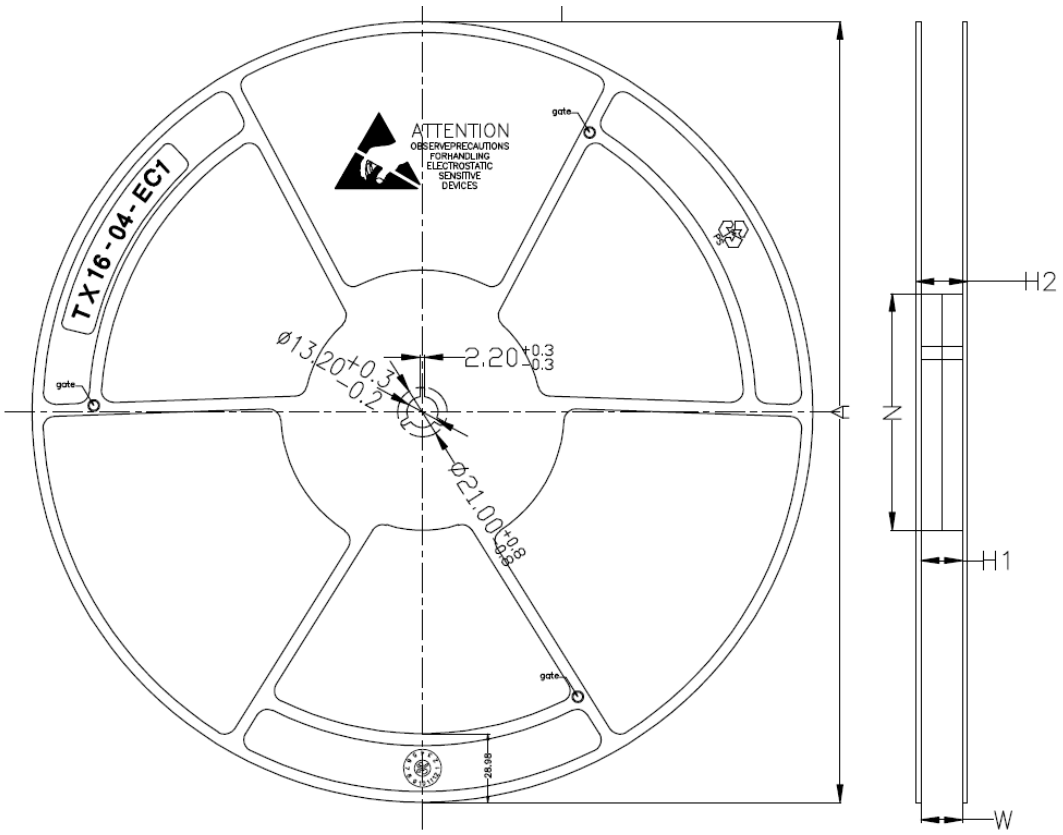
Part Number Rule:



12. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NSIP984x	Click here	Click here	Click here	Click here

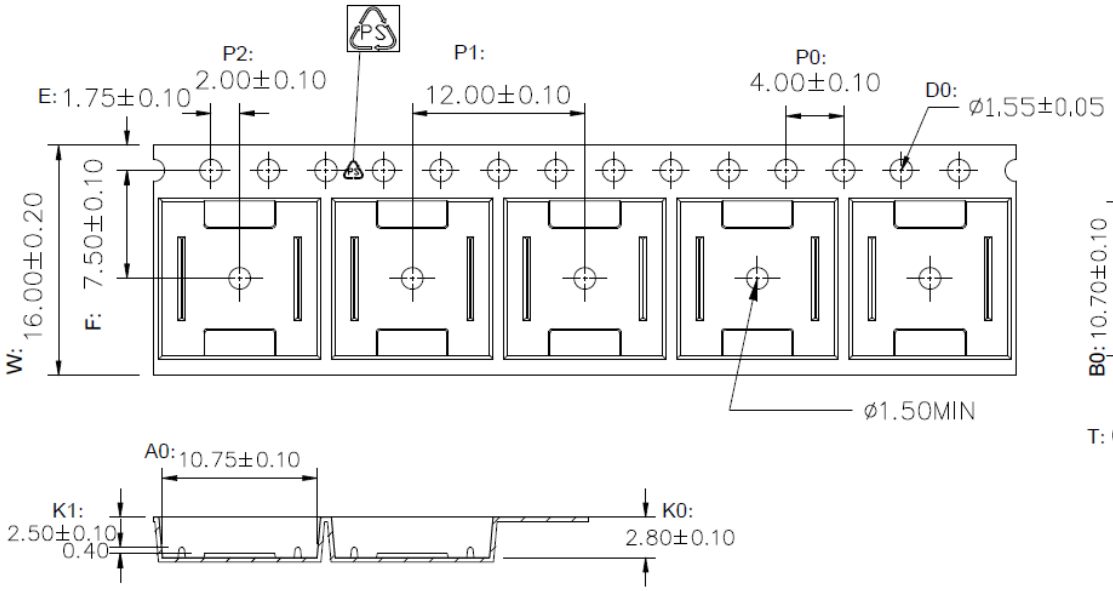
13. Tape And Reel Information



PRODUCT SPECIFICATIONS					
TAPE WIDTH	øA $^{+2}_{-2}$	øN $^{+2}_{-2}$	H1 $^{+2}_{-0}$	H2 $^{+1}_{-1}$	W $^{+3.5}_{-0.2}$
16MM	330	100	16.4	20.6	16.4

NOTES:
1.MATERIAL:DISSIPATIVE(BLACK)
2.FLANGE WARPAGE:3 MM MAXIMUM 5
3.ALL DIMENSIONS ARE IN MM
4.ESD - SURFACE RESISTIVITY-10 TO 10 OHMS/SQ
5.GENERAL TOLERANCE: ±0.25 MM

Figure 13.1 Tape Information of SOW16



1. 10 sprocket hole pitch cumulative tolerance ±0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy .
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 378 Meters.(復卷 N=122）
7. Component load per 13" reel : 1000 pcs.
8. Surface resistivity :10^{5} ~ 10^{10}Ω/□

RoHS

W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

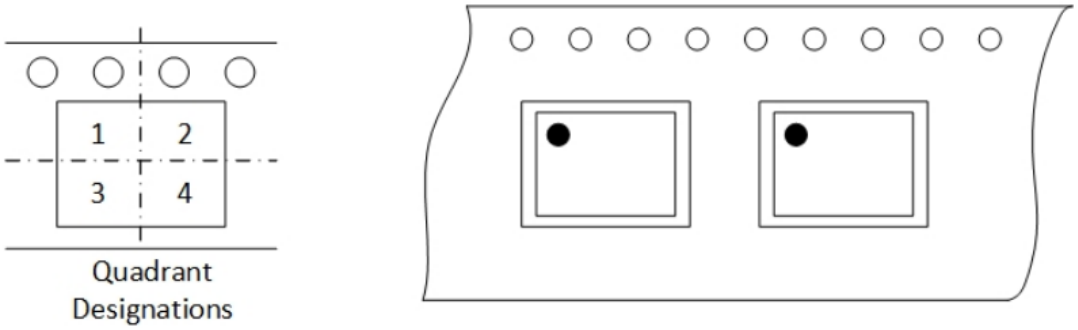


Figure 13.2 Reel Information of SOW16

14. Revision History

Revision	Description	Date
1.0	Initial version	2025/10/21

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