NOVOSENSE

NSIP6055A-Q1, NSIP6055B-Q1
1-A Transformer Drivers for Isolated Power Supplies
Datasheet (EN) 1.1

Product Overview
The NSIP6055x is a push-pull transformer driver specially designed for small size, low-power isolation power supply with low standby power consumption. The periphery of the circuit only requires simple input and output filter capacitors, isolation transformer, and rectifier circuits.

Its internal integrated oscillator provides a pair of high-precision complementary signals to drive two N-channel MOSFETs. The internal design of the chip follows a symmetrical structure, which can effectively ensure the high symmetry of the two power MOSFETs and avoid magnetic bias during the working process of the circuit.

Ultra-low noise and EMI are achieved by slew rate control of the output switch voltage and through Spread Spectrum Clocking (SSC). The internal protection features include over
current protection, under-voltage lockout, thermal shutdown and break-before-make circuitry. NSIP6055A has a 160 kHz internal oscillator for applications that need to minimize emissions. NSIP6055B has a 420kHz internal oscillators for application that require higher efficiency and smaller transformer size.

The NSIP6055x is available in a small SOT-23 (6) package, and is specified for operation at temperatures from –40°C to 125°C.

Key Features
- Push-pull driver for transformers
- Support 2.25V to 5.5V supply
- High output drive: 1 A at 5 V supply
- Precision internal oscillator options: 160 kHz (NSIP6055A) and 420 kHz (NSIP6055B)
- Ultra-low EMI
- Over-current protection (OCP)
- Over temperature protection
- Soft-start to reduce In-rush current
- Spread Spectrum Clocking
- Slew-rate control
- Small 6-Pin SOT-23 Package
- AEC-Q100 Grade 1 Qualified
- RoHS & REACH Compliance

Applications
- Isolated interface power supply for I2C, CAN, RS-485, RS-422, RS-232, SPI, Low-Power LAN
- IGBT gate drive power supply

Device Information

Part Number	Package	Body Size
NSIP6055A-Q1STCR	SOT23- 6L	2.90 mm x 1.60 mm
NSIP6055B-Q1STCR	SOT23- 6L	2.90 mm x 1.60 mm

Functional Block Diagrams

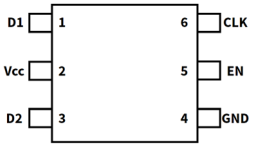

Figure 1. NSIP6055x

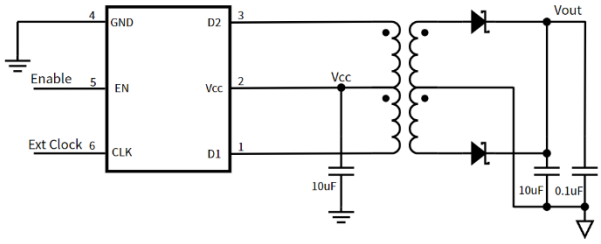

Figure 2. Simplified Schematic

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1. Pin Configuration and Functions

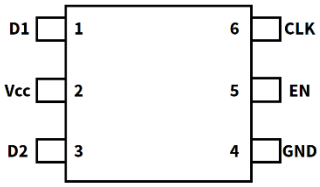


Figure 1.1 NSIP6055x

Table1.1 Pin Functions

PIN NO.	SYMBOL	FUNCTION
1	D1	Open Drain output 1. Connect to transformer primary side 1.
2	V_{CC}	Supply voltage input. Connect this pin to the center-tap of the transformer primary side. Buffer this voltage with a 0.1μF to 10μF ceramic capacitor.
3	D2	Open Drain output 2. Connect to transformer primary side 2.
4	GND	Device ground. Connect this pin to board ground.
5	EN	The EN pin turns the device on or off. Grounding or leaving this pin floating disables all internal circuitry. If unused this pin should be tied directly to V_{CC}.
6	CLK	This pin is used to run the device with external clock. Internally it is pulled down to GND. If valid clock is not detected on this pin, the device shifts automatically to internal clock.

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	V_{CC}	-0.5		6	V	
Output switch voltage	V_{D1}, V_{D2}			16	V	
Voltage	EN, CLK	-0.5		Vcc+0.5	V	
Peak output switch current	$I_{(D1)Pk}$, $I_{(D2)Pk}$			2.5	A	
Junction temperature	T_J	-40		150	°C	
Storage temperature	T_{stg}	-55		150	°C	

3. ESD Ratings

Parameters	Ratings	Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD ● All pins	±8.0	kV
	Charged device model (CDM), per AEC-Q100-011-RevB ● All pins	±2.0	kV

4. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit	Comments
Supply voltage	V_{CC}	2.25		5.5	V	
Output switch voltage	V_{D1}, V_{D2}	0		12	V	
D1 and D2 output switch current – Primary-side	I_{D1}, I_{D2}			1.36	A	V_{CC} = 5 V ± 10% V_{CC} = 3.3 V ± 10%
Ambient Temperature	T_A	-40		125	°C	

5. Thermal Information

Parameters	Symbol	SOT23-6	Unit
IC Junction-to-air thermal resistance	θ_{JA}	136.4	°C/W
Junction-to-board thermal resistance	θ_{JB}	53.4	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC(top)}$	85.4	°C/W
Junction-to-top characterization parameter	Ψ_{JT}	32.5	°C/W
Junction-to-board characterization parameter	Ψ_{JB}	52.4	°C/W

Notes

(1) Four layers 2s2p PCB JEDEC JESD 51-7.

6. Electrical Characteristics

Over full range of recommended operating conditions, unless otherwise noted. All typical value is at T_A= 25°C, V_{CC}= 5 V.

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Switch-on resistance	R_{ON}		0.18	0.35	Ω	V_{CC} = 5 V
			0.21	0.41	Ω	V_{CC} = 3.3V
Average supply current	I_{CC}		1.1	1.5	mA	Supply Current (2.8 V < V_{CC} < 5.5V) NSIP6055A
			1.45	2.0		Supply Current (2.8 V < V_{CC} < 5.5V) NSIP6055B
Leakage Current on EN and CLK pin	I_{IH}		12	20	μA	EN / CLK = V_{CC}
V_{CC} current for EN = 0	I_{DIS}		0.01		μA	
Leakage Current on D1, D2 for EN=0	$I_{LKG(D1)}$ $I_{LKG(D2)}$		0.1		μA	Voltage of D1, D2 = V_{CC}
Positive going UVLO threshold	$V_{CC+ (UVLO)}$			2.25	V	
Negative going UVLO threshold	$V_{CC- (UVLO)}$	1.7			V	
UVLO threshold hysteresis	$V_{HYS (UVLO)}$		0.3		V	
CLK, EN, pin logic high threshold	$V_{IN(ON)}$			0.7	V_{CC}	
CLK, EN pin logic low threshold	$V_{IN(OFF)}$	0.3			V_{CC}	
CLK, EN, pin threshold hysteresis	$V_{IN(HYS)}$		0.2		V_{CC}	
D1, D2 average switching Frequency (NSIP6055A)	F_{SW}	120	157	200	kHz	D1 and D2 connect 50Ω to V_{CC} See Figure 9.1
D1, D2 average switching Frequency (NSIP6055B)		320	425	550	kHz	D1 and D2 connect 50Ω to V_{CC} See Figure 9.1
External clock frequency on CLK pin (NSIP6055A)	$F_{(EXT)}$	100		600	kHz	D1 and D2 connect 50Ω to V_{CC} See Figure 9.1
External clock frequency on CLK pin (NSIP6055B)		100		1600	kHz	D1 and D2 connect 50Ω to V_{CC} See Figure 9.1

Over full range of recommended operating conditions, unless otherwise noted. All typical value is at T_A= 25°C, V_{CC}= 5 V.

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Spread Spectrum Clocking (NSIP6055A)			±6.5%			
Spread Spectrum Clocking (NSIP6055B)			±13%			
Protection Current Threshold		1.5	2.8	4.0	A	
Current limit			1.3		A	
THERMAL SHUT DOWN						
T_{SD} turn on temperature	T_{SD+}	152	169	180	°C	
T_{SD} turn off temperature	T_{SD-}	134	149	166	°C	
T_{SD} hysteresis	ΔT_{SD}	12	18		°C	

7. Switching Characteristics

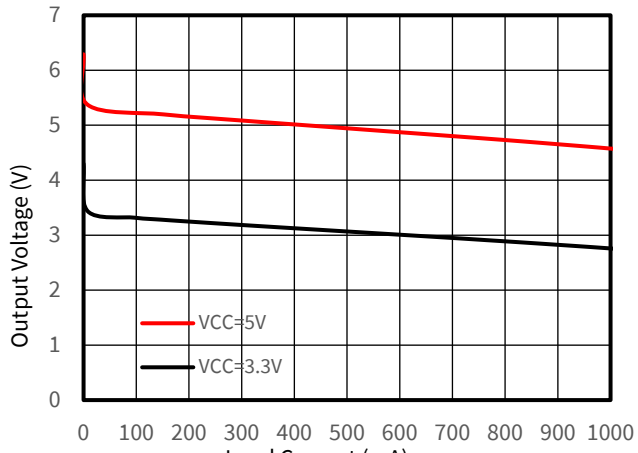
Over full range of recommended operating conditions, unless otherwise noted.

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Average on-time mismatch between D1 and D2	t_{mm}		0		µs	
Voltage slew rates on D1 and D2 for NSIP6055A	$V_{(SLEW)}$		38.5		V/µs	D1 and D2 connect 50Ω to V_{CC}, See Figure 9.1
Voltage slew rates on D1 and D2 for NSIP6055B	$V_{(SLEW)}$		100		V/µs	D1 and D2 connect 50Ω to V_{CC}, See Figure 9.1
Current slew rates on D1 and D2 for NSIP6055A	$I_{(SLEW)}$		12		A/µs	See Figure 9.3
Current slew rates on D1 and D2 for NSIP6055B	$I_{(SLEW)}$		36		A/µs	See Figure 9.3
Duration after which device switches to internal clock in case of invalid external clock	$t_{CLKTIMER}$		20		µs	
Break-before-make time NSIP6055A	t_{BBM}		175		ns	D1 and D2 connect 50Ω to V_{CC}, See Figure 9.1
Break-before-make time NSIP6055B			110		ns	D1 and D2 connect 50Ω to V_{CC}, See Figure 9.1
SOFT-START						
Soft-start time (NSIP6055A)	t_{SS}		2.3		ms	V_{out} rises from 10%-90% of the time, C_{LOAD} = 40uF, R_L= 5Ω

Over full range of recommended operating conditions, unless otherwise noted.

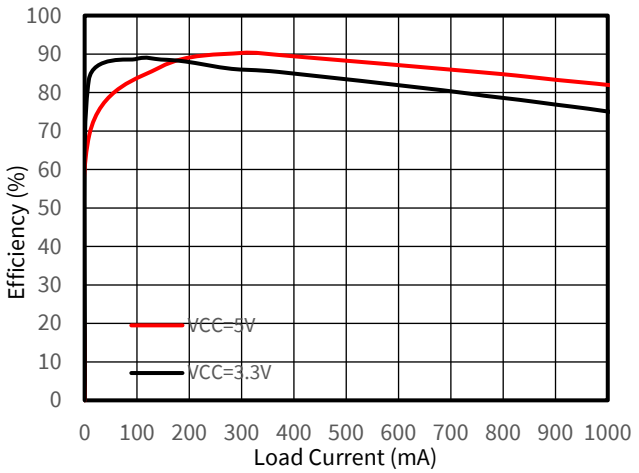
Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Soft-start time delay (NSIP6055A)	$t_{SSdelay}$		2.4		ms	Time from power on to V_{out} rising to 90%
SOFT-START						
Soft-start time (NSIP6055B)	t_{SS}		4.0		ms	V_{out} rises from 10%-90% of the time, C_{LOAD} = 40uF, R_L= 5Ω
Soft-start time delay (NSIP6055B)	$t_{SSdelay}$		4.8		ms	Time from power on to V_{out} rising to 90%

8. Typical Characteristics



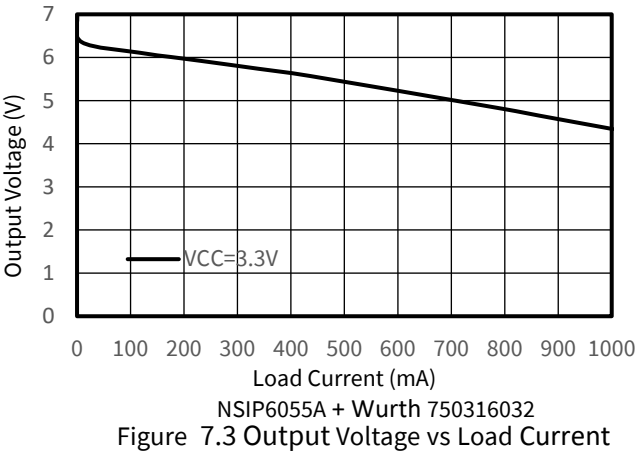
NSIP6055A + Wurth 750315240

Figure 7.1 Output Voltage vs Load Current



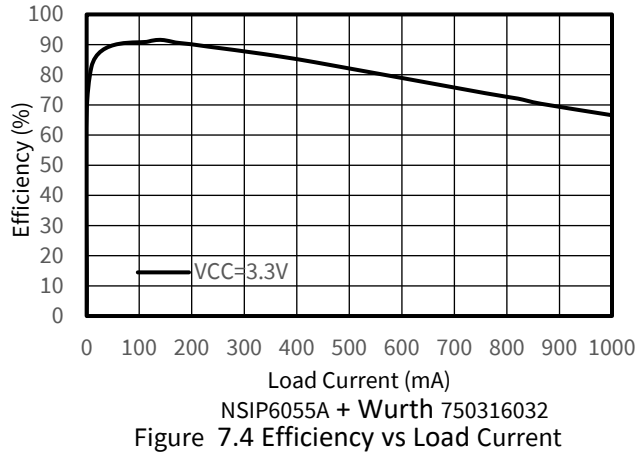
NSIP6055A + Wurth 750315240

Figure 7.2 Efficiency vs Load Current



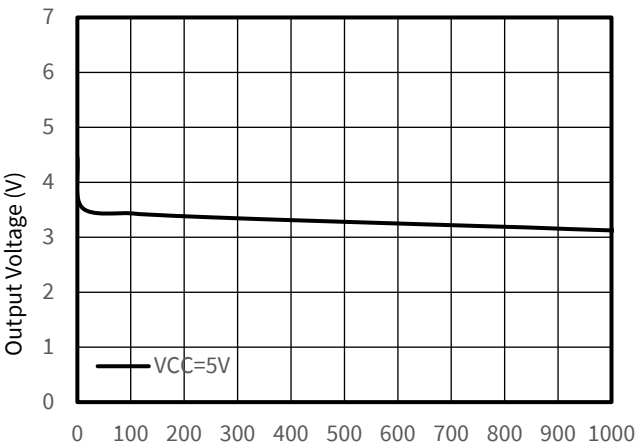
NSIP6055A + Wurth 750316032

Figure 7.3 Output Voltage vs Load Current



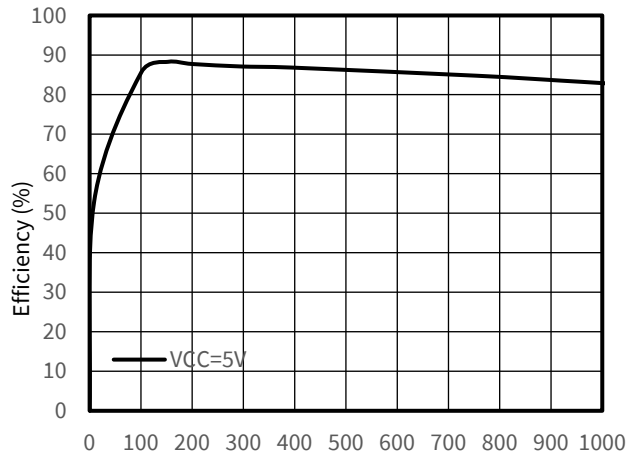
NSIP6055A + Wurth 750316032

Figure 7.4 Efficiency vs Load Current



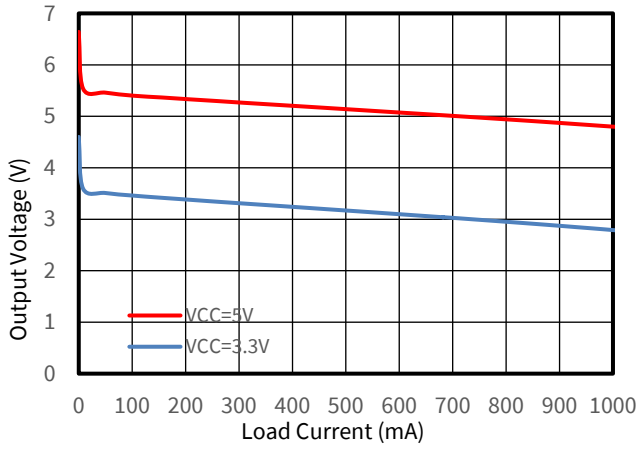
NSIP6055A + Wurth 750316033

Figure 7.5 Output Voltage vs Load Current



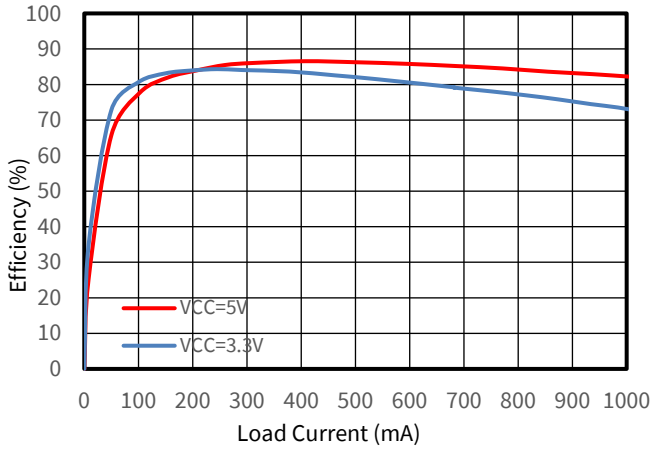
NSIP6055A + Wurth 750316033

Figure 7.6 Efficiency vs Load Current



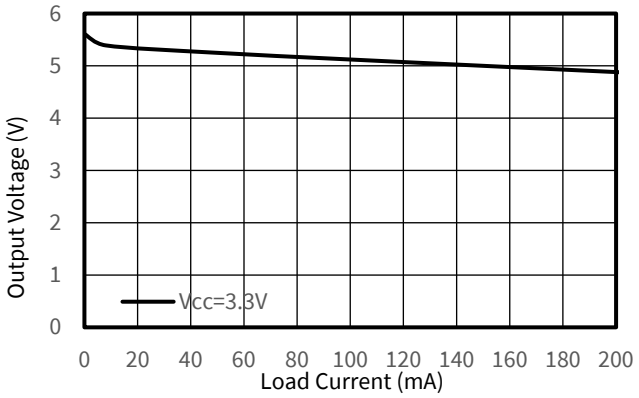
NSIP6055B-Q1 + Wurth 750315371

Figure 7.7 Output Voltage vs Load Current



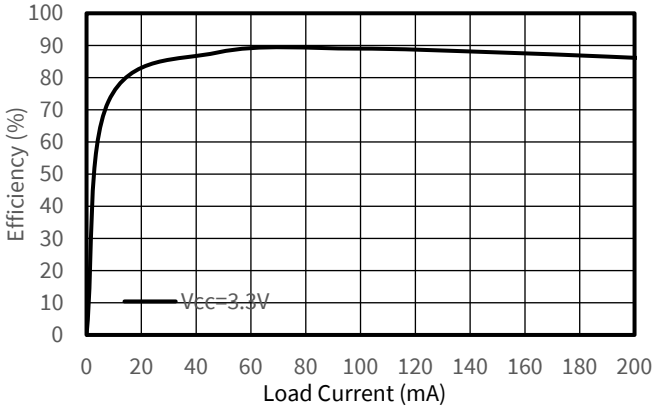
NSIP6055B-Q1 + Wurth 750315371

Figure 7.8 Efficiency vs Load Current



NSIP6055B-Q1 + Wurth 760390013

Figure 7.9 Output Voltage vs Load Current



NSIP6055B-Q1 + Wurth 760390013

Figure 7.10 Efficiency vs Load Current

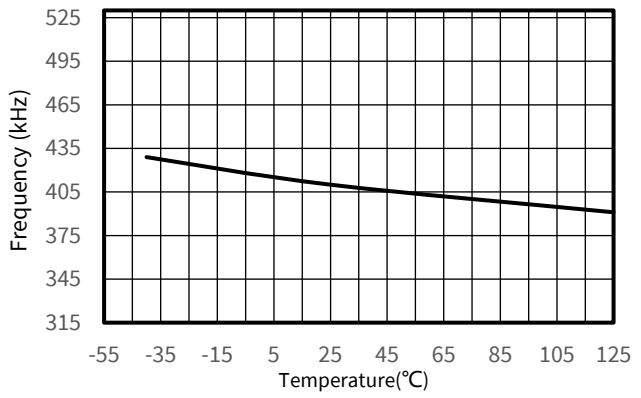


Figure 7.11 Average Frequency vs Free-Air Temperature NSIP6055B

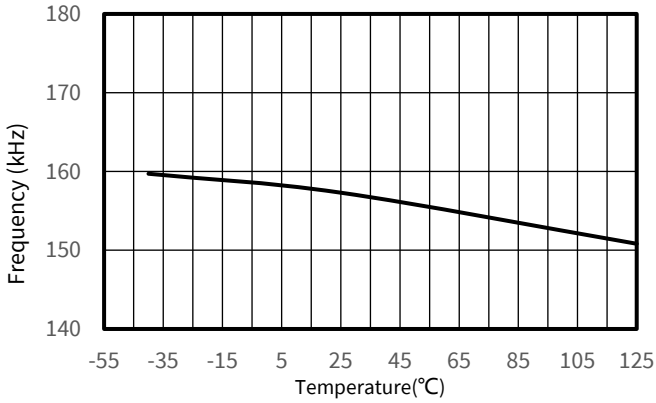


Figure 7.12 Average Frequency vs Free-Air Temperature NSIP6055A

9. Parameter Measurement Information

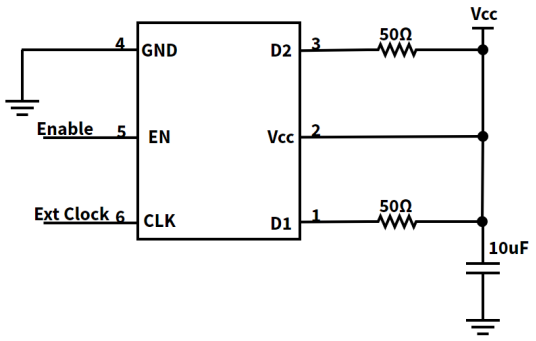


Figure 9.1 Test Circuit for FSW, $T_{r\text{-}D}$, $F_{t\text{-}D}$, T_{BBM}

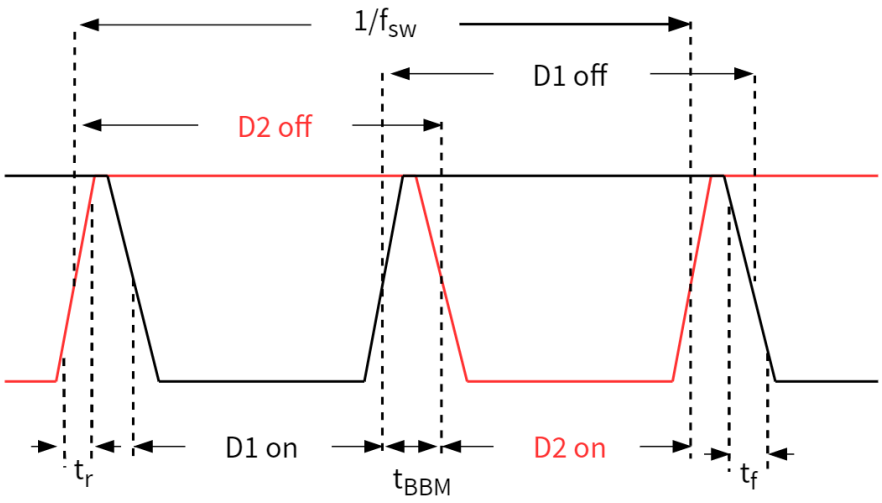


Figure 9.2 Timing Diagram

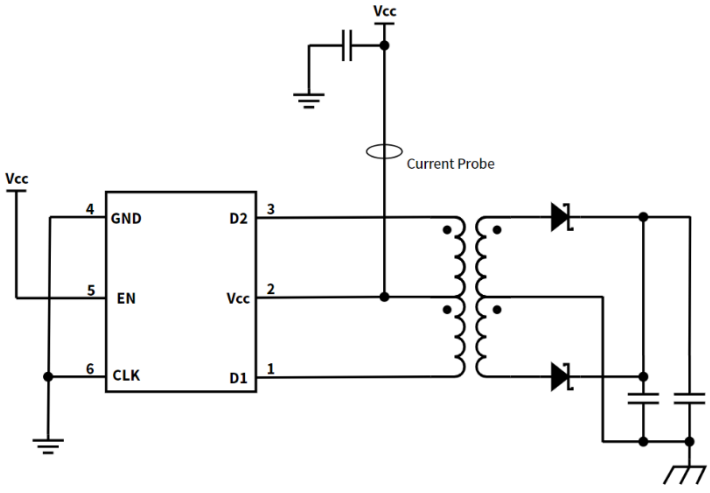


Figure 9.3 $I_{(slew)}$ Test Setup

10. Detailed Description

10.1 Overview

The NSIP6055x is transformer driver designed for low cost, small size, isolated DC-DC converters in push-pull topologies. The device consists of an oscillator and a gate driver. the output frequency of the oscillator is divided by frequency divider, which provides two complementary output signals with a duty cycle of 50%, and a dead time tBBM is designed between the two drives to avoid D1 and D2 conduction at the same time.

In order to improve EMI performance, the NSIP6055x oscillator has added spread spectrum clocking function. NSIP6055x integrates a thermal shutdown module and a current clamping function when the current is too large, to ensure that the chip itself works in the safety zone.

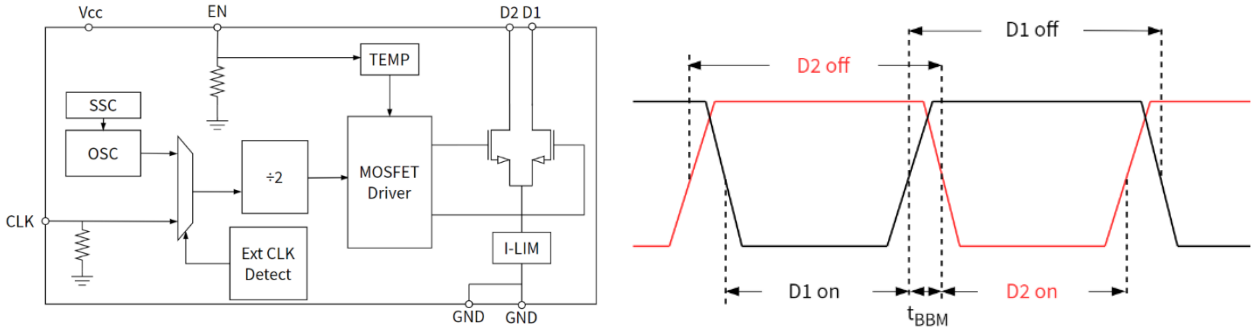


Figure 10.1 Functional Block Diagram and Output Timing with Break-Before-Make Action

10.2 Feature Description

10.2.1 Push-Pull Converter

Push-pull converters require transformers with center-taps to transfer power from the primary to the secondary.

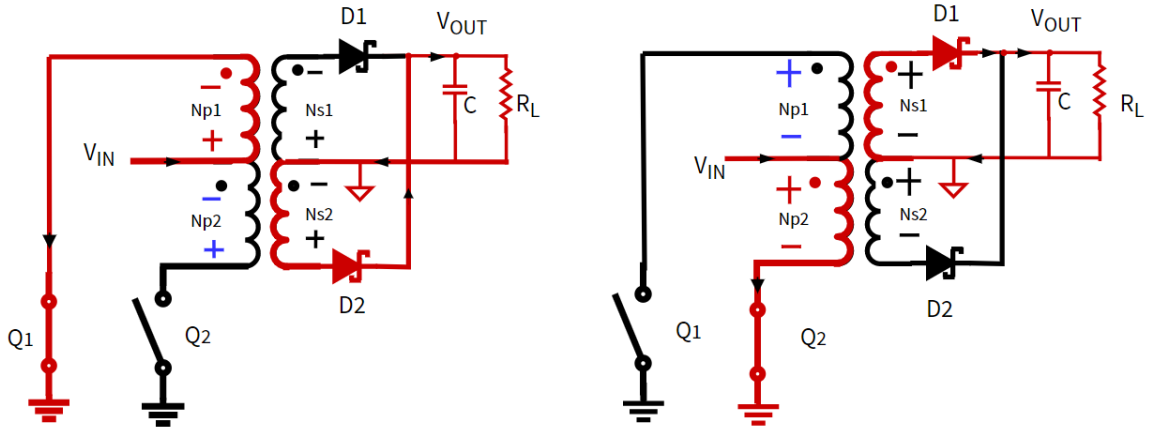


Figure 10.2 Switching Cycles of a Push-Pull Converter

The equivalent schematic diagram of the working process of a push-pull converter is shown in Figure 10.2. Switches Q1 and Q2 work in turns, with a duty cycle of nearly 50%. When Q1 is turned on, the input power flows from the center-tap input port Vin of the transformer to the transformer primary winding Np1, and from Np1 to switches Q1 and GND. At the same time, the energy is transferred to the secondary side through the transformer. The output current flows out from the secondary winding Ns2, transmits it to the output V_{OUT} through the rectifier diode D2, and finally returns to the Ns2 from the output GND after passing through the load. The working process of switch Q2 is basically the same as that of Q1.

When the circuit is working, each winding of the transformer (Np1, Np2, Ns1, Ns2) will generate a corresponding induced voltage. The amplitude of the induced voltage is proportional to the ratio of turns of the transformer winding. The voltage stress of Q1 and Q2 during the operation of the push-pull converter is 2×Vin voltage.

Start-Up Mode

When the voltage at the V_{CC} ramps up to 2.25V, the internal oscillator starts to work. The output stage starts to switch, and the drain signal amplitude of D1 and D2 has not reached the maximum value.

Current Limit

The NSIP6055x device performs current limiting by clamping the output current. When the output current increases to the threshold current, the output gate drive voltage clamp. The device has a current limiting function that can help isolate the overcurrent of the power transformer, but overheating losses need to be considered and may lead to over temperature protection.

Over Temperature Protection

The NSIP6055x device supports OverTemperature Protection. When the junction temperature of the device is higher than the protection temperature threshold, the device will turn off output to protect the device from overheating damage. When the junction temperature is lower than the T_{SD-}, the device will resume startup.

Spread Spectrum

Radiation emission is an important concern in high current switching power supplies. NSIP6055x has the ability to modulate its internal clock, distributing transmission energy over a wider frequency band rather than a narrow peak, greatly improving EMI performance through its spread spectrum feature.

Soft Start

The NSIP6055x devices support soft start feature by limiting output current. When the device starts up either by powering up or EN rising edge, the device slowly ramps up output current limit. The soft start feature can prevent in-rush current upon starting up and protect transformer accordingly.

External Clock Mode

The NSIP6055x device has external clock mode with CLK input to synchronize with external frequency. The CLK rising edge will be used as trigger and frequency is divided by two as switching clock frequency. When the external clock is present, the built-in emission reduction scheme of the spread spectrum clock is disabled.

11. Application and Implementation

Note

The information contained in the following application section is not part of the NOVOSENSE component specification and NOVOSENSE does not guarantee its accuracy or completeness. NOVOSENSE's customers are responsible for determining whether components are suitable for their purpose, as well as validating and testing their design implementations to confirm system functionality.

11.1 Typical Application

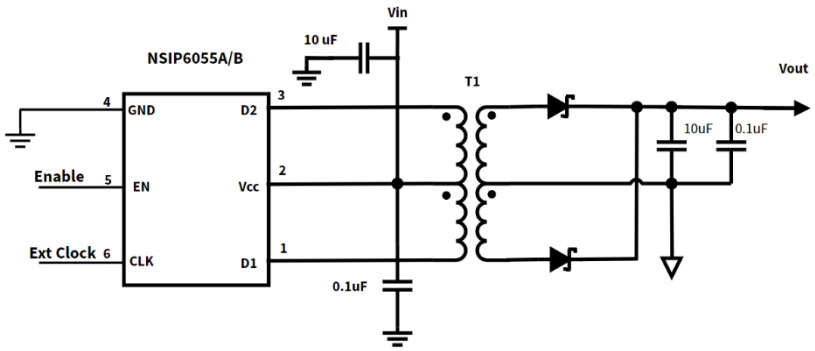


Figure 11.1 Typical Application Schematic

11.2 Design Requirements

For this design example, use the parameters listed in Table 11-1 as design parameters.

Table 11-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	3.3 V ± 10%
Output full load	5 V
Maximum load current	100 mA

11.2.1 Detailed Design Requirements

The following sections focus on the design of efficient push-pull conversions with high current drive capability.

11.2.1.1 LDO Selection

The minimum requirements for LDO: Note the following points:

- For a load current of 100 mA, it is recommended to choose a continuous output current capacity of 100 mA to 150 mA, slightly exceeding the specified load current.
- The output voltage of the isolated power supply should be greater than the output voltage of the LDO for proper operation of the LDO. Therefore, it is advisable to choose a LDO chip with the smallest possible dropout voltage.

$$V_{I\text{-}min} = V_{DO\text{-}max} + V_{O\text{-}max} \quad (1)$$

Note that the output voltage of the push-pull rectifier at the specified load current is equal to or higher $V_{I\text{-}min}$. Otherwise, the LDO will lose any line regulation.

- The maximum input voltage of the LDO must be higher than the rectified output at no-load. At this point, the secondary reaches its maximum voltage.

$$V_{S\text{-}max} = V_{IN\text{-}max} \times n \quad (2)$$

$V_{IN\text{-}max}$ is the maximum input voltage of the converter, and n is the ratio of turns of the transformer. Therefore, in order to prevent LDO damage, the maximum LDO input voltage must be higher than $V_{S\text{-}max}$.

11.2.1.2 Diode Selection

The selection of Schottky diodes needs to consider the following two points:

- Selecting a diode for the power supply, it is recommended to choose a low forward voltage and fast recovery diode. A low forward voltage helps improve the output efficiency of the power supply. For a low-cost option, the MBR0520L Schottky rectifier diode is recommend, with a typical forward voltage of 275mV and forward current of 100mA. However, if operating at ambient temperatures higher than 100°C, it is advisable to use the RB168M-40 diode.
- Considering the impact of temperature on forward voltage, it is advisable to select a rectifier with a low forward voltage drop, especially at low temperatures.

11.2.1.3 Capacitor Configuration

- In the design process, capacitors of 0.1μF and 10μF need to be placed in parallel between the input pin of the center-tap transformer and the device V_{cc} pin, to achieve the minimum line path and reduce the inductance of the wiring.
- To ensure low-inductance paths use two vias in parallel for each connection. The secondary rectifier output and the LDO output must be placed in parallel with 10μF and 0.1μF capacitors. It improves the stability of the power supply and reduce the output ripple.
- A low- ESR ceramic capacitor will meet circuit requirements.

11.2.1.4 Transformer Selection

11.2.1.4.1 V-t Product Calculation

Transformer selection needs to consider the Vt factor. the purpose is to prevent transformer saturation. The Vt_{min} is calculated by the maximum input voltage multiplying 50% of the maximum cycle time.

$$Vt_{min} \geq V_{IN-max} \times \frac{T_{max}}{2} = \frac{V_{IN-max}}{2 \times f_{min}} \quad (3)$$

Taking an example of f_{min} as 320kHz for NSIP6055B, Equation 3 yields the minimum V-t products of:

$$Vt_{min} \geq \frac{3.6V}{2 \times 320kHz} = 5.6V\mu s \quad \text{for 3.3V}$$

$$Vt_{min} \geq \frac{5.5V}{2 \times 320kHz} = 8.6V\mu s \quad \text{for 5V applications} \quad (4)$$

Other important factors such as isolation voltage, transformer power and turns ratio must be considered before the final selection decision is made.

11.2.1.4.2 Turns Ration Estimate

Assumed the rectifier diode and linear regulator have been selected, and the V-t product of the selected transformer is not less than 8.7Vμs. The minimum turns ratio that allows the push-pull converter to operate perfectly over a specified current and temperature range needs to be determined.

From the LDO selection section. The V_{S-min} must be large enough to allow the maximum voltage to drop V_{F-max} to cross the rectifier diode and still provide enough input voltage to the regulator to maintain voltage stability.

$$V_{S-min} = V_{F-max} + V_{DO-max} + V_{O-max} \quad (5)$$

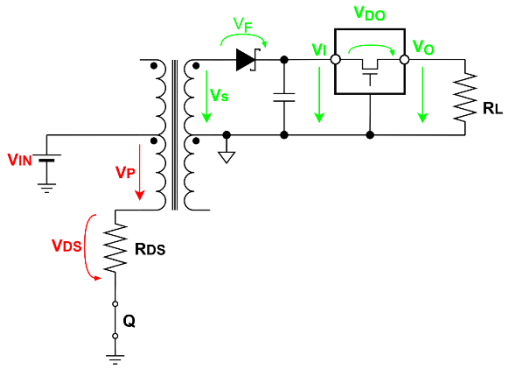


Figure 11.2 Establishing the Required Minimum Turns Ratio Through $N_{min} = 1.031 \times V_{s-min}/V_{P-min}$

The minimum available primary voltage V_{P-min} is calculated. Drain-source voltage of the NSIP6055x is V_{DS-max}. The minimum converter input voltage is V_{IN-min}:

$$V_{P-min} = V_{IN-min} - V_{DS-max} \quad (6)$$

V_{DS-max} is the product of the maximum $R_{DS(on)}$ and I_D values for a given supply specified in the NSIP6055x data sheet:

$$V_{DS-max} = R_{DS-max} \times I_{Dmax} \quad (7)$$

Then inserting Equation 7 into Equation 6 yields:

$$V_{P-min} = V_{IN-min} - R_{DS-max} \times I_{Dmax} \quad (8)$$

Inserting Equation 8 and Equation 5 into Equation 9 provides the minimum turns ration with:

$$n_{min} = 1.031 \times \frac{V_{F-max} + V_{DO-max} + V_{O-max}}{V_{IN-min} - R_{DS-max} \times I_{D-max}} \quad (9)$$

Example:

For a 3.3 V_{IN} to 5 V_{OUT} converter using the rectifier diode MBR0520 and the LDO TPS76350, at a load current of 100 mA and a maximum temperature of 85°C are $V_{F\text{-}max}$ = 0.2 V, $V_{DO\text{-}max}$ = 0.2 V, and $V_{O\_FullLoad\_max}$ = 5.175 V, $I_{OUT\text{-}max}$ = 0.1A.

Assume that the input power supply accuracy is ±2%, VIN-min = 3.234 V. From the NSIP6055x data sheet with RDS-max = 0.41Ω,
ID-max = 1.36A.
Inserting in these values and do the calculation:

$$N_{min} = 1.031 \times \frac{0.2V + 0.2V + 5.175V}{3.234V - 0.41\Omega \times 1.36A} = 2.08 \quad (10)$$

11.2.1.4.3 Recommended transformer configuration solution

The following circuits are recommended. Use the unstable output voltage circuit in Figure 11.3 or stable output voltage in Figure 11.4.

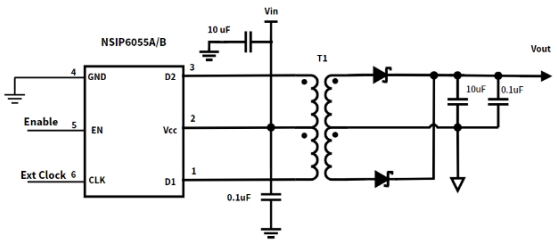


Figure 11.3 Unstable output voltage and low load current

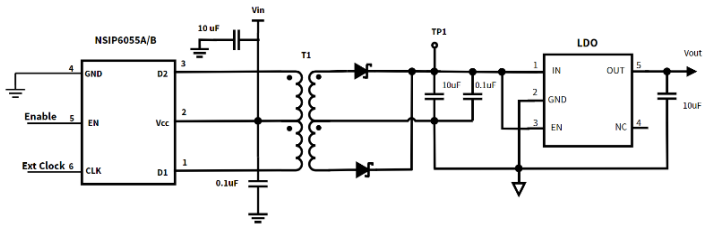


Figure 11.4 Stable output voltage and wide load current

Recommended transformer models can be found in NSIP6055x Demo Use Guide document.

12. Layout

12.1 Layout Guidelines

- The recommended capacitance value of the V_{IN} pin ranges from 1μF to 10μF and should be connected to the ground using a low ESR ceramic bypass capacitor.
- Refer to Figure 12.1 for PCB layout. The GND pin of the device should be connected to the PCB GND plane using two vias to achieve minimal inductance.
- The connection of the device D1 and D2 pins to the primary terminal of the transformer, and the connection of the device V_{CC} pins to the center tap of the transformer must be as close as possible to reduce the inductance of the wire.
- The recommended rectifier diode is the Schottky diode, which has a low forward voltage to maximize efficiency.
- The device V_{CC} pins and transformer center taps must be buffered to GND using a low ESR ceramic bypass capacitor. The recommended capacitors should have a voltage rating of at least 16V and capacitance values ranging from 1μF to 10μF.
- The V_{OUT} pins must be buffered to ISO ground by a low ESR ceramic bypass capacitor. It is recommended to use 0.1μF in parallel with 10μF. Capacitors must have a minimum16V rated voltage.

12.2 Layout Example

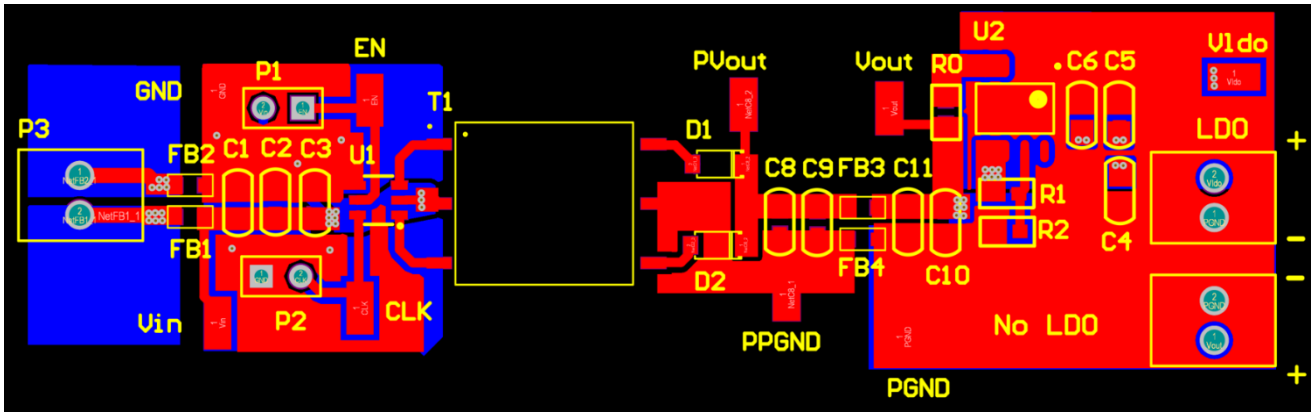
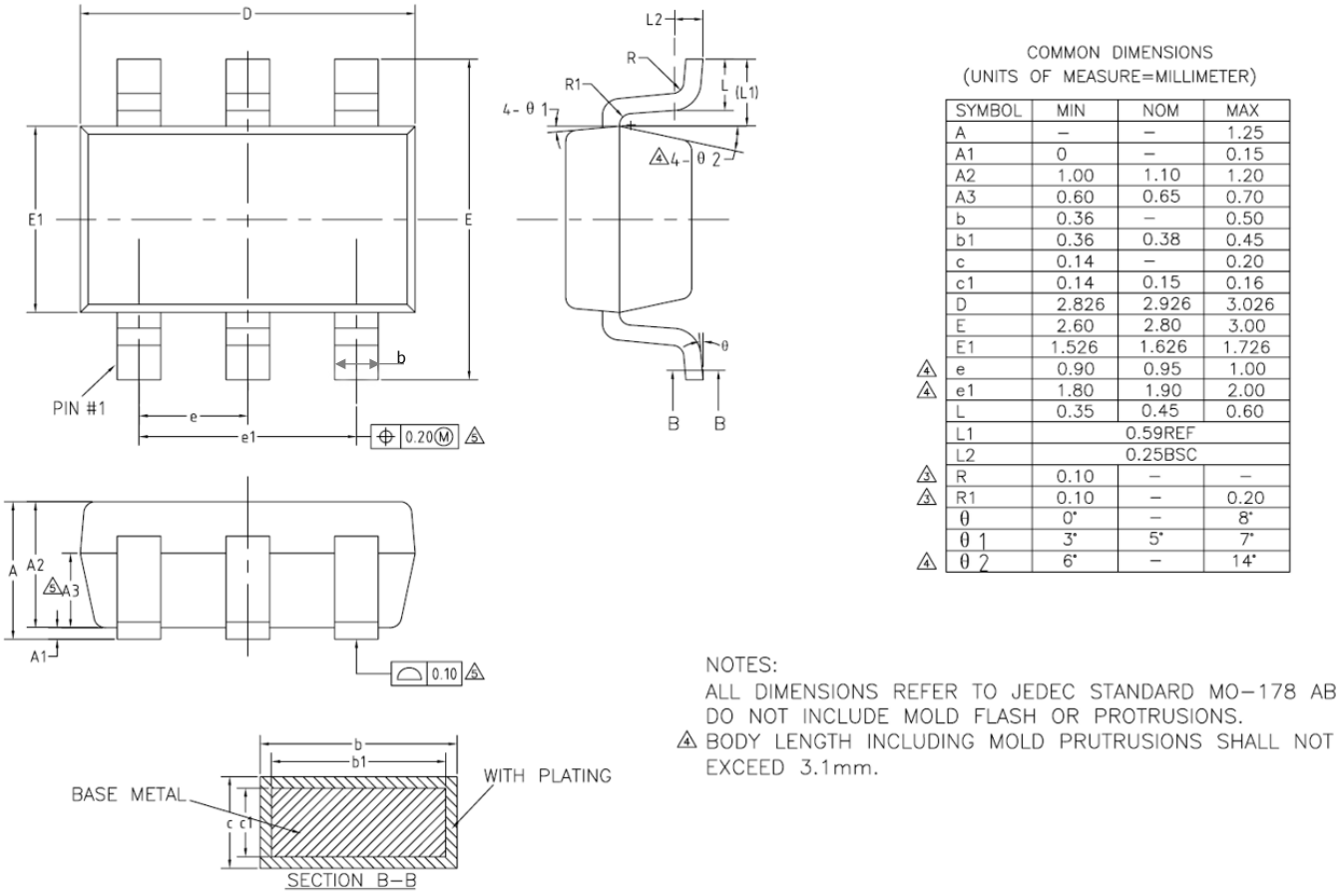


Figure 12.1 Layout Example of 2-Layer Board (NSIP6055x)

13. Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.25
A1	0	–	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.36	–	0.50
b1	0.36	0.38	0.45
c	0.14	–	0.20
c1	0.14	0.15	0.16
D	2.826	2.926	3.026
E	2.60	2.80	3.00
E1	1.526	1.626	1.726
4 e	0.90	0.95	1.00
4 e1	1.80	1.90	2.00
L	0.35	0.45	0.60
L1	0.59REF		
L2	0.25BSC		
3 R	0.10	–	–
3 R1	0.10	–	0.20
θ	0°	–	8°
θ 1	3°	5°	7°
4 θ 2	6°	–	14°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO–178 AB
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4 BODY LENGTH INCLUDING MOLD PRUTRUSIONS SHALL NOT EXCEED 3.1mm.

Figure 13.1 SOT23-6 Package Shape and Dimension in millimeters

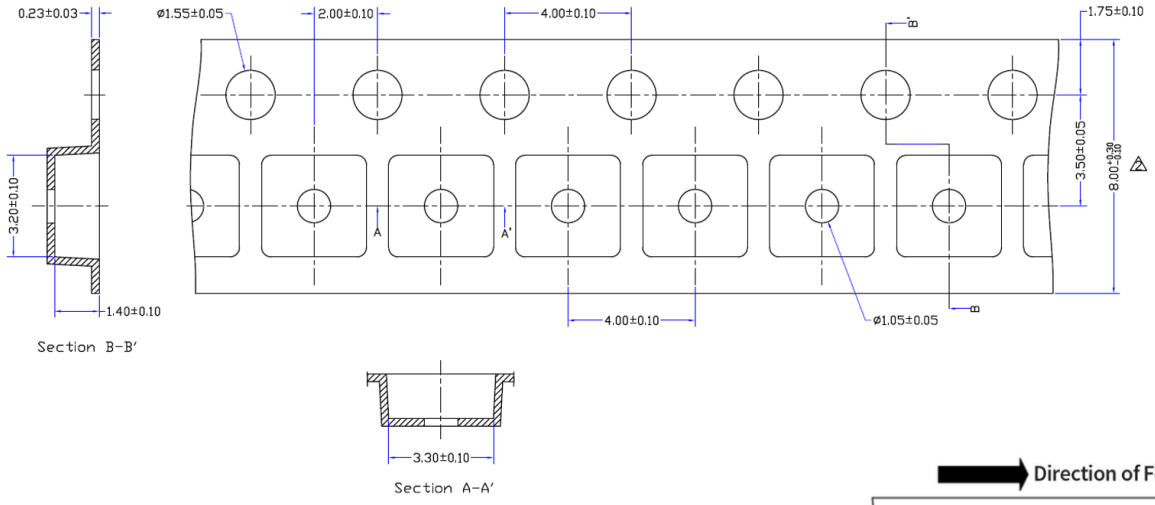
14. Order Information

Part Number	*Operating Temperature Range*	*Marking Information*	*MSL*	*Package Type*	*Package Drawing*	*SPQ*
NSIP6055A-Q1STCR	−40 to 125°C	55AQ	1	SOT23-6L	SOT23-6L	3000
NSIP6055B-Q1STCR	−40 to 125°C	55BQ	1	SOT23-6L	SOT23-6L	3000

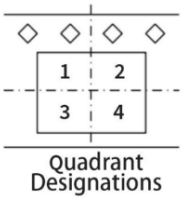
15. Documentation Support

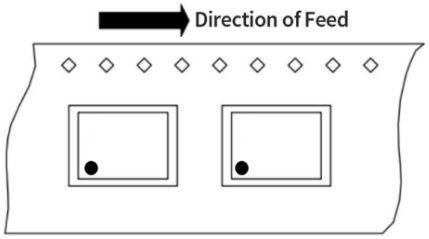
Part Number	*Product Folder*	*Datasheet*	*Application Note*
NSIP6055A-Q1STCR	Click here	Click here	Click here
NSIP6055B-Q1STCR	Click here	Click here	Click here

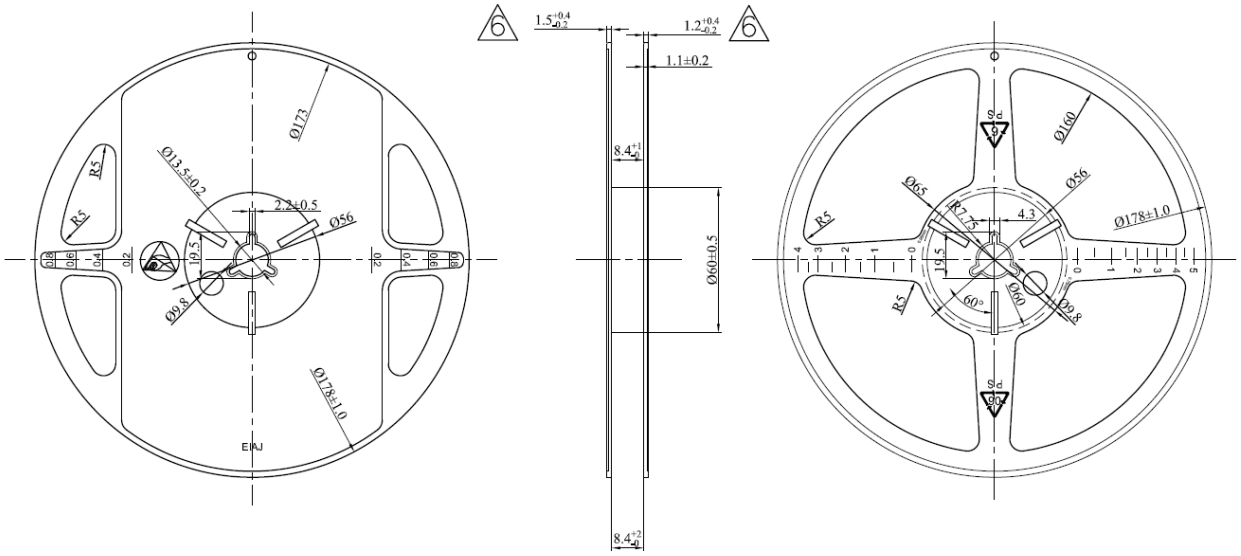
16. Tape and Reel Information



NOTES:
1.MATERIAL:CONDUCTIVE PS
2.ALL DIMS IN MM
3.There must not be foreign body adhesion and the state of the surface must be excellent
4.A permissible difference of the accumulation pitch of the sending hole is assumed to be ±0.2 up to 10 pitches
5.ø560 PAPER-Reel, 255000pockets(1020m)
6.Surface resistance 1X10E5~1X10E9 OHMS/SQ







NOTES:
1、Material: Polystyrene (black).
2、Flatness: Maximum allowed 2mm.
3、All dimensions are in millimeters.
4、Surface resistivity: 10^5 to 10^{10} OHMS/SQ.
5、All dimensions, unless specified, have a tolerance of ±0.25.

Figure 16.1 Tape and Reel Information of SOT23-6L

17. Revision History

Revision	Description	Date
1.0	Initial Version	2024/8/8
1.1	Update quadrant designations of tape and reel information. Added the Soft-start time and Soft-start time delay parameters of NSIP6055B.	2024/12/10

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