NOVOSENSE

NSIP6051-Q1

Transformer Driver for Isolated Power Supplies

Datasheet (EN) 1.1

Product Overview

The NSIP6051 is a push-pull transformer driver specially designed for small size, low-power isolation power supply with low standby power consumption. The periphery of the circuit only requires simple input and output filter capacitors, isolation transformer, and rectifier circuits.

Its internal integrated oscillator provides a pair of high-precision complementary signals to drive two N-channel MOSFETs. The internal design of the chip follows a symmetrical structure, which can effectively ensure the high symmetry of the two power MOSFETs and avoid magnetic bias during the working process of the circuit.

Ultra-low noise and EMI are achieved by slew rate control of the output switch voltage and through Spread Spectrum Clocking (SSC). The internal protection features include over

current protection, under-voltage lockout, thermal shutdown and break-before-make circuitry.

The NSIP6051 is available in a small SOT-23 (5) package, and is specified for operation at temperatures from –40°C to 125°C.

Key Features

- Push-pull driver for transformers
- Support 2.25V to 5.5V supply
- Ultra-low EMI
- Over-current protection (OCP)
- Over temperature protection
- Spread spectrum clocking
- Slew-rate control
- Small 5-pin SOT-23 package
- AEC-Q100 Grade 1 Qualified
- RoHS & REACH Compliance

Applications

- Isolated interface power supply for I2C, CAN, RS-485, RS-422, RS-232, SPI, Low-Power LAN
- IGBT gate drive power supply

Device Information

Part Number	Package	Body Size
NSIP6051-Q1STAR	SOT23- 5L	2.90 mm x 1.60 mm

Functional Block Diagrams

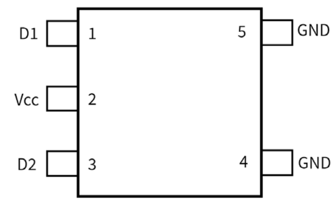

Figure 1. NSIP6051

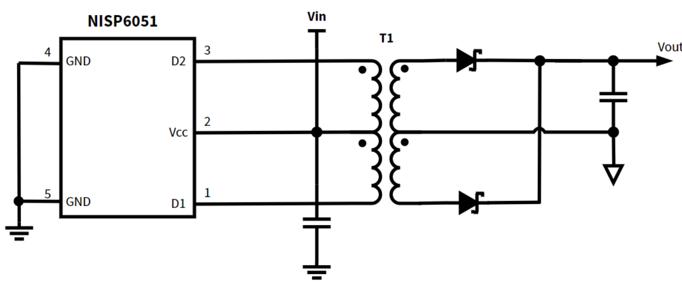

Figure 2. Simplified Schematic

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1. Pin Configuration and Functions

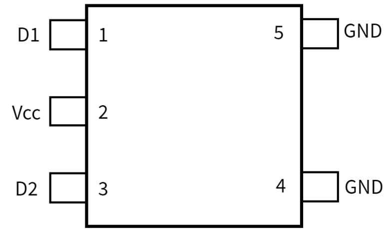


Figure 1.1 NSIP6051

Table1.1 Pin Functions

PIN NO.	SYMBOL	FUNCTION
1	D1	Open Drain output 1. Connect to transformer primary side 1.
2	V_{CC}	Power supply. Connect a 0.1μF and a 10μF low ESR capacitor.
3	D2	Open Drain output 2. Connect to transformer primary side 2.
4,5	GND	Device ground. Connect this pin to board ground.

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	V_{CC}	-0.3		6	V	
Output switch voltage	V_{D1}, V_{D2}			16	V	
Junction temperature	T_J	-40		150	°C	
Storage Temperature	T_{stg}	-55		150	°C	

3. ESD Ratings

Parameters	Ratings	Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD ● All pins	±8.0	kV
	Charged device model (CDM), per AEC-Q100-011-RevB ● All pins	±2.0	kV

4. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit	Comments
Supply voltage	V_{CC}	2.25		5.5	V	
Output switch voltage	V_{D1}, V_{D2}			12	V	
D1 and D2 output switch current – Primary-side	I_{D1}, I_{D2}			350	mA	V_{CC} = 5 V ± 10% V_{CC} = 3.3 V ± 10%
Ambient Temperature	Ta	-40		125	℃	

5. Thermal Information

Parameters	Symbol	SOT23-5	Unit
IC Junction-to-air thermal resistance	θ_{JA}	162.5	°C/W
Junction-to-board thermal resistance	θ_{JB}	56.2	°C/W
Junction-to-case (top) thermal resistance	θ_{JCtop}	96.2	°C/W
Junction-to-top characterization parameter	Ψ_{JT}	35	°C/W
Junction-to-board characterization parameter	Ψ_{JB}	55	°C/W

6. Electrical Characteristics

Over full range of recommended operating conditions, unless otherwise noted. All typical value is at T_A=25°C, V_{CC}=5V.

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Switch-on resistance	R_{ON}		0.74	1.5	Ω	V_{CC} = 3.3 V ± 10%,
			0.59	1.27	Ω	V_{CC} = 5 V ± 10%,
Average supply current	I_{CC}		0.87	1.1	mA	V_{CC} = 3.3 V ± 10%, no load
			1	1.25		V_{CC} = 5 V ± 10%, no load
D1, D2 Average switching frequency	f_{SW}	320	425	550	kHz	V_{CC} = 5 V ± 10%, V_{CC} = 3.3 V ± 10% See Figure 9.1
Spread Spectrum Clocking			±5.5 %			
Positive-going UVLO threshold	V_{CC+} (UVLO)			2.25	V	
Negative-going UVLO threshold	V_{CC-} (UVLO)	1.7			V	
UVLO threshold hysteresis	VHYS (UVLO)		0.3		V	
Protection current threshold		0.35	0.67	0.99	A	
Current limit			0.38	0.55	A	
THERMAL SHUT DOWN						
T_{SD} turn on temperature	T_{SD+}	152	169	180	°C	
T_{SD} turn off temperature	T_{SD-}	130	150	166	°C	
T_{SD} hysteresis	ΔT_{SD}	13	19		°C	

7. Switching Characteristics

Over full range of recommended operating conditions, unless otherwise noted.

Parameters	Symbol	Min	Typ	Max	Unit	Comments
D1, D2 output rise time	t_{r-D}		78		ns	V_{CC} = 3.3 V ± 10%, See Figure 9.1
			91		ns	V_{CC} = 5 V ± 10%, See Figure 9.1
D1, D2 output fall time	t_{f-D}		54		ns	V_{CC} = 3.3 V ± 10%, See Figure 9.1
			60		ns	V_{CC} = 5 V ± 10%, See Figure 9.1
Break-before-make time	t_{BBM}		150		ns	V_{CC} = 3.3 V ± 10%, See Figure 9.1
			150		ns	V_{CC} = 5 V ± 10%, See Figure 9.1

8. Typical Characteristics

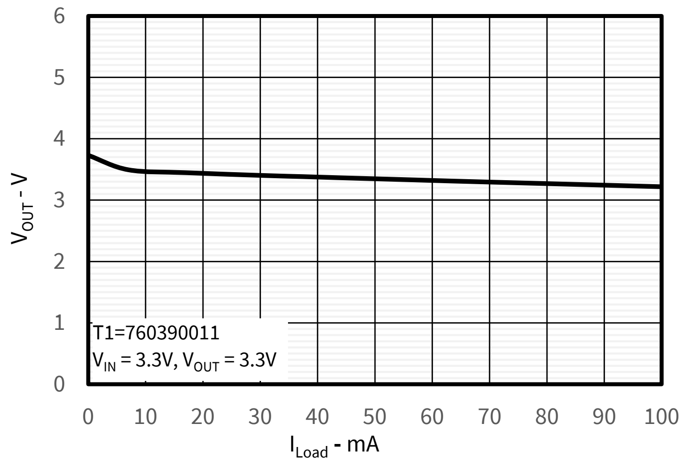


Figure 8.1 Output Voltage vs Load Current

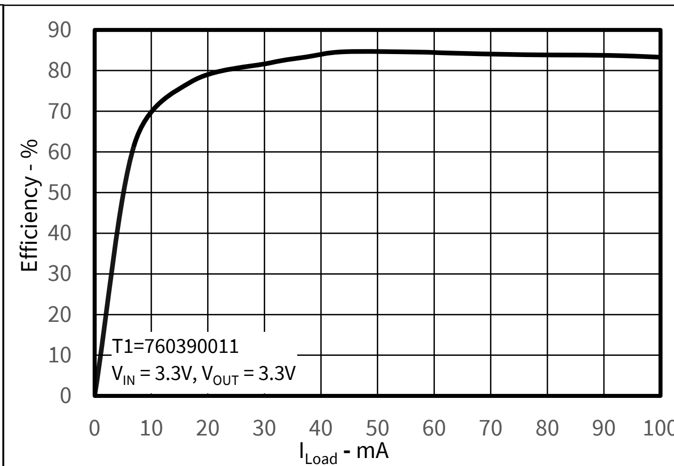


Figure 8.2 Efficiency vs Load Current

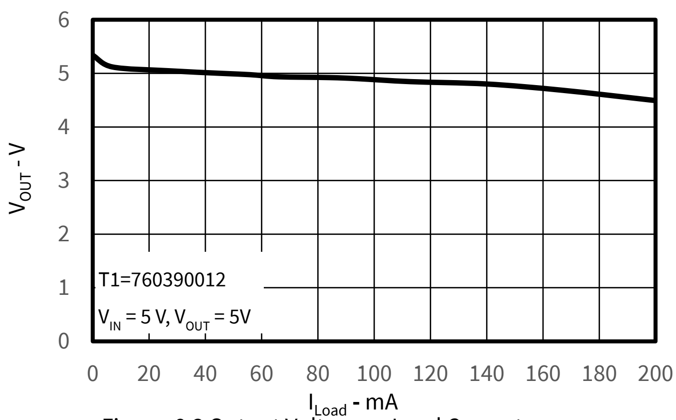


Figure 8.3 Output Voltage vs Load Current

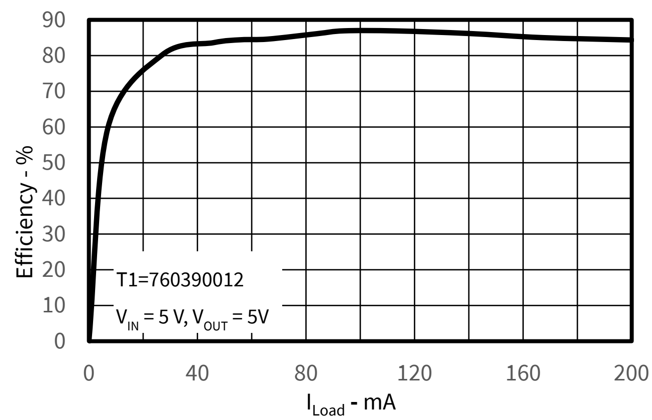


Figure 8.4 Efficiency vs Load Current

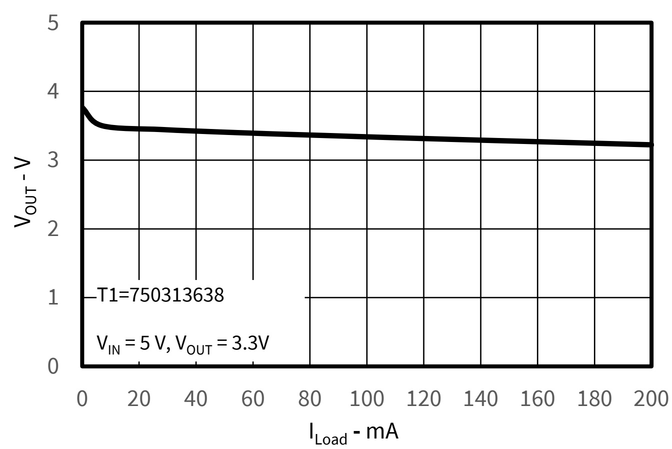


Figure 8.5 Output Voltage vs Load Current

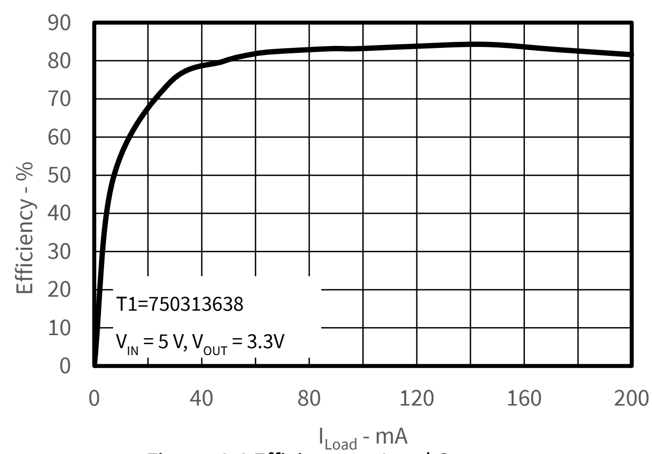


Figure 8.6 Efficiency vs Load Current

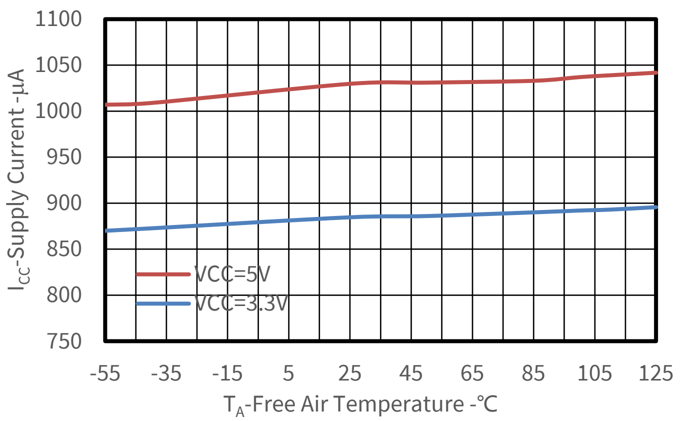


Figure 8.7 Average Supply Current vs Free-Air Temperature

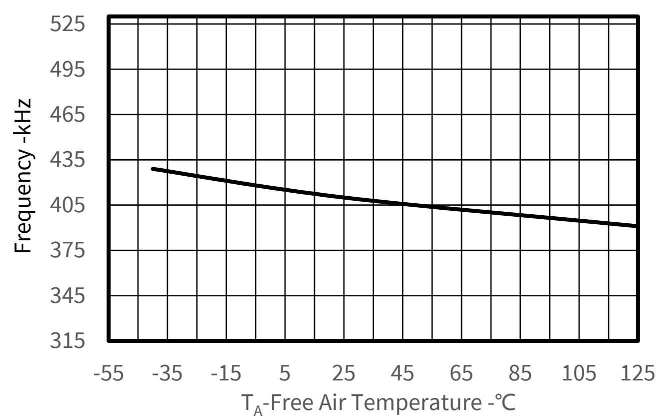


Figure 8.8 Average Frequency vs Free-Air Temperature

9. Parameter Measurement Information

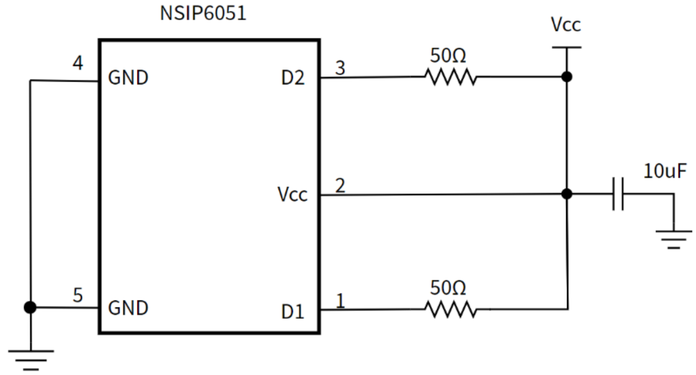


Figure 9.1 Test Circuit for FSW, $T_{r\text{-}D}$, $F_{t\text{-}D}$, T_{BBM}

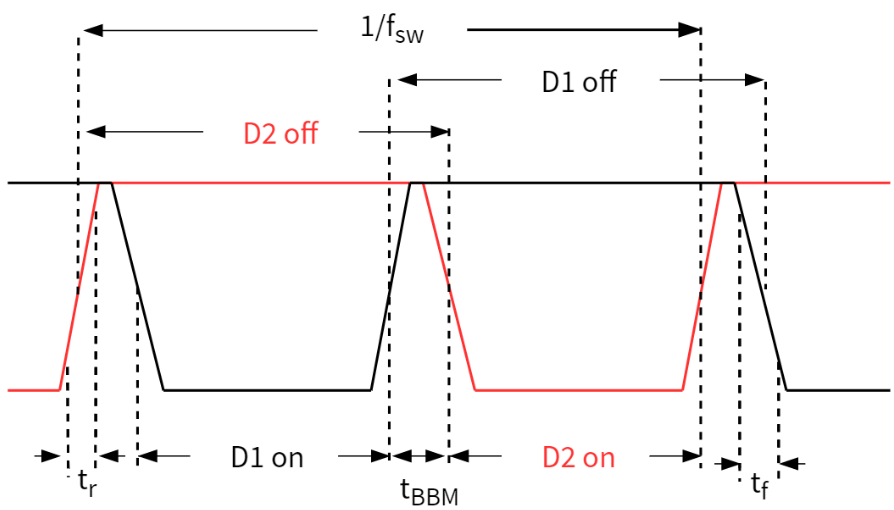


Figure 9.2 Timing Diagram

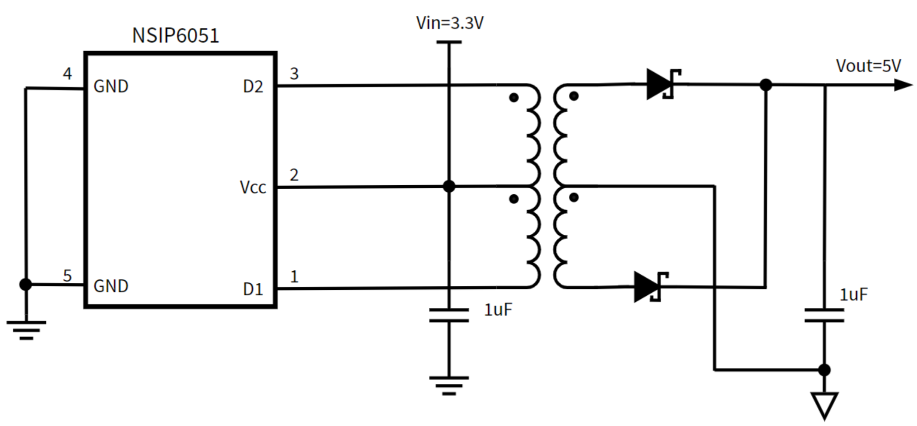


Figure 9.3 Measurement Circuit for Unregulated Output

10. Detailed Description

10.1 Overview

The NSIP6051 is transformer driver designed for low cost, small size, isolated DC-DC converters in push-pull topologies. The device consists of an oscillator and a gate driver. the output frequency of the oscillator is divided by frequency divider, which provides two complementary output signals with a duty cycle of 50%, and a dead time tBBM is designed between the two drives to avoid D1 and D2 conduction at the same time.

In order to improve EMI performance, the NSIP6051 oscillator has added spread spectrum clocking function. NSIP6051 integrates a thermal shutdown module and a current clamping function when the current is too large, to ensure that the chip itself works in the safety zone.

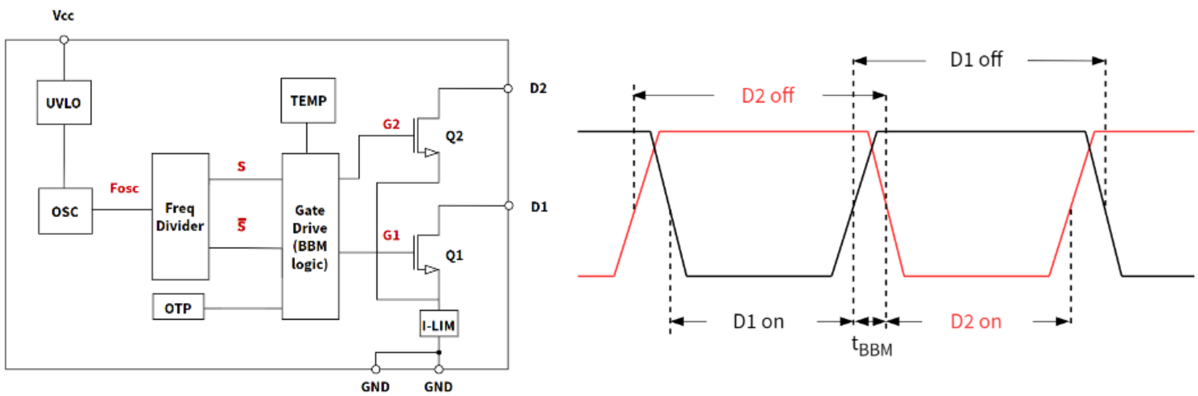


Figure 10.1 Functional Block Diagram and Output Timing with Break-Before-Make Action

10.2 Feature Description

10.2.1 Push-Pull Converter

Push-pull converters require transformers with center-taps to transfer power from the primary to the secondary.

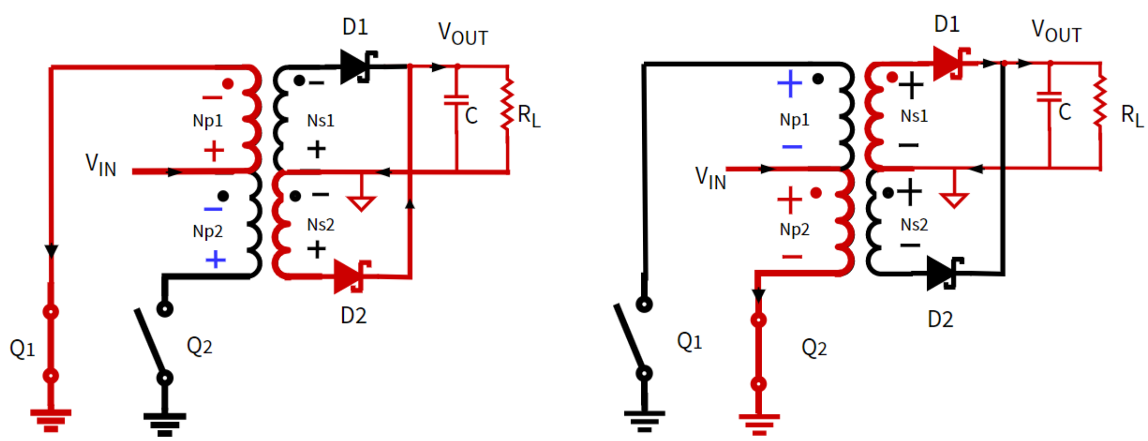


Figure 10.2 Switching Cycles of a Push-Pull Converter

The equivalent schematic diagram of the working process of a push-pull converter is shown in Figure 10.2. Switches Q1 and Q2 work in turns, with a duty cycle of nearly 50%. When Q1 is turned on, the input power flows from the center-tap input port Vin of the transformer to the transformer primary winding Np1, and from Np1 to switches Q1 and GND. At the same time, the energy is transferred to the secondary side through the transformer. The output current flows out from the secondary winding Ns2, transmits it to the output V_{OUT} through the rectifier diode D2, and finally returns to the Ns2 from the output GND after passing through the load. The working process of switch Q2 is basically the same as that of Q1.

When the circuit is working, each winding of the transformer (Np1, Np2, Ns1, Ns2) will generate a corresponding induced voltage. The amplitude of the induced voltage is proportional to the ratio of turns of the transformer winding. The voltage stress of Q1 and Q2 during the operation of the push-pull converter is 2×Vin voltage.

Start-Up Mode

When the voltage at the V_{CC} ramps up to 2.25V, the internal oscillator starts to work. The output stage starts to switch, and the drain signal amplitude of D1 and D2 has not reached the maximum value.

Current Limit

The NSIP6051 device performs current limiting by clamping the output current. When the output current increases to the threshold current, the output gate drive voltage clamp. The device has a current limiting function that can help isolate the overcurrent of the power transformer, but overheating losses need to be considered and may lead to overtemperature protection.

Over Temperature Protection

The NSIP6051 device supports Over Temperature Protection. When the junction temperature of the device is higher than the protection temperature threshold, the device will turn off output to protect the device from overheating damage. When the junction temperature is lower than the T_{SD-}, the device will resume startup.

Spread Spectrum

Radiation emission is an important concern in high current switching power supplies. NSIP6051 has the ability to modulate its internal clock, distributing transmission energy over a wider frequency band rather than a narrow peak, greatly improving EMI performance through its spread spectrum feature.

11. Application and Implementation

Note

The information contained in the following application section is not part of the NOVOSENSE component specification and NOVOSENSE does not guarantee its accuracy or completeness. NOVOSENSE's customers are responsible for determining whether components are suitable for their purpose, as well as validating and testing their design implementations to confirm system functionality.

11.1 Typical Application

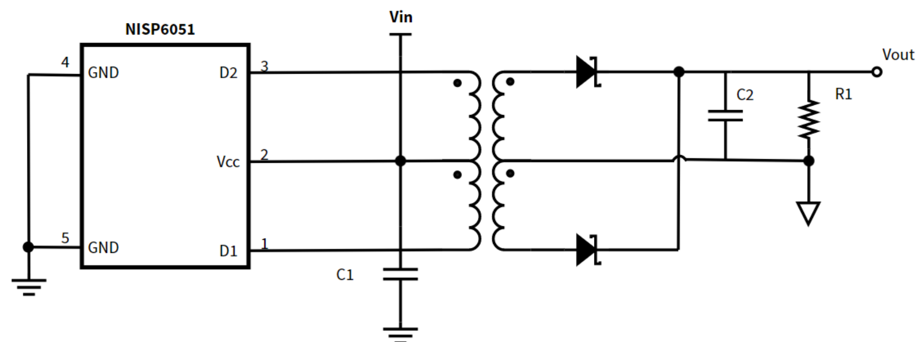


Figure 11.1 Typical Application Schematic

11.2 Design Requirements

For this design example, use the parameters listed in Table 11-1 as design parameters.

Table 11-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	3.3 V ± 10%
Output full load	5 V
Maximum load current	100 mA

11.2.1 Detailed Design Requirements

The following sections focus on the design of efficient push-pull conversions with high current drive capability.

11.2.1.1 LDO Selection

The minimum requirements for LDO: Note the following points:

- For a load current of 100 mA, it is recommended to choose a continuous output current capacity of 100 mA to 150 mA, slightly exceeding the specified load current.
- The output voltage of the isolated power supply should be greater than the output voltage of the LDO for proper operation of the LDO. Therefore, it is advisable to choose a LDO chip with the smallest possible dropout voltage.

$$V_{I\text{-}min} = V_{DO\text{-}max} + V_{O\text{-}max} \quad (1)$$

Note that the output voltage of the push-pull rectifier at the specified load current is equal to or higher $V_{I\text{-}min}$. Otherwise, the LDO will lose any line regulation.

- The maximum input voltage of the LDO must be higher than the rectified output at no-load. At this point, the secondary reaches its maximum voltage.

$$V_{S\text{-}max} = V_{IN\text{-}max} \times n \quad (2)$$

$V_{IN\text{-}max}$ is the maximum input voltage of the converter, and n is the ratio of turns of the transformer. Therefore, in order to prevent LDO damage, the maximum LDO input voltage must be higher than $V_{S\text{-}max}$.

11.2.1.2 Diode Selection

The selection of Schottky diodes needs to consider the following two points:

- Selecting a diode for the power supply, it is recommended to choose a low forward voltage and fast recovery diode. A low forward voltage helps improve the output efficiency of the power supply. For a low-cost option, the MBR0520L Schottky rectifier diode is recommend, with a typical forward voltage of 275mV and forward current of 100mA. However, if operating at ambient temperatures higher than 100°C, it is advisable to use the RB168M-40 diode.
- Considering the impact of temperature on forward voltage, it is advisable to select a rectifier with a low forward voltage drop, especially at low temperatures.

11.2.1.3 Capacitor Configuration

- In the design process, capacitors of 0.1μF and 10μF need to be placed in parallel between the input pin of the center-tap transformer and the device V_{cc} pin, to achieve the minimum line path and reduce the inductance of the wiring.
- To ensure low-inductance paths use two vias in parallel for each connection. The secondary rectifier output and the LDO output must be placed in parallel with 10μF and 0.1μF capacitors. It improves the stability of the power supply and reduce the output ripple.
- A low- ESR ceramic capacitor will meet circuit requirements.

11.2.1.4 Transformer Selection

11.2.1.4.1 V-t Product Calculation

Transformer selection needs to consider the Vt factor. the purpose is to prevent transformer saturation. The Vt_{min} is calculated by the maximum input voltage multiplying 50% of the maximum cycle time.

$$Vt_{min} \geq V_{IN-max} \times \frac{T_{max}}{2} = \frac{V_{IN-max}}{2 \times f_{min}} \quad (3)$$

Take the values from the data sheet into Equation 3 yields:

$$Vt_{min} \geq \frac{3.6V}{2 \times 320kHz} = 5.6V\mu s \quad \text{for 3.3V}$$

$$Vt_{min} \geq \frac{5.5V}{2 \times 320kHz} = 8.6V\mu s \quad \text{for 5V applications} \quad (4)$$

Other important factors such as isolation voltage, transformer power and turns ratio must be considered before the final selection decision is made.

11.2.1.4.2 Turns Ration Estimate

Assumed the rectifier diode and linear regulator have been selected, and the V-t product of the selected transformer is not less than 8.7Vμs. The minimum turns ratio that allows the push-pull converter to operate perfectly over a specified current and temperature range needs to be determined.

From the LDO selection section. The V_{S-min} must be large enough to allow the maximum voltage to drop V_{F-max} to cross the rectifier diode and still provide enough input voltage to the regulator to maintain voltage stability.

$$V_{S-min} = V_{F-max} + V_{DO-max} + V_{O-max} \quad (5)$$

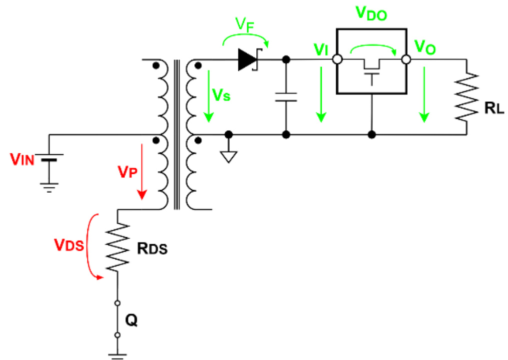


Figure 11.2 Establishing the Required Minimum Turns Ratio Through $N_{min} = 1.031 \times V_{s-min}/V_{P-min}$

The minimum available primary voltage V_{P-min} is calculated. Drain-source voltage of the NSIP6051 is V_{DS-max}. The minimum converter input voltage is V_{IN-min}:

$$V_{P-min} = V_{IN-min} - V_{DS-max} \quad (6)$$

V_{DS-max} is the product of the maximum $R_{DS(on)}$ and I_D values for a given supply specified in the NSIP6051 data sheet:

$$V_{DS-max} = R_{DS-max} \times I_{Dmax} \quad (7)$$

Then inserting Equation 7 into Equation 6 yields:

$$V_{P-min} = V_{IN-min} - R_{DS-max} \times I_{Dmax} \quad (8)$$

Inserting Equation 8 and Equation 5 into Equation 9 provides the minimum turns ration with:

$$n_{min} = 1.031 \times \frac{V_{F-max} + V_{DO-max} + V_{O-max}}{V_{IN-min} - R_{DS-max} \times I_{D-max}} \quad (9)$$

Example:

For a 3.3 V_{IN} to 5 V_{OUT} converter using the rectifier diode MBR0520 and the LDO TPS76350, at a load current of 100 mA and a maximum temperature of 85°C are V_{F-max} = 0.2 V, V_{DO-max} = 0.2 V, and $V_{O\_FullLoad\_max}$ = 5.175 V, $I_{OUT-max}$ = 0.1A.

Assume that the input power supply accuracy is ±2%, VIN-min = 3.234 V. From the NSIP6051 data sheet with RDS-max = 1.27Ω,
ID-max = 350 mA.
Inserting in these values and do the calculation:

$$N_{min} = 1.031 \times \frac{0.2V + 0.2V + 5.175V}{3.234V - 1.5\Omega \times 350mA} = 2.12 \quad (10)$$

11.2.1.4.3 Recommended transformer configuration solution

The following circuits are recommended. Use the unstable output voltage circuit in Figure 11.3 or stable output voltage in Figure 11.4.

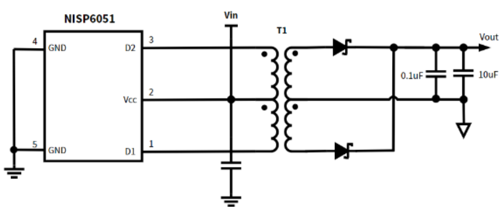


Figure 11.3 Unstable output voltage and low load current

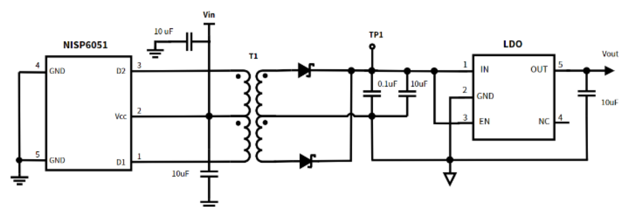


Figure 11.4 Stable output voltage and wide load current

Recommended transformer models can be found in NSIP6051 Demo Use Guide document.

12. Layout

12.1 Layout Guidelines

- The recommended capacitance value of the V_{IN} pin ranges from 1μF to 10μF and should be connected to the ground using a low ESR ceramic bypass capacitor.
- Refer to Figure 12.1 for PCB layout. The GND pin of the device should be connected to the PCB GND plane using two vias to achieve minimal inductance.
- The connection of the device D1 and D2 pins to the primary terminal of the transformer, and the connection of the device V_{CC} pins to the center tap of the transformer must be as close as possible to reduce the inductance of the wire.
- The recommended rectifier diode is the Schottky diode, which has a low forward voltage to maximize efficiency.
- The device V_{CC} pins and transformer center taps must be buffered to GND using a low ESR ceramic bypass capacitor. The recommended capacitors should have a voltage rating of at least 16V and capacitance values ranging from 1μF to 10μF.
- The V_{OUT} pins must be buffered to ISO ground by a low ESR ceramic bypass capacitor. It is recommended to use 0.1μF in parallel with 10μF. Capacitors must have a minimum16V rated voltage.

12.2 Layout Example

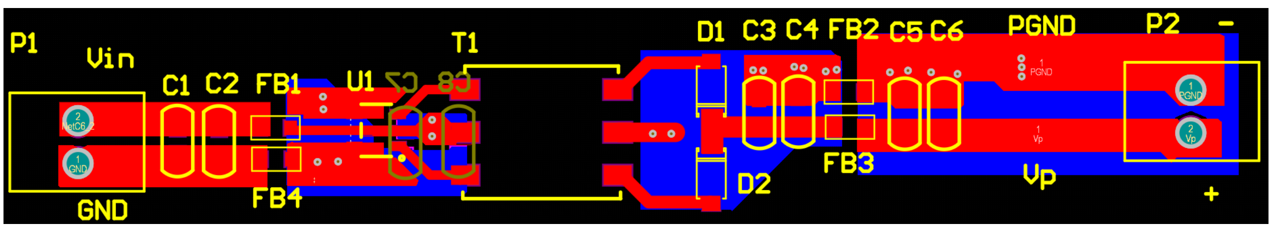
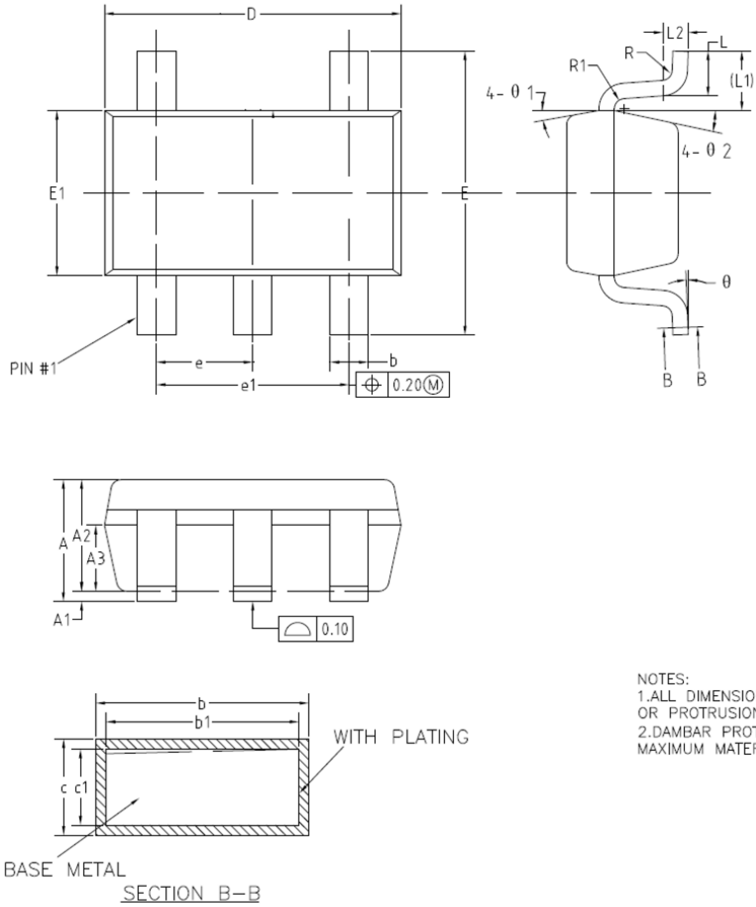


Figure 12.1 Layout Example of 2-Layer Board (NSIP6051)

13. Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.25
A1	0	–	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b (4)	0.34	–	0.45
b1 (4)	0.34	0.38	0.41
c (4)	0.12	–	0.20
c1 (4)	0.12	0.15	0.16
D	2.826	2.926	3.026
E	2.60	2.80	3.00
E1 (3)	1.526	1.626	1.700
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
K (2)	0	–	0.20
L	0.30	0.40	0.60
L1	0.59REF		
L2	0.25BSC		
M (2)	0.10	0.15	0.20
R	0.05	–	0.20
R1	0.05	–	0.20
θ	0°	–	8°
θ1	8°	10°	12°
θ2	10°	12°	14°

NOTES:
1. ALL DIMENSIONS REFER TO JEDEC STANDARD MO-178 AA DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION.

Figure 13.1 SOT23-5 Package Shape and Dimension in millimeters

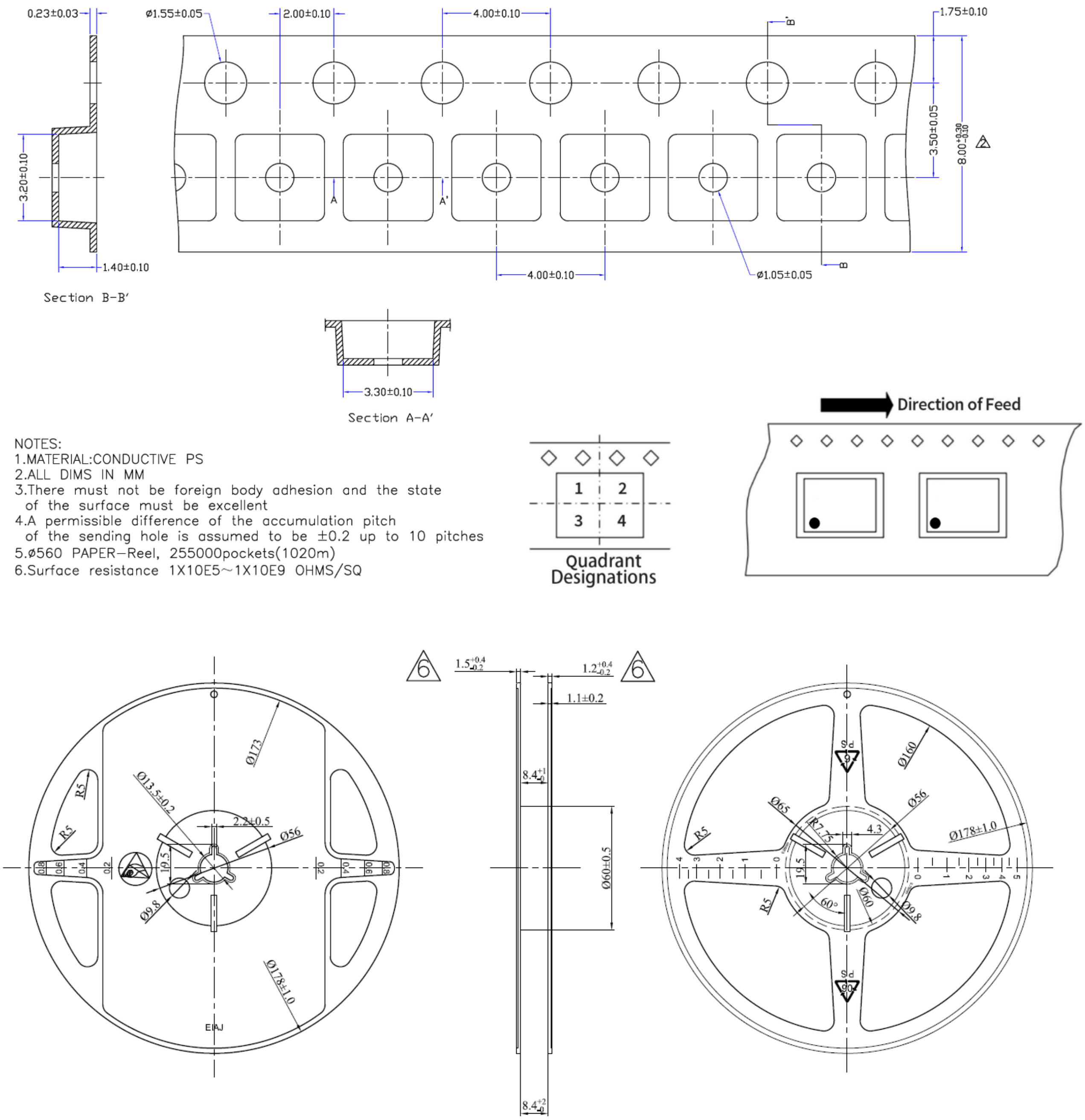
14. Order Information

Part Number	***Operating Temperature Range***	***Marking Information***	***MSL***	***Package Type***	***Package Drawing***	***SPQ***
NSIP6051-Q1STAR	(−40 to 125) °C	051Q	1	SOT23-5L	SOT23-5L	3000

15. Documentation Support

Part Number	***Product Folder***	***Datasheet***	***Application Note***
NSIP6051-Q1STAR	Click here	Click here	Click here

16. Tape and Reel Information



NOTES:

1、Material: Polystyrene (black).

2、Flatness: Maximum allowed 2mm.

3、All dimensions are in millimeters.

4、Surface resistivity: 10^5 to 10^{10} OHMS/SQ.

5、All dimensions, unless specified, have a tolerance of ±0.25.

Figure 16.1 Tape and Reel Information of SOT23-5L

17. Revision History

Revision	Description	Date
1.0	Initial Version	2024/8/8
1.1	Update protection current threshold, quadrant designations of tape and reel information.	2025/7/10

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