NOVOSENSE

NSIP3266-Q1

26V H-Bridge Transformer Driver for Isolated Supplies

Datasheet (EN) 1.0

Product Overview

The NSIP3266 H-bridge transformer driver provides a simple solution for designing isolated power supplies. The device drives the primary coil of the transformer with a voltage range from 6.5V to 26V. The transformer's secondary-to-primary turn ratio defines the output voltage, allowing selection of virtually any isolated output voltage.

The NSIP3266 features adjustable switching frequency from 100 kHz to 1MHz with an external resistor, which provides the flexibility to optimize either efficiency or external component size.

A $\overline{\text{FAULT}}$ output is asserted when the device detects an overtemperature or overcurrent condition. In addition, the device features a low-power mode to reduce the overall supply current to 0.7mA (typ) when the driver is disabled.

The NSIP3266 is available in HMSOP8 package with operating temperature range from -40°C to 125°C.

Key Features

- Wide supply voltage range: 6.5 to 26V
- Ability to handle negative swing of (-10V) at EN pin
- Fault Detection and Indication
- Adjustable Frequency: 100 kHz to 1MHz
- Over-Temperature Protection
- Over-Current Protection
- Low supply current when disabled
- Undervoltage Lockout for input voltage
- Operating temperature range: -40°C to 125°
- AEC-Q100 Grade 1 Qualified
- RoHS & REACH Compliance

Applications

- Automotive On-Board Charger (OBC)
- Automotive DC/DC converter
- Automotive traction inverter & motor control
- GaN, IGBT and SiC gate driver bias supply

Device Information

Part Number	Package	Body Size
NSIP3266-Q1HMSR	HMSOP8	3.0 mm × 3.0 mm

Block Diagram

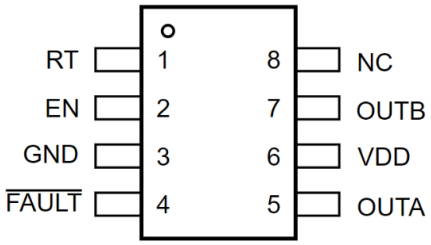

Figure 1. NSIP3266-Q1

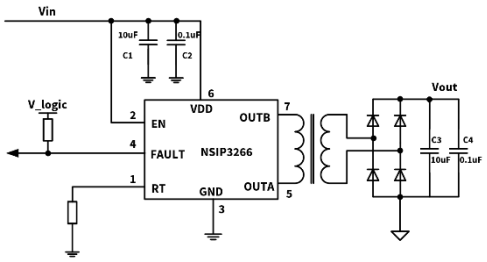

Figure 2. Simplified Schematic

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1. Pin Configuration and Functions

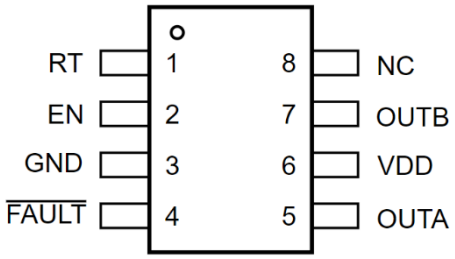


Figure 1.1 NSIP3266-Q1 Pin Configuration

Table 1.1 NSIP3266-Q1 Pin Description

NSIP3266 PIN NO.	*SYMBOL*	*FUNCTION*
1	RT	**Frequency Setting** Configure switching frequency (100 kHz–1 MHz) via external resistor between RT and GND. Defaults to 200 kHz if left floating.
2	EN	**Enable Control** **Enable:** Tie to VDD; **Disable:** Connect to GND. Disables all internal circuits.
3	GND	**Ground** Common reference for power and signals.
4	$\overline{\text{FAULT}}$	**Open-Drain $\overline{\text{FAULT}}$ Indicator** **Active Low:** Asserted during OCP (overcurrent) or OTP (overtemperature); **High-Z:** Normal operation. Requires external pull-up resistor (e.g., 10kΩ) to monitor status.
5	OUTA	**Transformer Drive Output A** H-bridge driver output for primary-side switching.
6	VDD	**Supply Voltage** Input voltage (6.5V–26V).
7	OUTB	**Transformer Drive Output B** H-bridge driver output for primary-side switching.
8	NC	**No Connection** Leave unconnected.
EP	GND	**Thermal Pad** Internally connected to GND. Solder to PCB ground plane with multiple vias for heat dissipation.

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit	Comments
Supply Voltage	V_{DD}	-0.3	30	V	
Output Voltage	V_{OUTA}, V_{OUTB}	-0.3	VDD+0.3	V	
		-2	VDD+0.3	V	Pulse<200ns
V_{OUTA}, V_{OUTB} I_{PK} Current	$I_{out(max)}$		0.8	A	
Enable Pins Voltage	EN	-10	VDD	V	
$\overline{FAULT}$ to GND	$\overline{FAULT}$	-0.3	6	V	
RT to GND	RT	-0.3	6	V	
Operating Junction Temperature	T_J	-40	150	°C	
Storage Temperature	T_{STG}	-55	150	°C	

3. ESD Ratings

Parameters	Ratings	Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD ● All pins	±2.0	kV
	Charged device model (CDM), per AEC-Q100-011-RevB ● All pins	±2.0	kV

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	6	26	V
V_{OUTA}, V_{OUTB} Continuous Current (RMS)	$I_{out(rms)}$		0.5	A
Enable Pin Voltage	V_{EN}	-6	V_{DD}	V
Operating Ambient Temperature	T_A	-40	125	°C

5. Thermal Information

Parameters	Symbol	HMSOP8	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	58.5	°C/W
Junction-to-Board Thermal Resistance	θ_{JB}	28.2	°C/W
Junction-to-Case (Top) Thermal Resistance	$\theta_{JC(top)}$	57.6	°C/W
Junction-to-Top Characterization Parameter	Ψ_{JT}	5.4	°C/W
Junction-to-Board Characterization Parameter	Ψ_{JB}	27.9	°C/W

Notes
(1) Four layers 2s2p PCB JEDEC JESD 51-7.

6. Electrical Characteristics

Over full range of recommended operating conditions, unless otherwise noted. All typical values are at T_A=25°C, V_{DD}=12V.

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Bias Currents						
Average supply current	I_{DD}		1.6	2	mA	V_{DD} = 12V, Fsw = 200kHz, EN = V_{DD}
Disable supply current	I_{DIS}		0.7	1.56	mA	V_{DD} = 12V, EN = GND
Over current protection threshold	$I_{threshold}$	1.5	2.6	3.2	A	
Deglitch time of OUTA or OUTB short circuit protection	T_{SCP}		500		ns	
Under Voltage Lockout (UVLO)						
V_{DD} turn-on threshold	$V_{DD\ ON}$		4.7	5.4	V	V_{DD} rising until device activation
V_{DD} turn-off threshold	$V_{DD\ OFF}$	4.1	4.4		V	V_{DD} falling until device shutdown
V_{DD} hysteresis	$V_{DD\ HYS}$		0.3		V	V_{DD} voltage difference between turn-on and turn-off thresholds
Enable Characteristics						
Enable signal high transition	V_{EN_H}		2.1	3.3	V	EN rising until device activation
Enable signal low transition	V_{EN_L}	1.0	1.3		V	EN falling until device shutdown
Enable signal hysteresis	$V_{EN\ HYS}$		0.8		V	EN voltage difference between turn-on and turn-off thresholds
Output Characteristics						
Output pull-up resistance	R_{OH}		1.26	2.0	Ω	I_{OUT} = -100mA, V_{DD} = 12V
Output pulldown resistance	R_{OL}		0.65	1.5	Ω	I_{OUT} = 100mA, V_{DD} = 12V
Max soft start time	SST		5		ms	The gate drive voltage of the power-MOSFETs rises from 0 V to 5 V
OUTA, OUTB leakage current	I_{LKG}	-1	0.1	1	μA	EN = GND, OUTA/OUTB is GND or V_{DD}
$\overline{\text{FAULT}}$ Open Drain Output						
Output low voltage	V_{OL}			0.5	V	Output is asserted, I_{OL} = 5mA
Leakage current at output high level	I_{LKG_FAULT}		0.4	1	μA	$\overline{\text{FAULT}}$ is not asserted, V_{FAULT} = 6V
Thermal Shut Down						
T_{SD} turn on temperature	T_{SD+}		175	181	°C	T_{SD} rising until device shutdown
T_{SD} turn off temperature	T_{SD-}	135	150		°C	T_{SD} falling until device activation
T_{SD} hysteresis	$T_{SD\ HYS}$		25		°C	T_{SD} thermal difference between turn-on and turn-off thresholds

7. Switching Characteristics

Over full range of recommended operating conditions, unless otherwise noted. All typical values are at T_A= 25°C, V_{DD}= 12 V.

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Initial switching frequency	F_{sw0}	156	200	235	kHz	RT pin floating
Adjustable switching frequency	F_{sw}	100		1000	kHz	
Switching frequency at RT = 39kΩ	$F_{sw\ 39k\Omega}$	372	417	470	kHz	RT = 39kΩ
Rise time	T_R		6		ns	OUTA/OUTB = 20% to 80% of V_{DD}, RL = 50Ω, CL = 50pF, V_{DD} = 12V, showing in Figure 9.1
Fall time	T_F		7		ns	OUTA/OUTB = 80% to 20% of V_{DD}, RL = 50Ω, CL = 50pF, V_{DD} = 12V, showing in Figure 9.1
Dead time	DT		4		ns	Connect a 20 Ω resistor in series between OUTA and OUTB., showing in Figure 9.2
EN Blanking Time	T_{BLANK}		2.3	3	μs	
Spread Spectrum Clocking						
Spread spectrum clocking	Δf_C		±6.7%			
Spread spectrum modulation frequency	fm		25		kHz	

8. Typical Characteristics

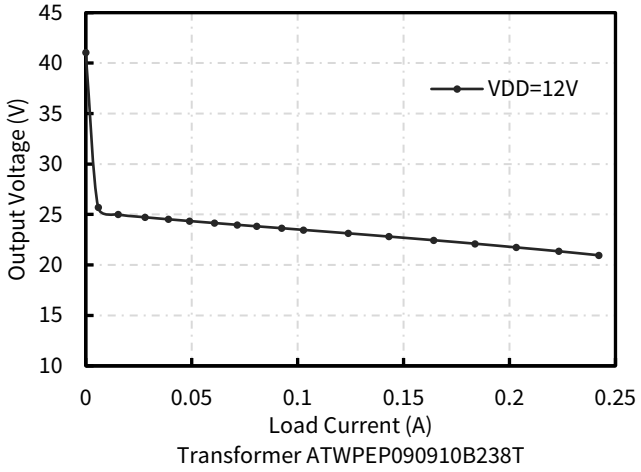


Figure 8.1 Output Voltage vs Load Current

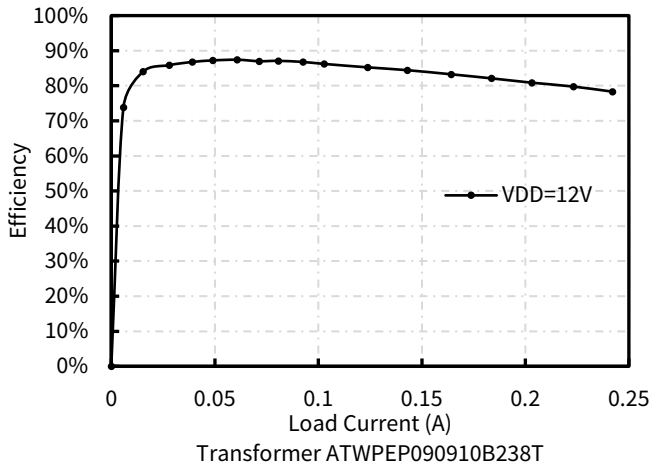


Figure 8.2 Efficiency vs Load Current

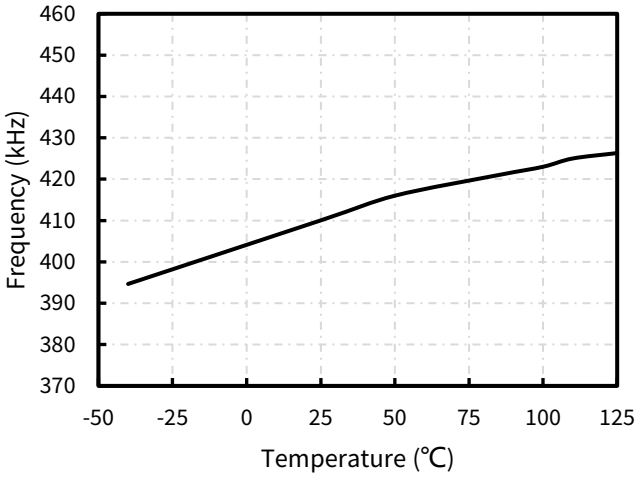


Figure 8.3 Frequency vs Free-Air Temperature at RT = 39kΩ

9. Parameter Measurement Information

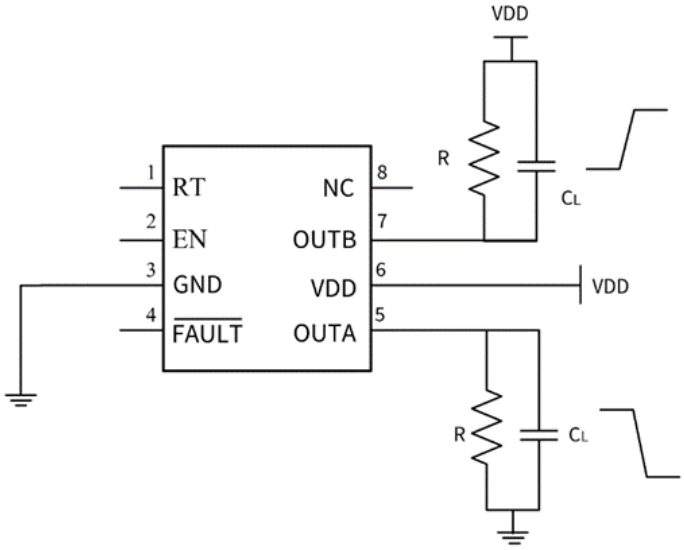


Figure 9.1 Test Circuit for T_R, T_F

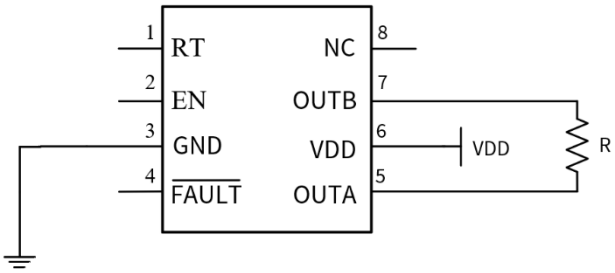


Figure 9.2 Test Circuit for DT

10. Function Description

10.1 Overview

The NSIP3266 is an isolated DC-DC switching controller optimized for H-bridge topologies. Compared to alternative solutions, the H-bridge architecture inherently simplifies design by eliminating the need for center-tapped transformers, reducing peripheral components, and lowering system cost. Operating from a wide input range of 6.5V to 26V, the device ensures broad compatibility across applications.

The NSIP3266 incorporates an short-circuit protection function that is triggered when the current exceeds safe thresholds, confining operation within the safe operating area (SOA) and shielding external components from surge damage. Switching frequency (100kHz–1MHz) is set via an external resistor on the RT pin for flexibility in efficiency and component size trade-offs.

The NSIP3266 provides a fault alarm signal ($\overline{\text{FAULT}}$ pin). When the device enters a short-circuit or overtemperature state, the $\overline{\text{FAULT}}$ pin outputs a low-level signal. If this pin is used, it should be connected to a 5V or 3.3V supply through a 10kΩ pull-up resistor. Additionally, the device includes internal oscillator and soft-start functions to eliminate dependency on external MCUs.

Functional Diagram

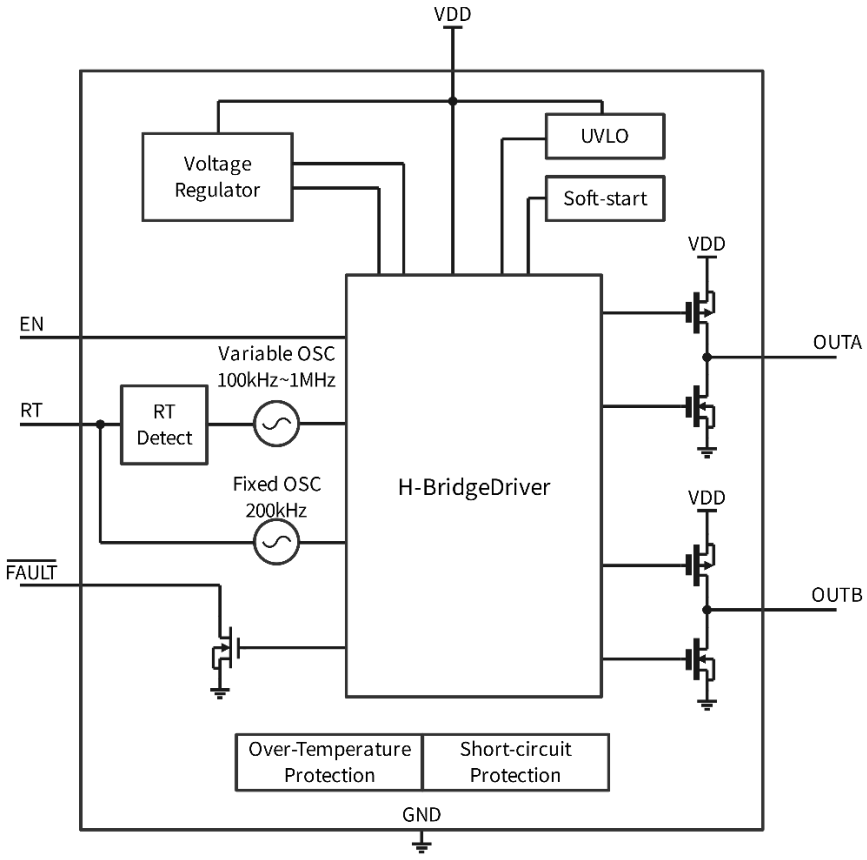


Figure 10.1 Functional Diagram

10.2 Feature Description

Start-Up Mode

Once the V_{DD} supply reaches 4.7V (typ) and the EN pin voltage rises above 2.1V (typ), the internal oscillator initiates operation, triggering switching activity in the output stage. However, during this initial phase, the gate voltage amplitude of MOSFETs D1 and D2 remains below its maximum rated value due to controlled soft-start behavior.

Soft Start

The NSIP3266 device implements a soft-start mechanism to prevent inrush current and protect transformers during startup. This feature is triggered under three conditions: initial power-up, enable signal (EN) rising edge, or post-protection recovery. During soft-start, the IC modulates the MOSFET's V_{gs} within the saturation region (where I_d is V_{gs}-controlled), enabling linear current scaling without dependency on the supply voltage. By incrementally stepping up V_{gs} in a staircase pattern, the drain current (I_d) rises gradually, eliminating current overshoot. Once startup completes, the MOSFET transitions to the variable-

resistance region (linear region), where stabilized V_{gs} minimizes conduction losses via low $R_{ds(on)}$. This approach balances smooth startup, transformer protection, and optimized efficiency in power systems demanding high reliability. The actual startup time (SST) is influenced by the output capacitance and load conditions. Under recommended operating conditions, the SST is typically less than 5ms.

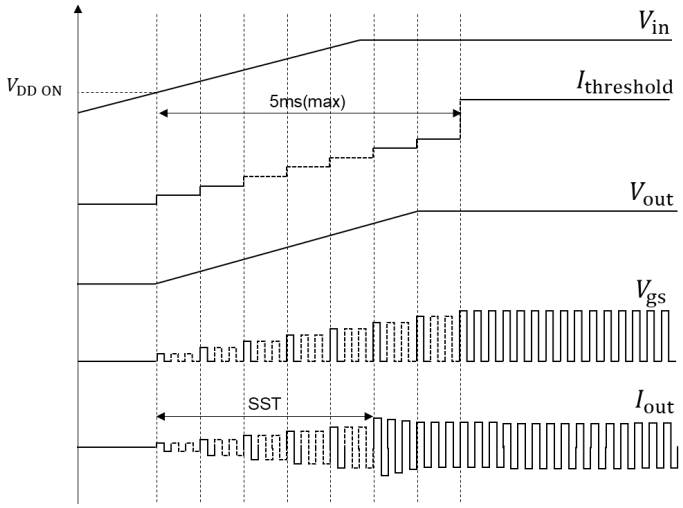


Figure 10.2 Waveform schematic diagram during soft start time

Disable Mode

The NSIP3266 incorporates a low-power disabled mode designed to minimize quiescent current consumption. When disabled, both OUTA and OUTB outputs enter a high-impedance (Hi-Z) state, effectively isolating the output stage to prevent unintended load interaction.

Short-Circuit Protection and $\overline{\text{FAULT}}$ asserts

The NSIP3266 features a multi-stage overcurrent protection (OCP) mechanism designed to address output overcurrent or short-circuit conditions. When the NMOS current exceeds a 2.6A (typical) threshold for 500ns, the protection system is triggered. Upon detection, the $\overline{\text{FAULT}}$ pin is immediately pulled low to disable N/PMOS switching signals, halting power delivery. If the fault persists, the system enters a 112ms hiccup shutdown phase to prevent thermal stress and component damage. After this period, the $\overline{\text{FAULT}}$ pin releases high, initiating a 5ms soft-start process to attempt system recovery. If the fault remains unresolved, the cycle (500ns detection, 112ms shutdown, and soft-start) repeats until normal operation resumes.

This hierarchical design ensures rapid fault response while prioritizing system safety. The 500ns deglitch time minimizes false triggers, and the hiccup mode reduces heat accumulation during prolonged faults. The inclusion of soft-start during recovery enables controlled power ramp-up, enhancing reliability in demanding applications. By balancing precision thresholds, thermal management, and staged recovery, the NSIP3266 delivers robust protection for power systems requiring high resilience.

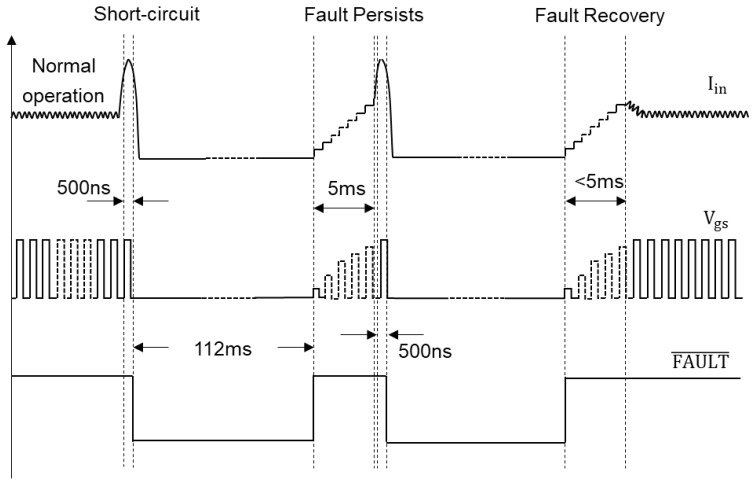


Figure 10.3 Waveform schematic diagram during over current protection

Over Temperature Protection

The NSIP3266 device supports overtemperature protection. When the junction temperature of the device is exceeds T_{SD+}, the device will turn off output to protect the device from overheating damage. When the junction temperature is lower than T_{SD-}, the device will resume startup.

Programming the Switching Frequency

The switching frequency f_{sw} of the NSIP3266 can be programmed by the resistor R_{set} connected between the RT pin and GND. The R_{set} can be determined by a given switching frequency. RT floating defaults to 200 kHz. Use Equation 1 or the curve in Figure 10.4.

$$R_{set}\,(k\Omega) = 28860 * fsw(KHz)^{-1.104} \quad (1)$$

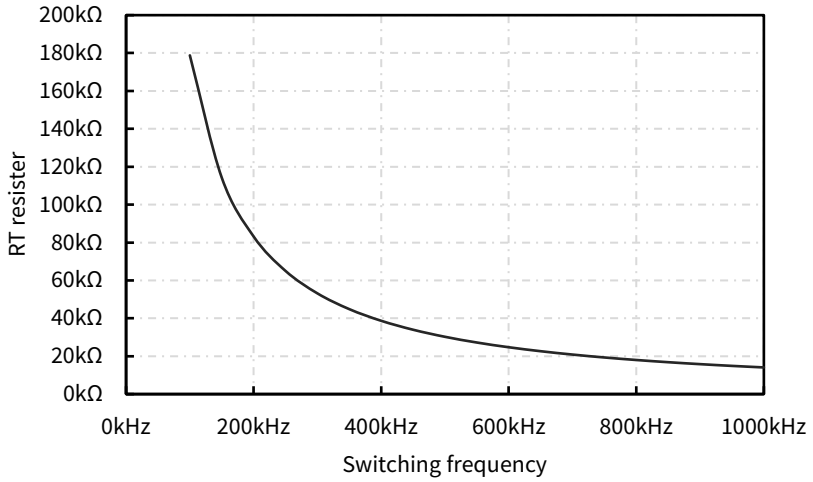


Figure 10.4 RT resister vs Switching frequency

Table 10.1 gives typical R_{set} values for a given f_{SW}.

Table 10.1 Typical Frequency vs. RT Resistance

R_{set} (KΩ)	f_{sw}(kHz)
180	100
68	246
33	464
24	607
20	700
16	900
13	1000

11. Application Note

11.1 Typical Application

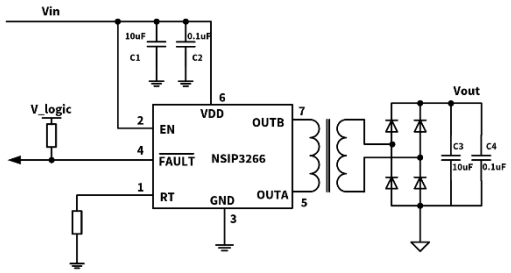


Figure 11.1 Typical Application Schematic

11.2 Design Requirements

For this design example, refer to Table 11.1 for key design parameters.

Table 11.1 Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	12 V ± 5%
Output voltage at full load	23 V
Maximum load current	170mA
Switching frequency	417KHz

11.2.1 Detailed Design Requirements

The following sections focus on the design of efficient H-bridge conversions with high voltage drive capability.

11.2.1.1 Input capacitance selection

As shown in Figure 11.1, capacitor C1 serves critical roles in input voltage stabilization, including energy buffering, low-frequency filtering, and bulk decoupling. To enhance high-frequency performance, ceramic capacitor C2 is deployed as a localized decoupling component and must be positioned in close proximity to the chip's power pins. During H-bridge converter switching transitions, C1 compensates for instantaneous current demands, with its capacitance value optimally selected between 1μF and 10μF. This range effectively balances transient response capability with input ripple attenuation, while C2 addresses high-frequency impedance through its ultra-low ESL characteristics. The dual-capacitor architecture ensures robust power integrity across both low and high frequency domains.

Voltage ratings must incorporate substantial derating margins (typically ≥150% of maximum input voltage) to ensure reliable operation. Multilayer ceramic capacitors (MLCCs) are strongly recommended due to their ultra-low equivalent series resistance (ESR), minimal parasitic inductance, and stable X7R/X8R temperature characteristics.

11.2.1.2 Output capacitance selection

While the H-bridge converter theoretically supports 100% duty cycle operation for full energy transfer, practical implementation mandates a defined dead-time interval (typically 10–100 ns) during complementary switching transitions. This prevents catastrophic shoot-through currents arising from simultaneous conduction in the bridge arms. During the dead-time phase, the output filter capacitor C3 assumes critical responsibility for maintaining load current continuity and voltage stability.

For optimal performance, C3 should be implemented as a multilayer ceramic capacitor (MLCC) with Capacitance range of 4.7μF to 10μF, which provides optimal filtering performance for the converter.

11.2.1.3 Output rectifier diode selection

The selection of output rectifier diodes needs to consider the following four points:

- **Low Forward Voltage:** Prioritize diodes with low V_f (typically <0.4V at rated current) to minimize conduction losses and improve power supply efficiency.
- **Fast Recovery Speed**: Select diodes with short reverse recovery time (trr) to reduce switching losses and prevent voltage overshoot.

- **High Thermal Stability:** Choose diodes with stable forward voltage across temperature ranges, especially in high ambient temperatures (e.g., >85°C).
- **Minimal junction capacitance:** Considering the increase in output voltage caused by the oscillation of rectifier diode junction capacitance and transformer leakage inductance under light load, it is recommended to choose rectifier diodes with smaller junction capacitance as much as possible.

11.2.1.4 Transformer Selection

11.2.1.4.1 V-t Product Calculation

Transformer selection needs to consider the Vt factor. The purpose is to prevent transformer saturation. The Vt_{min} is calculated by the maximum input voltage multiplying 50% of the maximum cycle time.

$$Vt_{min} \geq V_{IN-max} \times \frac{T_{max}}{2} = \frac{V_{IN-max}}{2 \times f_{min}} \quad (1)$$

Taking an example of f_{min} as 360kHz for NSIP3266, Equation 2 yields the minimum V-t products of:

$$Vt_{min} \geq \frac{12V*105\%}{2 \times 370kHz} = 17\ V\mu s \qquad \text{for 12V} \quad (2)$$

Other important factors such as isolation voltage, transformer power and turns ratio must be considered before the final selection decision is made.

11.2.1.4.2 Turns Ration Estimate

Assuming the rectifier diode have been selected, the V-t product of the selected transformer is not less than 17.5Vμs. The minimum turns ratio that allows the H-bridge converter to operate perfectly over a specified current and temperature range needs to be determined.

The forward voltage drop V_F of the rectifier diode at maximum output load is to be considered.

$$V_{S-min} = V_{F-max} + V_{O-max} \quad (3)$$

The minimum available primary voltage V_{P-min} is calculated. Drain-source voltage of the NSIP3266 is V_{DS-max}. The minimum converter input voltage is V_{IN-min}:

$$V_{P-min} = V_{IN-min} - V_{DS-max} \quad (4)$$

V_{DS-max} is the product of the maximum $R_{DS(on)}$ and I_D values for a given supply specified in the NSIP3266 data sheet:

$$V_{DS-max} = (R_{OH-max} + R_{OL-max}) \times I_{Dmax} \quad (5)$$

Then inserting Equation 5 into Equation 4 yields:

$$V_{P-min} = V_{IN-min} - (R_{OH-max} + R_{OL-max}) \times I_{Dmax} \quad (6)$$

Inserting Equation 6 and Equation 3 into Equation 7 provides the minimum turns ratio:

$$N_{sp-min} = \frac{V_{F-max} + V_{O-max}}{V_{IN-min} - \frac{P_{O-max}}{\eta \times V_{IN-min}} \times (R_{OH-max} + R_{OL-max})} \quad (7)$$

Example:

For a 12 V_{IN} to 23 V_{OUT} converter using the rectifier diode MBRS140T3G, at a load current of 170 mA and a maximum temperature of 125°C, V_{F-max} = 0.19V, $V_{O\_FullLoad\_max}$ = 23 V, and $I_{OUT-max}$ = 0.17A.

Assume that the input power supply accuracy is ±5%, VIN-min = 11.4 V. From the NSIP3266 data sheet with R_{OH-max} = 2.0Ω,
R_{OL-max} = 1.5Ω, I_{D-max} = 0.17A.

Inserting these values and performing calculations:

$$N_{sp-min} = \frac{0.19V + 23V}{12V - \frac{23V \times 0.17A}{0.85 \times 11.4} \times (2.0+1.5)\Omega} = 2.2 \quad (8)$$

11.3 Layout

- A 1μF to 10μF low-ESR ceramic bypass capacitor should be connected between the VDD pin and ground to ensure stable power supply operation. The capacitor should be placed as close as possible to the VDD pin to minimize high-frequency impedance.
- The PCB layout is shown in Figure 11.2. The GND pin must be connected to the PCB ground plane via two vias to minimize inductance.
- The OUTA and OUTB pins of the device should be connected with the primary terminal of the transformer. The wiring connections must be as close together as possible to reduce the inductance of the wires.
- The recommended rectifier diode is the Schottky diode, which has a low forward voltage to maximize efficiency. However, if stringent output voltage regulation is required under light loads, please replace Schottky diodes with fast recovery diodes with smaller junction capacitance to achieve stable output voltage under light load.
- The V_{OUT} pins must be decoupled to the ISO ground with low-ESR ceramic bypass capacitors. A 10μF capacitor should be used in parallel with a 0.1μF capacitor, and the rated voltage of both capacitors is at least 35V.

Layout Example

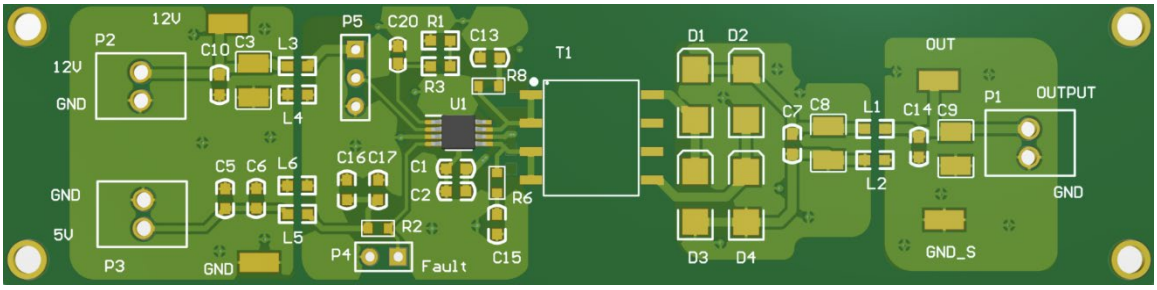
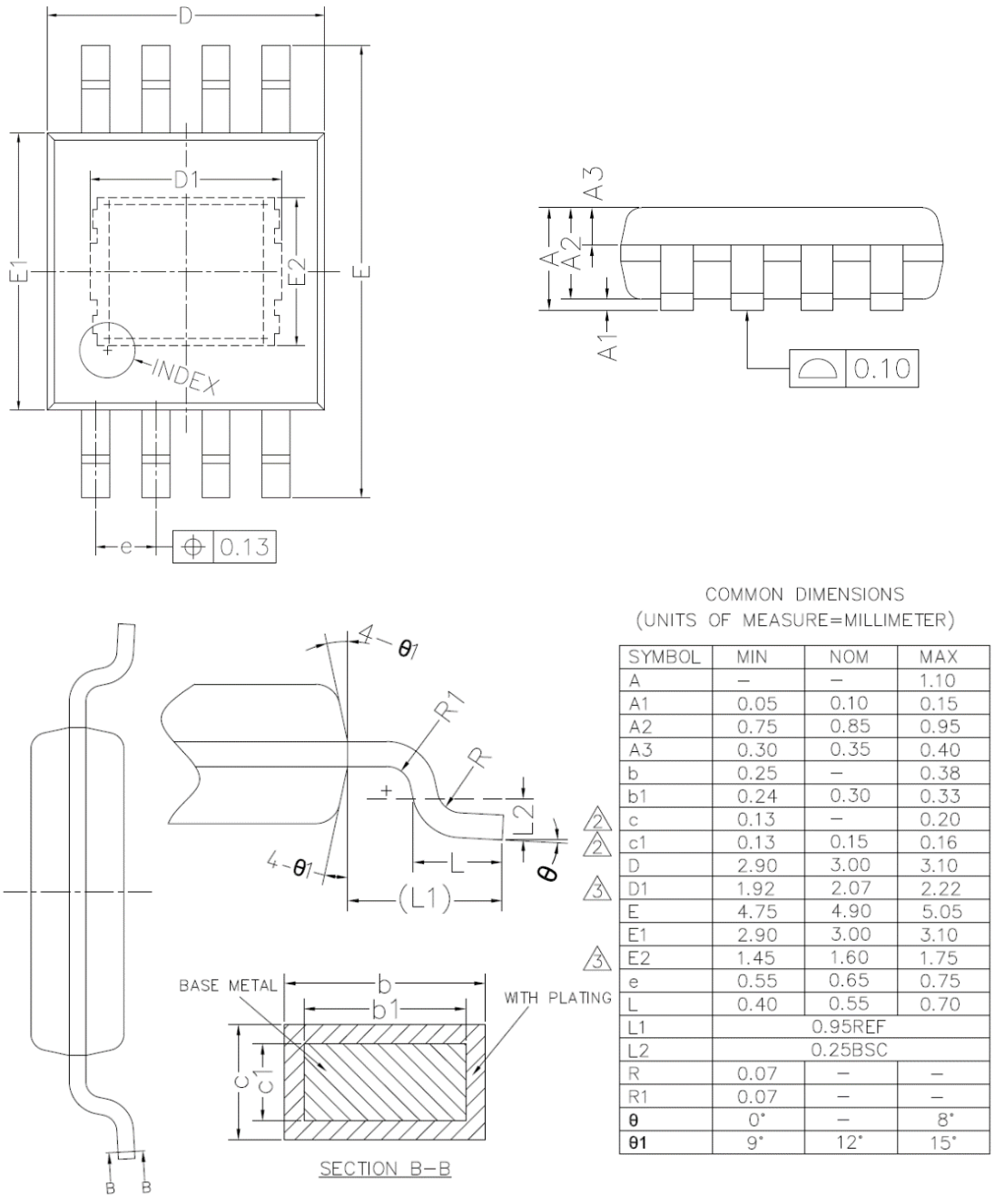


Figure 11.2 Layout Example of 2-Layer Board (NSIP3266-Q1)

12. Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.25	–	0.38
b1	0.24	0.30	0.33
c	0.13	–	0.20
c1	0.13	0.15	0.16
D	2.90	3.00	3.10
D1	1.92	2.07	2.22
E	4.75	4.90	5.05
E1	2.90	3.00	3.10
E2	1.45	1.60	1.75
e	0.55	0.65	0.75
L	0.40	0.55	0.70
L1	0.95REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
θ	0°	–	8°
θ1	9°	12°	15°

NOTES: 1. ALL DIMENSIONS IN MILLIMETERS REFER TO JEDEC STANDARD MO-187 AA-T
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. INDEX ø0.60±0.10 WITH 0.05MAX DEPTH.
3.'D1' AND 'E2' ARE VARIABLES DEPENDING ON DIE PAD SIZES.

Figure 12.1 HMSOP8 Package Shape and Dimension

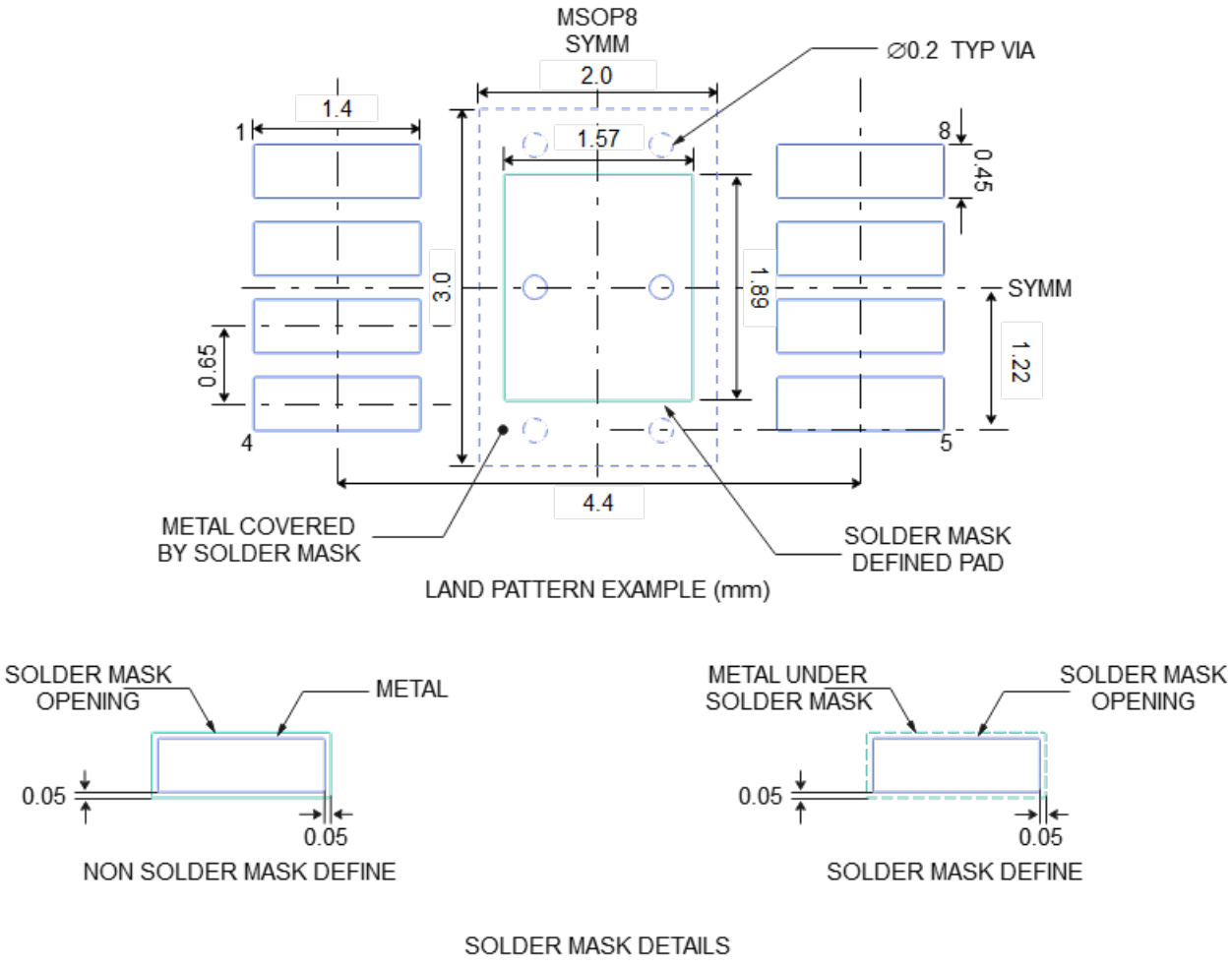


Figure 12.2 HMSOP8 Package Board Layout Example

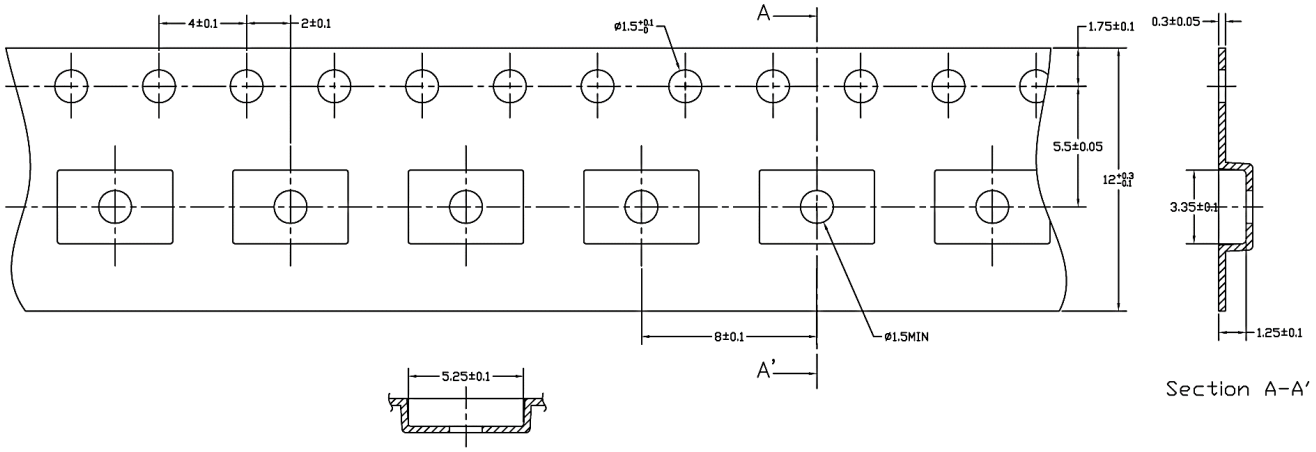
13. Ordering Information

Part No.	*Temperature*	*Auto-motive*	*Package Drawing*	*MSL*	*SPQ*
NSIP3266-Q1HMSR	-40 to 125℃	Y	HMSOP8	2	2500

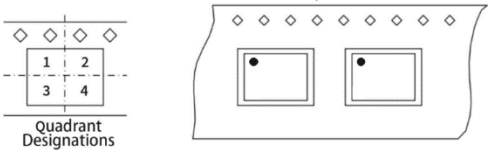
14. Documentation Support

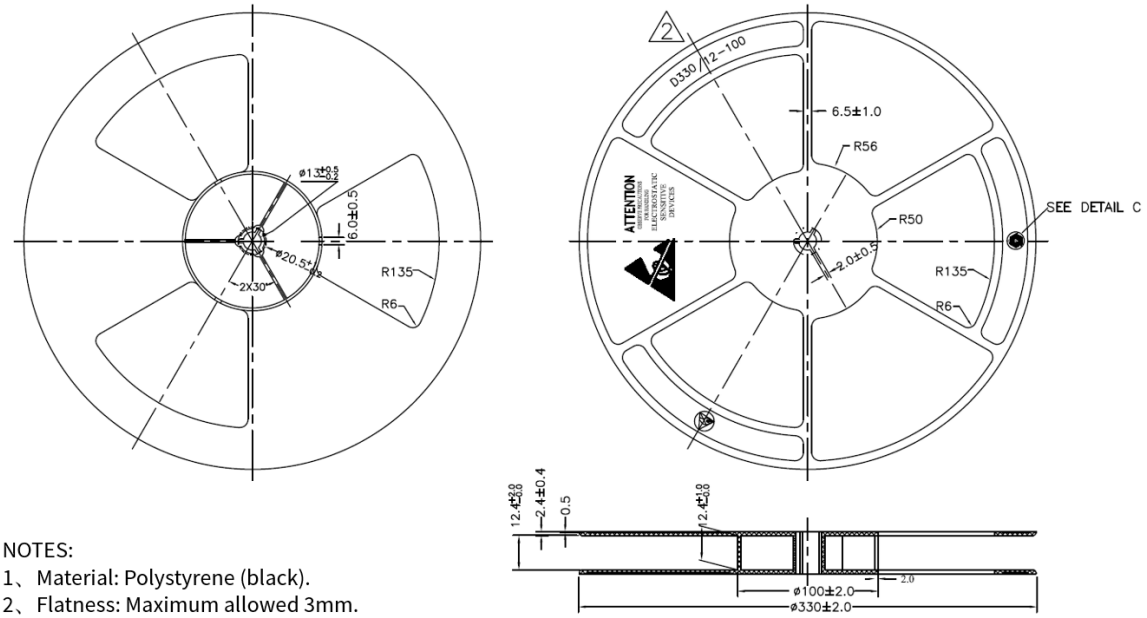
Part Number	*Product Folder*	*Datasheet*	*Application Note*
NSIP3266-Q1HMSR	Click here	Click here	Click here

15. Tape and Reel Information



NOTES:
1.MATERIAL:Hard polystyrene(PS)
2.ALL DIMS IN MM
3.There must not be foreign body adhesion and the state of the surface must be excellent
4.The meander of the tape is assumed with 1mm or less every 100mm between 250mm
5.A permissible difference of the accumulation pitch of the sending hole is assumed to be ±0.3 up to 50 pitches
6.ø560 Paper-Reel, 60000 pockets(480M)
7.Corner R=0.3max
8.Surface resistance 1X10E5≤Rs≤1X10E9 OHMS/SQ





NOTES:
1、Material: Polystyrene (black).
2、Flatness: Maximum allowed 3mm.
3、All dimensions are in millimeters.
4、Surface resistivity: 1*10E5 to 1*10E10 OHMS/SQ.
5、All unmarked tolerances: ±0.25.

Figure 15.1 Tape and Reel Information of HMSOP8

16. Doc History

Revision	*Description*	*Date*
1.0	Initial Version	2025/7/9

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