

Product Overview

NSI8366 is a high reliability six-channel digital isolator. The NSI8366 device is safety certified by UL1577 and supports 5kV_{RMS} insulation withstand voltage, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of NSI8366 is up to 30Mbps, and the common-mode transient immunity (CMTI) is up to 200kV/μs. NSI8366's default output is low when input power is lost to prevent IPM switching during power on stage. Wide supply voltage of NSI8366 supports to connect with most digital interfaces directly. High system level EMC performance enhances reliability and stability of use.

NSI8366 has the interlock function for adjacent channels to provide the shoot-through protection, to eliminate the short-circuit risk of IGBT inside the IPM, to enhance system robustness.

Key Features

- Up to 5000V_{RMS} Insulation voltage
- Data rate: DC to 30Mbps
- Power supply voltage: 2.5V to 5.5V
- High CMTI: 200kV/μs
- Chip level ESD: HBM: ±8kV
- Interlock function
- Robust Electromagnetic Compatibility (EMC)
 - System-Level ESD, EFT, and Surge Immunity
 - Low Emissions
- Default output low level option
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <50ns
- Operation temperature: -40°C~125°C
- RoHS-compliant packages: SOP16(300mil)

Safety Regulatory Approvals

- UL recognition: up to 5000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor Control

Device Information

Part Number	Package	Body Size
NSI8366W0-DSWR	SOP16(300mil)	10.30mm × 7.30mm

Functional Block Diagrams

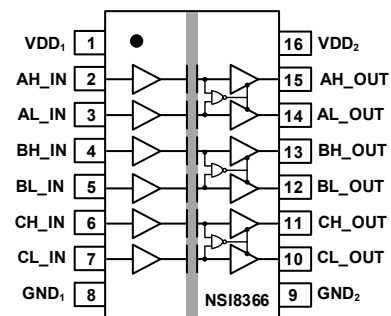


Figure 1. NSI8366 Block Diagram

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1. Pin Configuration and Functions

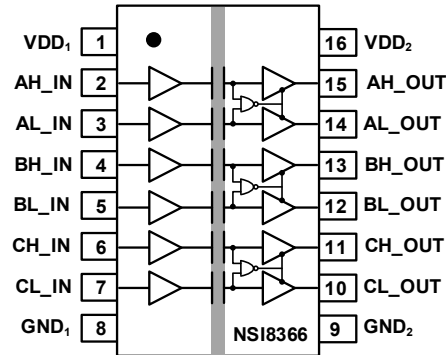


Figure 1.1 NSI8366 Package

Table 1.1 NSI8366 Pin Configuration and Description

NSI8366 PIN NO.	SYMBOL	FUNCTION
1	VDD ₁	Power Supply for Isolator Side 1
2	AH_IN	High side Logic Input AH
3	AL_IN	Low side Logic Input AL
4	BH_IN	High side Logic Input BH
5	BL_IN	Low side Logic Input BL
6	CH_IN	High side Logic Input CH
7	CL_IN	Low side Logic Input CL
8	GND ₁	Ground 1, the ground reference for Isolator Side 1
9	GND ₂	Ground 2, the ground reference for Isolator Side 2
10	CL_OUT	Low side Logic Output CL
11	CH_OUT	High side Logic Output CH
12	BL_OUT	Low side Logic Output BL
13	BH_OUT	High side Logic Output BH
14	AL_OUT	Low side Logic Output AL
15	AH_OUT	High side Logic Output AH
16	VDD ₂	Power Supply for Isolator Side 2

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	VINA, VINB, VINC, VIND, VINE, VINI	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Output Voltage	VOUTA, VOUTB, VOUTC, VOUTD, VOUTE, VOUTF	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Input/Output Pulse Voltage	ALL I/O Pin	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Output current	I _o	-15		15	mA	
Operating Temperature	T _{opr}	-40		125	°C	
Junction Temperature	T _j			150	°C	
Storage Temperature	T _{stg}	-65		150	°C	

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating conditions. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.
- (2) Power supply voltage and input/output voltage are respect to the local ground terminal (GND1 or GND2) voltage values.

3. ESD Ratings

Parameters	Ratings	Value	Unit
Electrostatic discharge (ESD)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽²⁾	±8000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽³⁾	±2000	V

- (1) Though this device features proprietary protection circuitry, proper ESD precautions should be considered to avoid performance degradation of damage due to high energy ESD event. Charged devices and circuit boards may discharge without detection.
- (2) Safe manufacturing requires 500-V HBM and standard ESD precautions, per JEDEC document JEP155.
- (3) Safe manufacturing requires 250-V CDM and standard ESD precautions, per JEDEC document JEP157.

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	VDD1, VDD2	2.5		5.5	V
High-level Input Voltage	VIH	0.7*VDD			V
Low-level Input Voltage	VIL			0.3*VDD	V
Data Rate	DR	0		30	Mbps
Ambient Temperature	Ta	-40		125	°C

5. Thermal Information

Parameters	Symbol	SOP16(300mil)	Unit
Junction-to-ambient thermal resistance	R _{θJA}	78.9	°C/W
Junction-to-case(top) thermal resistance	R _{θJC (top)}	41.6	°C/W
Junction-to-board thermal resistance	R _{θJB}	43.6	°C/W
Junction-to-top characterization parameter	Ψ _{JT}	7.0	°C/W
Junction-to-board characterization parameter	Ψ _{JB}	23.0	°C/W

6. Specifications

6.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power on Reset	VDD _{POR} ⁽¹⁾	2	2.2	2.4	V	POR threshold as during power-up
	VDD _{HYS} ⁽¹⁾		0.1		V	POR threshold Hysteresis
Rising input switching threshold	V _{IT+} ⁽¹⁾		0.6* VDD	0.7* VDD	V	
Falling input switching threshold	V _{IT-} ⁽¹⁾	0.3* VDD	0.4* VDD		V	

Input threshold voltage hysteresis	$V_{IT_HYS}^{(1)}$		0.2* VDD		V	
High Level Output Voltage	V_{OH}	VDD-0.4			V	$I_{OH} = -4mA$
Low Level Output Voltage	V_{OL}			0.4	V	$I_{OL} = 4mA$
Output Impedance	$R_{out}^{(1)}$		50		ohm	
Input Pull high or low Current	I_{pull}		5	10	μA	
Start Up Time after POR	trbs ⁽²⁾		15	30	μs	
Common Mode Transient Immunity	CMTI	± 150	± 200		kV/ μs	See Figure 6.2 , $C_L = 15pF$
⁽¹⁾ Not test covered, guaranteed by characterization.						
⁽²⁾ Not test covered, guaranteed by design.						

6.2. Supply Current Characteristics – 5V Supply

(VDD1=5V $\pm$ 10%, VDD2=5V $\pm$ 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V**, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSI8366					
	$I_{DD1}(Q0)$		1.5	2.13	mA	All Input 0V
	$I_{DD2}(Q0)$		3.84	6.09	mA	
	$I_{DD1}(Q1)$		8.35	11.34	mA	All Input at supply
	$I_{DD2}(Q1)$		3.91	6.20	mA	
	$I_{DD1}(1M)$		4.95	6.70	mA	All Input with 1Mbps, $C_L=15pF$
	$I_{DD2}(1M)$		4.0	6.31	mA	

6.3. Supply Current Characteristics –3.3V Supply

(VDD1=3.3V $\pm$ 10%, VDD2=3.3V $\pm$ 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V**, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSI8366					
	$I_{DD1}(Q0)$		1.45	2.06	mA	All Input 0V

	I _{DD2} (Q0)		3.71	5.88	mA	All Input at supply
	I _{DD1} (Q1)		8.22	11.15	mA	
	I _{DD2} (Q1)		3.79	5.99	mA	
	I _{DD1} (1M)		4.86	6.57	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		3.80	6.04	mA	

6.4. Supply Current Characteristics–2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 2.5V**, **VDD2 = 2.5V**, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSI8366					
	I _{DD1} (Q0)		2.01	2.02	mA	All Input 0V
	I _{DD2} (Q0)		3.65	5.78	mA	
	I _{DD1} (Q1)		8.13	11.03	mA	All Input at supply
	I _{DD2} (Q1)		3.71	5.91	mA	
	I _{DD1} (1M)		4.79	6.46	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		3.75	5.92	mA	

6.5. Switching Characteristics - 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		30	Mbps	
Minimum Pulse Width	PW			30	ns	
Propagation Delay	t _{PLH}		35.88	50	ns	See Figure 6.1 , C _L = 15pF
	t _{PHL}		33.94	50	ns	See Figure 6.1 , C _L = 15pF
Pulse Width Distortion t _{PHL} - t _{PLH}	PWD			5.0	ns	See Figure 6.1 , C _L = 15pF
Rising Time	t _r			5.0	ns	See Figure 6.1 , C _L = 15pF
Falling Time	t _f			5.0	ns	See Figure 6.1 , C _L = 15pF
Part-to-Part Delay Skew	t _{SK} (p2p)			5.0	ns	

6.6. Switching Characteristics - 3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25°C**)

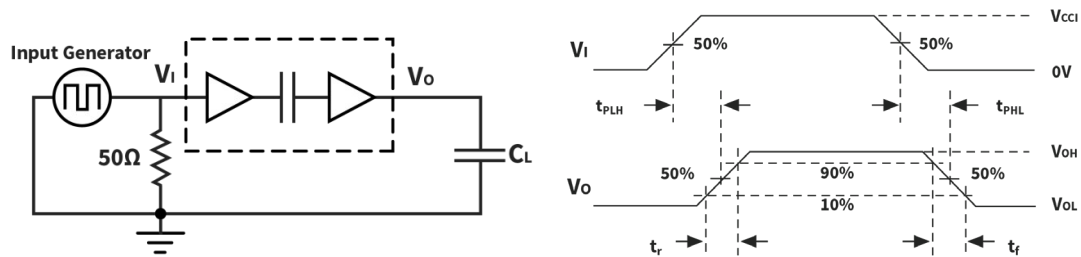
Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		30	Mbps	
Minimum Pulse Width	PW			30	ns	
Propagation Delay	t _{PLH}		37.1	50	ns	See Figure 6.1 , C _L = 15pF
	t _{PHL}		35.13	50	ns	See Figure 6.1 , C _L = 15pF
Pulse Width Distortion t _{PHL} - t _{PLH}	PWD			5.0	ns	See Figure 6.1 , C _L = 15pF
Rising Time	t _r			5.0	ns	See Figure 6.1 , C _L = 15pF
Falling Time	t _f			5.0	ns	See Figure 6.1 , C _L = 15pF
Part-to-Part Delay Skew	t _{SK} (p2p)			5.0	ns	

6.7. Switching Characteristics - 2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		30	Mbps	
Minimum Pulse Width	PW	0		30	ns	
Propagation Delay	t_{PLH}		38.76	50	ns	See Figure 6.1 , $C_L = 15pF$
	t_{PHL}		37.12	50	ns	See Figure 6.1 , $C_L = 15pF$
Pulse Width Distortion $ t_{PHL} - t_{PLH} $	PWD			5.0	ns	See Figure 6.1 , $C_L = 15pF$
Rising Time	t_r			5.0	ns	See Figure 6.1 , $C_L = 15pF$
Falling Time	t_f			5.0	ns	See Figure 6.1 , $C_L = 15pF$
Part-to-Part Delay Skew	$t_{SK(p2p)}$			5.0	ns	

6.8. Parameter Measurement Information



(1) Input Generator Characteristics : PRR $\leq$ 50kHz, $t_r \leq 3$ ns, $t_f \leq 3$ ns, Duty cycle = 50%, $Z_o = 50 \Omega$.

Figure 6.1 Switching Characteristics Test Circuit and Waveform

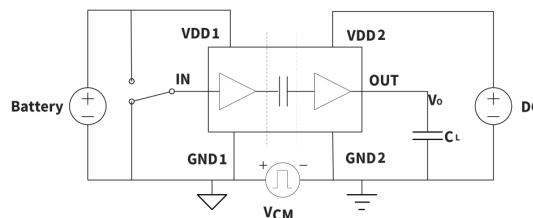


Figure 6.2 Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value		Comments
		SOP16 (300mil)	Unit	
Minimum External Clearance	CLR	8	mm	IEC 60664-1
Minimum External Creepage	CPG	8	mm	IEC 60664-1
Distance Through Insulation	DTI	24	μ m	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

Description	Test Condition	Value
		SOP16 (300mil)
Overvoltage Category per IEC60664-1	For Rated Mains Voltage $\leq$ 150Vrms	I to IV

Description	Test Condition	Value
		SOP16 (300mil)
	For Rated Mains Voltage $\leq$ 300Vrms	I to IV
	For Rated Mains Voltage $\leq$ 600Vrms	I to IV
	For Rated Mains Voltage $\leq$ 1000Vrms	I to III
Climatic Classification		40/125/21
Pollution Degree per DIN VDE 0110		2

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value	
			SOP16 (300mil)	Unit
Maximum repetitive isolation voltage		V_{IORM}	2121	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	1500	V_{RMS}
	DC Voltage		2121	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, $t_{ini} = 60s$, $V_{pd(m)}=1.2*V_{IORM}$, $t_m=10s$	q_{pd}	<5	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, $t_{ini}=60s$, $V_{pd(m)}=1.6*V_{IORM}$, $t_m=10s$			pC
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}$, $t_{ini}=1s$ $V_{pd(m)}=1.875*V_{IORM}$, $t_m=1s$ (method b1) or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$ (method b2)			pC

Description	Test Condition	Symbol	Value	
			SOP16 (300mil)	Unit
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, $t_{ini} = 60s$, $V_{pd(m)}=1.2*V_{IORM}$, $t_m=10s$	q_{pd}	\	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, $t_{ini}=60s$, $V_{pd(m)}=1.3*V_{IORM}$, $t_m=10s$			pC
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}$, $t_{ini}=1s$ $V_{pd(m)}=1.5*V_{IORM}$, $t_m=1s$ (method b1) or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$ (method b2)			pC
Maximum transient isolation voltage	$t = 60s$	V_{IOTM}	8000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50 μs waveform per IEC62368-1	V_{IMP}	6250	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50 μs waveform, $V_{IOSM} \geq V_{IMP} \times$ 1.3	V_{IOSM}	10000	V_{PEAK}
Isolation resistance	$V_{IO} = 500V$, $T_{amb}=25^{\circ}C$	R_{IO}	$>10^{12}$	Ω
	$V_{IO} = 500V$, $100^{\circ}C \leq T_{amb} \leq$ 125 $^{\circ}C$	R_{IO}	$>10^{11}$	Ω
	$V_{IO} = 500V$, $T_{amb}=T_S$	R_{IO}	$>10^9$	Ω
Isolation capacitance	$f = 1MHz$	C_{IO}	0.8	pF
Insulation voltage per UL	$V_{TEST} = V_{ISO}$, $t = 60s$ (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, $t = 1s$ (100% production test)	V_{ISO}	5000	V_{RMS}

7.3. Safety-Limiting Values

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI836xWx-DSWR.

Description	Test Condition	Symbol	Value	Unit
Safety Supply Power	$R_{\theta JA} = 78.9 \text{ }^{\circ}\text{C/W}^{(1)}$, $T_J = 150 \text{ }^{\circ}\text{C}$, $T_A = 25 \text{ }^{\circ}\text{C}$		1584	mW
Safety Supply Current	$R_{\theta JA} = 78.9 \text{ }^{\circ}\text{C/W}^{(1)}$, $V_I = 5\text{V}$, $T_J = 150 \text{ }^{\circ}\text{C}$, $T_A = 25 \text{ }^{\circ}\text{C}$		316.8	mA
Safety Temperature ²⁾		T_S	150	$^{\circ}\text{C}$

- 1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP16(300mil) package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

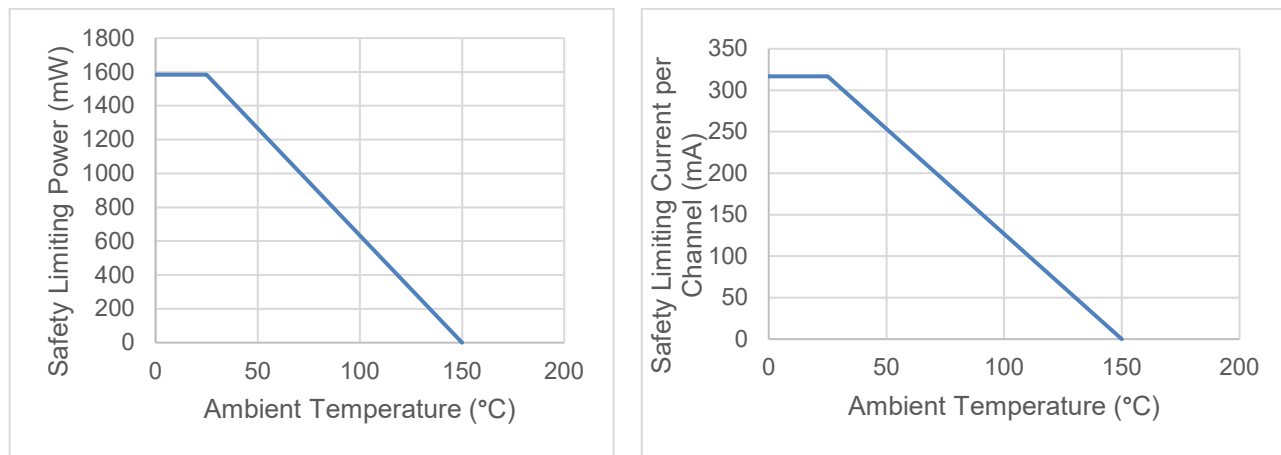


Figure 7.1 NSI836x Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17).

7.4. Regulatory Information

The NSI836xWx-DSWR are approved by the organizations listed in table.

UL		CQC	TUV	
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to GB4943.1-2022	DIN EN IEC 60747-17 (VDE 0884-17)	Certified According to EN IEC 62368-1
Single Protection, 5000V _{rms} Isolation voltage	Single Protection, 5000V _{rms} Isolation voltage	Reinforced insulation	Reinforced Insulation V _{IORM} =2121V _{peak} V _{IOTM} =8000V _{peak} V _{IOSM} =10000V _{peak}	5000V _{rms} for 1min
E500602	E500602	CQC20001264939	R 50632560	R 50574061

8. Function Description

8.1. Overview

NSI8366 is a high reliability six-channel digital isolator. NSI8366 is safety certified by UL1577 and supports 5kV_{rms} insulation withstand voltages, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate is up to 30Mbps, and the common-mode transient immunity (CMTI) is up to 200kV/us. NSI8366's default output is low when input power is lost to prevent IPM switching during power on stage. Wide supply voltage of NSI8366 and supports connecting with most digital interfaces directly, making level shifting easy. High system level EMC performance enhance reliability and stability of use.

NSI8366 has a default output status when VDD1 is unready and VDD2 is ready as shown in Table 8.1, which helps for diagnosis when power is missing at the transmitter side. The other outputs follow the same status as the input A after powering up respectively.

Table 8.1 Output status vs. power status

<i>XH_IN</i>	<i>XL_IN</i>	<i>VDD1 status</i>	<i>VDD2 status</i>	<i>XH_OUT</i>	<i>XL_OUT</i>	<i>Comment</i>
H	H	Ready	Ready	L	L	Normal operation.
L or NC	H	Ready	Ready	L	H	
H	L or NC	Ready	Ready	H	L	
L or NC	L or NC	Ready	Ready	L	L	
X	X	Unready	Ready	L	L	The output follows the Normal operation after input side VDD1 is powered on.
X	X	Ready	Unready	Undetermined	Undetermined	The output follows the Normal operation after output side VDD2 is powered on.

Note: H=Logic high; L=Logic low; X=Logic low or logic high
VDD1 is input side power; VDD2 is outside power.

8.2. OOK Modulation

NSI8366 is based on a capacitive isolation barrier technique and the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, as shown in Fig8.1, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI.

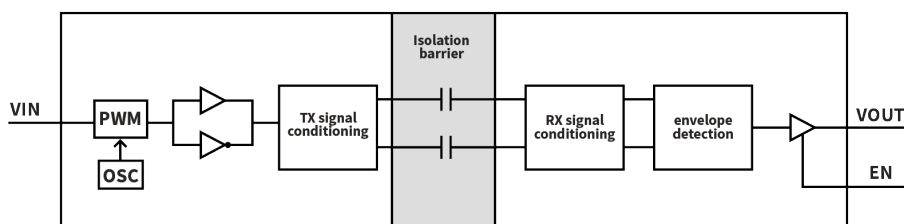


Figure 8.1 Single Channel Function Block Diagram

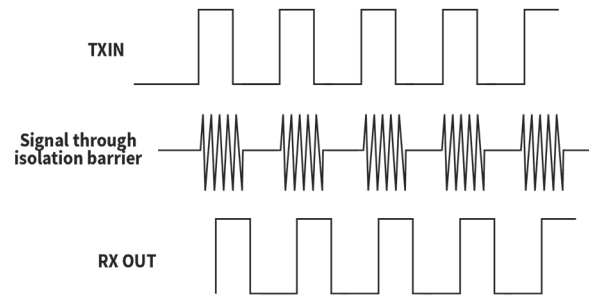


Figure 8.2 OOK Modulation

8.3. Shoot Through Protection

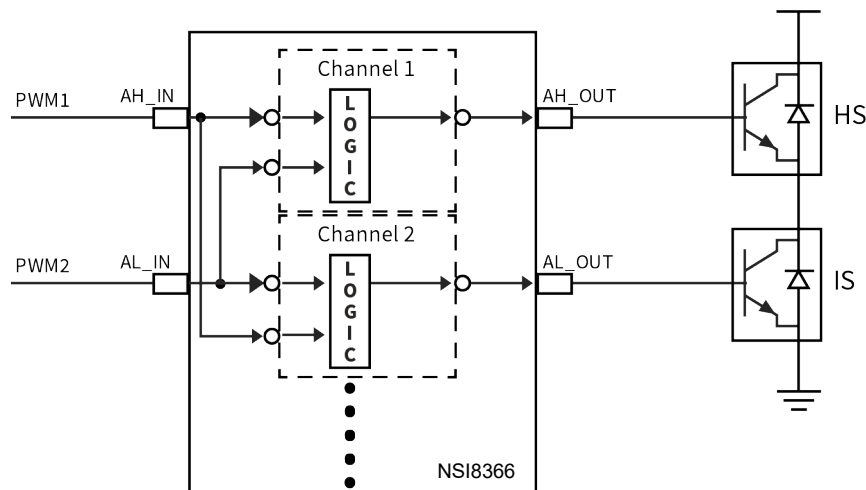


Figure 8.3 Typical IPM isolated driving Circuit

As shown in Fig 8.3, NSI8366 has the interlock function to provide the shoot through protection to prevent both high-side and low-side switches from being activated simultaneously, if one of the adjacent channels is in ON state, the counterpart PWM signal is inhibited, preventing it from turning high. Fig 8.4 show the test waveform.



Figure 8.4 NSI8366 driving signal with interlock triggered

9. Application Note

9.1. Typical Application Circuit

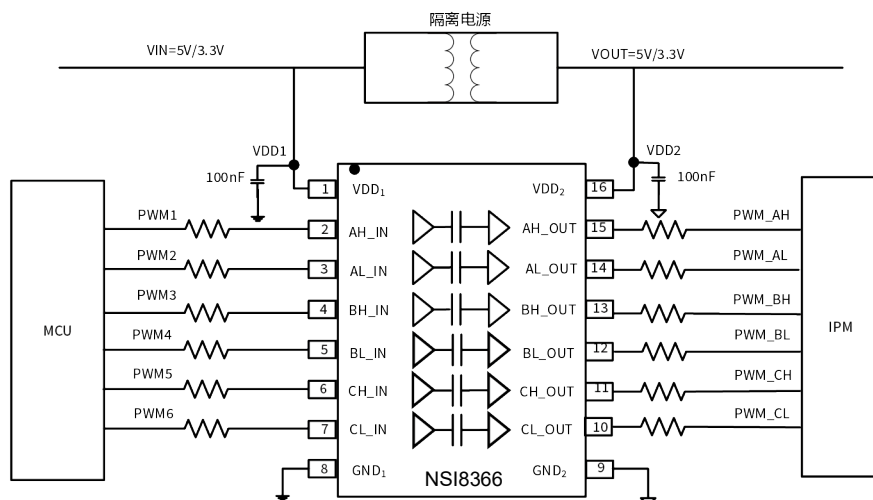


Figure 9.1 Typical IPM isolated driving Circuit

9.2. PCB Layout

NSI8366 requires a 0.1 μF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. Figure 9.2 to Figure 9.3 show the recommended PCB layout, make sure the space under the chip should be kept free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω , $\pm 40\%$. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

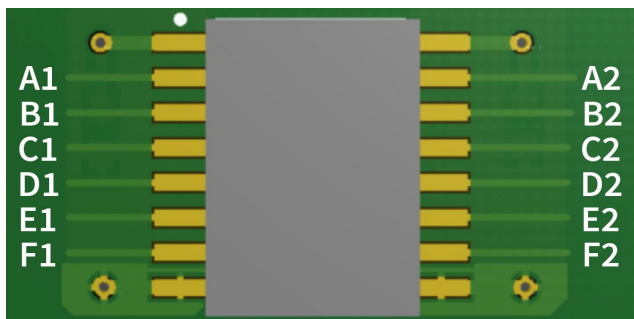


Figure 9.2 Recommended PCB Layout — Top Layer



Figure 9.3 Recommended PCB Layout — Bottom Layer

9.3. High Speed Performance

Figure 9.4 shows the eye diagram of NSI8366 at 30Mbps data rate output. The result shows a typical measurement on NSI8366 with low jitter and wide-open eye characteristics.

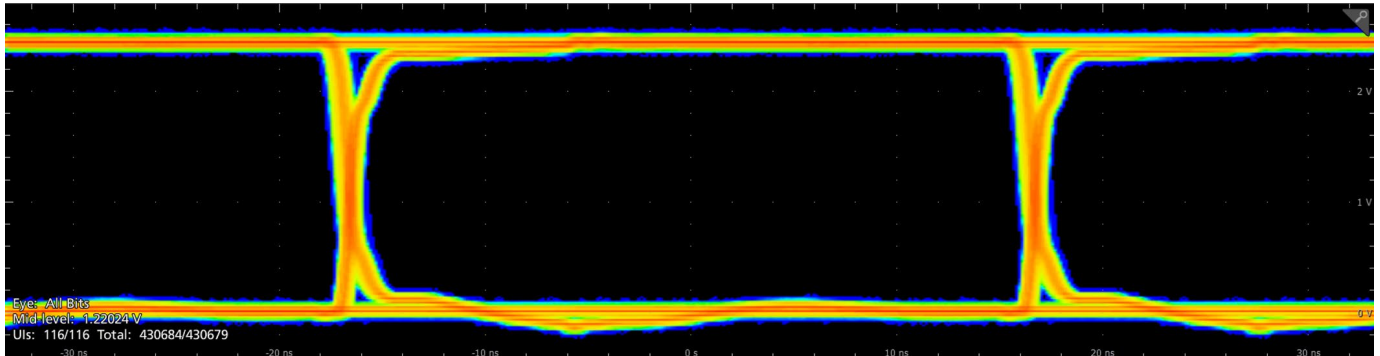
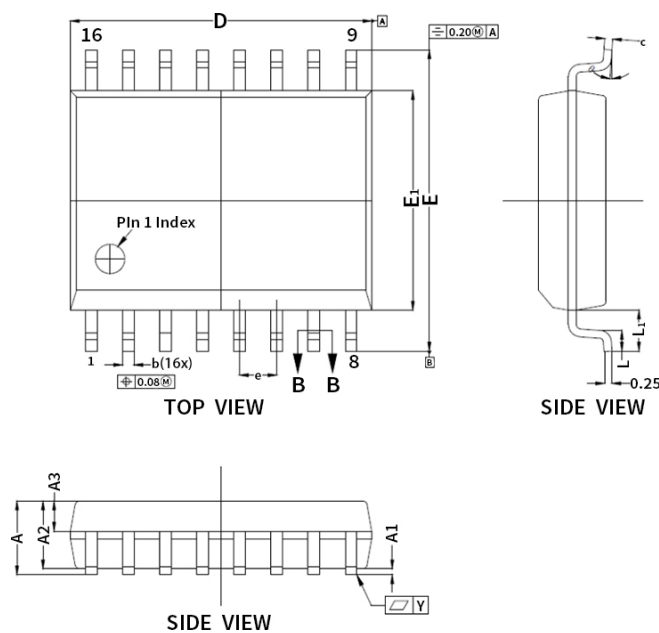


Figure9.4 Eye Diagram at 30Mbps PRBS 2¹⁵-1, 2.5V and 25°C

10. Package Information



* CONTROLLING DIMENSION:MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

Figure 10.1 SOP16(300mil)/SOW16 Package Shape and Dimension in millimeters

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

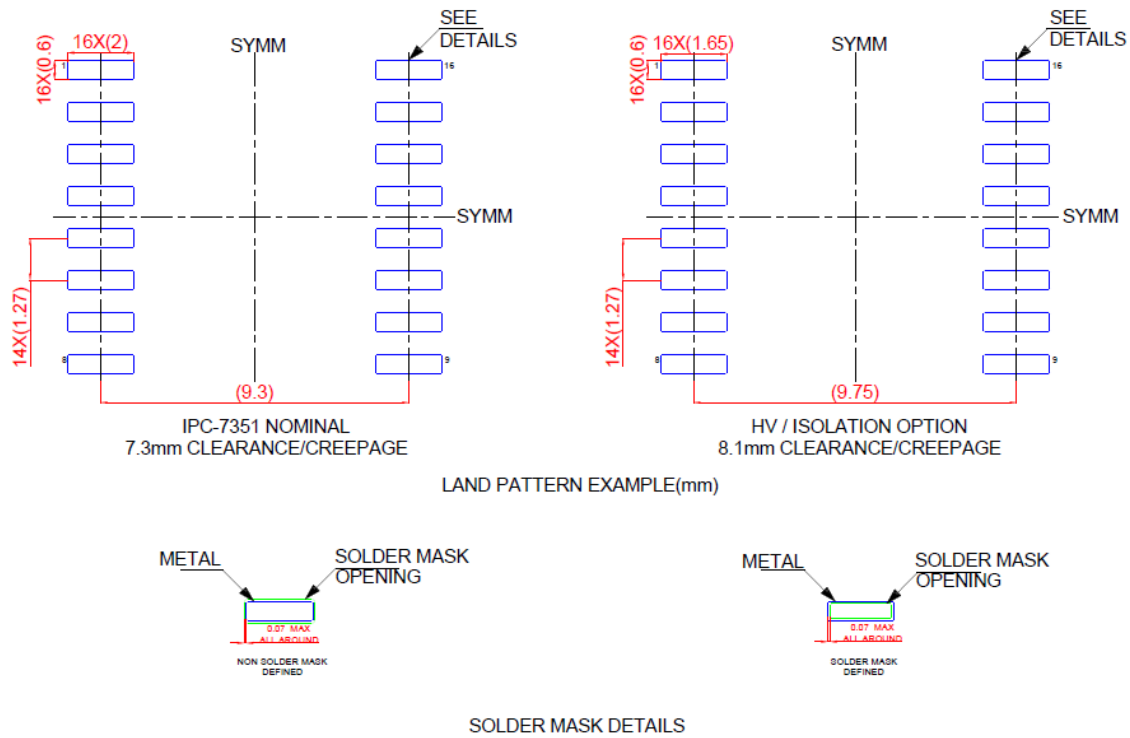
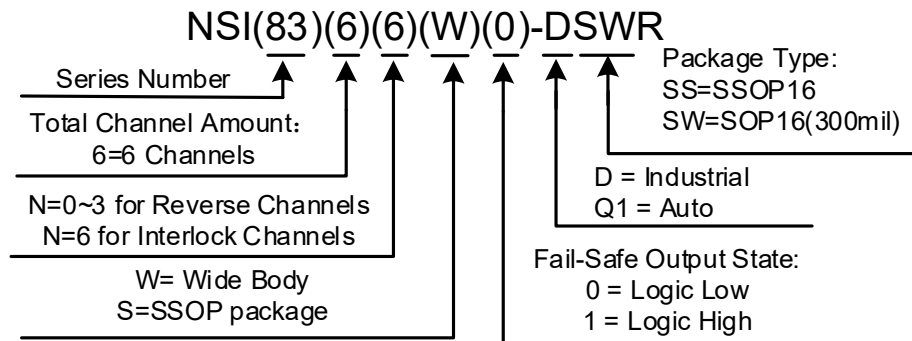


Figure 10.2 SOP16(300mil) SOW16 Package Board Layout Example

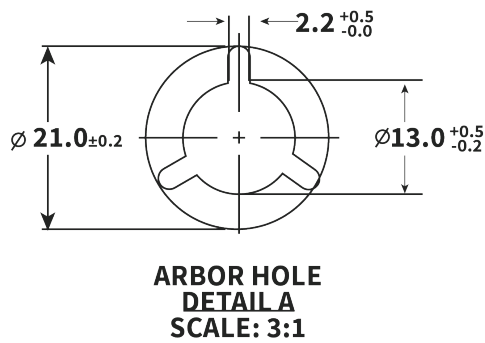
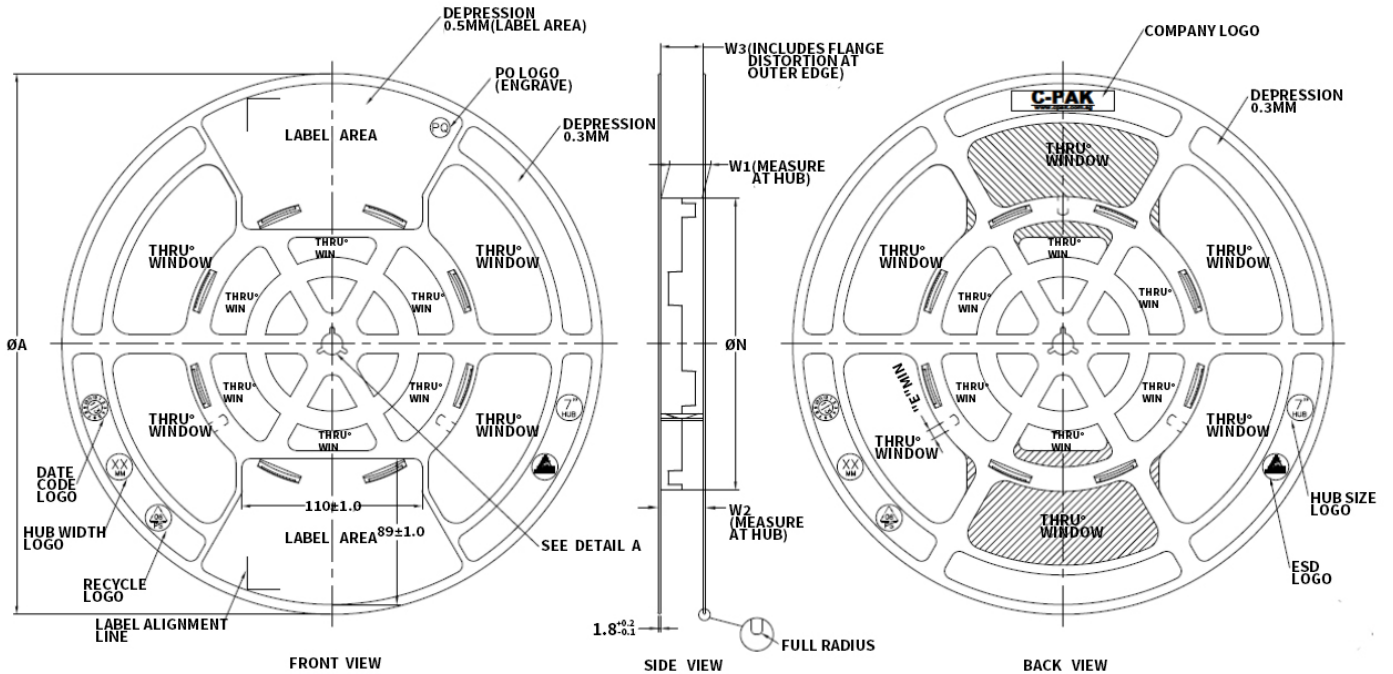
11. Ordering Information

Part Number	Isolation Rating (kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	MSL	Package Type	Package Drawing	SPQ	MPQ
NSI8366W0-DSWR	5	6	0	30	Low	-40 to 125°C	3	SOP16 (300mil)	SOW16	1000	1000

Part Number Rule:



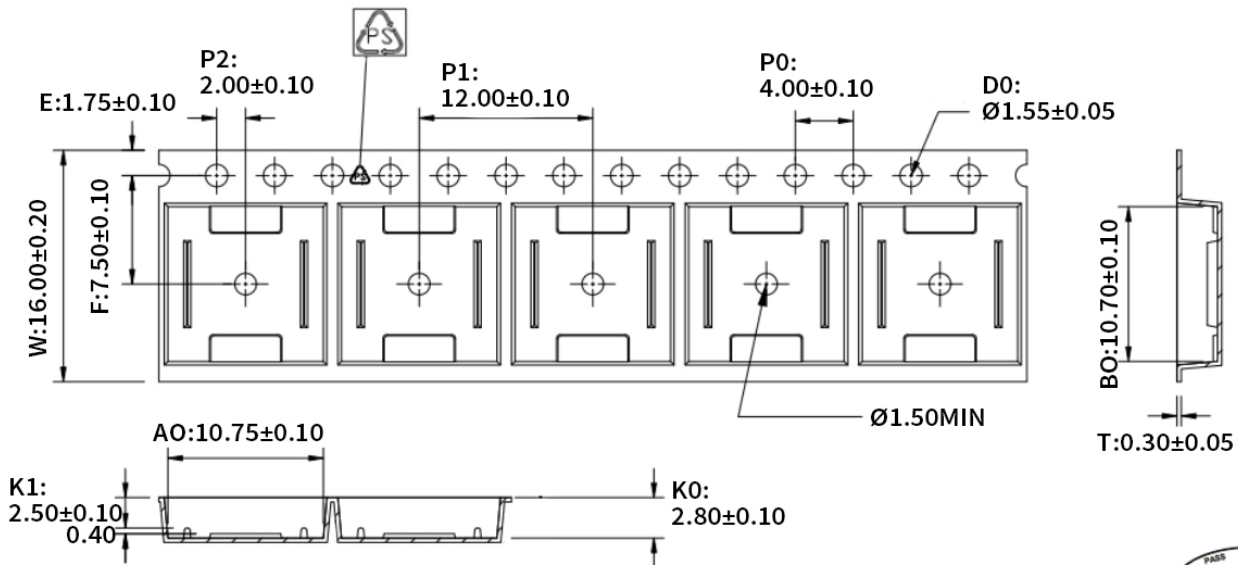
12. Tape and Reel Information



PRODUCT SPECIFICATION						
TAPE WIDTH	Ø A ±2.0	Ø N ±2.0	W1	W2 (Max)	W3	E (MIN)
08MM	330	178	8.4 ^{+1.5} _{-0.0}	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 ^{+2.0} _{-0.0}	18.4		5.5
16MM	330	178	16.4 ^{+2.0} _{-0.0}	22.4		5.5
24MM	330	178	24.4 ^{+2.0} _{-0.0}	30.4		5.5
32MM	330	178	32.4 ^{+2.0} _{-0.0}	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10 ¹²	ANTISTATIC	ALL TYPES
B	10 ⁵ TO 10 ¹¹	STATIC DISSIPATIVE	BLACK ONLY
C	10 ⁵ & BELOW 10 ⁵	CONDUCTIVE(GENERIC)	BLACK ONLY
E	10 ⁹ TO 10 ¹¹	ANTISTATIC(COATED)	ALL TYPES

Figure 12.1 Reel Information (for all packages)



1. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness: $0.30 \pm 0.05 \text{ mm}$.
6. Packing length per 22" reel: 378 Meters. (Rewind N=122)
7. Component load per 13" reel: 1000 pcs.
8. Surface resistivity: $10^5 \sim 10^{10} \Omega/\square$



W	16.00 ± 0.20
A0	10.75 ± 0.10
B0	10.70 ± 0.10
K0	2.80 ± 0.10
K1	2.50 ± 0.10

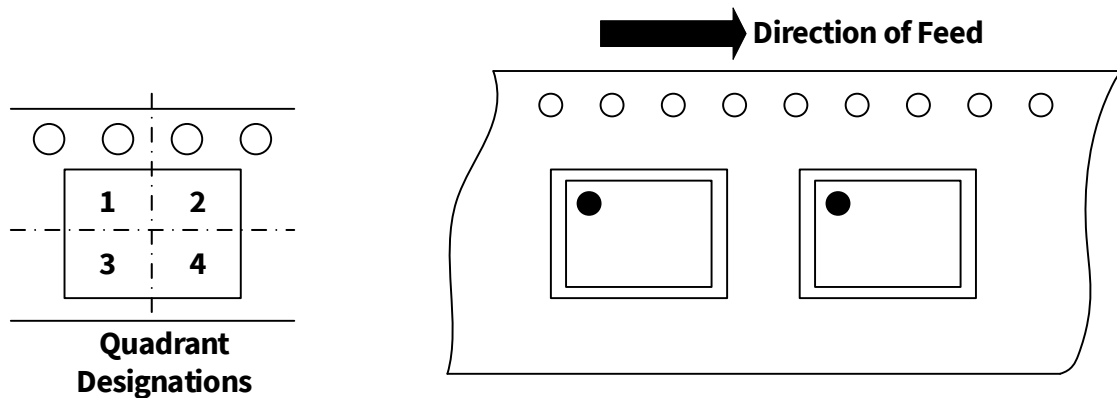


Figure 12.2 Tape Information of SOP16(300mil)

13. Revision History

Revision	Description	Date
1.0	Initial version	2026/6/29

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