

Product Overview

The NSI836x-Q1 devices are high reliability six-channel digital isolators. The NSI836x-Q1 device is safety certified by UL1577 and supports 5kV_{rms} insulation withstand voltage, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI836x-Q1 is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 250kV/μs. The NSI836x-Q1 device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI836x-Q1 device supports connecting with most digital interfaces directly, making level shifting easy. High system level EMC performance enhances reliability and stability of use. AEC-Q100 (Grade 1) option is provided for all devices.

Key Features

- Up to 5000V_{rms} Insulation voltage
- Data rate: DC to 150Mbps
- Power supply voltage: 2.5V to 5.5V
- High CMTI: 250kV/μs
- Chip level ESD: HBM: ±8kV
 - System-Level ESD, EFT, and Surge Immunity
 - Low Emissions
- Default output high level or low-level option
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <18ns
- Operation temperature: -40°C~125°C
- RoHS-compliant packages:
 - SOP16(300mil)

Safety Regulatory Approvals

- UL recognition: up to 5000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation

Device Information

Part Number	Package	Body Size
NSI836xWx-Q1SWR	SOP16(300mil)	10.30mm × 7.50mm

Functional Block Diagrams

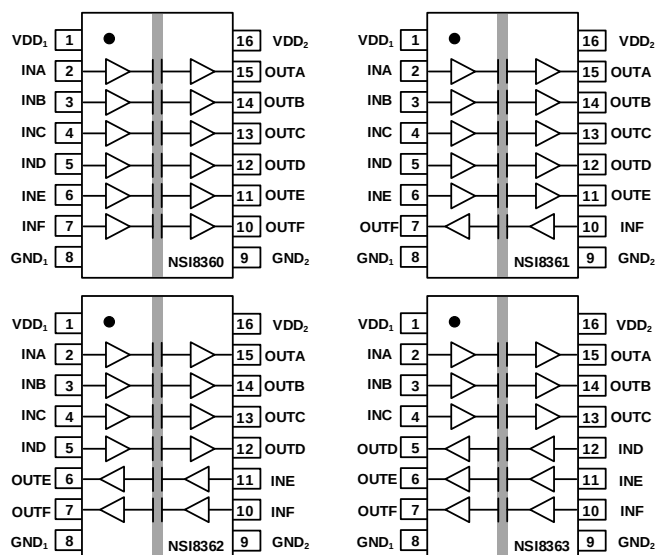


Figure 1. NSI836x-Q1 Block Diagram

INDEX

1. PIN CONFIGURATION AND FUNCTIONS	3
2. ABSOLUTE MAXIMUM RATINGS	4
3. ESD RATINGS	4
4. RECOMMENDED OPERATING CONDITIONS.....	5
5. THERMAL INFORMATION	5
6. SPECIFICATIONS	5
6.1. ELECTRICAL CHARACTERISTICS	5
6.2. SUPPLY CURRENT CHARACTERISTICS – 5V SUPPLY	6
6.3. SUPPLY CURRENT CHARACTERISTICS –3.3V SUPPLY	8
6.4. SUPPLY CURRENT CHARACTERISTICS–2.5V SUPPLY	9
6.5. SWITCHING CHARACTERISTICS - 5V SUPPLY	12
6.6. SWITCHING CHARACTERISTICS - 3.3V SUPPLY	12
6.7. SWITCHING CHARACTERISTICS - 2.5V SUPPLY	13
6.8. PARAMETER MEASUREMENT INFORMATION	13
7. HIGH VOLTAGE FEATURE DESCRIPTION	14
7.1. INSULATION AND SAFETY RELATED SPECIFICATIONS.....	14
7.2. INSULATION CHARACTERISTICS	14
7.3. SAFETY-LIMITING VALUES	16
7.4. REGULATORY INFORMATION.....	17
8. FUNCTION DESCRIPTION	18
8.1. OVERVIEW	18
8.2. OOK MODULATION	19
9. APPLICATION NOTE.....	20
9.1. TYPICAL APPLICATION CIRCUIT.....	20
9.2. PCB LAYOUT.....	20
9.3. HIGH SPEED PERFORMANCE	21
10. PACKAGE INFORMATION.....	22
11. ORDER INFORMATION	23
12. TAPE AND REEL INFORMATION	24
13. REVISION HISTORY	26

1. Pin Configuration and Functions

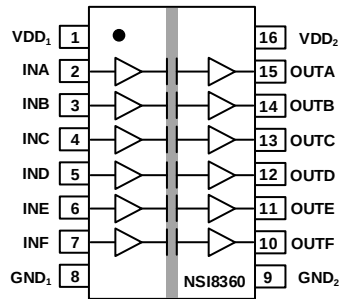


Figure 1.1 NSI8360 Package

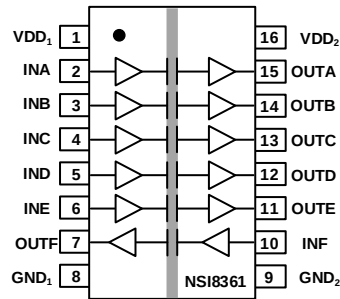


Figure 1.2 NSI8361 Package

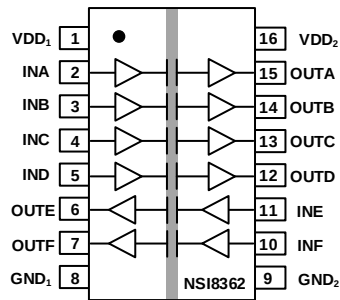


Figure 1.3 NSI8362 Package

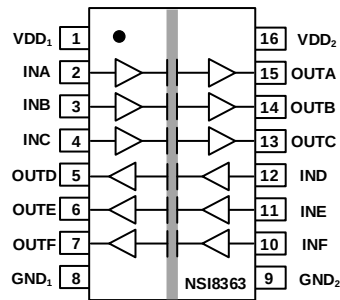


Figure 1.4 NSI8363 Package

Table 1.1 NSI836x-Q1 Pin Configuration and Description

NSI8360 PIN NO.	NSI8361 PIN NO.	NSI8362 PIN NO.	NSI8363 PIN NO.	SYMBOL	FUNCTION
1	1	1	1	VDD ₁	Power Supply for Isolator Side 1
2	2	2	2	INA	Logic Input A
3	3	3	3	INB	Logic Input B
4	4	4	4	INC	Logic Input C
5	5	5	12	IND	Logic Input D
6	6	11	11	INE	Logic Input E
7	10	10	10	INF	Logic Input F
8	8	8	8	GND ₁	Ground 1, the ground reference for Isolator Side 1
9	9	9	9	GND ₂	Ground 2, the ground reference for Isolator Side 2
10	7	7	7	OUTF	Logic Output F
11	11	6	6	OUTE	Logic Output E

NSI8360 PIN NO.	NSI8361 PIN NO.	NSI8362 PIN NO.	NSI8363 PIN NO.	SYMBOL	FUNCTION
12	12	12	5	OUTD	Logic Output D
13	13	13	13	OUTC	Logic Output C
14	14	14	14	OUTB	Logic Output B
15	15	15	15	OUTA	Logic Output A
16	16	16	16	VDD ₂	Power Supply for Isolator Side 2

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	VINA, VINB, VINC, VIND, VINE, VINP	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Output Voltage	VOUTA, VOUTB, VOUTC, VOUTD, VOUTE, VOUTF	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Input /Output Pulse Voltage	ALL I/O Pin	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Output current	I _o	-15		15	mA	
Operating Temperature	T _{opr}	-40		125	°C	
Junction Temperature	T _j			150	°C	
Storage Temperature	T _{stg}	-65		150	°C	

3. ESD Ratings

Parameters	Ratings	Value	Unit
Electrostatic discharge (ESD)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽²⁾	±8000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽³⁾	±2000	V

(1) Though this device features proprietary protection circuitry, proper ESD precautions should be considered to avoid performance degradation of damage due to high energy ESD event. Charged devices and circuit boards may discharge without detection.

- (2) Safe manufacturing requires 500-V HBM and standard ESD precautions, per JEDEC document JEP155.
 (3) Safe manufacturing requires 250-V CDM and standard ESD precautions, per JEDEC document JEP157.

4. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit
Power Supply Voltage	VDD1, VDD2	2.5		5.5	V
Operating Temperature	Topr	-40		125	°C
High Level Input Voltage	VIH	0.7*VDD			V
Low Level Input Voltage	VIL			0.3*VDD	V
Data rate	DR			150	Mbps

5. Thermal Information

Parameters	Symbol	SOP16(300mil)	Unit
IC Junction-to-Air Thermal Resistance	R _{θJA}	78.9	°C/W
Junction-to-case (top) thermal resistance	R _{θJC (top)}	41.6	°C/W
Junction-to-board thermal resistance	R _{θJB}	43.6	°C/W
Junction-to-top characterization parameter	Ψ _{JT}	7.0	°C/W
SJunction-to-board characterization parameter	Ψ _{JB}	23.0	°C/W

6. Specifications

6.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power on Reset	VDD _{POR} ⁽¹⁾	2	2.2	2.4	V	POR threshold as during power-up
	VDD _{HYS} ⁽¹⁾		0.1		V	POR threshold Hysteresis
Rising input switching threshold	V _{IT+} ⁽¹⁾		0.6*V _D	0.7*V _D	V	
Falling input switching threshold	V _{IT-} ⁽¹⁾	0.3*V _{DD}	0.4*V _D		V	

Input threshold voltage hysteresis	$V_{IT_HYS}^{(1)}$		$0.2 \cdot V_{DD}$		V	
High Level Output Voltage	V_{OH}	$V_{DD} - 0.4$			V	$I_{OH} = -4mA$
Low Level Output Voltage	V_{OL}			0.4	V	$I_{OL} = 4mA$
Output Impedance	$R_{out}^{(1)}$		50		ohm	
Input Pull high or low Current	I_{pull}		5	10	μA	
Start Up Time after POR	$trbs^{(2)}$		10	30	μs	
Common Mode Transient Immunity	CMTI	± 200	± 250		kV/us	See Figure 6.2 , $C_L = 15pF$
⁽¹⁾ Not test covered, guaranteed by characterization.						
⁽²⁾ Not test covered, guaranteed by design.						

6.2. Supply Current Characteristics – 5V Supply

($V_{DD1} = 5V \pm 10\%$, $V_{DD2} = 5V \pm 10\%$, $T_a = -40^\circ C$ to $125^\circ C$. Unless otherwise noted, Typical values are at **$V_{DD1} = 5V$, $V_{DD2} = 5V$** , $T_a = 25^\circ C$)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSI8360					
	I _{DD1} (Q0)		1.60	2.55	mA	All Input 0V for NSI8360x0 Or All Input at supply for NSI8360x1
	I _{DD2} (Q0)		3.85	5.78	mA	
	I _{DD1} (Q1)		8.38	12.04	mA	All Input at supply for NSI8360x0 Or All Input 0V for NSI8360x1
	I _{DD2} (Q1)		3.91	5.67	mA	
	I _{DD1} (1M)		4.91	6.34	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		4.35	6.25	mA	
	I _{DD1} (10M)		5.18	7.77	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		8.78	11.61	mA	
	I _{DD1} (100M)		8.63	12.94	mA	All Input with 100Mbps, C _L =15pF
	I _{DD2} (100M)		24.86	37.30	mA	
	NSI8361					
	I _{DD1} (Q0)		2.06	2.78	mA	All Input 0V for NSI8361x0 Or All Input at supply for NSI8361x1
	I _{DD2} (Q0)		3.88	5.23	mA	
	I _{DD1} (Q1)		7.72	10.95	mA	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I _{DD2} (Q1)		5.72	6.81	mA	All Input at supply for NSI8361x0 Or All Input 0V for NSI8361x1
	I _{DD1} (1M)		4.90	7.03	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		4.86	6.27	mA	
	I _{DD1} (10M)		5.08	7.49	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		8.04	10.59	mA	
	I _{DD1} (100M)		11.34	17.00	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		22.16	33.24	mA	
	NSI8362					
	I _{DD1} (Q0)		2.51	3.38	mA	All Input 0V for NSI8362x0 Or All Input at supply for NSI8362x1
	I _{DD2} (Q0)		3.42	4.58	mA	
	I _{DD1} (Q1)		7.06	9.25	mA	All Input at supply for NSI8362x0 Or All Input 0V for NSI8362x1
	I _{DD2} (Q1)		5.74	7.46	mA	
	I _{DD1} (1M)		4.89	6.31	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		4.87	6.28	mA	
	I _{DD1} (10M)		5.82	7.51	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		7.30	9.56	mA	
	I _{DD1} (100M)		14.04	21.06	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		19.45	29.18	mA	
	NSI8363					
	I _{DD1} (Q0)		2.97	3.98	mA	All Input 0V for NSI8363x0 Or All Input at supply for NSI8363x1
	I _{DD2} (Q0)		2.97	3.98	mA	
	I _{DD1} (Q1)		6.40	8.36	mA	All Input at supply for NSI8363x0 Or All Input 0V for NSI8363x1
	I _{DD2} (Q1)		6.40	8.36	mA	
	I _{DD1} (1M)		4.88	6.30	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		4.88	6.30	mA	
	I _{DD1} (10M)		6.56	8.54	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		6.56	8.54	mA	
I _{DD1} (100M)		16.75	25.12	mA	All Input with 100Mbps,	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I _{DD2} (100M)		16.75	25.12	mA	C _L = 15pF

6.3. Supply Current Characteristics –3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSI8360					
	I _{DD1} (Q0)		1.54	2.11	mA	All Input 0V for NSI8360x0 Or All Input at supply for NSI8360x1
	I _{DD2} (Q0)		3.72	5.62	mA	
	I _{DD1} (Q1)		8.23	10.85	mA	All Input at supply for NSI8360x0 Or All Input 0V for NSI8360x1
	I _{DD2} (Q1)		3.78	5.51	mA	
	I _{DD1} (1M)		4.89	6.41	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		4.53	5.93	mA	
	I _{DD1} (10M)		4.76	6.29	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		6.95	8.99	mA	
	I _{DD1} (100M)		9.45	13.85	mA	All Input with 100Mbps, C _L =15pF
	I _{DD2} (100M)		16.29	24.38	mA	
	NSI8361					
	I _{DD1} (Q0)		1.99	2.70	mA	All Input 0V for NSI8361x0 Or All Input at supply for NSI8361x1
	I _{DD2} (Q0)		3.77	5.04	mA	
	I _{DD1} (Q1)		7.58	9.96	mA	All Input at supply for NSI8361x0 Or All Input 0V for NSI8361x1
	I _{DD2} (Q1)		4.96	6.40	mA	
	I _{DD1} (1M)		4.83	6.33	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		4.59	6.01	mA	
	I _{DD1} (10M)		5.13	6.74	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		6.59	8.54	mA	
	I _{DD1} (100M)		10.59	15.61	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		15.15	22.63	mA	
	NSI8362					
	I _{DD1} (Q0)		2.43	3.28	mA	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I _{DD2} (Q0)		3.32	4.45	mA	All Input 0V for NSI8361x0 Or All Input at supply for NSI8361x1
	I _{DD1} (Q1)		6.92	9.07	mA	All Input at supply for NSI8361x0 Or All Input 0V for NSI8361x1
	I _{DD2} (Q1)		5.61	7.29	mA	
	I _{DD1} (1M)		4.77	6.25	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		4.65	6.09	mA	
	I _{DD1} (10M)		5.49	7.19	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		6.22	8.09	mA	
	I _{DD1} (100M)		11.73	17.36	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		14.01	20.87	mA	
	NSI8363					
	I _{DD1} (Q0)		2.88	3.87	mA	All Input 0V for NSI8362x0 Or All Input at supply for NSI8362x1
	I _{DD2} (Q0)		2.88	3.87	mA	
	I _{DD1} (Q1)		6.27	8.18	mA	All Input at supply for NSI8362x0 Or All Input 0V for NSI8362x1
	I _{DD2} (Q1)		6.27	8.18	mA	
	I _{DD1} (1M)		4.71	6.17	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		4.71	6.17	mA	
	I _{DD1} (10M)		5.86	7.64	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		5.86	7.64	mA	
	I _{DD1} (100M)		12.87	19.12	mA	All Input with 100Mbps, C _L = 15pF
I _{DD2} (100M)		12.87	19.12	mA		

6.4. Supply Current Characteristics–2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSI8360					
	I _{DD1} (Q0)		1.50	2.05	mA	All Input 0V for NSI8360x0 Or All Input at supply for NSI8360x1
	I _{DD2} (Q0)		4.14	5.53	mA	
	I _{DD1} (Q1)		8.12	10.63	mA	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I _{DD2} (Q1)		3.71	5.53	mA	All Input at supply for NSI8360x0 Or All Input 0V for NSI8360x1
	I _{DD1} (1M)		4.81	6.42	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		4.39	5.64	mA	
	I _{DD1} (10M)		4.78	6.27	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		6.19	8.10	mA	
	I _{DD1} (100M)		6.42	10.02	mA	All Input with 100Mbps, C _L =15pF
	I _{DD2} (100M)		14.19	20.52	mA	
	NSI8361					
	I _{DD1} (Q0)		1.94	2.63	mA	All Input 0V for NSI8361x0 Or All Input at supply for NSI8361x1
	I _{DD2} (Q0)		3.70	4.95	mA	
	I _{DD1} (Q1)		7.47	9.78	mA	All Input at supply for NSI8361x0 Or All Input 0V for NSI8361x1
	I _{DD2} (Q1)		4.87	6.38	mA	
	I _{DD1} (1M)		4.74	6.29	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		4.46	5.77	mA	
	I _{DD1} (10M)		5.02	6.58	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		5.96	7.80	mA	
	I _{DD1} (100M)		7.72	11.77	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		12.90	18.77	mA	
	NSI8362					
	I _{DD1} (Q0)		2.38	3.21	mA	All Input 0V for NSI8361x0 Or All Input at supply for NSI8361x1
	I _{DD2} (Q0)		3.26	4.37	mA	
	I _{DD1} (Q1)		6.82	8.93	mA	All Input at supply for NSI8361x0 Or All Input 0V for NSI8361x1
	I _{DD2} (Q1)		5.52	7.23	mA	
	I _{DD1} (1M)		4.67	6.16	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		4.53	5.90	mA	
	I _{DD1} (10M)		5.25	6.88	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		5.72	7.49	mA	
	I _{DD1} (100M)		9.01	13.52	mA	All Input with 100Mbps,

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I _{DD2} (100M)		11.60	17.02	mA	C _L = 15pF
	NSI8363					
	I _{DD1} (Q0)		2.82	3.79	mA	All Input 0V for NSI8362x0 Or All Input at supply for NSI8362x1
	I _{DD2} (Q0)		2.82	3.79	mA	
	I _{DD1} (Q1)		6.17	8.08	mA	All Input at supply for NSI8362x0 Or All Input 0V for NSI8362x1
	I _{DD2} (Q1)		6.17	8.08	mA	
	I _{DD1} (1M)		4.60	6.03	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		4.60	6.03	mA	
	I _{DD1} (10M)		5.49	7.19	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		5.49	7.19	mA	
	I _{DD1} (100M)		10.31	15.27	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		10.31	15.27	mA	

6.5. Switching Characteristics - 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V**, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t _{PLH}		10.7	15	ns	See Figure 6.1 , C _L = 15pF
	t _{PHL}		9.4	15	ns	See Figure 6.1 , C _L = 15pF
Pulse Width Distortion t _{PHL} - t _{PLH}	PWD			5.0	ns	See Figure 6.1 , C _L = 15pF
Rising Time	t _r			5.0	ns	See Figure 6.1 , C _L = 15pF
Falling Time	t _f			5.0	ns	See Figure 6.1 , C _L = 15pF
Peak Eye Diagram Jitter	t _{JIT} (PK)		2.0		ns	
Channel-to-Channel Delay Skew	t _{SK} (c2c)			2.5	ns	
Part-to-Part Delay Skew	t _{SK} (p2p)			5.0	ns	

6.6. Switching Characteristics - 3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V**, Ta = 25°C)

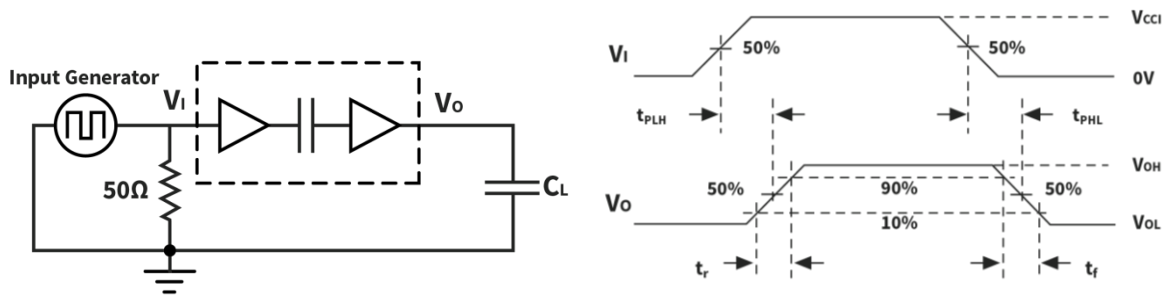
Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t _{PLH}		11.4	17	ns	See Figure 6.1 , C _L = 15pF
	t _{PHL}		10.5	17	ns	See Figure 6.1 , C _L = 15pF
Pulse Width Distortion t _{PHL} - t _{PLH}	PWD			5.0	ns	See Figure 6.1 , C _L = 15pF
Rising Time	t _r			5.0	ns	See Figure 6.1 , C _L = 15pF
Falling Time	t _f			5.0	ns	See Figure 6.1 , C _L = 15pF
Peak Eye Diagram Jitter	t _{JIT} (PK)		2.0		ns	
Channel-to-Channel Delay Skew	t _{SK} (c2c)			2.5	ns	
Part-to-Part Delay Skew	t _{SK} (p2p)			5.0	ns	

6.7. Switching Characteristics - 2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}		12.4	18	ns	See Figure 6.1 , $C_L = 15\text{pF}$
	t_{PHL}		11.7	18	ns	See Figure 6.1 , $C_L = 15\text{pF}$
Pulse Width Distortion $ t_{PHL} - t_{PLH} $	PWD			5.0	ns	See Figure 6.1 , $C_L = 15\text{pF}$
Rising Time	t_r			5.0	ns	See Figure 6.1 , $C_L = 15\text{pF}$
Falling Time	t_f			5.0	ns	See Figure 6.1 , $C_L = 15\text{pF}$
Peak Eye Diagram Jitter	$t_{JIT(PK)}$		2.0		ns	
Channel-to-Channel Delay Skew	$t_{SK(c2c)}$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK(p2p)}$			5.0	ns	

6.8. Parameter Measurement Information



(1) Input Generator Characteristics : PRR ≤ 50kHz, $t_r \leq 3\text{ns}$, $t_f \leq 3\text{ns}$, Duty cycle = 50%, $Z_o = 50\ \Omega$.

Figure 6.1 Switching Characteristics Test Circuit and Waveform

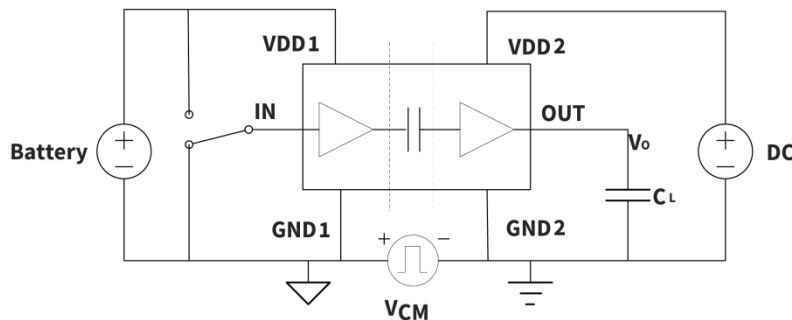


Figure 6.2 Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

<i>Parameters</i>	<i>Symbol</i>	<i>Value</i>		<i>Comments</i>
		SOP16 (300mil)	<i>Unit</i>	
Minimum External Clearance	CLR	8	mm	IEC 60664-1
Minimum External Creepage	CPG	8	mm	IEC 60664-1
Distance Through Insulation	DTI	24	µm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

<i>Description</i>	<i>Test Condition</i>	<i>Value</i>
		SOP16 (300mil)
Overvoltage Category per IEC60664-1	For Rated Mains Voltage $\leq$ 150Vrms	I to IV
	For Rated Mains Voltage $\leq$ 300Vrms	I to IV
	For Rated Mains Voltage $\leq$ 600Vrms	I to IV
	For Rated Mains Voltage $\leq$ 1000Vrms	I to III
Climatic Classification		40/125/21
Pollution Degree per DIN VDE 0110		2

7.2. Insulation Characteristics

<i>Description</i>	<i>Test Condition</i>	<i>Symbol</i>	<i>Value</i>	<i>Unit</i>
			SOP16 (300mil)	
Maximum repetitive isolation voltage		V_{IORM}	2121	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	1500	V_{RMS}
	DC Voltage		2121	V_{DC}

Description	Test Condition	Symbol	Value	
			SOP16 (300mil)	Unit
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, $t_{ini} = 60\text{ s}$, $V_{pd(m)}=1.2*V_{IORM}$, $t_m=10\text{s}$.	q_{pd}	<5	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, $t_{ini}=60\text{s}$, $V_{pd(m)}=1.6*V_{IORM}$, $t_m=10\text{s}$			pC
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}$, $t_{ini}=1\text{s}$ $V_{pd(m)}=1.875*V_{IORM}$, $t_m=1\text{s}$ (method b1) or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$ (method b2)			pC
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, $t_{ini} = 60\text{ s}$, $V_{pd(m)}=1.2*V_{IORM}$, $t_m=10\text{s}$.	q_{pd}	\	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, $t_{ini}=60\text{s}$, $V_{pd(m)}=1.3*V_{IORM}$, $t_m=10\text{s}$			pC
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}$, $t_{ini}=1\text{s}$ $V_{pd(m)}=1.5*V_{IORM}$, $t_m=1\text{s}$ (method b1) or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$ (method b2)			pC
Maximum transient isolation voltage	$t = 60\text{ sec}$	V_{IOTM}	8000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50-us waveform per IEC62368-1	V_{IMP}	6250	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us	V_{IOSM}	10000	V_{PEAK}

Description	Test Condition	Symbol	Value	
			SOP16 (300mil)	Unit
	waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$			
Isolation resistance	$V_{IO} = 500V, T_{amb} = 25^{\circ}C$	R_{IO}	$>10^{12}$	Ω
	$V_{IO} = 500V, 100^{\circ}C \leq T_{amb} \leq 125^{\circ}C$	R_{IO}	$>10^{11}$	Ω
	$V_{IO} = 500V, T_{amb} = T_s$	R_{IO}	$>10^9$	Ω
Isolation capacitance	$f = 1MHz$	C_{IO}	0.8	pF
Insulation voltage per UL	$V_{TEST} = V_{ISO}, t = 60 s$ (qualification), $V_{TEST} = 1.2 \times V_{ISO}, t = 1 s$ (100% production test)	V_{ISO}	5000	V_{RMS}

7.3. Safety-Limiting Values

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI836x-Q1-DSWR.

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{\theta JA} = 78.9^{\circ}C/W^{(1)}, T_J = 150^{\circ}C, T_A = 25^{\circ}C$	1584	mW
Safety Supply Current	$R_{\theta JA} = 78.9^{\circ}C/W^{(1)}, V_I = 5V, T_J = 150^{\circ}C, T_A = 25^{\circ}C$	316.8	mA
Safety Temperature ²⁾		150	$^{\circ}C$

- 1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP16(300mil) package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

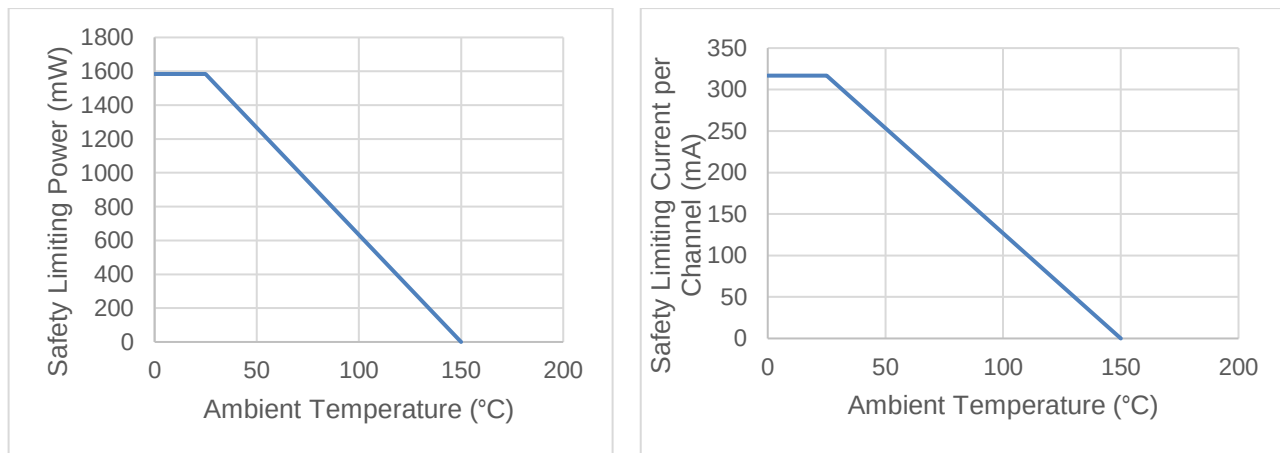


Figure 7.1 NSI836x-Q1 Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17).

7.4. Regulatory Information

The NSI836x-Wx-Q1SWR are approved by the organizations listed in table.

UL		CQC		TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to GB4943.1-2022	DIN EN IEC 60747-17 (VDE 0884-17)	Certified According to EN IEC 62368-1
Single Protection, 5000V _{rms} Isolation voltage	Single Protection, 5000V _{rms} Isolation voltage	Reinforced insulation	Reinforced Insulation V _{IORM} =2121V _{peak} V _{IOTM} =8000V _{peak} V _{IOSM} =10000V _{peak}	5000V _{rms} for 1min
E500602	E500602	CQC20001264939	R 50632560	R 50574061

8. Function Description

8.1. Overview

The NSI836x-Q1 is a Six-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NSI836x-Q1 devices are high reliability six-channel digital isolators. The NSI836x-Q1 device is safety certified by UL1577 and supports $5kV_{rms}$ insulation withstand voltages, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI836x-Q1 is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 250kV/us. The NSI836x-Q1 device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI836x-Q1 device supports connecting with most digital interfaces directly, making level shifting easy. High system level EMC performance enhances reliability and stability of use.

The NSI836x-Q1 has a default output status when VDDIN is unready and VDDOUT is ready as shown in Table 8.1, which helps with diagnosis when power is missing at the transmitter side. The output B follows the same status as the input A after powering up.

Table 8.1 Output status vs. power status

Input ¹	VDDIN status	VDDOUT status	Output	Comment
H	Ready	Ready	H	Normal operation.
L	Ready	Ready	L	
X	Unready	Ready	L(NSI836xx0) H(NSI836xx1)	The output follows the same status with the input after input side VDD is powered on.
X	Ready	Unready	Undetermined	The output follows the same status with the input after output side VDD2 is powered on.
Note: H=Logic high; L=Logic low; X=Logic low or logic high VDDIN is input side power; VDDOUT is output side power. (1) There is a protection diode between the input and the VDDIN. When the VDDIN is floating, the strong drive signal through the input pin will put the VDDIN in an indeterminate state.				

8.2. OOK Modulation

NSI836x-Q1 is based on a capacitive isolation barrier technique and the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, as shown in Figure 8.1 to Figure 8.2, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI.

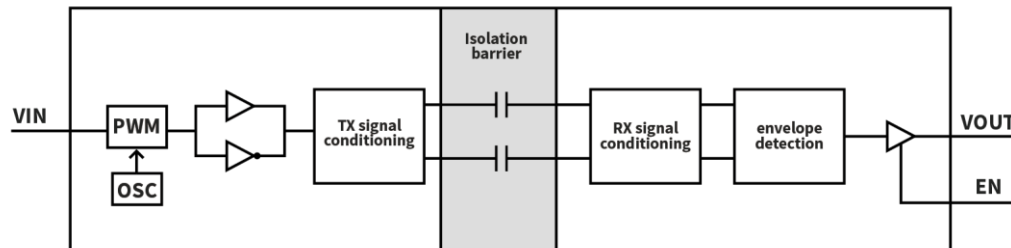


Figure 8.1 Single Channel Function Block Diagram

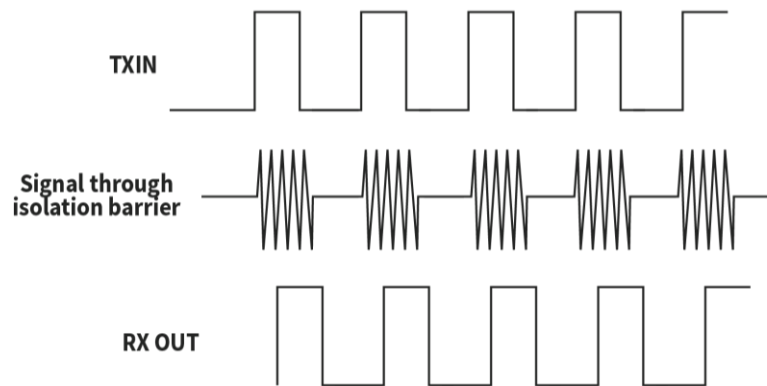


Figure 8.2 OOK Modulation

9. Application Note

9.1. Typical Application Circuit

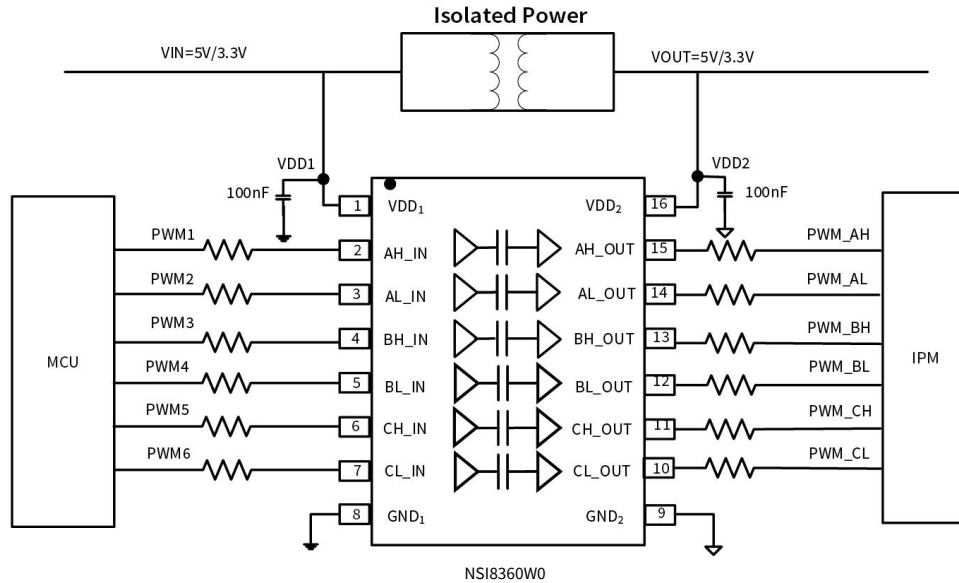


Figure 9.1 Typical PWM isolation circuit for IPM

9.2. PCB Layout

The NSI836x-Q1 requires a 0.1 μF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. Figure 9.2 to Figure 9.3 show the recommended PCB layout, make sure the space under the chip should be kept free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω , $\pm 40\%$. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

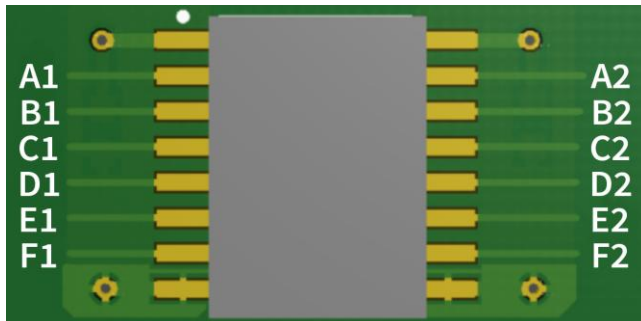


Figure 9.2 Recommended PCB Layout — Top Layer



Figure 9.3 Recommended PCB Layout — Bottom Layer

9.3. High Speed Performance

Figure 9.4 shows the eye diagram of NSI836x-Q1 at 50Mbps data rate output. The result shows a typical measurement on NSI836x-Q1 with low jitter and wide open eye characteristics.

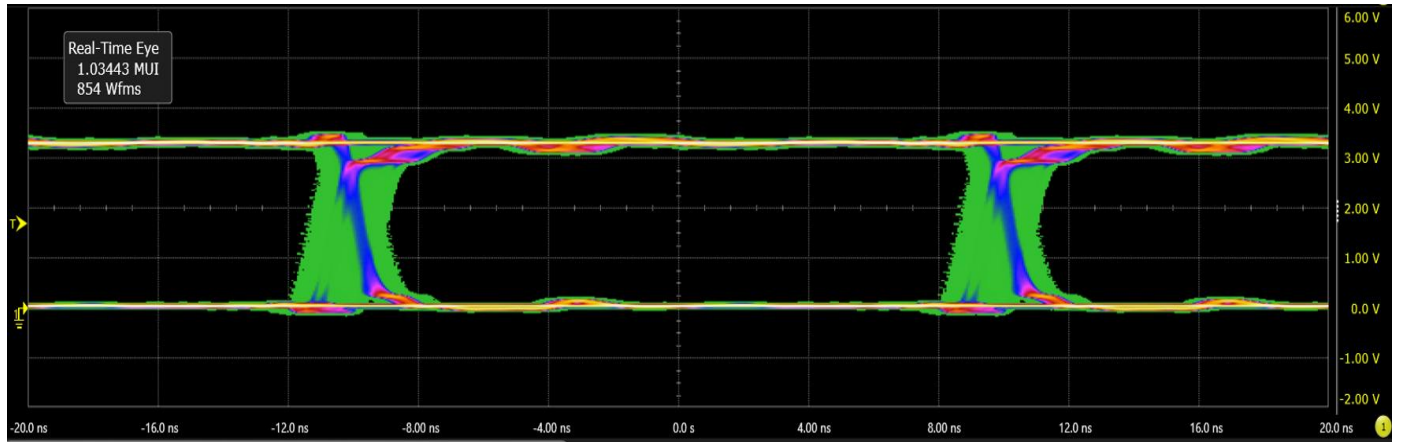


Figure9.4 Eye Diagram at 50Mbps PRBS $2^{16}-1$, 2.5V and 25°C

10. Package Information

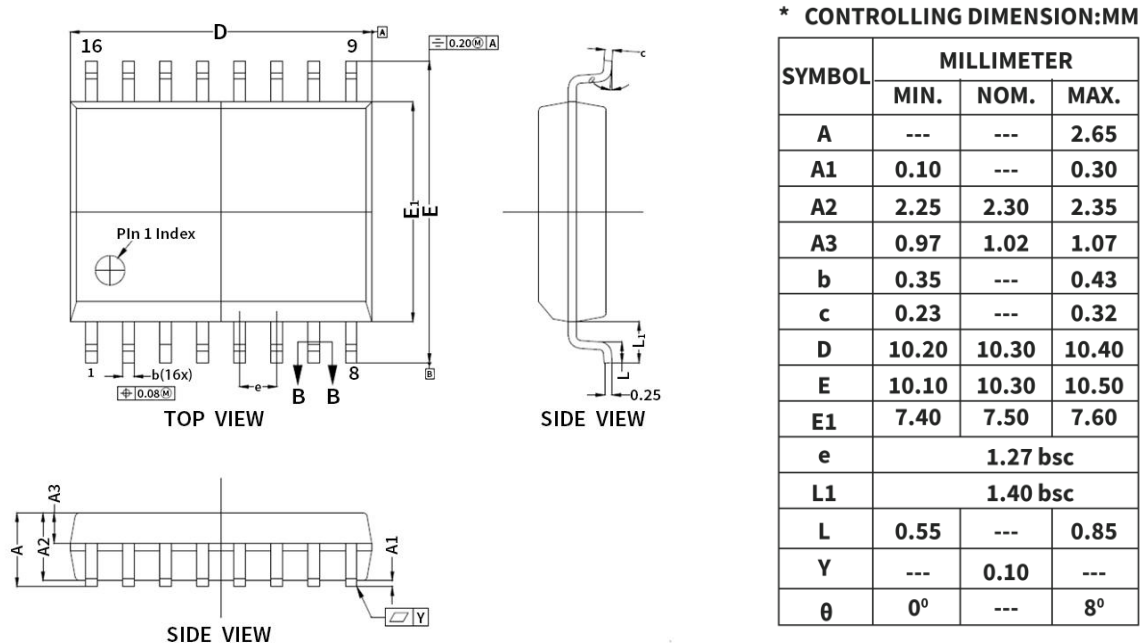


Figure 10.1 SOP16(300mil)/SOW16 Package Shape and Dimension in millimeters

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

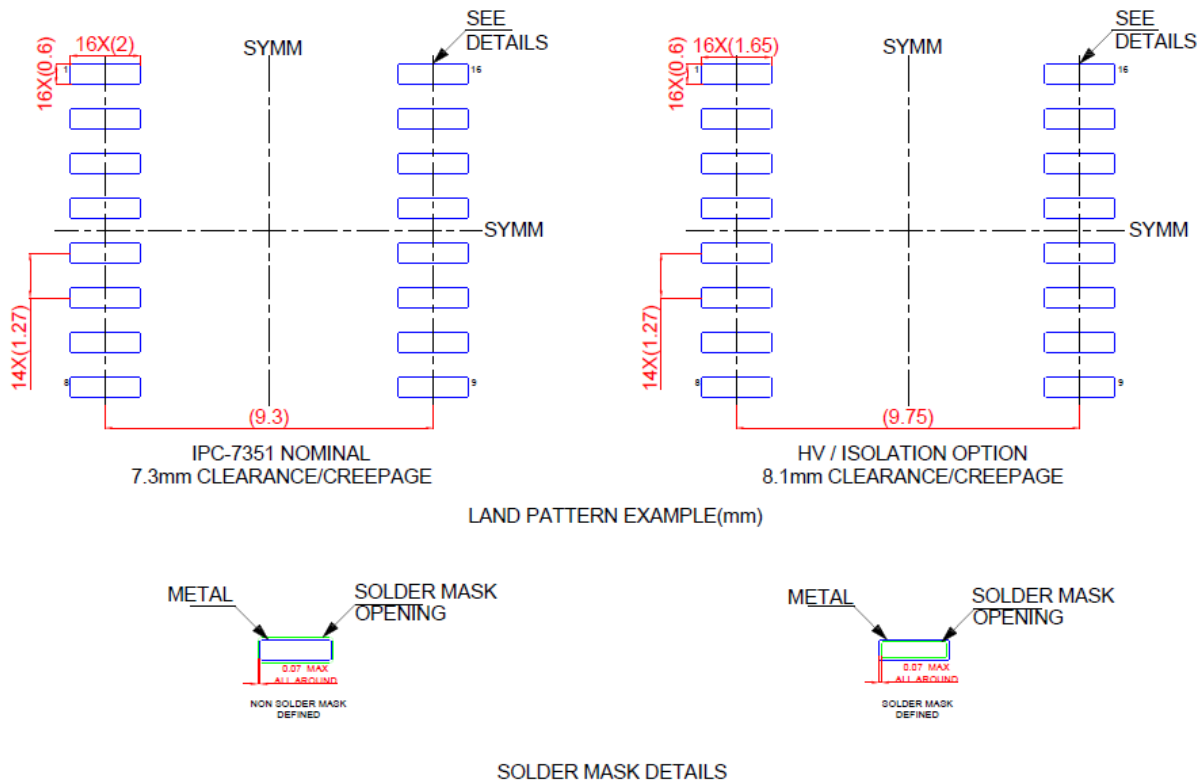


Figure 10.2 SOP16(300mil) SOW16 Package Board Layout Example

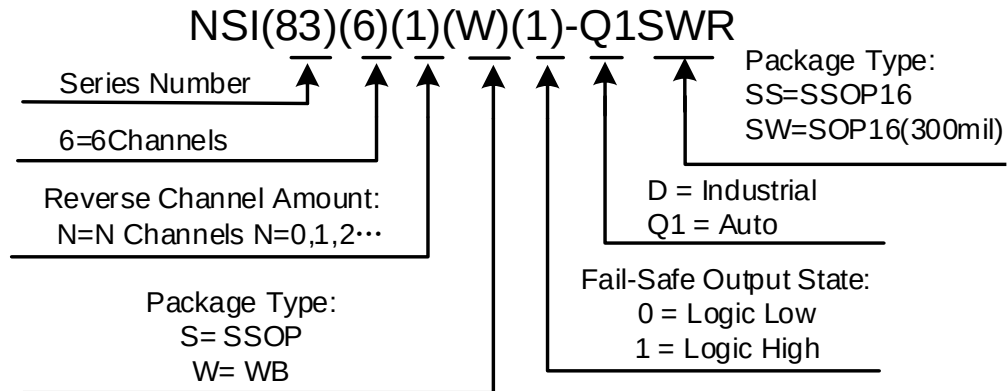
11. Order Information

Part Number	Isolation Rating (kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	MSL	Package Type	Package Drawing	SPQ	MPQ
NSI8360W0-Q1SWR	5	6	0	150	Low	-40 to 125°C	3	SOP16 (300mil)	SOW16	1000	1000
NSI8360W1-Q1SWR	5	6	0	150	High	-40 to 125°C	3	SOP16 (300mil)	SOW16	1000	1000
NSI8361W0-Q1SWR	5	5	1	150	Low	-40 to 125°C	3	SOP16 (300mil)	SOW16	1000	1000
NSI8361W1-Q1SWR	5	5	1	150	High	-40 to 125°C	3	SOP16 (300mil)	SOW16	1000	1000
NSI8362W0-Q1SWR	5	4	2	150	Low	-40 to 125°C	3	SOP16 (300mil)	SOW16	1000	1000
NSI8362W1-Q1SWR	5	4	2	150	High	-40 to 125°C	3	SOP16 (300mil)	SOW16	1000	1000
NSI8363W0-Q1SWR	5	3	3	150	Low	-40 to 125°C	3	SOP16 (300mil)	SOW16	1000	1000
NSI8363W1-Q1SWR	5	3	3	150	High	-40 to 125°C	3	SOP16 (300mil)	SOW16	1000	1000

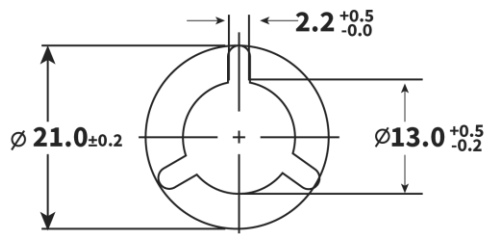
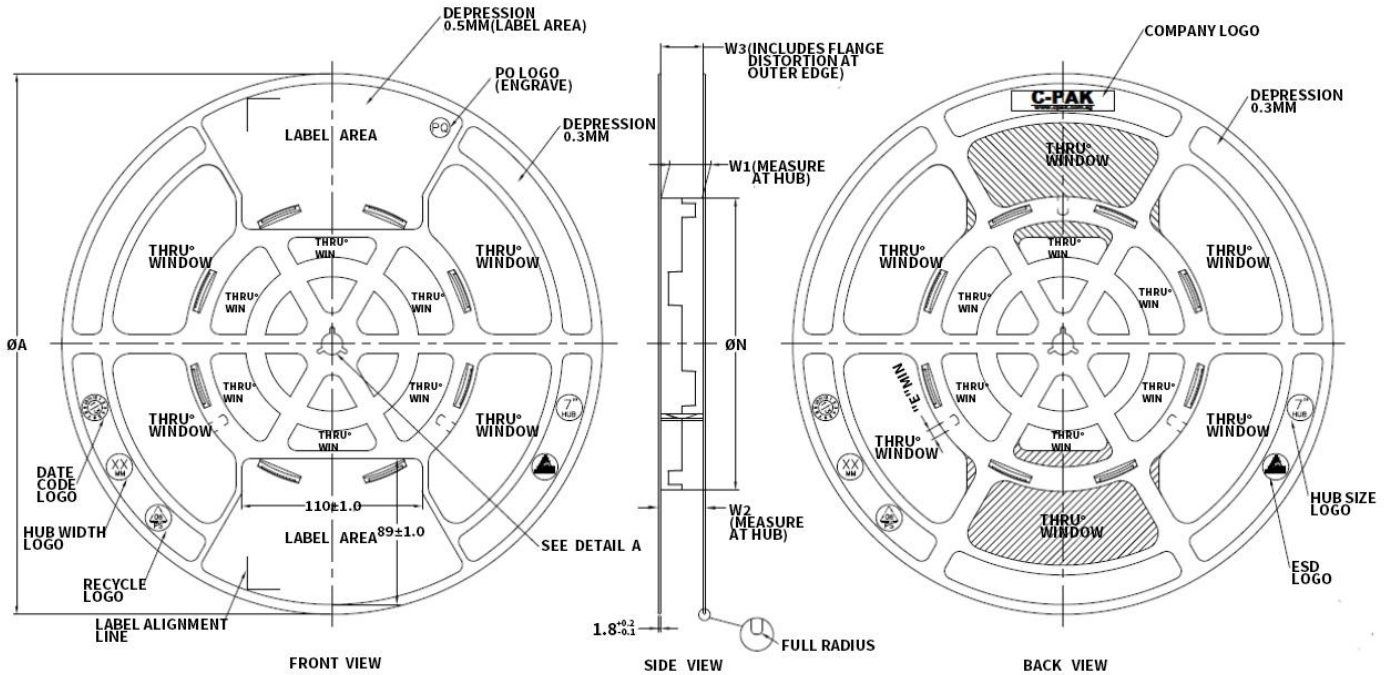
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 360 °C according to the JEDEC industry standard classifications and peak solder temperatures.

All devices are AEC-Q100 qualified.

Part Number Rule:



12. Tape and Reel Information

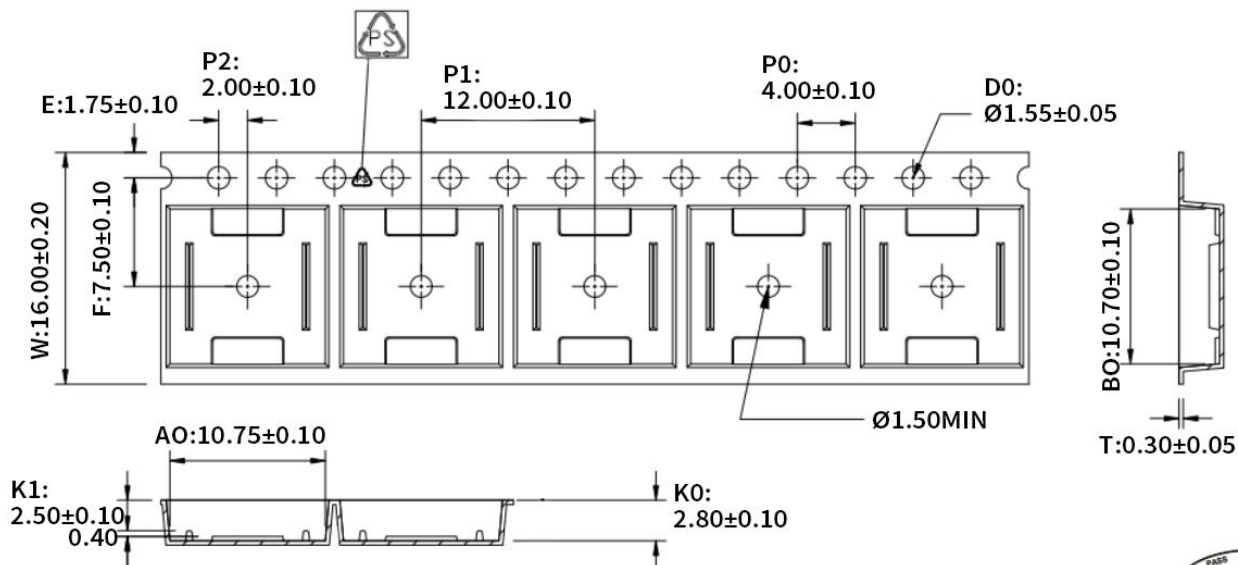


**ARBOR HOLE
DETAIL A
SCALE: 3:1**

PRODUCT SPECIFICATION						
TAPE WIDTH	Ø A ±2.0	Ø N ±2.0	W1	W2 (Max)	W3	E (MIN)
08MM	330	178	8.4 ^{+1.5} _{-0.0}	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 ^{+2.0} _{-0.0}	18.4		5.5
16MM	330	178	16.4 ^{+2.0} _{-0.0}	22.4		5.5
24MM	330	178	24.4 ^{+2.0} _{-0.0}	30.4		5.5
32MM	330	178	32.4 ^{+2.0} _{-0.0}	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10 ¹²	ANTISTATIC	ALL TYPES
B	10 ⁶ TO 10 ¹¹	STATIC DISSIPATIVE	BLACK ONLY
C	10 ⁵ & BELOW 10 ⁵	CONDUCTIVE(GENERIC)	BLACK ONLY
E	10 ⁹ TO 10 ¹¹	ANTISTATIC(COATED)	ALL TYPES

Figure 12.1 Reel Information (for all packages)



1. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness: 0.30 ± 0.05 mm.
6. Packing length per 22" reel: 378 Meters. (Rewind N=122)
7. Component load per 13" reel: 1000 pcs.
8. Surface resistivity: $10^5 \sim 10^{10} \Omega/\square$



W	16.00 ± 0.20
A0	10.75 ± 0.10
B0	10.70 ± 0.10
K0	2.80 ± 0.10
K1	2.50 ± 0.10

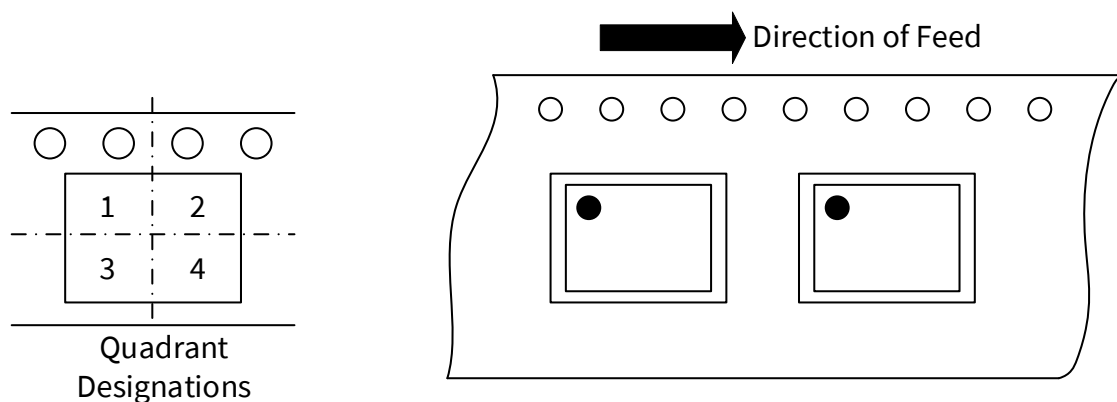


Figure 12.2 Tape Information of SOP16(300mil)

13. Revision History

Revision	Description	Date
1.0	Initial version	2026/6/25

IMPORTANT NOTICE

The information given in this document (the “Document”) shall in no event be regarded as any warranty or authorization of, express or implied, including but not limited to accuracy, completeness, merchantability, fitness for a particular purpose or infringement of any third party’s intellectual property rights.

Users of this Document shall be solely responsible for the use of NOVOSENSE’s products and applications, and for the safety thereof. Users shall comply with all laws, regulations and requirements related to NOVOSENSE’s products and applications, although information or support related to any application may still be provided by NOVOSENSE.

This Document is provided on an “AS IS” basis, and is intended only for skilled developers designing with NOVOSENSE’s products. NOVOSENSE reserves the rights to make corrections, modifications, enhancements, improvements or other changes to the products and services provided without notice. NOVOSENSE authorizes users to use this Document exclusively for the development of relevant applications or systems designed to integrate NOVOSENSE’s products. No license to any intellectual property rights of NOVOSENSE is granted by implication or otherwise. Using this Document for any other purpose, or any unauthorized reproduction or display of this Document is strictly prohibited. In no event shall NOVOSENSE be liable for any claims, damages, costs, losses or liabilities arising out of or in connection with this Document or the use of this Document.

For further information on applications, products and technologies, please contact NOVOSENSE (www.novosns.com).

Suzhou NOVOSENSE Microelectronics Co., Ltd