

Product Overview

The NSI834x devices are high reliability quad-channel digital isolators. The NSI834x device is safety certified by UL1577 and supports 3kV_{rms} insulation withstand voltage, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI834x is up to 100Mbps, and the common-mode transient immunity (CMTI) is up to $200\text{kV}/\mu\text{s}$. The NSI834x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI834x device supports direct connection to most digital interfaces, making level shifting easy. High system level EMC performance enhance reliability and stability of use. AEC-Q100 (Grade 1) option is provided for all devices.

Key Features

- Up to $3000\text{V}_{\text{rms}}$ Insulation voltage
- Data rate: DC to 100Mbps
- Power supply voltage: 2.5V to 5.5V
- High CMTI: $200\text{kV}/\mu\text{s}$
- Chip level ESD: HBM: $\pm 8\text{kV}$
- Robust Electromagnetic Compatibility (EMC)
 - System-Level ESD, EFT, and Surge Immunity
 - Low Emissions
- Default output high level or low-level option
- Low power consumption: $1.5\text{mA}/\text{ch}$ (1 Mbps)
- Low propagation delay: $<18\text{ns}$
- Operation temperature: $-40^{\circ}\text{C}\sim 125^{\circ}\text{C}$
- AEC-Q100 Qualified

- RoHS-compliant packages:
 - SSOP16

Safety Regulatory Approvals

- UL recognition: up to $3000\text{V}_{\text{rms}}$ for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor control

Device Information

Part Number	Package	Body Size
NSI834xSx-Q1SSR	SSOP16	$5.40\text{mm} \times 3.90\text{mm}$

Functional Block Diagrams

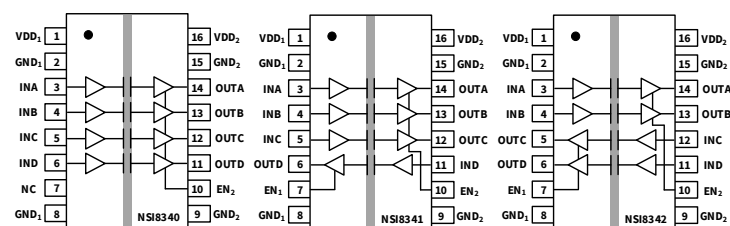


Figure 1. NSI834x Block Diagram

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1. Pin Configuration and Functions

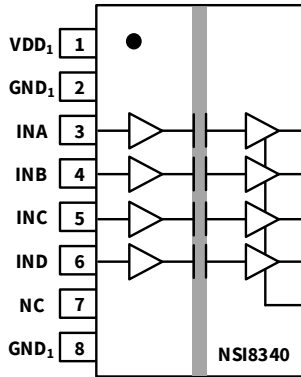


Figure 1.1 NSI8340 Package

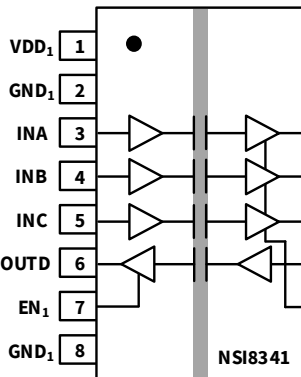


Figure 1.2 NSI8341 Package

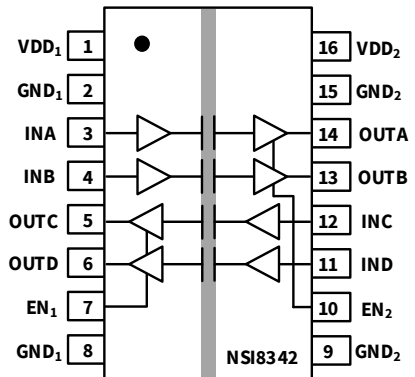


Figure 1.3 NSI8342 Package

Table 1.1 NSI834x Pin Configuration and Description

NSI8340 PIN NO.	NSI8341 PIN NO.	NSI8342 PIN NO.	SYMBOL	FUNCTION
1	1	1	VDD ₁	Power Supply for Isolator Side 1
2	2	2	GND ₁	Ground 1, the ground reference for Isolator Side 1
3	3	3	INA	Logic Input A
4	4	4	INB	Logic Input B
5	5	12	INC	Logic Input C
6	11	11	IND	Logic Input D
7	7	7	NC/EN ₁	No Connection (NSI8340). Or Output Enable 1 (NSI8341/2). Active high logic input. When EN ₁ is high or NC, the output of Side 1 is enabled. When EN ₁ is low, the output of Side 1 is disabled to high impedance state.
8	8	8	GND ₁	Ground 1, the ground reference for Isolator Side 1
9	9	9	GND ₂	Ground 2, the ground reference for Isolator Side 2
10	10	10	EN ₂	Output Enable 2. Active high logic input. When EN ₂ is high or NC, the output of Side 2 is enabled. When EN ₂ is low, the output of Side 2 is disabled to high impedance state.
11	6	6	OUTD	Logic Output D
12	12	5	OUTC	Logic Output C
13	13	13	OUTB	Logic Output B
14	14	14	OUTA	Logic Output A
15	15	15	GND ₂	Ground 2, the ground reference for Isolator Side 2
16	16	16	VDD ₂	Power Supply for Isolator Side 2

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	VINA, VINB, VINC, VIND	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Output Voltage	VOUTA, VOUTB, VOUTC, VOUTD	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Input/Output Pulse Voltage	VINA, VINB, VINC, VIND, VOUTA, VOUTB, VOUTC, VOUTD	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Output current	I _o	-15		15	mA	
Operating Temperature	T _{opr}	-40		125	°C	
Junction Temperature	T _j			150	°C	
Storage Temperature	T _{stg}	-65		150	°C	

3. ESD Ratings

Parameters	Ratings	Value	Unit
Electrostatic discharge (ESD)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽²⁾	±8000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽³⁾	±2000	V

(1) Though this device features proprietary protection circuitry, proper ESD precautions should be considered to avoid performance degradation of damage due to high energy ESD event. Charged devices and circuit boards may discharge without detection.

(2) Safe manufacturing requires 500-V HBM and standard ESD precautions, per JEDEC document JEP155.

(3) Safe manufacturing requires 250-V CDM and standard ESD precautions, per JEDEC document JEP157.

4. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit
Power Supply Voltage	VDD1, VDD2	2.5		5.5	V
Operating Temperature	T _{opr}	-40		125	°C
High Level Input Voltage	V _{IH}	2			V
Low Level Input Voltage	V _{IL}			0.8	V
Data rate	DR			100	Mbps

5. Thermal Information

Parameters	Symbol	SSOP16	Unit
IC Junction-to-Air Thermal Resistance	$R_{\theta JA}$	140	$^{\circ}\text{C/W}$
Junction-to-case (top) thermal resistance	$R_{\theta JC (top)}$	54.4	$^{\circ}\text{C/W}$
Junction-to-board thermal resistance	$R_{\theta JB}$	51.9	$^{\circ}\text{C/W}$
Junction-to-top characterization parameter	Ψ_{JT}	6.7	$^{\circ}\text{C/W}$
Junction-to-board characterization parameter	Ψ_{JB}	33	$^{\circ}\text{C/W}$

6. Specifications

6.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power on Reset	$V_{DDPOR}^{(1)}$	2	2.2	2.4	V	POR threshold as during power-up
	$V_{DDHYS}^{(1)}$		0.1		V	POR threshold Hysteresis
Rising input switching threshold	$V_{IT+}^{(1)}$		1.5	2	V	
Falling input switching threshold	$V_{IT-}^{(1)}$	0.8	1.15		V	
Input threshold voltage hysteresis	$V_{ITHYS}^{(1)}$		0.35		V	
High Level Output Voltage	V_{OH}	VDD-0.4			V	$I_{OH} = -4\text{mA}$
Low Level Output Voltage	V_{OL}			0.4	V	$I_{OL} = 4\text{mA}$
Output Impedance	$R_{out}^{(1)}$		50		ohm	
Input Pull high or low Current	I_{pull}		5	10	μA	
Start Up Time after POR	trbs ⁽²⁾		22	32	μs	
Common Mode Transient Immunity	CMTI	± 150	± 200		$\text{kV}/\mu\text{s}$	See Figure 6.11 , $C_L = 15\text{pF}$

⁽¹⁾ Not test covered, guaranteed by characterization.

⁽²⁾ Not test covered, guaranteed by design.

6.2. Supply Current Characteristics – 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSI8340					
	I _{DD1} (Q0)		1.48	1.74	mA	All Input 0V for NSI8340x0 Or All Input at supply for NSI8340x1
	I _{DD2} (Q0)		4.28	5.10	mA	
	I _{DD1} (Q1)		6.20	7.44	mA	All Input at supply for NSI8340x0 Or All Input 0V for NSI8340x1
	I _{DD2} (Q1)		4.30	5.14	mA	
	I _{DD1} (1M)		3.93	4.71	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		4.37	5.29	mA	
	I _{DD1} (10M)		4.16	5.20	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		5.80	7.00	mA	
	I _{DD1} (100M)		4.77	5.95	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		26.39	32.99	mA	
	NSI8341					
	I _{DD1} (Q0)		2.18	2.58	mA	All Input 0V for NSI8341x0 Or All Input at supply for NSI8341x1
	I _{DD2} (Q0)		3.58	4.26	mA	
	I _{DD1} (Q1)		5.72	6.86	mA	All Input at supply for NSI8341x0 Or All Input 0V for NSI8341x1
	I _{DD2} (Q1)		4.77	5.71	mA	
	I _{DD1} (1M)		4.04	4.85	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		4.26	5.14	mA	
	I _{DD1} (10M)		4.57	5.65	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		5.39	6.55	mA	
	I _{DD1} (100M)		10.17	12.71	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		20.98	26.23	mA	
	NSI8342					
	I _{DD1} (Q0)		2.88	3.42	mA	All Input 0V for NSI8342x0 Or All Input at supply for NSI8342x1
	I _{DD2} (Q0)		2.88	3.42	mA	
	I _{DD1} (Q1)		5.25	6.29	mA	All Input at supply for NSI8342x0
	I _{DD2} (Q1)		5.25	6.29	mA	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
						Or All Input 0V for NSI8342x1
	I _{DD1} (1M)		4.15	5.00	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		4.15	5.00	mA	
	I _{DD1} (10M)		4.98	6.10	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		4.98	6.10	mA	
	I _{DD1} (100M)		15.58	19.47	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		15.58	19.47	mA	

6.3. Supply Current Characteristics –3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSI8340					
	I _{DD1} (Q0)		1.19	1.68	mA	All Input 0V for NSI8340x0 Or All Input at supply for NSI8340x1
	I _{DD2} (Q0)		3.93	5.00	mA	
	I _{DD1} (Q1)		5.84	7.30	mA	All Input at supply for NSI8340x0 Or All Input 0V for NSI8340x1
	I _{DD2} (Q1)		3.94	5.04	mA	
	I _{DD1} (1M)		3.58	4.60	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		3.98	5.12	mA	
	I _{DD1} (10M)		3.82	5.09	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		4.92	6.27	mA	
	I _{DD1} (100M)		4.94	5.92	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		17.08	20.50	mA	
	NSI8341					
	I _{DD1} (Q0)		1.87	2.51	mA	All Input 0V for NSI8341x0 Or All Input at supply for NSI8341x1
	I _{DD2} (Q0)		3.24	4.17	mA	
	I _{DD1} (Q1)		5.36	6.73	mA	All Input at supply for NSI8341x0 Or All Input 0V for NSI8341x1
	I _{DD2} (Q1)		4.41	5.60	mA	
	I _{DD1} (1M)		3.68	4.73	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		3.88	4.99	mA	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I _{DD1} (10M)		4.09	5.38	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		4.64	5.97	mA	
	I _{DD1} (100M)		7.97	9.56	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		14.04	16.85	mA	
	NSI8342					
	I _{DD1} (Q0)		2.56	3.34	mA	All Input 0V for NSI8342x0 Or All Input at supply for NSI8342x1
	I _{DD2} (Q0)		2.56	3.34	mA	
	I _{DD1} (Q1)		4.89	6.17	mA	All Input at supply for NSI8342x0 Or All Input 0V for NSI8342x1
	I _{DD2} (Q1)		4.89	6.17	mA	
	I _{DD1} (1M)		3.78	4.86	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		3.78	4.86	mA	
	I _{DD1} (10M)		4.37	5.68	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		4.37	5.68	mA	
	I _{DD1} (100M)		11.00	13.21	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		11.00	13.21	mA	

6.4. Supply Current Characteristics–2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	NSI8340					
	I _{DD1} (Q0)		1.17	1.64	mA	All Input 0V for NSI8340x0 Or All Input at supply for NSI8340x1
	I _{DD2} (Q0)		3.71	4.82	mA	
	I _{DD1} (Q1)		5.74	6.87	mA	All Input at supply for NSI8340x0 Or All Input 0V for NSI8340x1
	I _{DD2} (Q1)		3.86	5.03	mA	
	I _{DD1} (1M)		3.50	4.21	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		3.86	5.13	mA	
	I _{DD1} (10M)		3.68	4.88	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		4.56	5.82	mA	
	I _{DD1} (100M)		4.66	5.63	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		13.58	16.29	mA	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	NSI8341					
	I _{DD1} (Q0)		1.80	2.43	mA	All Input 0V for NSI8341x0 Or All Input at supply for NSI8341x1
	I _{DD2} (Q0)		3.07	4.02	mA	
	I _{DD1} (Q1)		5.27	6.41	mA	All Input at supply for NSI8341x0 Or All Input 0V for NSI8341x1
	I _{DD2} (Q1)		4.33	5.49	mA	
	I _{DD1} (1M)		3.59	4.44	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		3.77	4.90	mA	
	I _{DD1} (10M)		3.90	5.11	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		4.34	5.58	mA	
	I _{DD1} (100M)		6.89	8.29	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		11.35	13.62	mA	
	NSI8342					
	I _{DD1} (Q0)		2.44	3.23	mA	All Input 0V for NSI8342x0 Or All Input at supply for NSI8342x1
	I _{DD2} (Q0)		2.44	3.23	mA	
	I _{DD1} (Q1)		4.80	5.95	mA	All Input at supply for NSI8342x0 Or All Input 0V for NSI8342x1
	I _{DD2} (Q1)		4.80	5.95	mA	
	I _{DD1} (1M)		3.68	4.67	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		3.68	4.67	mA	
	I _{DD1} (10M)		4.12	5.35	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		4.12	5.35	mA	
	I _{DD1} (100M)		9.12	10.96	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		9.12	10.96	mA	

6.5. Switching Characteristics - 5V Supply

(V_{DD1}=5V± 10%, V_{DD2}=5V± 10%, T_a=-40°C to 125°C. Unless otherwise noted, Typical values are at **V_{DD1} = 5V, V_{DD2} = 5V, T_a = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		100	Mbps	
Minimum Pulse Width	PW			8.3	ns	
Propagation Delay	t _{PLH}		12.0	18	ns	See Figure 6.9 , C _L = 15pF

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	t_{PHL}		12.5	18	ns	See Figure 6.9 , $C_L = 15pF$
Pulse Width Distortion $ t_{PHL} - t_{PLH} $	PWD			5.0	ns	See Figure 6.9 , $C_L = 15pF$
Rising Time	t_r			5.0	ns	See Figure 6.9 , $C_L = 15pF$
Falling Time	t_f			5.0	ns	See Figure 6.9 , $C_L = 15pF$
Peak Eye Diagram Jitter	$t_{JIT(PK)}$		2.5		ns	
Channel-to-Channel Delay Skew	$t_{SK(c2c)}$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK(p2p)}$			5.0	ns	
Disable high to Tri-State	t_{PHZ}		8.67	30	ns	See Figure 6.10 , $C_L = 15pF$, $R_L=1k$
Enable to Data high Valid	t_{PZH}		8.75	30	ns	See Figure 6.10 , $C_L = 15pF$, $R_L=1k$
Disable low to Tri-State	t_{PLZ}		7.7	30	ns	See Figure 6.10 , $C_L = 15pF$, $R_L=1k$
Enable to Data low Valid	t_{PZL}		9.5	30	ns	See Figure 6.10 , $C_L = 15pF$, $R_L=1k$

6.6. Switching Characteristics - 3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 3.3V**, **VDD2 = 3.3V**, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		100	Mbps	
Minimum Pulse Width	PW			8.3	ns	
Propagation Delay	t_{PLH}		12.85	19	ns	See Figure 6.9 , $C_L = 15pF$
	t_{PHL}		12.60	19	ns	See Figure 6.9 , $C_L = 15pF$
Pulse Width Distortion $ t_{PHL} - t_{PLH} $	PWD			5.0	ns	See Figure 6.9 , $C_L = 15pF$
Rising Time	t_r			5.0	ns	See Figure 6.9 , $C_L = 15pF$
Falling Time	t_f			5.0	ns	See Figure 6.9 , $C_L = 15pF$
Peak Eye Diagram Jitter	$t_{JIT(PK)}$		2.5		ns	
Channel-to-Channel Delay Skew	$t_{SK(c2c)}$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK(p2p)}$			5.0	ns	

Disable high to Tri-State	t_{PHZ}		11	30	ns	See Figure 6.10 , $C_L = 15\text{pF}$, $R_L=1\text{k}$
Enable to Data high Valid	t_{PZH}		11.5	30	ns	See Figure 6.10 , $C_L = 15\text{pF}$, $R_L=1\text{k}$
Disable low to Tri-State	t_{PLZ}		9.3	30	ns	See Figure 6.10 , $C_L = 15\text{pF}$, $R_L=1\text{k}$
Enable to Data low Valid	t_{PZL}		12.3	30	ns	See Figure 6.10 , $C_L = 15\text{pF}$, $R_L=1\text{k}$

6.7. Switching Characteristics - 2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 2.5V**, **VDD2 = 2.5V**, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		100	Mbps	
Minimum Pulse Width	PW			8.3	ns	
Propagation Delay	t_{PLH}		13.97	20	ns	See Figure 6.9 , $C_L = 15\text{pF}$
	t_{PHL}		12.72	20	ns	See Figure 6.9 , $C_L = 15\text{pF}$
Pulse Width Distortion $ t_{PHL} - t_{PLH} $	PWD			5.0	ns	See Figure 6.9 , $C_L = 15\text{pF}$
Rising Time	t_r			5.0	ns	See Figure 6.9 , $C_L = 15\text{pF}$
Falling Time	t_f			5.0	ns	See Figure 6.9 , $C_L = 15\text{pF}$
Peak Eye Diagram Jitter	$t_{JIT(PK)}$		2.5		ns	
Channel-to-Channel Delay Skew	$t_{SK(c2c)}$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK(p2p)}$			5.0	ns	
Disable high to Tri-State	t_{PHZ}		13.9	30	ns	See Figure 6.10 , $C_L = 15\text{pF}$, $R_L=1\text{k}$
Enable to Data high Valid	t_{PZH}		15.6	30	ns	See Figure 6.10 , $C_L = 15\text{pF}$, $R_L=1\text{k}$
Disable low to Tri-State	t_{PLZ}		12.6	30	ns	See Figure 6.10 , $C_L = 15\text{pF}$, $R_L=1\text{k}$
Enable to Data low Valid	t_{PZL}		16.8	30	ns	See Figure 6.10 , $C_L = 15\text{pF}$, $R_L=1\text{k}$

6.8. Typical Performance Characteristics

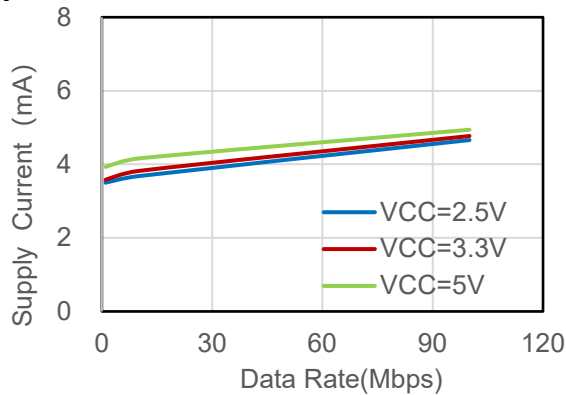


Figure 6.1 NSI83x0 VDD1 Supply Current vs Data Rate

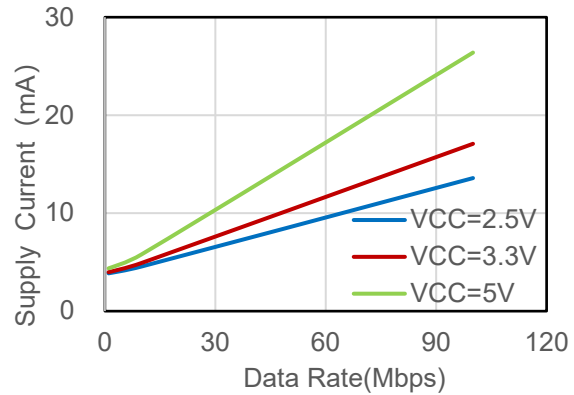


Figure 6.2 NSI83x0 VDD2 Supply Current vs Data Rate

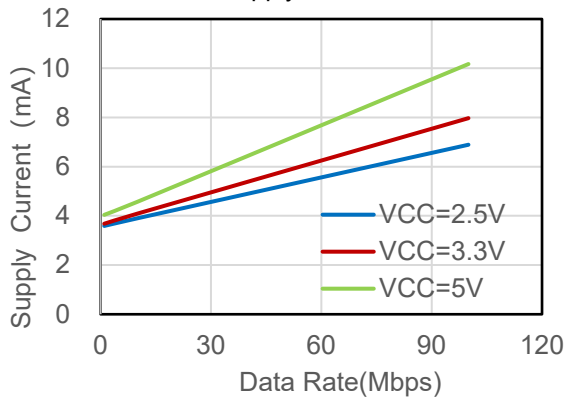


Figure 6.3 NSI83x1 VDD1 Supply Current vs Data Rate

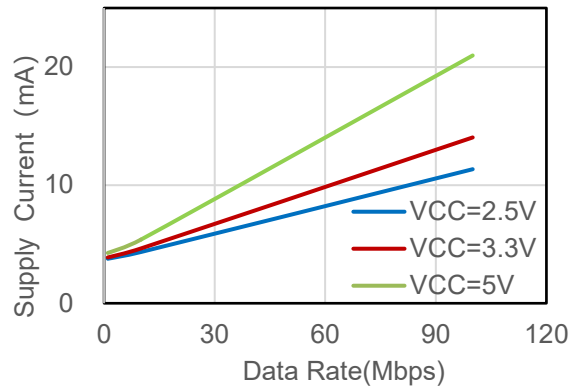


Figure 6.4 NSI83x1 VDD2 Supply Current vs Data Rate

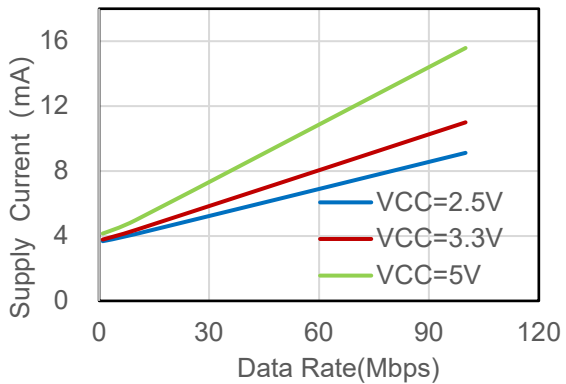


Figure 6.5 NSI83x2 VDD1 Supply Current vs Data Rate

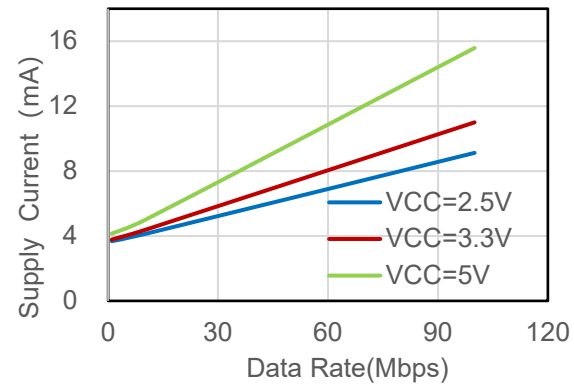


Figure 6.6 NSI83x2 VDD2 Supply Current vs Data Rate

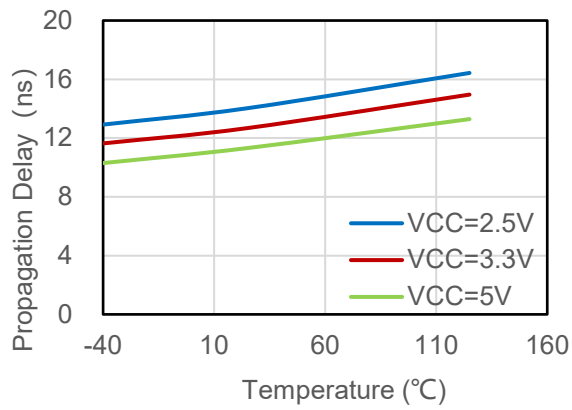


Figure 6.7 Rising Edge Propagation Delay Vs Temp

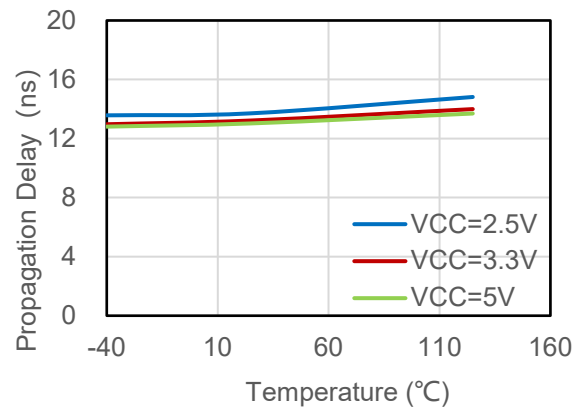
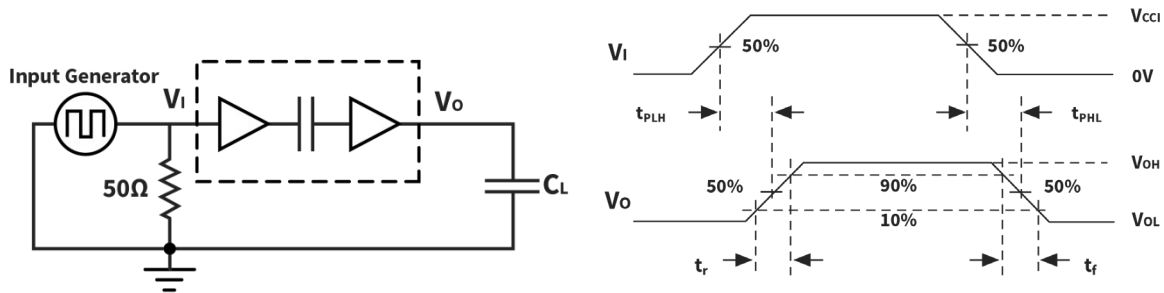


Figure 6.8 Falling Edge Propagation Delay Vs Temp

6.9. Parameter Measurement Information



(1) Input Generator Characteristics : PRR $\leq$ 50kHz, $t_r \leq 3$ ns, $t_f \leq 3$ ns, Duty cycle = 50%, $Z_o = 50 \Omega$.

Figure 6.9 Switching Characteristics Test Circuit and Waveform

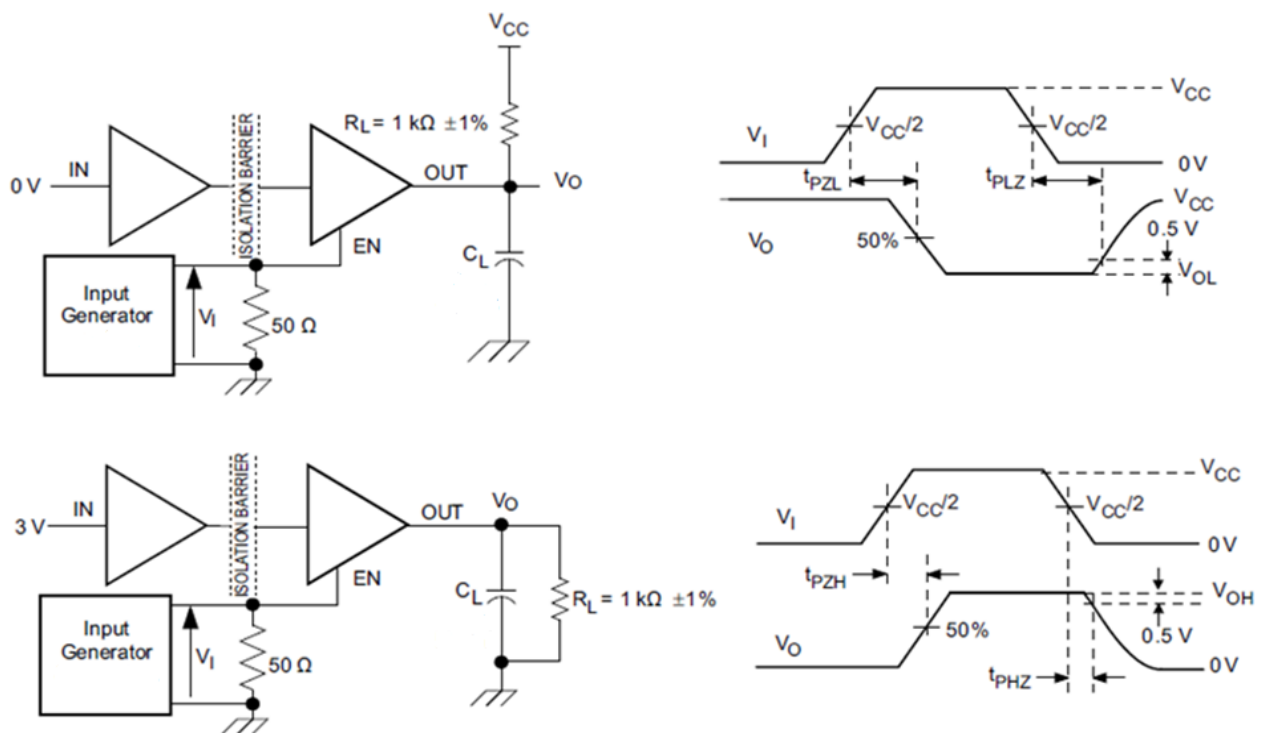


Figure 6.10 Enable/Disable Propagation Delay Time Test Circuit and Waveform

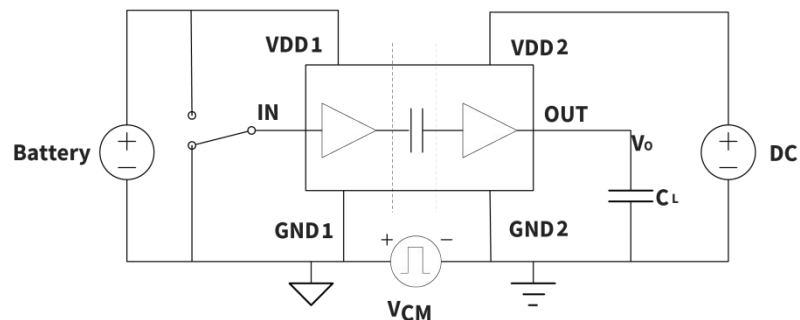


Figure 6.11 Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

<i>Parameters</i>	<i>Symbol</i>	<i>Value</i> SSOP16	<i>Unit</i>	<i>Comments</i>
Minimum External Clearance	CLR	4	mm	IEC 60664-1
Minimum External Creepage	CPG	4	mm	IEC 60664-1
Distance Through Insulation	DTI	24	µm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

<i>Description</i>	<i>Test Condition</i>	<i>Value</i> SSOP16
Overvoltage Category per IEC60664-1	For Rated Mains Voltage $\leq$ 150Vrms	I to IV
	For Rated Mains Voltage $\leq$ 300Vrms	I to III
	For Rated Mains Voltage $\leq$ 600Vrms	I to II
	For Rated Mains Voltage $\leq$ 1000Vrms	I
Climatic Classification		40/125/21
Pollution Degree per DIN VDE 0110		2

7.2. Insulation Characteristics

<i>Description</i>	<i>Test Condition</i>	<i>Symbol</i>	<i>Value</i> SSOP16	<i>Unit</i>
Maximum repetitive isolation voltage		V_{IORM}	565	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	400	V_{RMS}
	DC Voltage		565	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3,		\	pC

Description	Test Condition	Symbol	Value	
			SSOP16	Unit
	$V_{ini}=V_{IOTM}$, $t_{ini} = 60\text{ s}$, $V_{pd(m)}=1.2*V_{IORM}$, $t_m=10\text{s}$.	q_{pd}		
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, $t_{ini}=60\text{s}$, $V_{pd(m)}=1.6*V_{IORM}$, $t_m=10\text{s}$			pC
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}$, $t_{ini}=1\text{s}$ $V_{pd(m)}=1.875*V_{IORM}$, $t_m=1\text{s}$ (method b1) or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$ (method b2)			pC
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, $t_{ini} = 60\text{ s}$, $V_{pd(m)}=1.2*V_{IORM}$, $t_m=10\text{s}$.	q_{pd}	<5	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, $t_{ini}=60\text{s}$, $V_{pd(m)}=1.3*V_{IORM}$, $t_m=10\text{s}$			pC
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}$, $t_{ini}=1\text{s}$ $V_{pd(m)}=1.5*V_{IORM}$, $t_m=1\text{s}$ (method b1) or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$ (method b2)			pC
Maximum transient isolation voltage	$t = 60\text{ sec}$	V_{IOTM}	5000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50-us waveform per IEC62368-1	V_{IMP}	5384	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$	V_{IOSM}	10000	V_{PEAK}
Isolation resistance	$V_{IO} = 500\text{V}$, $T_{amb}=25^\circ\text{C}$	R_{IO}	$>10^{12}$	Ω

Description	Test Condition	Symbol	Value	
			SSOP16	Unit
	$V_{IO} = 500V, 100^{\circ}C \leq T_{amb} \leq 125^{\circ}C$	R_{IO}	$>10^{11}$	Ω
	$V_{IO} = 500V, T_{amb} = T_s$	R_{IO}	$>10^9$	Ω
Isolation capacitance	$f = 1MHz$	C_{IO}	0.8	pF
UL1577				
Insulation voltage per UL	$V_{TEST} = V_{ISO}, t = 60 s$ (qualification), $V_{TEST} = 1.2 \times V_{ISO}, t = 1s$ (100% production test)	V_{ISO}	3000	V_{RMS}

7.3. Safety-Limiting Values

Basic isolation safety-limiting values as outlined in VDE-0884-17 of NSI834xSx-Q1SSR (SSOP16)

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{\theta JA} = 140^{\circ}C/W^{1)}$, $T_J = 150^{\circ}C$, $T_A = 25^{\circ}C$	880	mW
Safety Supply Current	$R_{\theta JA} = 140^{\circ}C/W^{1)}$, $V_I = 5V$, $T_J = 150^{\circ}C$, $T_A = 25^{\circ}C$	176	mA
Safety Temperature ²⁾		150	$^{\circ}C$

- 1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SSOP16 package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

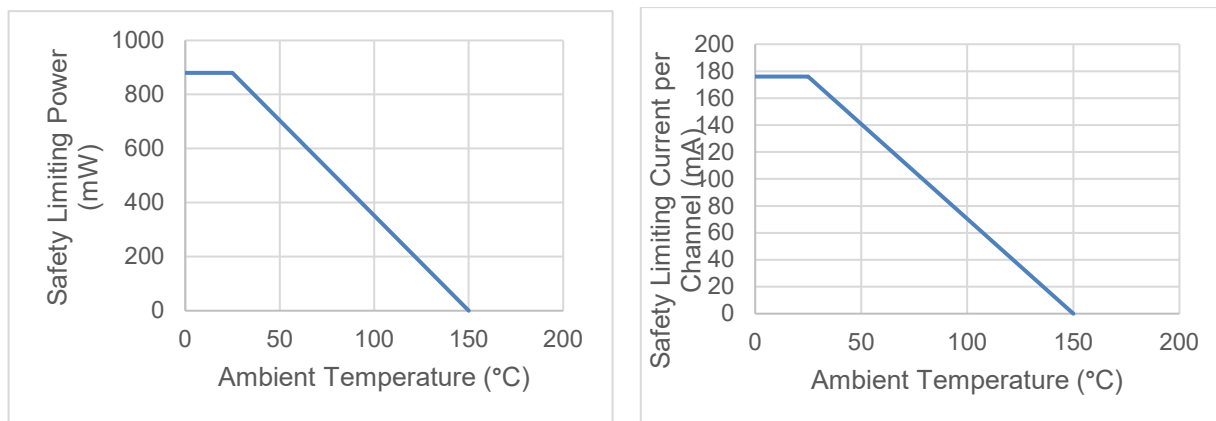


Figure 7.1 NSI834xSx Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17).

7.4. Regulatory Information

The NSI834xSx-Q1SSR are approved by the organizations listed in table.

<i>UL</i>		<i>CQC</i>	<i>TUV</i>	
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to GB4943.1	DIN EN IEC 60747-17 (VDE 0884-17)	Certified According to EN IEC 62368-1
Single Protection, 3000Vrms Isolation voltage	Single Protection, 3000Vrms Isolation voltage	Basic Insulation	Basic insulation VIORM=565Vpeak VIOTM=5000Vpeak VIO SM=10000Vpeak	3000Vrms for 1min
E500602	E500602	CQC20001264940	Pending	R 50574061

8. Function Description

8.1. Overview

The NSI834x is a quad-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the receiver side.

The NSI834x devices are high reliability quad-channel digital isolators. The NSI834x device is safety certified by UL1577 and supports 3kV_{rms} insulation withstand voltage, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI834x is up to 100Mbps, and the common-mode transient immunity (CMTI) is up to 200kV/μs. The NSI834x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI834x device supports connection to most digital interfaces directly, making level shifting easy. High system level EMC performance enhances reliability and stability of use.

The NSI834x has a default output status when VDD_{IN} is unready and VDD_{OUT} is ready as shown in Table 7.1, which helps with diagnosis when power is missing at the transmitter side. The output B follows the same status as the input A after powering up.

Table 7.1 Output status vs. power status

Input ¹	EN _x ²	VDD _{IN} status	VDD _{OUT} status	Output	Comment
H	H or NC	Ready	Ready	H	Normal operation.
L	H or NC	Ready	Ready	L	
X	L	Ready	Ready	Z	Output Disabled, the output is high impedance (Internal pull up to VDD _{OUT} with NSI834xx1 or internal pull down to GND with NSI834xx0)
X	H or NC	Unready	Ready	L(NSI834xx0) H(NSI834xx1)	The output follows the same status with the input after input side VDD _{IN} is powered on.
X	L	Unready	Ready	Z	Output Disabled, the output is high impedance (Internal pull up to VDD _{OUT} with NSI834xx1 or internal pull down to GND with NSI834xx0)
X	X	Ready	Unready	Undetermined	The output follows the same status with the input after output side VDD _{OUT} is powered on.
Note: H=Logic high; L=Logic low; X=Logic low or logic high VDD_{IN} is input side power; VDD_{OUT} is output side power. (1) There is a protection diode between the input and the VDD_{IN}. When the VDD_{IN} is floating, the strong drive signal through the input pin will put the VDD_{IN} in an indeterminate state. (2) The EN_x is output side enable.					

8.2. OOK Modulation

NSI834x is based on a capacitive isolation barrier technique and the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, as shown in Figure 8.1 to Figure 8.2, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI.

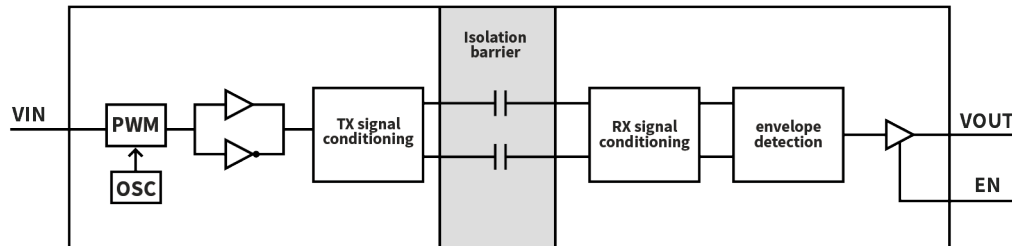


Figure 8.1 Single Channel Function Block Diagram

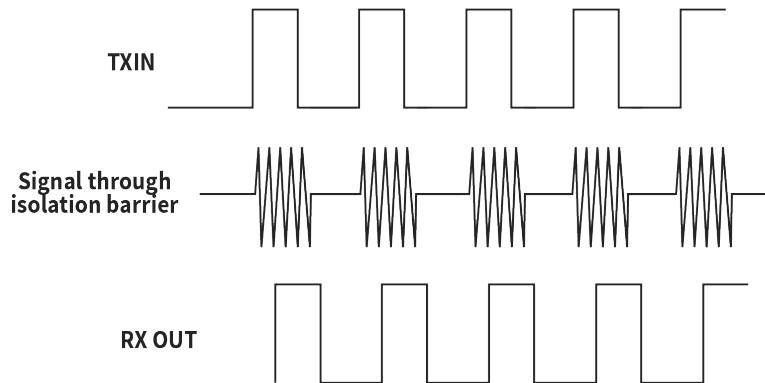


Figure 8.2 OOK Modulation

9. Application Note

9.1. Typical Application Circuit

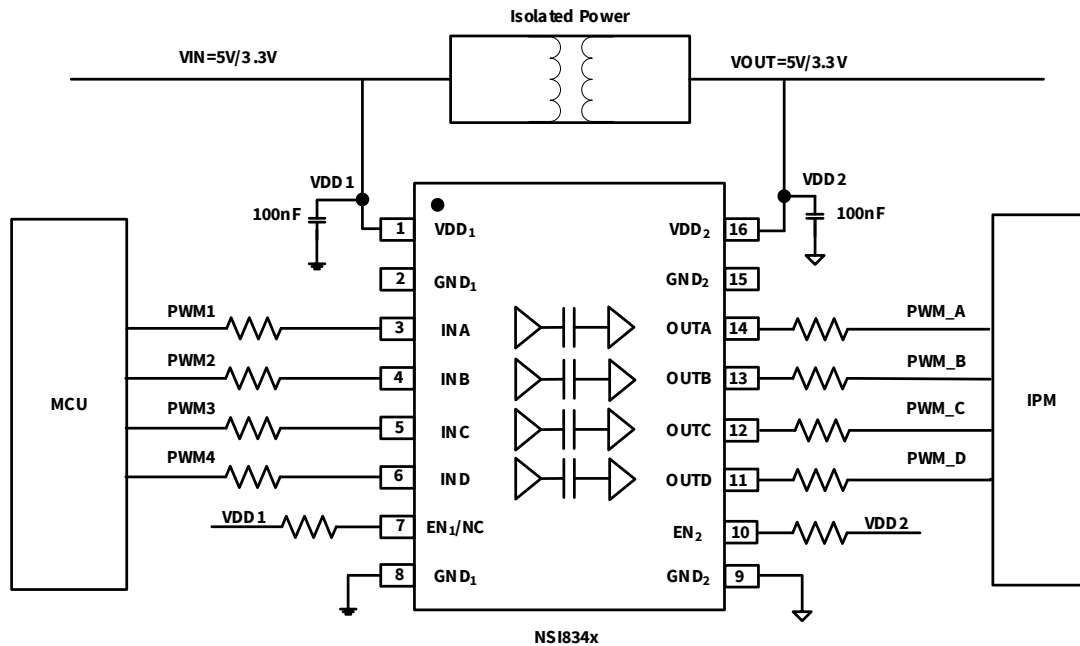


Figure 9.1 Typical PWM isolation circuit for IPM

9.2. PCB Layout

The NSI834x requires a 0.1 μF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. It is recommended to make sure the space under the chip should be kept free from planes, traces, pads and vias. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω , $\pm 40\%$. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

9.3. High Speed Performance

Figure 9.2 shows the eye diagram of NSI834x at 50Mbps data rate output. The result shows a typical measurement on NSI834x with low jitter and wide open eye characteristics.

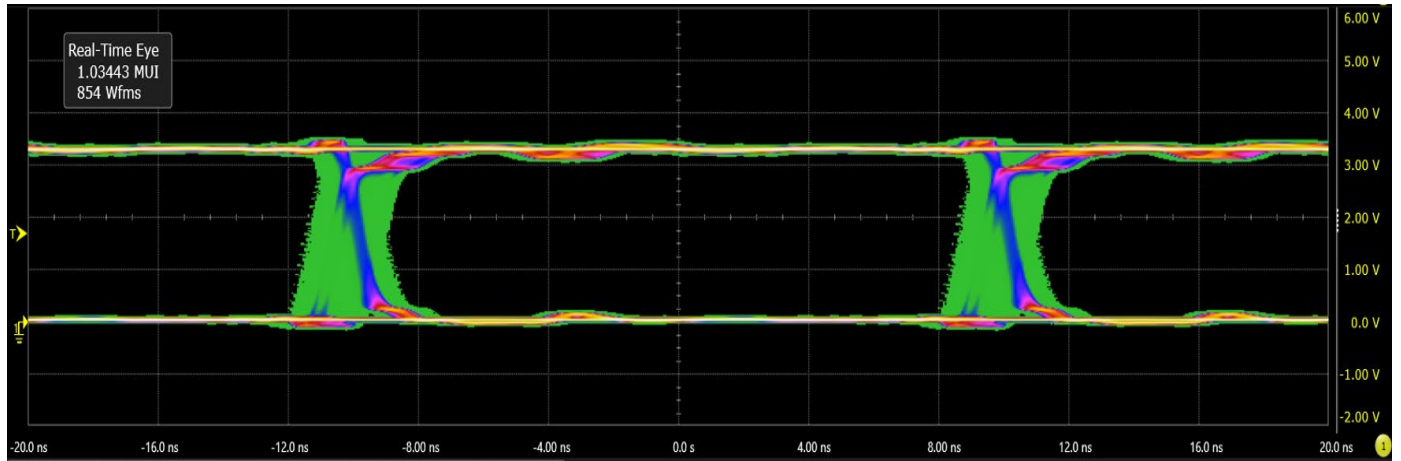


Figure 9.2 Eye Diagram at 50Mbps PRBS 2¹⁶-1, 2.5V and 25°C

9.4. Typical Supply Current Equations

The typical supply current of NSI834x can be calculated using below equations. IDD1 and IDD2 are typical supply currents measured in mA, f is data rate measured in Mbps, CL is the capacitive load measured in pF.

NSI8340:

$$IDD1 = 0.298 \cdot a1 + 1.458 \cdot b1 + 0.878 \cdot c1.$$

$$IDD2 = 3.93 + 0.5 \cdot VDD2 \cdot f \cdot CL \cdot c1 \cdot 10^{-3}$$

When a1 is the channel number of default state input at side 1, b1 is the channel number of non-default state input at side 1, c1 is the channel number of switch signal input at side 1.

NSI8341:

$$IDD1 = 1.875 + 1.16 \cdot b1 + 0.58 \cdot c1 + 0.5 \cdot VDD1 \cdot f \cdot CL \cdot c2 \cdot 10^{-3}$$

$$IDD2 = 3.245 + 1.16 \cdot b2 + 0.58 \cdot c2 + 0.5 \cdot VDD2 \cdot f \cdot CL \cdot c1 \cdot 10^{-3}$$

When b1 is the channel number of non-default state input at side 1, c1 is the channel number of switch signal input at side 1, b2 is the channel number of non-default state input at side 2, c2 is the channel number of switch signal input at side 2.

NSI8342:

$$IDD1 = 2.56 + 1.16 \cdot b1 + 0.58 \cdot c1 + 0.5 \cdot VDD1 \cdot f \cdot CL \cdot c2 \cdot 10^{-3}$$

$$IDD2 = 2.56 + 1.16 \cdot b2 + 0.58 \cdot c2 + 0.5 \cdot VDD2 \cdot f \cdot CL \cdot c1 \cdot 10^{-3}$$

When b1 is the channel number of non-default state input at side 1, c1 is the channel number of switch signal input at side 1, b2 is the channel number of non-default state input at side 2, c2 is the channel number of switch signal input at side 2.

10. Package Information

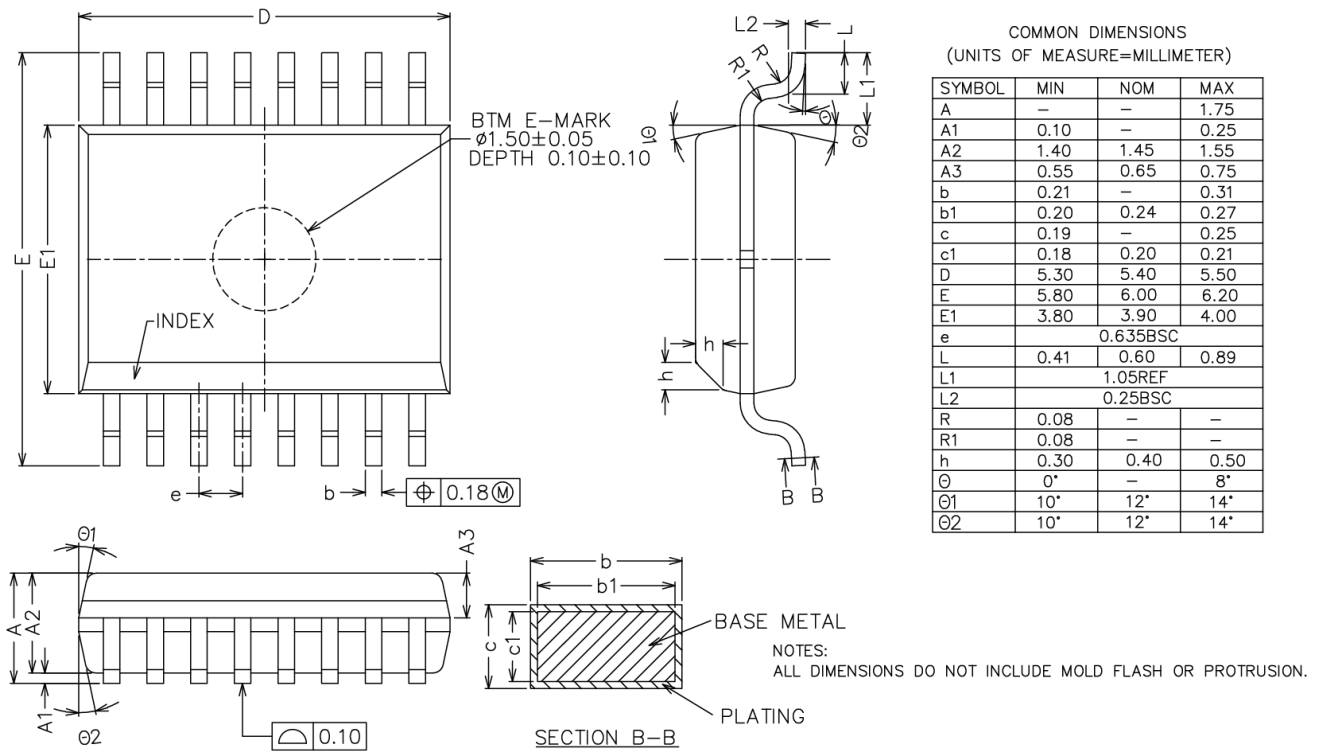


Figure 10.1 SSOP16 Package Shape and Dimension in millimeters

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

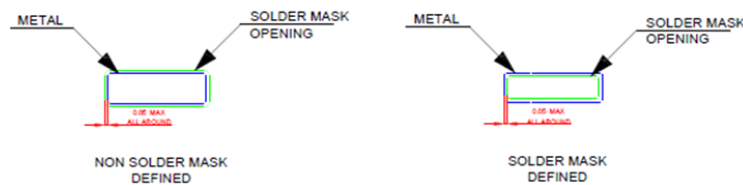
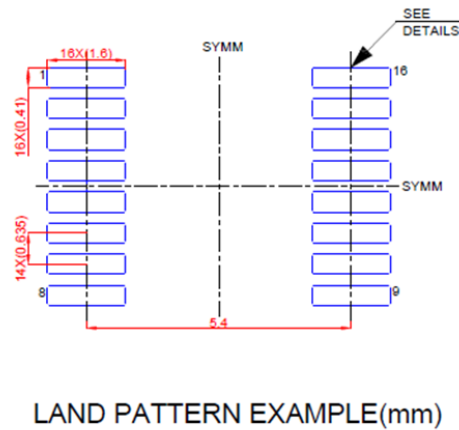


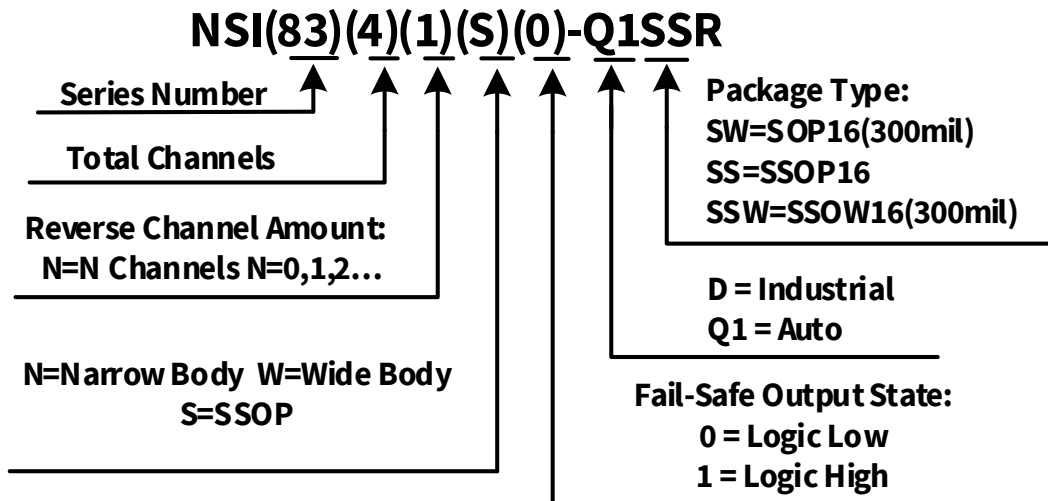
Figure 10.2 SSOP16 Package Board Layout Example

11. Order Information

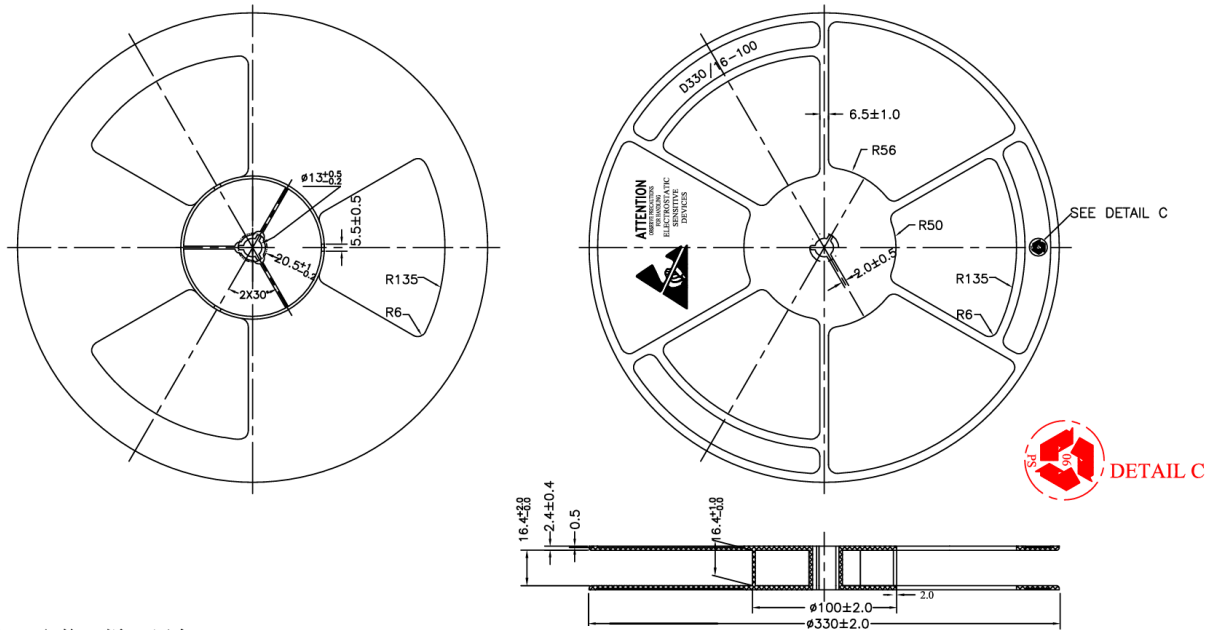
Part Number	Isolation Rating (kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	M S L	Package Type	Package Drawing	SPQ	MPQ	Marking
NSI8340S0-Q1SSR	3	4	0	100	Low	-40 to 125°C	3	SSOP16	SSOP16	2500	2500	NSi83 40S0Q
NSI8340S1-Q1SSR	3	4	0	100	High	-40 to 125°C	3	SSOP16	SSOP16	2500	2500	NSi83 40S1Q
NSI8341S0-Q1SSR	3	3	1	100	Low	-40 to 125°C	3	SSOP16	SSOP16	2500	2500	NSi83 41S0Q
NSI8341S1-Q1SSR	3	3	1	100	High	-40 to 125°C	3	SSOP16	SSOP16	2500	2500	NSi83 41S1Q
NSI8342S0-Q1SSR	3	2	2	100	Low	-40 to 125°C	3	SSOP16	SSOP16	2500	2500	NSi83 42S0Q
NSI8342S1-Q1SSR	3	2	2	100	High	-40 to 125°C	3	SSOP16	SSOP16	2500	2500	NSi83 42S1Q

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.

Part Number Rule:



12. Tape and Reel Information



注意：

1. 材料：聚苯乙烯（黑色）；
2. 平整度：最大允许3 毫米；
3. 所有尺寸为毫米；
4. 表面电阻： 10^5 TO 10^{11} OHMS/SQ.
5. 所有未注公差： ± 0.25 。

Figure 13.1 Reel Information of SSOP16

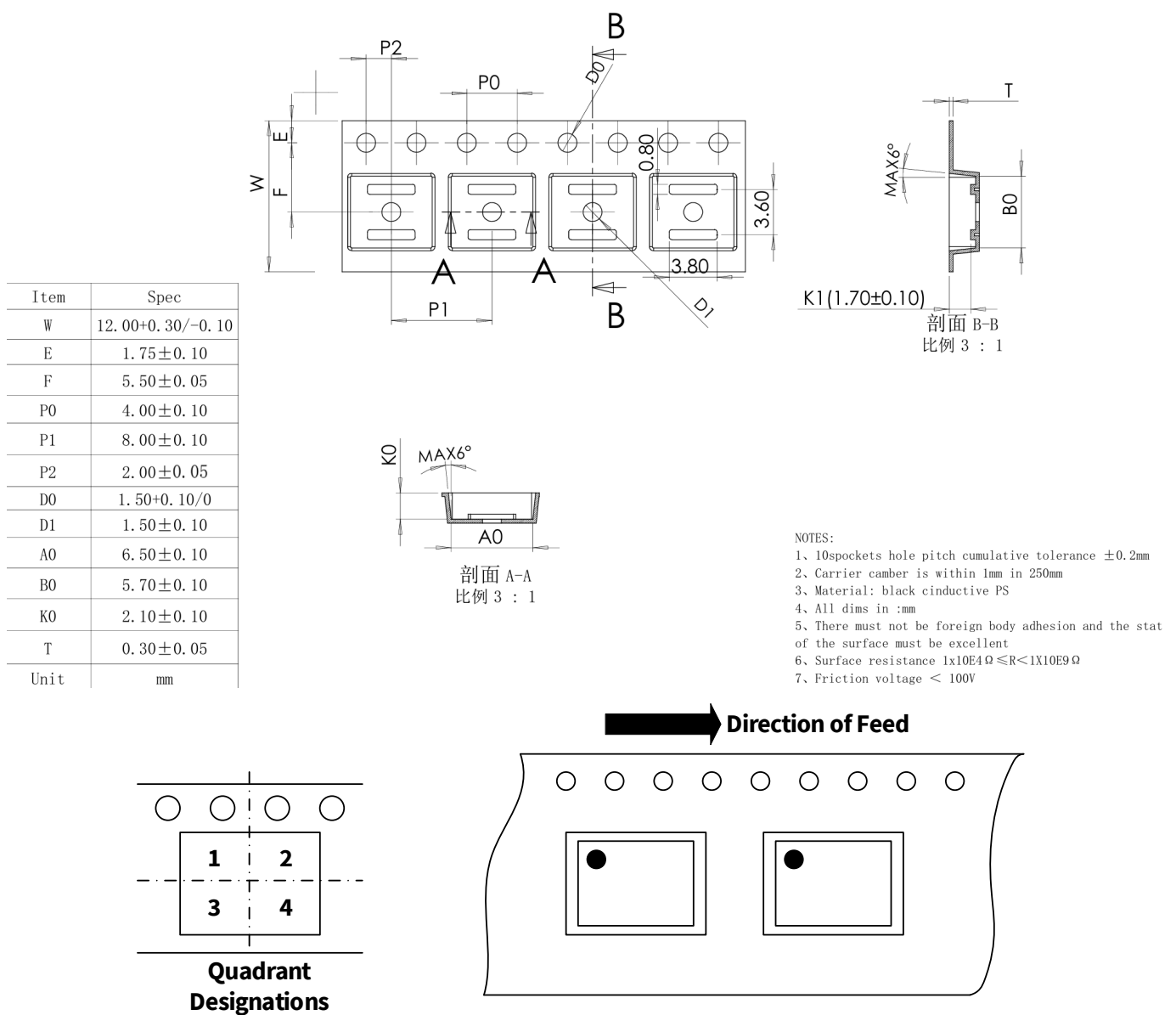


Figure 13.2 Tape Information of SSOP16

13. Revision History

Revision	Description	Date
1.0	Initial version	2026/6/30
1.1	Update the function diagram Remove 3CH information Update tape Information P2	2026/8/21

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