

## Product Overview

The NSI833x devices are high reliability triple-channel digital isolators. The NSI833x device is safety certified by UL1577 support 5kV<sub>rms</sub> insulation withstand voltage, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI833x is up to 100Mbps, and the common-mode transient immunity (CMTI) is up to 200kV/μs. The NSI833x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI833x device supports to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use. AEC-Q100 (Grade 1) option is provided for all devices.

## Key Features

- Up to 5000V<sub>rms</sub> Insulation voltage
- Data rate: DC to 100Mbps
- Power supply voltage: 2.5V to 5.5V
- High CMTI: 200kV/μs
- Chip level ESD: HBM: ±8kV
- Robust Electromagnetic Compatibility (EMC)
  - System-Level ESD, EFT, and Surge Immunity
  - Low Emissions
- Default output high level or low-level option
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <18ns
- Operation temperature: -40°C~125°C
- RoHS-compliant packages:
  - SOP16(300mil)

## Safety Regulatory Approvals

- UL recognition: up to 5000V<sub>rms</sub> for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

## Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor control

## Device Information

Part Number	Package	Body Size
NSI833xWx-Q1SWR	SOP16(300mil)	10.30mm × 7.50mm

## Functional Block Diagrams

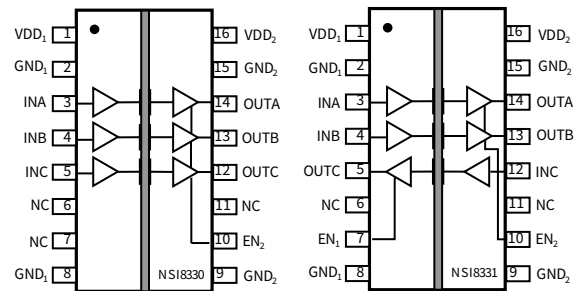


Figure 1. NSI833x Block Diagram

## INDEX

1. PIN CONFIGURATION AND FUNCTIONS .....	3
2. ABSOLUTE MAXIMUM RATINGS .....	4
3. ESD RATINGS .....	4
4. RECOMMENDED OPERATING CONDITIONS.....	5
5. THERMAL INFORMATION .....	5
6. SPECIFICATIONS .....	5
6.1. ELECTRICAL CHARACTERISTICS .....	5
6.2. SUPPLY CURRENT CHARACTERISTICS – 5V SUPPLY .....	6
6.3. SUPPLY CURRENT CHARACTERISTICS –3.3V SUPPLY .....	7
6.4. SUPPLY CURRENT CHARACTERISTICS–2.5V SUPPLY .....	8
6.5. SWITCHING CHARACTERISTICS - 5V SUPPLY .....	9
6.6. SWITCHING CHARACTERISTICS - 3.3V SUPPLY .....	9
6.7. SWITCHING CHARACTERISTICS - 2.5V SUPPLY .....	10
6.8. TYPICAL PERFORMANCE CHARACTERISTICS .....	11
6.9. PARAMETER MEASUREMENT INFORMATION .....	12
7. HIGH VOLTAGE FEATURE DESCRIPTION .....	13
7.1. INSULATION AND SAFETY RELATED SPECIFICATIONS.....	13
7.2. INSULATION CHARACTERISTICS .....	13
7.3. SAFETY-LIMITING VALUES.....	15
7.4. REGULATORY INFORMATION.....	16
8. FUNCTION DESCRIPTION .....	17
8.1. OVERVIEW .....	17
8.2. OOK MODULATION .....	18
9. APPLICATION NOTE.....	19
9.1. TYPICAL APPLICATION CIRCUIT.....	19
9.2. PCB LAYOUT.....	19
9.3. HIGH SPEED PERFORMANCE .....	20
9.4. TYPICAL SUPPLY CURRENT EQUATIONS .....	20
10. PACKAGE INFORMATION .....	21
11. ORDER INFORMATION .....	22
12. DOCUMENTATION SUPPORT .....	23
13. TAPE AND REEL INFORMATION .....	24
14. REVISION HISTORY .....	26

# 1. Pin Configuration and Functions

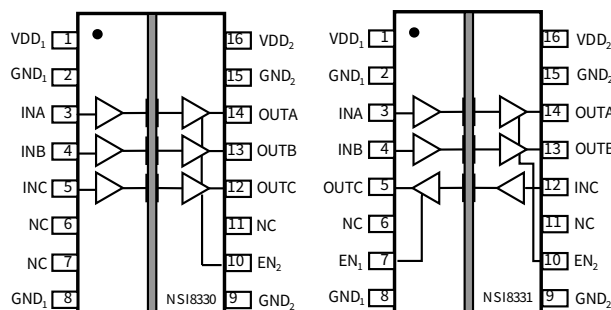


Figure 1.1 NSI8330 Package Figure 1.2 NSI8331 Package

Table 1.1 NSI833x Pin Configuration and Description

NSI8330 PIN NO.	NSI8331 PIN NO.	SYMBOL	FUNCTION
1	1	VDD <sub>1</sub>	Power Supply for Isolator Side 1
2	2	GND <sub>1</sub>	Ground 1, the ground reference for Isolator Side 1
3	3	INA	Logic Input A
4	4	INB	Logic Input B
5	12	INC	Logic Input C
6	6	NC	No Connection.
7	7	NC /EN <sub>1</sub>	No Connection. Or Output Enable 1. Active high logic input. When EN <sub>1</sub> is high or NC, the output of Side 1 is enabled. When EN <sub>1</sub> is low, the output of Side 1 is disabled to high impedance state.
8	8	GND <sub>1</sub>	Ground 1, the ground reference for Isolator Side 1
9	9	GND <sub>2</sub>	Ground 2, the ground reference for Isolator Side 2
10	10	EN <sub>2</sub>	Output Enable 2. Active high logic input. When EN <sub>2</sub> is high or NC, the output of Side 2 is enabled. When EN <sub>2</sub> is low, the output of Side 2 is disabled to high impedance state.
11	11	NC	No Connection.
12	5	OUTC	Logic Output C
13	13	OUTB	Logic Output B
14	14	OUTA	Logic Output A
15	15	GND <sub>2</sub>	Ground 2, the ground reference for Isolator Side 2
16	16	VDD <sub>2</sub>	Power Supply for Isolator Side 2

## 2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	VINA, VINB, VINC	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Output Voltage	VOUTA, VOUTB, VOUTC	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Input/Output Pulse Voltage	VINA, VINB, VINC, VOUTA, VOUTB, VOUTC	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Output current	I <sub>o</sub>	-15		15	mA	
Operating Temperature	T <sub>opr</sub>	-40		125	°C	
Junction Temperature	T <sub>j</sub>			150	°C	
Storage Temperature	T <sub>stg</sub>	-65		150	°C	

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating conditions. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.
- (2) Power supply voltage and input/output voltage are respect to the local ground terminal (GND1 or GND2) voltage values.

## 3. ESD Ratings

Parameters	Ratings	Value	Unit
Electrostatic discharge (ESD)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(2)</sup>	±8000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(3)</sup>	±2000	V

- (1) Though this device features proprietary protection circuitry, proper ESD precautions should be considered to avoid performance degradation of damage due to high energy ESD event. Charged devices and circuit boards may discharge without detection.
- (2) Safe manufacturing requires 500-V HBM and standard ESD precautions, per JEDEC document JEP155.
- (3) Safe manufacturing requires 250-V CDM and standard ESD precautions, per JEDEC document JEP157.

## 4. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit
Power Supply Voltage	VDD1, VDD2	2.5		5.5	V
Operating Temperature	Topr	-40		125	°C
High Level Input Voltage	VIH	2			V
Low Level Input Voltage	VIL			0.8	V
Data rate	DR			100	Mbps

## 5. Thermal Information

Parameters	Symbol	SOP16(300mil)	Unit
IC Junction-to-Air Thermal Resistance	R <sub>θJA</sub>	78.9	°C/W
Junction-to-case (top) thermal resistance	R <sub>θJC (top)</sub>	41.6	°C/W
Junction-to-board thermal resistance	R <sub>θJB</sub>	43.6	°C/W
Junction-to-top characterization parameter	Ψ <sub>JT</sub>	7.0	°C/W
Junction-to-board characterization parameter	Ψ <sub>JB</sub>	23.0	°C/W

## 6. Specifications

### 6.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power on Reset	VDD <sub>POR</sub>	2	2.2	2.4	V	POR threshold as during power-up
	VDD <sub>HYS</sub>		0.1		V	POR threshold Hysteresis
Rising input switching threshold	V <sub>IT+</sub>		1.5	2	V	
Falling input switching threshold	V <sub>IT-</sub>	0.8	1.15		V	
Input threshold voltage hysteresis	V <sub>I(HYS)</sub>		0.35		V	

High Level Output Voltage	V <sub>OH</sub>	VDD-0.4			V	I <sub>OH</sub> = -4mA
Low Level Output Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 4mA
Output Impedance	R <sub>out</sub>		50		ohm	
Input Pull high or low Current	I <sub>pull</sub>		5	10	μA	
Start Up Time after POR	tr <sub>bs</sub>		22	32	μs	
Common Mode Transient Immunity	CMTI	±150	±200		kV/μs	See <a href="#">Figure 6.9</a> , C <sub>L</sub> = 15pF

### 6.2. Supply Current Characteristics – 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V, Ta = 25°C**)

Parameters	Symbol	Min	Typ.	Max	Unit	Comments
Supply current	<b>NSI8330</b>					
	I <sub>DD1</sub> (Q0)		1.40	1.78	mA	All Input 0V for NSI8330x0 Or All Input at supply for NSI8330x1
	I <sub>DD2</sub> (Q0)		4.14	5.03	mA	
	I <sub>DD1</sub> (Q1)		4.94	5.99	mA	All Input at supply for NSI8330x0 Or All Input 0V for NSI8330x1
	I <sub>DD2</sub> (Q1)		4.15	5.06	mA	
	I <sub>DD1</sub> (1M)		3.24	3.94	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		4.20	5.17	mA	
	I <sub>DD1</sub> (10M)		3.41	4.31	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		5.28	6.45	mA	
	I <sub>DD1</sub> (100M)		3.87	4.87	mA	All Input with 100Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (100M)		20.72	25.95	mA	
	<b>NSI8331</b>					
	I <sub>DD1</sub> (Q0)		2.74	3.35	mA	All Input 0V for NSI8331x0 Or All Input at supply for NSI8331x1
	I <sub>DD2</sub> (Q0)		2.80	3.39	mA	
I <sub>DD1</sub> (Q1)		5.10	6.21	mA	All Input at supply for NSI8331x0 Or All Input 0V for NSI8331x1	
I <sub>DD2</sub> (Q1)		3.99	4.84	mA		
I <sub>DD1</sub> (1M)		3.98	4.88	mA	All Input with 1Mbps, C <sub>L</sub> =15pF	
I <sub>DD2</sub> (1M)		3.46	4.23	mA		

	I <sub>DD1</sub> (10M)		4.46	5.55	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		4.23	5.21	mA	
	I <sub>DD1</sub> (100M)		9.91	12.43	mA	All Input with 100Mbps, C <sub>L</sub> = 15pF
	I <sub>DD2</sub> (100M)		14.68	18.39	mA	

### 6.3. Supply Current Characteristics –3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25°C)

Parameters	Symbol	Min	Typ.	Max	Unit	Comments
Supply current	<b>NSI8330</b>					
	I <sub>DD1</sub> (Q0)		1.18	1.68	mA	All Input 0V for NSI8330x0 Or All Input at supply for NSI8330x1
	I <sub>DD2</sub> (Q0)		3.87	4.95	mA	
	I <sub>DD1</sub> (Q1)		4.67	5.88	mA	All Input at supply for NSI8330x0 Or All Input 0V for NSI8330x1
	I <sub>DD2</sub> (Q1)		3.94	4.98	mA	
	I <sub>DD1</sub> (1M)		2.98	3.86	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		3.91	5.04	mA	
	I <sub>DD1</sub> (10M)		3.15	4.22	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		4.61	5.90	mA	
	I <sub>DD1</sub> (100M)		3.99	4.85	mA	All Input with 100Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (100M)		13.73	16.58	mA	
	<b>NSI8331</b>					
	I <sub>DD1</sub> (Q0)		2.56	3.29	mA	All Input 0V for NSI8331x0 Or All Input at supply for NSI8331x1
	I <sub>DD2</sub> (Q0)		2.56	3.33	mA	
	I <sub>DD1</sub> (Q1)		4.83	6.11	mA	All Input at supply for NSI8331x0 Or All Input 0V for NSI8331x1
	I <sub>DD2</sub> (Q1)		3.72	4.75	mA	
	I <sub>DD1</sub> (1M)		3.71	4.78	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		3.18	4.12	mA	
	I <sub>DD1</sub> (10M)		4.06	5.31	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		3.70	4.81	mA	
I <sub>DD1</sub> (100M)		7.66	9.29	mA	All Input with 100Mbps, C <sub>L</sub> = 15pF	
I <sub>DD2</sub> (100M)		10.06	12.14	mA		

**6.4. Supply Current Characteristics–2.5V Supply**

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25°C)

Parameters	Symbol	Min	Typ.	Max	Unit	Comments
Supply current	<b>NSI8330</b>					
	I <sub>DD1</sub> (Q0)		1.17	1.64	mA	All Input 0V for NSI8330x0 Or All Input at supply for NSI8330x1
	I <sub>DD2</sub> (Q0)		3.71	4.82	mA	
	I <sub>DD1</sub> (Q1)		4.60	5.56	mA	All Input at supply for NSI8330x0 Or All Input 0V for NSI8330x1
	I <sub>DD2</sub> (Q1)		3.82	4.98	mA	
	I <sub>DD1</sub> (1M)		2.92	3.57	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		3.82	5.05	mA	
	I <sub>DD1</sub> (10M)		3.05	4.07	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		4.35	5.57	mA	
	I <sub>DD1</sub> (100M)		3.79	4.63	mA	All Input with 100Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (100M)		11.11	13.42	mA	
	<b>NSI8331</b>					
	I <sub>DD1</sub> (Q0)		2.44	3.23	mA	All Input 0V for NSI8331x0 Or All Input at supply for NSI8331x1
	I <sub>DD2</sub> (Q0)		2.44	3.23	mA	
	I <sub>DD1</sub> (Q1)		4.76	5.90	mA	All Input at supply for NSI8331x0 Or All Input 0V for NSI8331x1
	I <sub>DD2</sub> (Q1)		3.66	4.64	mA	
	I <sub>DD1</sub> (1M)		3.64	4.59	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		3.10	4.03	mA	
	I <sub>DD1</sub> (10M)		3.91	5.10	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		3.49	4.54	mA	
I <sub>DD1</sub> (100M)		6.65	8.09	mA	All Input with 100Mbps, C <sub>L</sub> = 15pF	
I <sub>DD2</sub> (100M)		8.25	9.96	mA		

## 6.5. Switching Characteristics - 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		100	Mbps	
Minimum Pulse Width	PW			8.3	ns	
Propagation Delay	t <sub>PLH</sub>		12.0	18	ns	See <a href="#">Figure 6.7</a> , C <sub>L</sub> = 15pF
	t <sub>PHL</sub>		12.5	18	ns	See <a href="#">Figure 6.7</a> , C <sub>L</sub> = 15pF
Pulse Width Distortion  t <sub>PHL</sub> - t <sub>PLH</sub>	PWD			5.0	ns	See <a href="#">Figure 6.7</a> , C <sub>L</sub> = 15pF
Rising Time	t <sub>r</sub>			5.0	ns	See <a href="#">Figure 6.7</a> , C <sub>L</sub> = 15pF
Falling Time	t <sub>f</sub>			5.0	ns	See <a href="#">Figure 6.7</a> , C <sub>L</sub> = 15pF
Peak Eye Diagram Jitter	t <sub>JIT(PK)</sub>		2.5		ns	
Channel-to-Channel Delay Skew	t <sub>SK(c2c)</sub>			2.5	ns	
Part-to-Part Delay Skew	t <sub>SK(p2p)</sub>			5.0	ns	
Disable high to Tri-State	t <sub>PHZ</sub>		8.67	30	ns	See <a href="#">Figure 6.8</a> , C <sub>L</sub> = 15pF, R <sub>L</sub> =1k
Enable to Data high Valid	t <sub>PZH</sub>		8.75	30	ns	See <a href="#">Figure 6.8</a> , C <sub>L</sub> = 15pF, R <sub>L</sub> =1k
Disable low to Tri-State	t <sub>PLZ</sub>		7.7	30	ns	See <a href="#">Figure 6.8</a> , C <sub>L</sub> = 15pF, R <sub>L</sub> =1k
Enable to Data low Valid	t <sub>PZL</sub>		9.5	30	ns	See <a href="#">Figure 6.8</a> , C <sub>L</sub> = 15pF, R <sub>L</sub> =1k

## 6.6. Switching Characteristics - 3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		100	Mbps	
Minimum Pulse Width	PW			8.3	ns	
Propagation Delay	t <sub>PLH</sub>		12.85	19	ns	See <a href="#">Figure 6.7</a> , C <sub>L</sub> = 15pF
	t <sub>PHL</sub>		12.60	19	ns	See <a href="#">Figure 6.7</a> , C <sub>L</sub> = 15pF
Pulse Width Distortion  t <sub>PHL</sub> - t <sub>PLH</sub>	PWD			5.0	ns	See <a href="#">Figure 6.7</a> , C <sub>L</sub> = 15pF
Rising Time	t <sub>r</sub>			5.0	ns	See <a href="#">Figure 6.7</a> , C <sub>L</sub> = 15pF

Falling Time	$t_f$			5.0	ns	See <a href="#">Figure 6.7</a> , $C_L = 15\text{pF}$
Peak Eye Diagram Jitter	$t_{JIT(PK)}$		2.5		ns	
Channel-to-Channel Delay Skew	$t_{SK(c2c)}$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK(p2p)}$			5.0	ns	
Disable high to Tri-State	$t_{PHZ}$		11	30	ns	See <a href="#">Figure 6.8</a> , $C_L = 15\text{pF}$ , $R_L=1\text{k}$
Enable to Data high Valid	$t_{PZH}$		11.5	30	ns	See <a href="#">Figure 6.8</a> , $C_L = 15\text{pF}$ , $R_L=1\text{k}$
Disable low to Tri-State	$t_{PLZ}$		9.3	30	ns	See <a href="#">Figure 6.8</a> , $C_L = 15\text{pF}$ , $R_L=1\text{k}$
Enable to Data low Valid	$t_{PZL}$		12.3	30	ns	See <a href="#">Figure 6.8</a> , $C_L = 15\text{pF}$ , $R_L=1\text{k}$

### 6.7. Switching Characteristics - 2.5V Supply

( $V_{DD1}=2.5\text{V}\pm 10\%$ ,  $V_{DD2}=2.5\text{V}\pm 10\%$ ,  $T_a=-40^\circ\text{C}$  to  $125^\circ\text{C}$ . Unless otherwise noted, Typical values are at **VDD1 = 2.5V**, **VDD2 = 2.5V**,  $T_a = 25^\circ\text{C}$ )

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		100	Mbps	
Minimum Pulse Width	PW			8.3	ns	
Propagation Delay	$t_{PLH}$		13.97	20	ns	See <a href="#">Figure 6.7</a> , $C_L = 15\text{pF}$
	$t_{PHL}$		12.72	20	ns	See <a href="#">Figure 6.7</a> , $C_L = 15\text{pF}$
Pulse Width Distortion $ t_{PHL} - t_{PLH} $	PWD			5.0	ns	See <a href="#">Figure 6.7</a> , $C_L = 15\text{pF}$
Rising Time	$t_r$			5.0	ns	See <a href="#">Figure 6.7</a> , $C_L = 15\text{pF}$
Falling Time	$t_f$			5.0	ns	See <a href="#">Figure 6.7</a> , $C_L = 15\text{pF}$
Peak Eye Diagram Jitter	$t_{JIT(PK)}$		2.5		ns	
Channel-to-Channel Delay Skew	$t_{SK(c2c)}$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK(p2p)}$			5.0	ns	
Disable high to Tri-State	$t_{PHZ}$		13.9	30	ns	See <a href="#">Figure 6.8</a> , $C_L = 15\text{pF}$ , $R_L=1\text{k}$
Enable to Data high Valid	$t_{PZH}$		15.6	30	ns	See <a href="#">Figure 6.8</a> , $C_L = 15\text{pF}$ , $R_L=1\text{k}$
Disable low to Tri-State	$t_{PLZ}$		12.6	30	ns	See <a href="#">Figure 6.8</a> , $C_L = 15\text{pF}$ , $R_L=1\text{k}$
Enable to Data low Valid	$t_{PZL}$		16.8	30	ns	See <a href="#">Figure 6.8</a> , $C_L = 15\text{pF}$ , $R_L=1\text{k}$

6.8. Typical Performance Characteristics

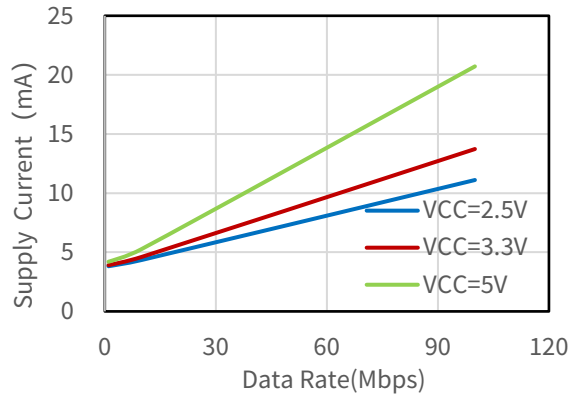
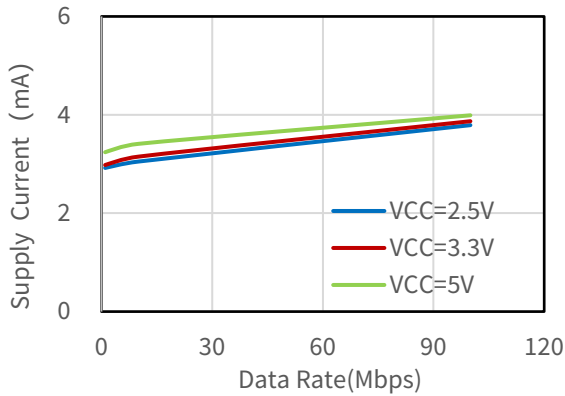


Figure 6.1 NSI8330 VDD1 Supply Current vs Data Rate    Figure 6.2 NSI8330 VDD2 Supply Current vs Data Rate

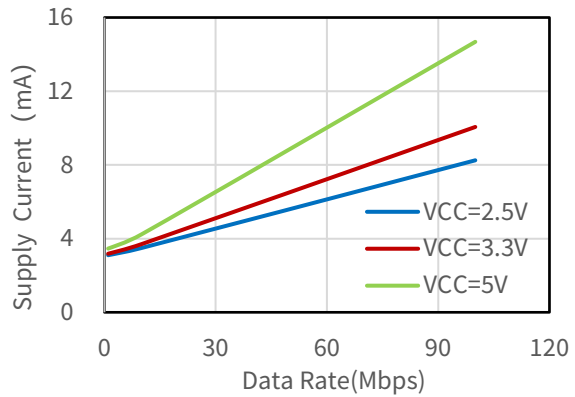
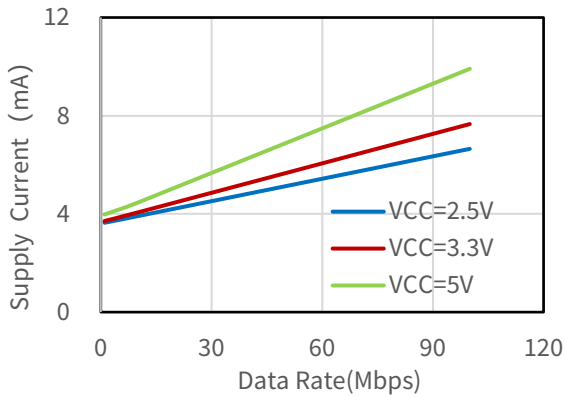


Figure 6.3 NSI8331 VDD1 Supply Current vs Data Rate    Figure 6.4 NSI8331 VDD2 Supply Current vs Data Rate

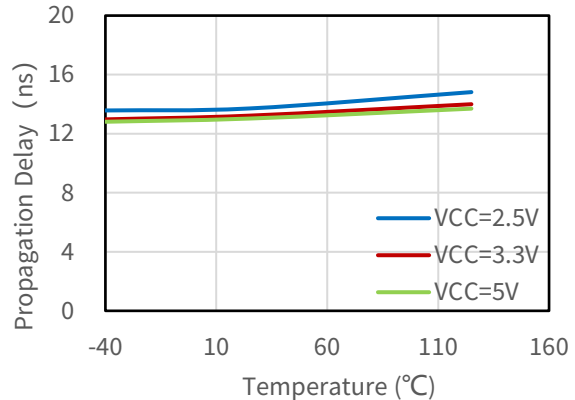
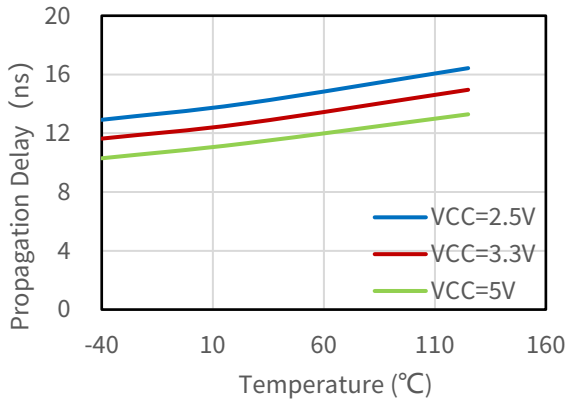
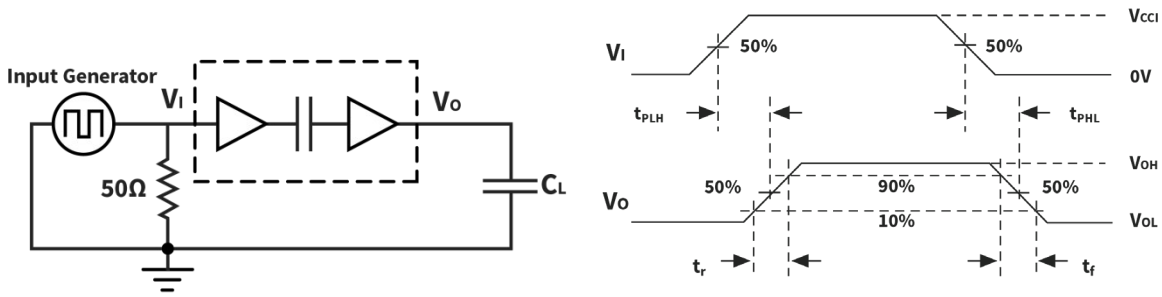


Figure 6.5 Rising Edge Propagation Delay Vs Temp

Figure 6.6 Falling Edge Propagation Delay Vs Temp

6.9. Parameter Measurement Information



(1) Input Generator Characteristics : PRR ≤ 50kHz, tr ≤ 3ns, tf ≤ 3ns, Duty cycle = 50%, Zo = 50 Ω.

Figure 6.7 Switching Characteristics Test Circuit and Waveform

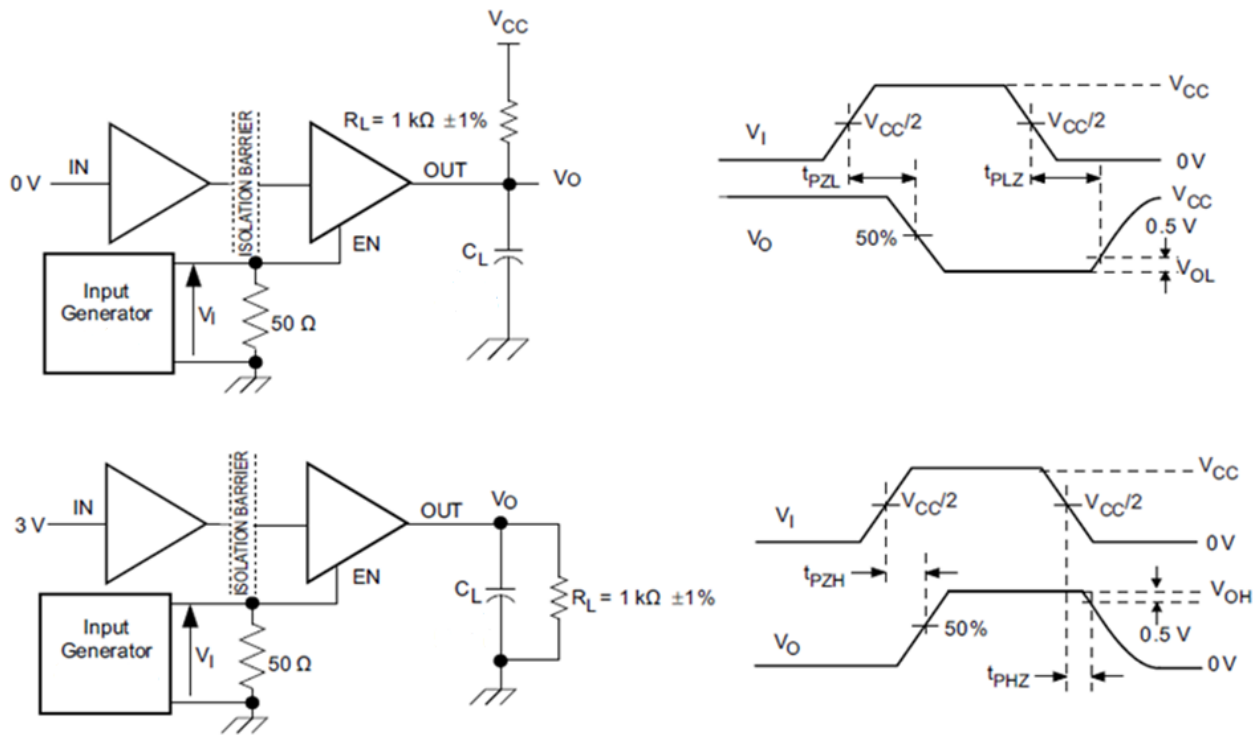


Figure 6.8 Enable/Disable Propagation Delay Time Test Circuit and Waveform

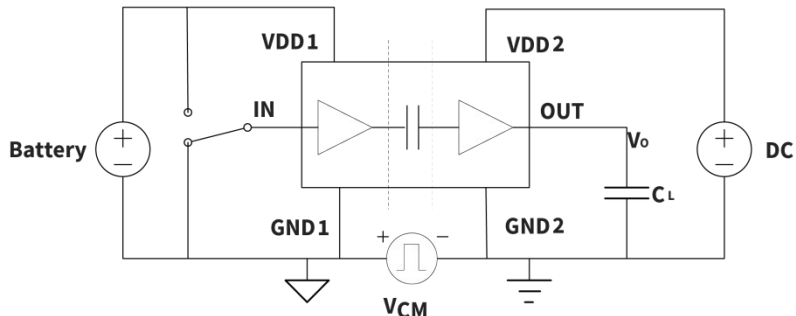


Figure 6.9 Common-Mode Transient Immunity Test Circuit

## 7. High Voltage Feature Description

### 7.1. Insulation and Safety Related Specifications

<i>Parameters</i>	<i>Symbol</i>	<i>Value</i>		<i>Comments</i>
		SOP16 (300mil)	<i>Unit</i>	
Minimum External Clearance	CLR	8	mm	IEC 60664-1:2007
Minimum External Creepage	CPG	8	mm	IEC 60664-1:2007
Distance Through Insulation	DTI	24	µm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

<i>Description</i>	<i>Test Condition</i>	<i>Value</i>
		SOP16 (300mil)
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	I to IV
	For Rated Mains Voltage ≤ 300Vrms	I to IV
	For Rated Mains Voltage ≤ 600Vrms	I to IV
	For Rated Mains Voltage ≤ 1000Vrms	I to III
Climatic Classification		40/125/21
Pollution Degree per DIN VDE 0110		2

### 7.2. Insulation Characteristics

<i>Description</i>	<i>Test Condition</i>	<i>Symbol</i>	<i>Value</i>	
			SOP16 (300mil)	<i>Unit</i>
Maximum repetitive isolation voltage		V <sub>IORM</sub>	2121	V <sub>PEAK</sub>
Maximum working isolation voltage	AC Voltage	V <sub>IOWM</sub>	1500	V <sub>RMS</sub>
	DC Voltage		2121	V <sub>DC</sub>

Description	Test Condition	Symbol	Value	
			SOP16 (300mil)	Unit
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$ , $t_{ini} = 60s$ , $V_{pd(m)}=1.2*V_{IORM}$ , $t_m=10s$ .	$q_{pd}$		pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$ , $t_{ini}=60s$ , $V_{pd(m)}=1.6*V_{IORM}$ , $t_m=10s$			pC
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}$ , $t_{ini}=1s$ $V_{pd(m)}=1.875*V_{IORM}$ , $t_m=1s$ (method b1) or $V_{pd(m)}=V_{ini}$ , $t_m=t_{ini}$ (method b2)			<5 pC
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$ , $t_{ini} = 60s$ , $V_{pd(m)}=1.2*V_{IORM}$ , $t_m=10s$ .	$q_{pd}$		pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$ , $t_{ini}=60s$ , $V_{pd(m)}=1.3*V_{IORM}$ , $t_m=10s$			pC
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}$ , $t_{ini}=1s$ $V_{pd(m)}=1.5*V_{IORM}$ , $t_m=1s$ (method b1) or $V_{pd(m)}=V_{ini}$ , $t_m=t_{ini}$ (method b2)			pC
Maximum transient isolation voltage	$t = 60 \text{ sec}$	$V_{IOTM}$	8000	$V_{PEAK}$
Maximum impulse voltage	Tested in air, 1.2/50 $\mu$ s waveform per IEC62368-1	$V_{IMP}$	6250	$V_{PEAK}$
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50 $\mu$ s waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$	$V_{IOSM}$	10000	$V_{PEAK}$

Description	Test Condition	Symbol	Value	
			SOP16 (300mil)	Unit
Isolation resistance	$V_{IO} = 500V, T_{amb} = 25^{\circ}C$	$R_{IO}$	$>10^{12}$	$\Omega$
	$V_{IO} = 500V, 100^{\circ}C \leq T_{amb} \leq 125^{\circ}C$	$R_{IO}$	$>10^{11}$	$\Omega$
	$V_{IO} = 500V, T_{amb} = T_s$	$R_{IO}$	$>10^9$	$\Omega$
Isolation capacitance	$f = 1MHz$	$C_{IO}$	0.8	pF
Insulation voltage per UL	$V_{TEST} = V_{ISO}, t = 60s$ (qualification), $V_{TEST} = 1.2 \times V_{ISO}, t = 1s$ (100% production test)	$V_{ISO}$	5000	$V_{RMS}$

### 7.3. Safety-Limiting Values

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI833x-Q1SWR.

Description	Test Condition	Symbol	Value	Unit
Safety Supply Power	$R_{\theta JA} = 78.9^{\circ}C/W^1), T_J = 150^{\circ}C, T_A = 25^{\circ}C$		1584	mW
Safety Supply Current	$R_{\theta JA} = 78.9^{\circ}C/W^1), V_I = 5V, T_J = 150^{\circ}C, T_A = 25^{\circ}C$		316.8	mA
Safety Temperature <sup>2)</sup>		$T_s$	150	$^{\circ}C$

- 1) Calculate with the junction-to-air thermal resistance,  $R_{\theta JA}$ , of SOP16(300mil) package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature ( $T_J$ ) specified for the device.

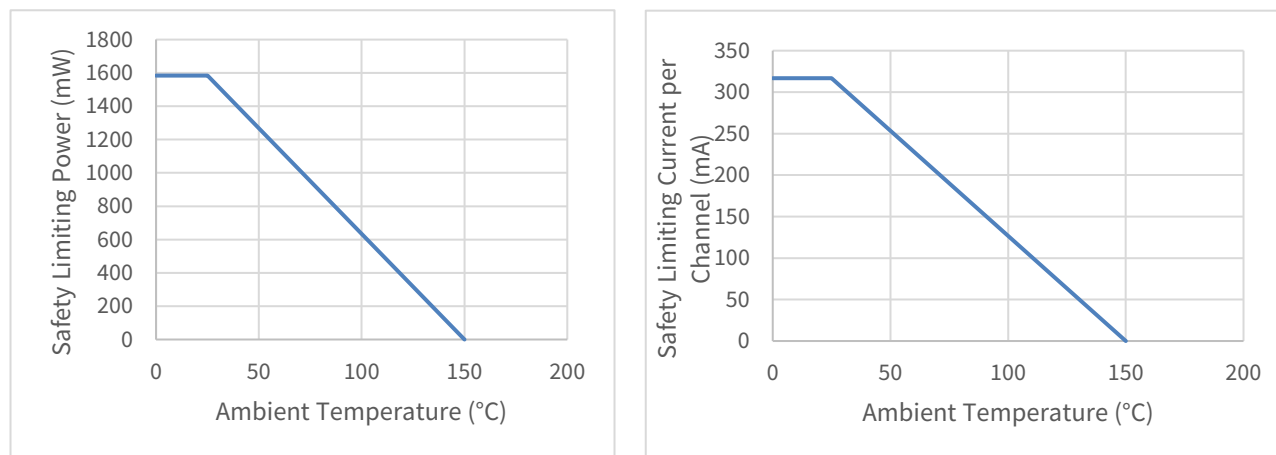


Figure 7.1 NSI833x Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17).

**7.4. Regulatory Information**

The NSI833xWx-Q1SWR are approved by the organizations listed in table.

<i>UL</i>		<i>CQC</i>		<i>TUV</i>
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to GB4943.1-2022	DIN EN IEC 60747-17 (VDE 0884-17)	Certified According to EN IEC 62368-1
Single Protection, 5000V <sub>rms</sub> Isolation voltage	Single Protection, 5000V <sub>rms</sub> Isolation voltage	Reinforced insulation	Reinforced Insulation V <sub>IORM</sub> =2121Vpeak V <sub>IOTM</sub> =8000Vpeak V <sub>IOSM</sub> =10000Vpeak	5000Vrms for 1min
E500602	E500602	CQC20001264939	R 50632560	R 50574061

## 8. Function Description

### 8.1. Overview

The NSI833x is a Triple-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NSI833x devices are high reliability triple-channel digital isolator. The NSI833x device is safety certified by UL1577 support 5kV<sub>rms</sub> insulation withstand voltages, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI833x is up to 100Mbps, and the common-mode transient immunity (CMTI) is up to 200kV/μs. The NSI833x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI833x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

The NSI833x has a default output status when VDD<sub>IN</sub> is unready and VDD<sub>OUT</sub> is ready as shown in Table 8.1, which helps for diagnosis when power is missing at the transmitter side. The output B follows the same status with the input A after powering up.

Table 8.1 Output status vs. power status

<i>Input<sup>1</sup></i>	<i>EN<sub>x</sub><sup>2</sup></i>	<i>VDD<sub>IN</sub> status</i>	<i>VDD<sub>OUT</sub> status</i>	<i>Output</i>	<i>Comment</i>
H	H or NC	Ready	Ready	H	Normal operation.
L	H or NC	Ready	Ready	L	
X	L	Ready	Ready	Z	Output disabled, the output is high impedance
X	H or NC	Unready	Ready	L(NSI833xx0) H(NSI833xx1)	The output follows the same status with the input after input side VDD <sub>IN</sub> is powered on.
X	L	Unready	Ready	Z	Output disabled, the output is high impedance
X	X	Ready	Unready	Undetermined	The output follows the same status with the input after output side VDD <sub>OUT</sub> is powered on.

Note: H=Logic high; L=Logic low; X=Logic low or logic high; Z=High impedance.  
VDD<sub>IN</sub> is input side power; VDD<sub>OUT</sub> is output side power.

(1) There is a protection diode between the input and the VDD<sub>IN</sub>. When the VDD<sub>IN</sub> is floating, the strong drive signal through the input pin will put the VDD<sub>IN</sub> in an indeterminate state.

(2) The EN<sub>x</sub> is output side enable.

### 8.2. OOK Modulation

NSI833x is based on a capacitive isolation barrier technique and the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, as shown in Figure 8.1 to Figure 8.2, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI.

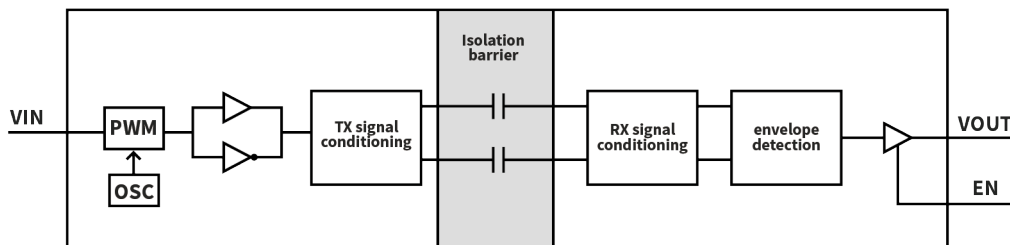


Figure 8.1 Single Channel Function Block Diagram

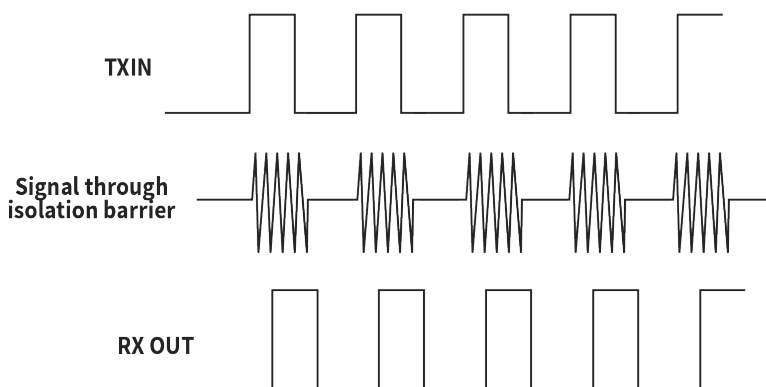


Figure 8.2 OOK Modulation

## 9. Application Note

### 9.1. Typical Application Circuit

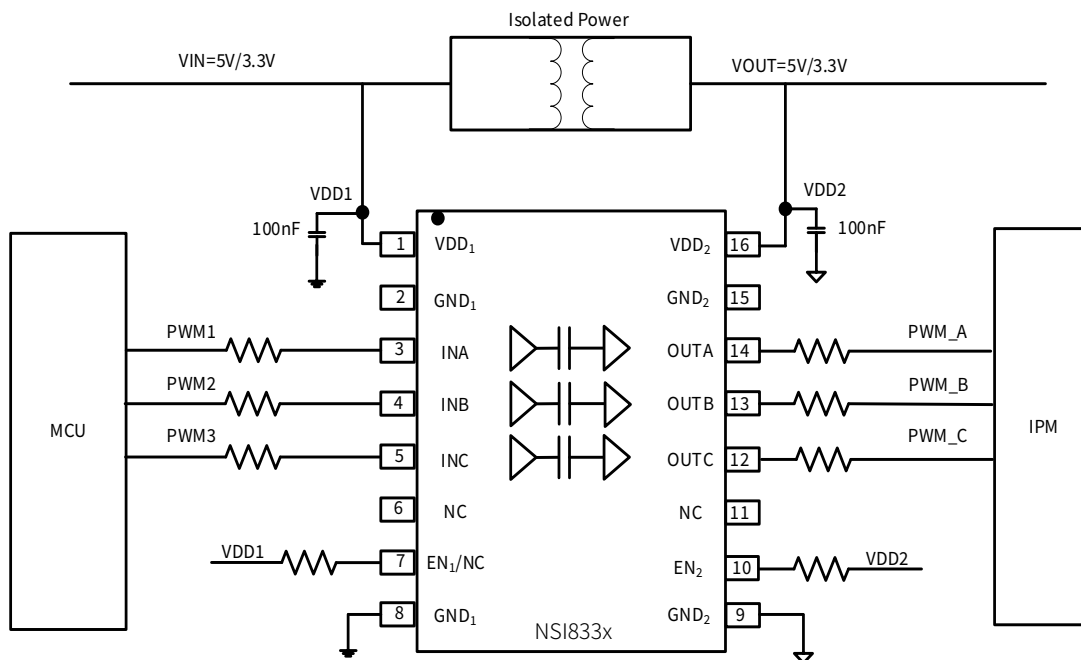


Figure 9.1 Typical PWM isolation circuit for IPM

### 9.2. PCB Layout

The NSI833x requires a 0.1  $\mu\text{F}$  bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. Figure 8.2 to Figure 8.3 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300  $\Omega$ ) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50  $\Omega$ ,  $\pm 40\%$ . When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

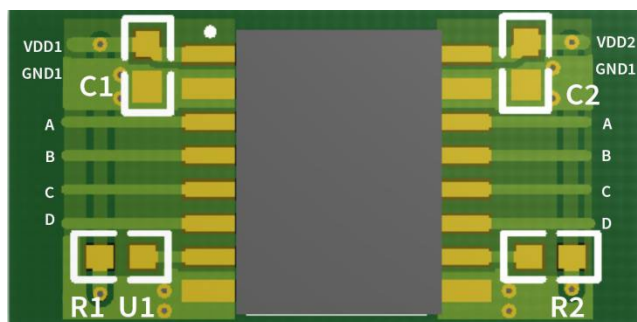


Figure 9.2 Recommended PCB Layout — Top Layer

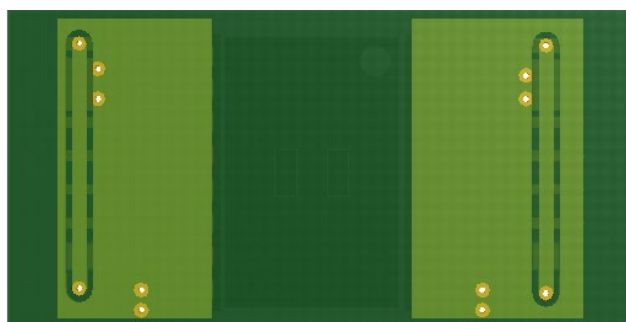


Figure 9.3 Recommended PCB Layout — Bottom Layer

### 9.3. High Speed Performance

Figure 9.4 shows the eye diagram of NSI833x-Q1 at 50Mbps data rate output. The result shows a typical measurement on NSI833x-Q1 with low jitter and wide open eye characteristics.

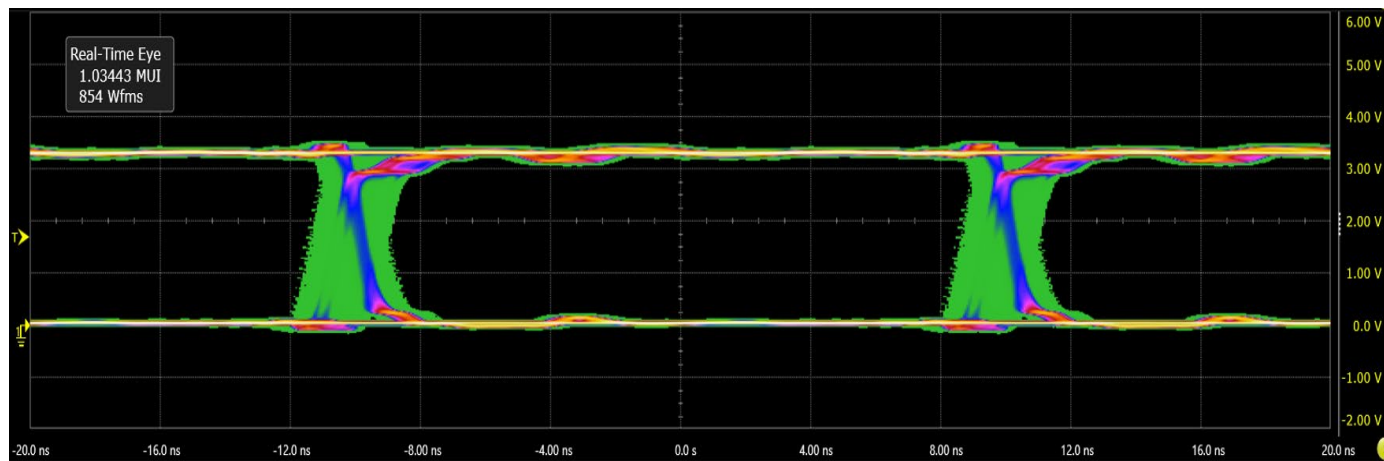


Figure9.4 Eye Diagram at 50Mbps PRBS 2<sup>16</sup>-1, 2.5V and 25°C

### 9.4. Typical Supply Current Equations

The typical supply current of NSI833x can be calculated using below equations.  $I_{DD1}$  and  $I_{DD2}$  are typical supply currents measured in mA,  $f$  is data rate measured in Mbps,  $C_L$  is the capacitive load measured in pF

#### NSI8330:

$$I_{DD1} = 0.298 * a1 + 1.458 * b1 + 0.878 * c1.$$

$$I_{DD2} = 3.93 + 0.5 * VDD2 * f * C_L * c1 * 10^{-3}$$

When  $a1$  is the channel number of default state input at side 1,  $b1$  is the channel number of non-default state input at side 1,  $c1$  is the channel number of switch signal input at side 1.

#### NSI8331:

$$I_{DD1} = 2.56 + 1.16 * b1 + 0.58 * c1 + 0.5 * VDD1 * f * C_L * c2 * 10^{-3}$$

$$I_{DD2} = 2.56 + 1.16 * b2 + 0.58 * c2 + 0.5 * VDD2 * f * C_L * c1 * 10^{-3}$$

When  $b1$  is the channel number of non-default state input at side 1,  $c1$  is the channel number of switch signal input at side 1,  $b2$  is the channel number of non-default state input at side 2,  $c2$  is the channel number of switch signal input at side 2.

### 10. Package Information

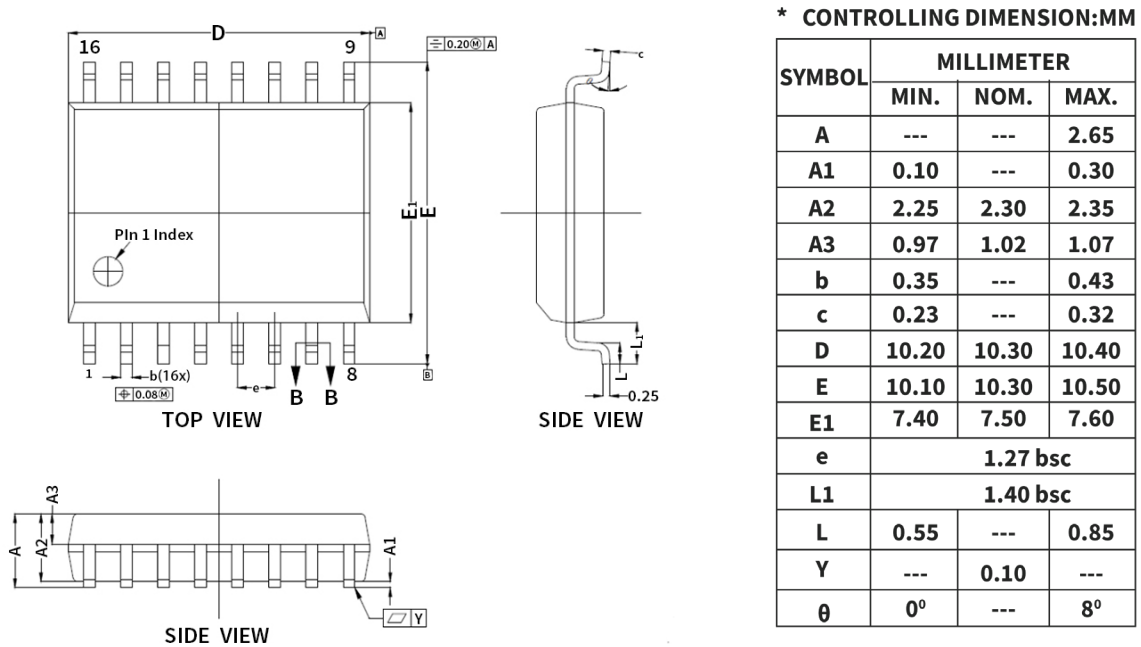


Figure 10.1 SOP16(300mil)/SOW16 Package Shape and Dimension in millimeters

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

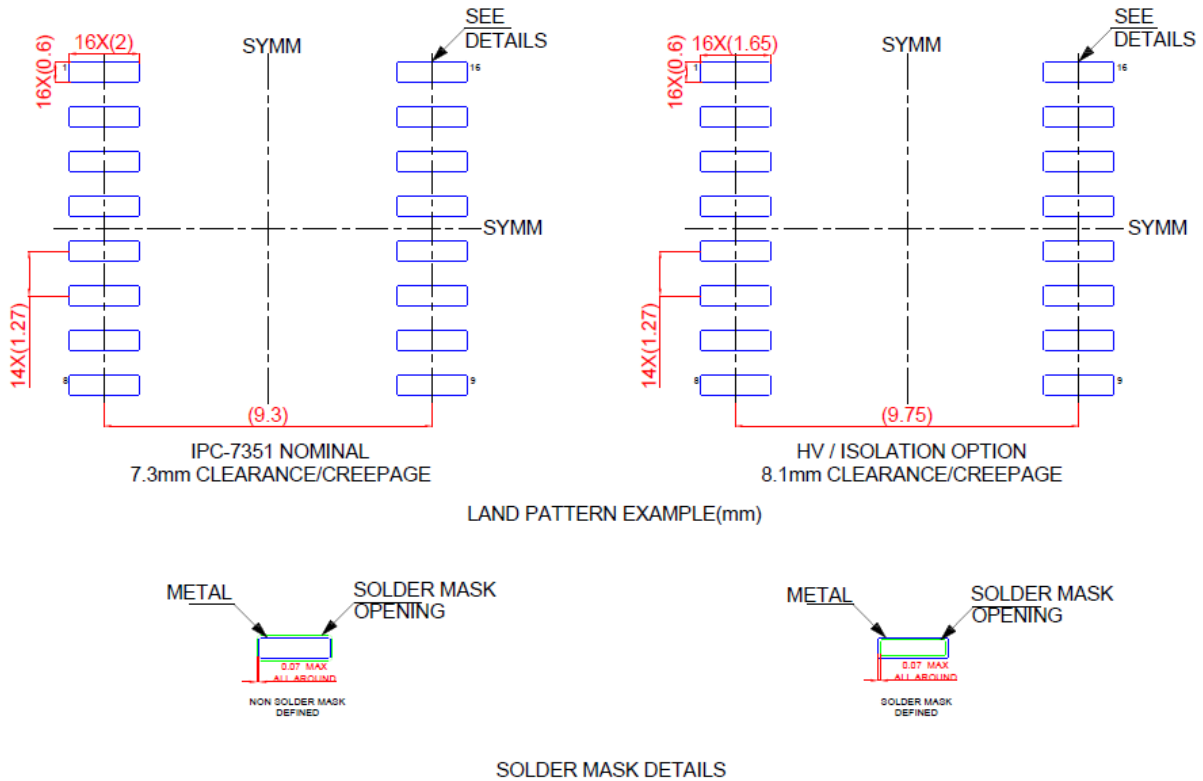


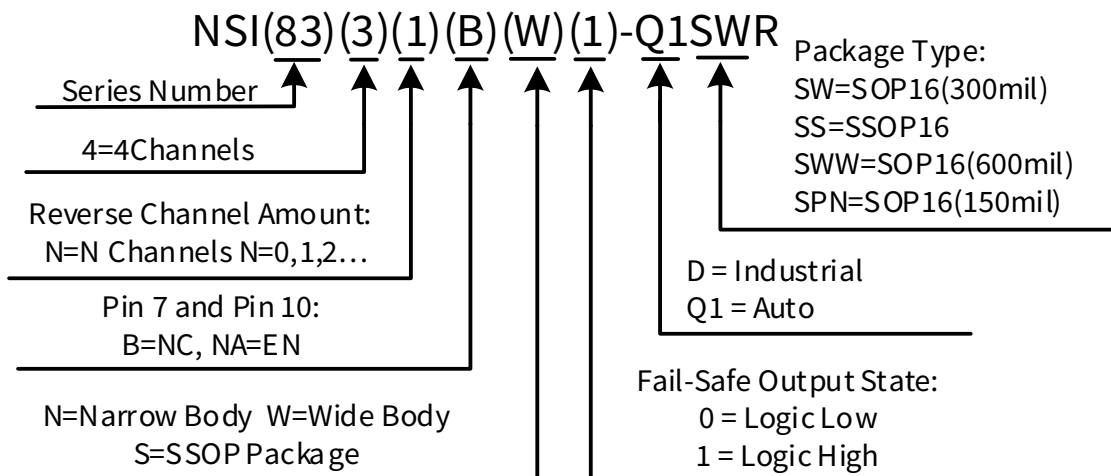
Figure 10.2 SOP16(300mil) SOW16 Package Board Layout Example

### 11. Order Information

Part Number	Isolation Rating (kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	M S L	Package Type	Package Drawing	SPQ
NSI8330W0-Q1SWR	5	3	0	100	Low	-40 to 125°C	3	SOP16 (300mil)	SOW16	1000
NSI8330W1-Q1SWR	5	3	0	100	High	-40 to 125°C	3	SOP16 (300mil)	SOW16	1000
NSI8331W0-Q1SWR	5	2	1	100	Low	-40 to 125°C	3	SOP16 (300mil)	SOW16	1000
NSI8331W1-Q1SWR	5	2	1	100	High	-40 to 125°C	3	SOP16 (300mil)	SOW16	1000

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.

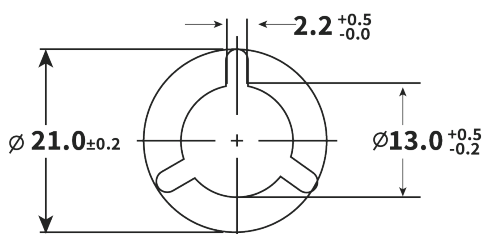
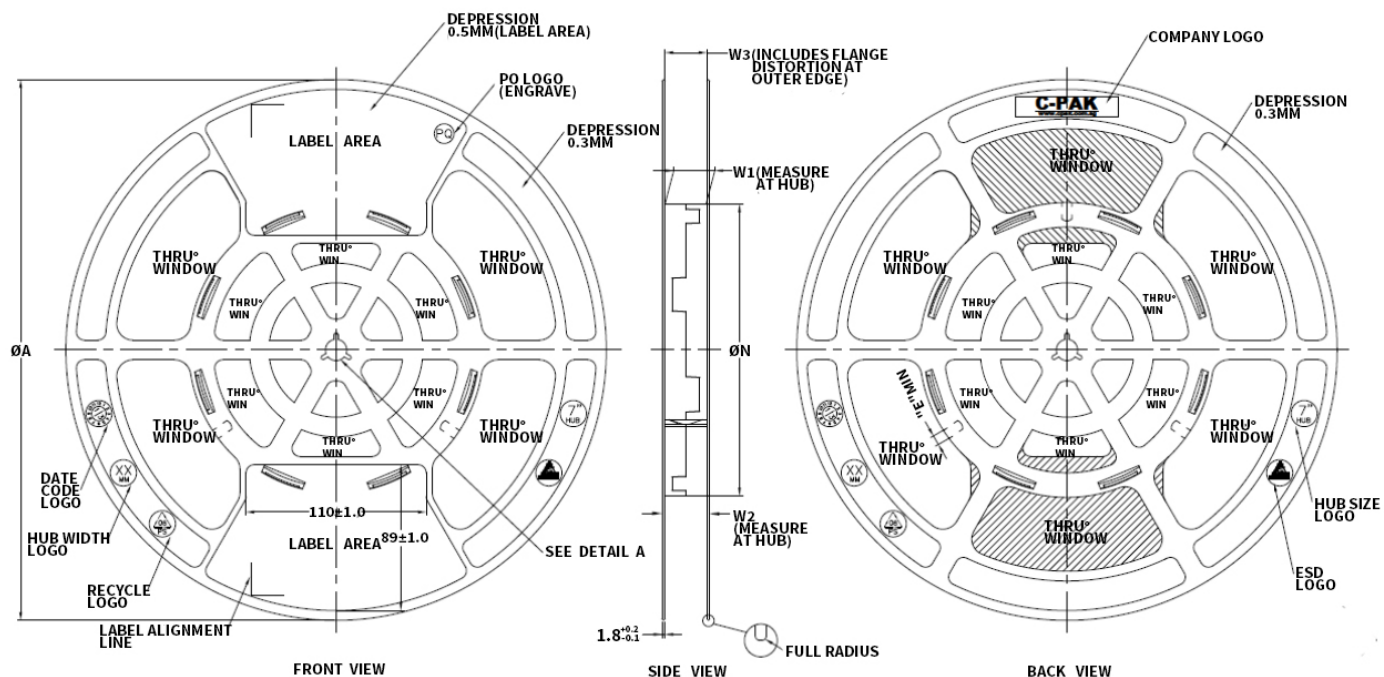
**Part Number Rule:**



## 12. Documentation Support

<i>Part Number</i>	<i>Product Folder</i>	<i>Datasheet</i>	<i>Technical Documents</i>	<i>Isolator selection guide</i>
NSI833x-Q1	tbd	tbd	tbd	tbd

### 13. Tape and Reel Information

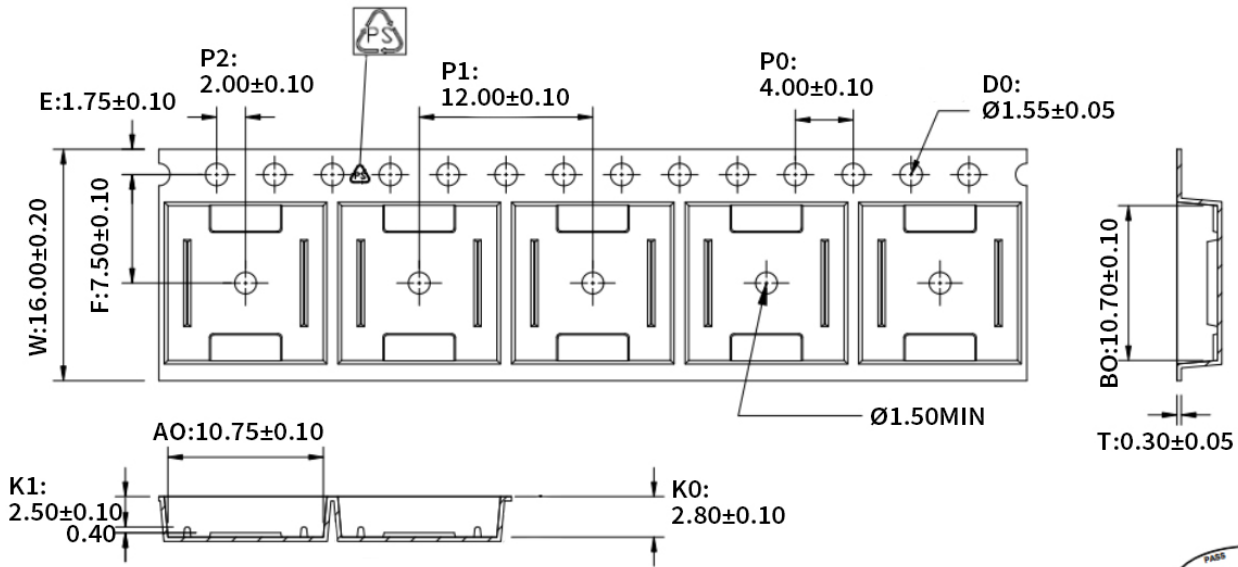


**ARBOR HOLE  
DETAIL A  
SCALE: 3:1**

PRODUCT SPECIFICATION						
TAPE WIDTH	$\varnothing A$ $\pm 2.0$	$\varnothing N$ $\pm 2.0$	W1	W2 (Max)	W3	E (MIN)
08MM	330	178	$8.4^{+1.5}_{-0.0}$	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	$12.4^{+2.0}_{-0.0}$	18.4		5.5
16MM	330	178	$16.4^{+2.0}_{-0.0}$	22.4		5.5
24MM	330	178	$24.4^{+2.0}_{-0.0}$	30.4		5.5
32MM	330	178	$32.4^{+2.0}_{-0.0}$	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW $10^{12}$	ANTISTATIC	ALL TYPES
B	$10^6$ TO $10^{11}$	STATIC DISSIPATIVE	BLACK ONLY
C	$10^5$ & BELOW $10^5$	CONDUCTIVE(GENERIC)	BLACK ONLY
E	$10^9$ TO $10^{11}$	ANTISTATIC(COATED)	ALL TYPES

Figure 13.1 Reel Information (for all packages)



1. 1.10 sprocket hole pitch cumulative tolerance  $\pm 0.20$ .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness:  $0.30 \pm 0.05$ mm.
6. Packing length per 22" reel: 378 Meters.(Rewind N=122 )
7. Component load per 13" reel: 1000 pcs.
8. Surface resistivity:  $10^5 \sim 10^{10} \Omega/\square$

W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

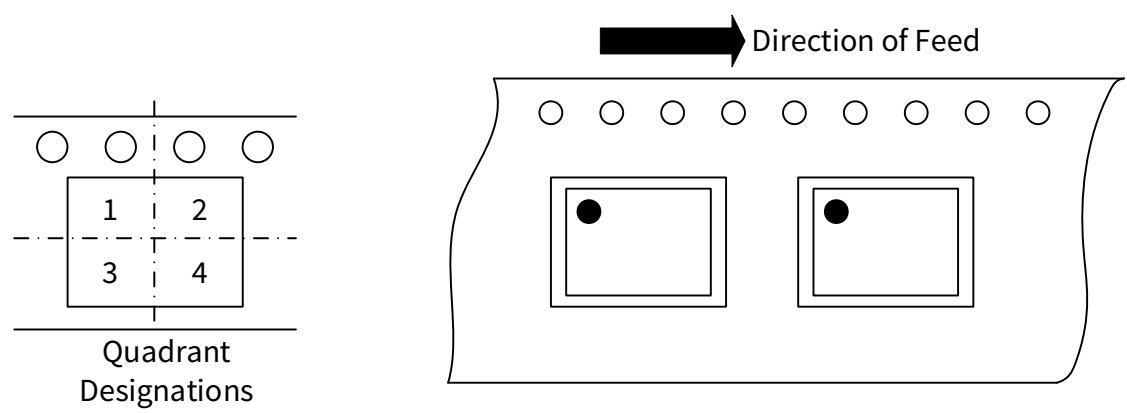


Figure 13.2 Tape Information of SOP16(300mil)

## 14. Revision History

Revision	Description	Date
1.0	Initial version	2025/10/10

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