

Product Overview

The NSI832xWx-DSWWAR, SOWW8 package (will be abbreviated as NSI832x in this datasheet) devices are high reliability dual-channel digital isolators. The NSI832x device is safety certified by UL1577 and supports 7500Vrms insulation withstand voltage, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI832x is up to 100Mbps, and the common-mode transient immunity (CMTI) is up to 250kV/μs. The NSI832x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI832x device supports to connect with most digital interface directly, making level shifting easy. High system level EMC performance enhances reliability and stability of use.

Key Features

- Up to 7500V_{rms} Insulation voltage
- Data rate: DC to 100Mbps
- Power supply voltage: 2.5V to 5.5V
- High CMTI: 250kV/μs
- Chip level ESD: HBM: ±8kV
- Robust EMC Reinforced Dual-Channel Digital Isolators for SOWW8 wide body
- Default output high level or low level option
- Isolation surge voltage: >10600V
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <18ns
- Operation temperature: -55°C~125°C
- RoHS-compliant packages:
SOWW8 wide body

Safety Regulatory Approvals

- UL recognition: up to 7500V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor control

Device Information

Part Number	Package	Body Size
NSI832xWx-DSWWAR	SOWW8	6.25mm × 13.60mm

Functional Block Diagrams

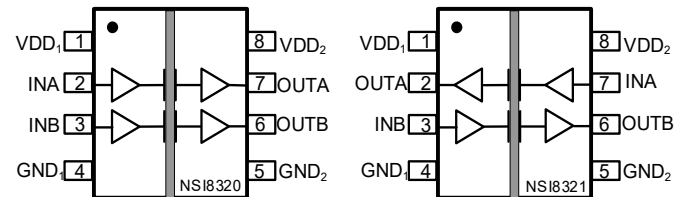


Figure 1 NSI8320
Block Diagram

Figure 2 NSI8321
Block Diagram

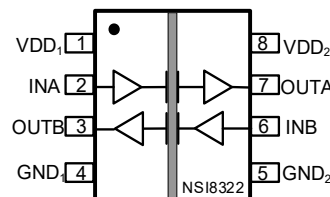


Figure 3 NSI8322
Block Diagram

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1. Pin Configuration and Functions

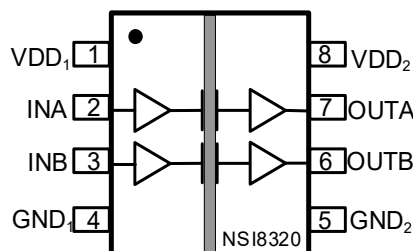


Figure 1.1 NSI8320 Package

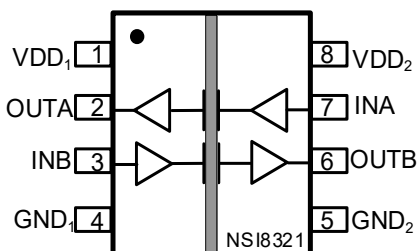


Figure 1.2 NSI8321 Package

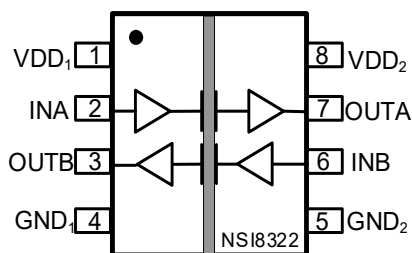


Figure 1.3 NSI8322 Package

Table1.1 NSI832x Pin Configuration and Description

NSI8320 PIN NO.	NSI8321 PIN NO.	NSI8322 PIN NO.	SYMBOL	FUNCTION
1	1	1	VDD ₁	Power Supply for Isolator Side 1
2	7	2	INA	Logic Input A
3	3	6	INB	Logic Input B
4	4	4	GND ₁	Ground 1, the ground reference for Isolator Side 1
5	5	5	GND ₂	Ground 2, the ground reference for Isolator Side 2
6	6	3	OUTB	Logic Output B
7	2	7	OUTA	Logic Output A
8	8	8	VDD ₂	Power Supply for Isolator Side 2

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	V _{INA} , V _{INB}	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Output Voltage	V _{OUTA} , V _{OUTB}	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Input/Output Pulse Voltage	V _{INA} , V _{INB} , V _{OUTA} , V _{OUTB}	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Output current	I _o	-15		15	mA	
Operating Temperature	T _{opr}	-55		125	°C	
Junction Temperature	T _j			150	°C	
Storage Temperature	T _{stg}	-65		150	°C	

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating conditions. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.
- (2) Power supply voltage and input/output voltage are respect to the local ground terminal (GND1 or GND2) voltage values.

3. ESD Ratings

Parameters	Ratings	Value	Unit
Electrostatic discharge (ESD)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽²⁾	±8000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽³⁾	±2000	V

- (1) Though this device features proprietary protection circuitry, proper ESD precautions should be considered to avoid performance degradation of damage due to high energy ESD event. Charged devices and circuit boards may discharge without detection.
- (2) Safe manufacturing requires 500-V HBM and standard ESD precautions, per JEDEC document JEP155.
- (3) Safe manufacturing requires 250-V CDM and standard ESD precautions, per JEDEC document JEP157.

4. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit
Power Supply Voltage	VDD1, VDD2	2.5		5.5	V

Operating Temperature	Topr	-55		125	°C
High Level Input Voltage	VIH	0.7*VDD			V
Low Level Input Voltage	VIL			0.3*VDD	V
Data rate	DR			100	Mbps

5. Thermal Characteristics

Parameters	Symbol	SOWW8	Unit
IC Junction-to-Air Thermal Resistance	$R_{\theta JA}$	78.9	°C/W
Junction-to-case (top) thermal resistance	$R_{\theta JC (top)}$	41.6	°C/W
Junction-to-board thermal resistance	$R_{\theta JB}$	43.6	°C/W
Junction-to-top characterization parameter	Ψ_{JT}	7.0	°C/W
Junction-to-board characterization parameter	Ψ_{JB}	28.0	°C/W

6. Specifications

6.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power on Reset	$V_{DDPOR}^{(1)}$	2	2.2	2.4	V	POR threshold as during power-up
	$V_{DDHYS}^{(1)}$		0.1		V	POR threshold Hysteresis
Rising input switching threshold	$V_{IT+}^{(1)}$		0.6*VDD	0.7*VDD	V	
Falling input switching threshold	$V_{IT-}^{(1)}$	0.3*VDD	0.4*VDD		V	
Input threshold voltage hysteresis	$V_{IT_HYS}^{(1)}$		0.2*VDD		V	
High Level Output Voltage	V_{OH}	VDD-0.4			V	$I_{OH} \leq 4mA$
Low Level Output Voltage	V_{OL}			0.4	V	$I_{OL} \leq 4mA$
Output Impedance	$R_{out}^{(1)}$		50		ohm	
Input Pull high or low Current	I_{pull}		5	10	μA	

	NSI832xWx					
Start Up Time after POR	trbs ⁽²⁾		22	32	μs	
Common Mode Transient Immunity	CMTI	±200	±250		kV/μs	See Figure 6.14

⁽¹⁾ Not test covered, guaranteed by characterization.

⁽²⁾ Not test covered, guaranteed by design.

6.2. Supply Current Characteristics –5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=–55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSI8320Wx					
	I _{DD1} (Q0)		0.79	1.24	mA	All Input 0V for NSI832xW0 Or All Input at supply for NSI832xW1
	I _{DD2} (Q0)		1.84	2.44	mA	
	I _{DD1} (Q1)		3.43	4.55	mA	All Input at supply for NSI832xW0 Or All Input 0V for NSI832xW1
	I _{DD2} (Q1)		1.95	2.56	mA	
	I _{DD1} (1M)		2.13	2.80	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		1.91	2.52	mA	
	I _{DD1} (10M)		2.15	2.82	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		3.03	3.65	mA	
	I _{DD1} (100M)		2.61	3.97	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		13.28	17.53	mA	
	NSI8321Wx / NSI8322Wx					
	I _{DD1} (Q0)		1.55	2.12	mA	All Input 0V for NSI832xW0 Or All Input at supply for NSI832xW1
	I _{DD2} (Q0)		1.55	2.12	mA	
	I _{DD1} (Q1)		2.88	3.83	mA	All Input at supply for NSI832xW0 Or All Input 0V for NSI832xW1
	I _{DD2} (Q1)		2.88	3.83	mA	
	I _{DD1} (1M)		2.28	2.98	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		2.28	2.98	mA	
	I _{DD1} (10M)		2.84	3.77	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		2.84	3.77	mA	

<i>Parameters</i>	<i>Symbol</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Unit</i>	<i>Comments</i>
	I _{DD1} (100M)		8.29	10.94	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		8.29	10.94	mA	

6.3. Supply Current Characteristics –3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSI8320Wx					
	I _{DD1} (Q0)		0.77	1.21	mA	All Input 0V for NSI832xW0 Or All Input at supply for NSI832xW1
	I _{DD2} (Q0)		1.80	2.43	mA	
	I _{DD1} (Q1)		3.39	4.54	mA	All Input at supply for NSI832xW0 Or All Input 0V for NSI832xW1
	I _{DD2} (Q1)		1.91	2.51	mA	
	I _{DD1} (1M)		2.10	2.76	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		1.87	2.46	mA	
	I _{DD1} (10M)		2.15	2.86	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		2.61	3.50	mA	
	I _{DD1} (100M)		2.57	3.44	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		9.39	12.58	mA	
	NSI8321Wx / NSI8322Wx					
	I _{DD1} (Q0)		1.50	1.98	mA	All Input 0V for NSI832xW0 Or All Input at supply for NSI832xW1
	I _{DD2} (Q0)		1.50	1.98	mA	
	I _{DD1} (Q1)		2.82	3.78	mA	All Input at supply for NSI832xW0 Or All Input 0V for NSI832xW1
	I _{DD2} (Q1)		2.82	3.78	mA	
	I _{DD1} (1M)		2.20	2.94	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		2.20	2.94	mA	
	I _{DD1} (10M)		2.57	3.44	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		2.57	3.44	mA	
	I _{DD1} (100M)		6.11	8.25	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		6.11	8.25	mA	

6.4. Supply Current Characteristics–2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 2.5V**, **VDD2 = 2.5V**, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSI8320Wx					
	I _{DD1} (Q0)		0.75	1.19	mA	All Input 0V for NSI832xW0 Or All Input at supply for NSI832xW1
	I _{DD2} (Q0)		1.77	2.37	mA	
	I _{DD1} (Q1)		3.34	4.41	mA	All Input at supply for NSI832xW0 Or All Input 0V for NSI832xW1
	I _{DD2} (Q1)		1.88	2.51	mA	
	I _{DD1} (1M)		2.06	2.72	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		1.84	2.44	mA	
	I _{DD1} (10M)		2.11	2.78	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		2.40	3.21	mA	
	I _{DD1} (100M)		2.52	3.30	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		7.57	9.98	mA	
	NSI8321Wx / NSI8322Wx					
	I _{DD1} (Q0)		1.46	1.93	mA	All Input 0V for NSI832xW0 Or All Input at supply for NSI832xW1
	I _{DD2} (Q0)		1.46	1.93	mA	
	I _{DD1} (Q1)		2.76	3.67	mA	All Input at supply for NSI832xW0 Or All Input 0V for NSI832xW1
	I _{DD2} (Q1)		2.76	3.67	mA	
	I _{DD1} (1M)		2.14	2.85	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		2.14	2.85	mA	
	I _{DD1} (10M)		2.42	3.22	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		2.42	3.22	mA	
	I _{DD1} (100M)		5.14	6.81	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		5.14	6.81	mA	

6.5. Switching Characteristics - 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V**, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
NSI832xWx						
Data Rate	DR	0		100	Mbps	
Minimum Pulse Width	PW			8.3	ns	
Propagation Delay	t _{PLH}		12.5	18	ns	See Figure 6.13 , C _L = 15pF
	t _{PHL}		12.1	18	ns	See Figure 6.13 , C _L = 15pF
Pulse Width Distortion t _{PHL} - t _{PLH}	PWD			5.0	ns	See Figure 6.13 , C _L = 15pF
Rising Time	t _r			5.0	ns	See Figure 6.13 , C _L = 15pF
Falling Time	t _f			5.0	ns	See Figure 6.13 , C _L = 15pF
Peak Eye Diagram Jitter	t _{JIT(PK)}		2.5		ns	
Channel-to-Channel Delay Skew	t _{SK(c2c)}			2.5	ns	
Part-to-Part Delay Skew	t _{SK(p2p)}			5.0	ns	

6.6. Switching Characteristics - 3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V**, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
NSI832xWx						
Data Rate	DR	0		100	Mbps	
Minimum Pulse Width	PW			8.3	ns	
Propagation Delay	t _{PLH}		13.0	19	ns	See Figure 6.13 , C _L = 15pF
	t _{PHL}		12.5	19	ns	See Figure 6.13 , C _L = 15pF
Pulse Width Distortion t _{PHL} - t _{PLH}	PWD			5.0	ns	See Figure 6.13 , C _L = 15pF
Rising Time	t _r			5.0	ns	See Figure 6.13 , C _L = 15pF
Falling Time	t _f			5.0	ns	See Figure 6.13 , C _L = 15pF

Peak Eye Diagram Jitter	$t_{JIT}(PK)$		2.5		ns	
Channel-to-Channel Delay Skew	$t_{SK}(c2c)$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK}(p2p)$			5.0	ns	

6.7. Switching Characteristics - 2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 2.5V**, **VDD2 = 2.5V**, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
NSI832xWx						
Data Rate	DR	0		100	Mbps	
Minimum Pulse Width	PW			8.3	ns	
Propagation Delay	t_{PLH}		14.2	20	ns	See Figure 6.13 , $C_L = 15pF$
	t_{PHL}		13.5	20	ns	See Figure 6.13 , $C_L = 15pF$
Pulse Width Distortion $ t_{PHL} - t_{PLH} $	PWD			5.0	ns	See Figure 6.13 , $C_L = 15pF$
Rising Time	t_r			5.0	ns	See Figure 6.13 , $C_L = 15pF$
Falling Time	t_f			5.0	ns	See Figure 6.13 , $C_L = 15pF$
Peak Eye Diagram Jitter	$t_{JIT}(PK)$		2.5		ns	
Channel-to-Channel Delay Skew	$t_{SK}(c2c)$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK}(p2p)$			5.0	ns	

6.8. Typical Performance Characteristics

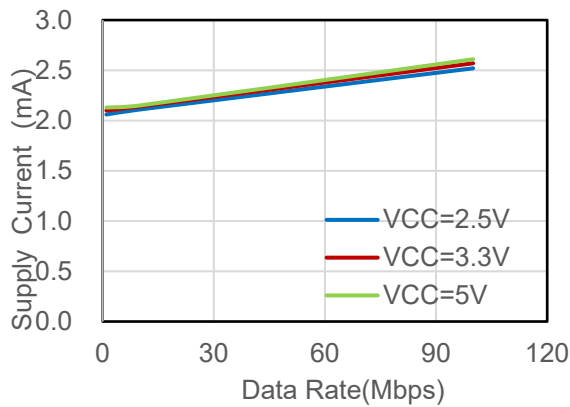


Figure 6.1 NSI8320Wx VDD1 Supply Current vs Data Rate

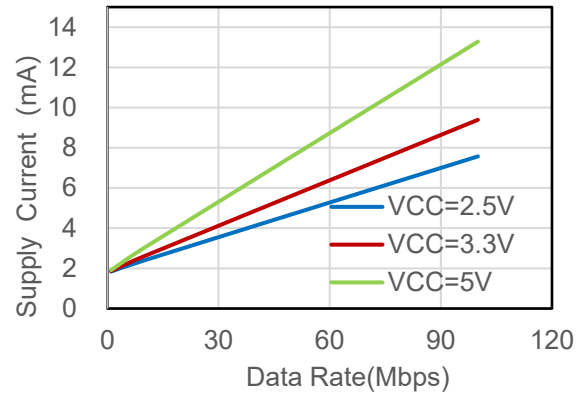


Figure 6.2 NSI8320Wx VDD2 Supply Current vs Data Rate

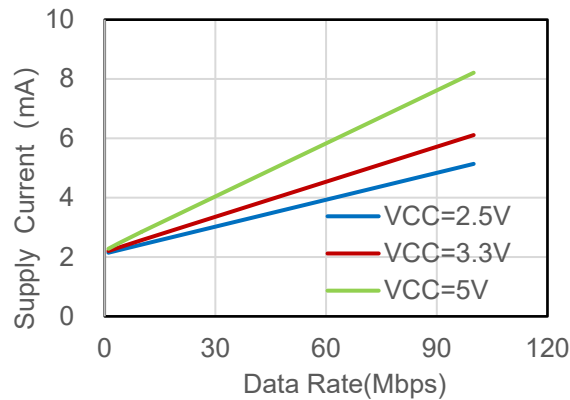


Figure 6.3 NSI8321Wx / NSI8322Wx
VDD1 Supply Current vs Data Rate

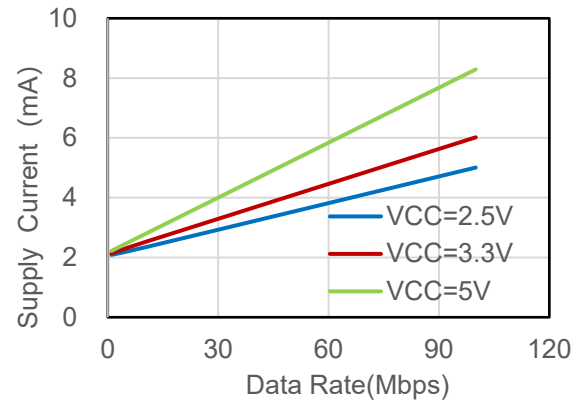


Figure 6.4 NSI8321Wx / NSI8322Wx
VDD2 Supply Current vs Data Rate

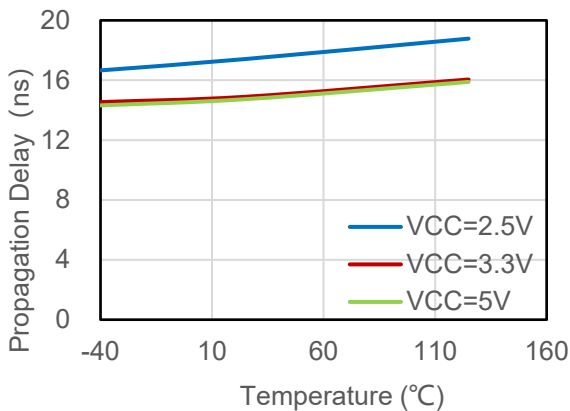


Figure 6.5 NSI832xWx Rising Edge
Propagation Delay Vs Temp

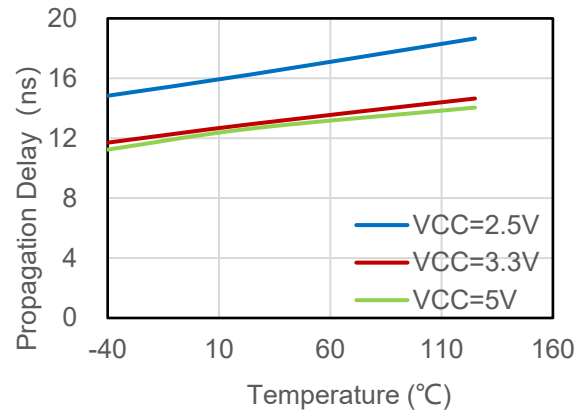
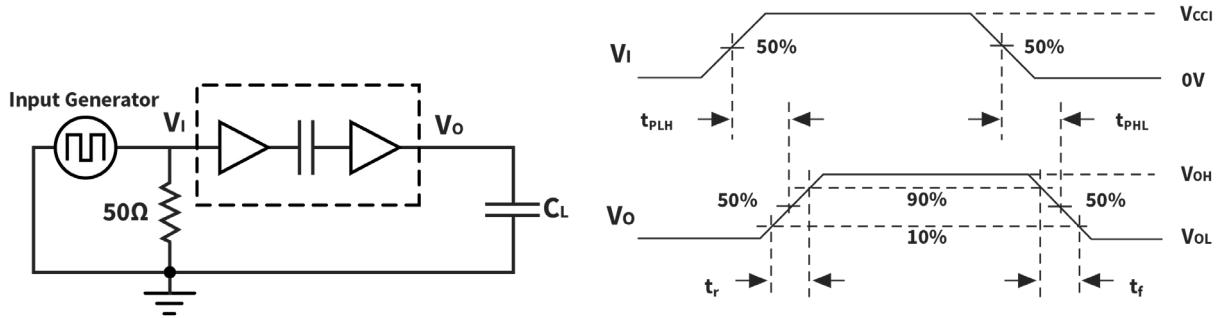


Figure 6.6 NSI832xWx Falling Edge
Propagation Delay Vs Temp

6.9. Parameter Measurement Information



(1) Input Generator Characteristics : PRR $\leq$ 50kHz, $t_r \leq$ 3ns, $t_f \leq$ 3ns, Duty cycle = 50%, $Z_o = 50 \Omega$.

Figure 6.7 Switching Characteristics Test Circuit and Waveform

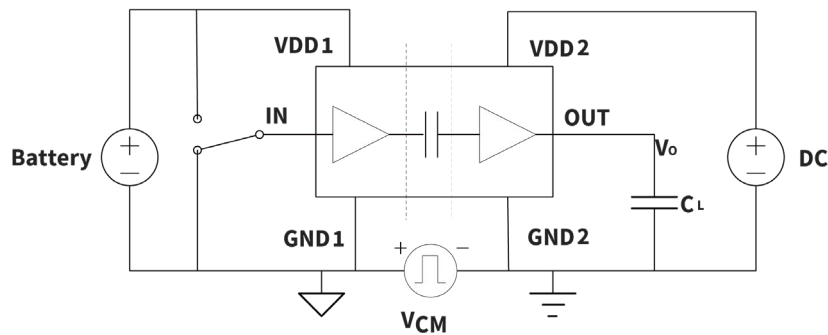


Figure 6.8 Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value SOWW8	Unit	Comments
Minimum External Clearance	CLR	15.0	mm	IEC 60664-1
Minimum External Creepage	CPG	15.0	mm	IEC 60664-1
Distance Through Insulation	DTI	24	μm	
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

Description	Test Condition	Value SOWW8
Overvoltage Category per IEC60664-1	For Rated Mains Voltage $\leq$ 150Vrms	I to IV
	For Rated Mains Voltage $\leq$ 300Vrms	I to IV
	For Rated Mains Voltage $\leq$ 600Vrms	I to IV
	For Rated Mains Voltage $\leq$ 1000Vrms	I to III
Climatic Classification		40/125/21
Pollution Degree per DIN VDE 0110,		2

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value SOWW8	Unit
Maximum repetitive isolation voltage		V_{IORM}	2828	V_{PEAK}
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	2000	V_{RMS}
	DC voltage		2828	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, $t_{ini}=60\text{ s}$, $V_{pd(m)}=1.2*V_{IORM}$, $t_m=10\text{ s}$.	q_{pd}	<5	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, $t_{ini}=60\text{ s}$, $V_{pd(m)}=1.6*V_{IORM}$, $t_m=10\text{ s}$			pC
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}$, $t_{ini}=1\text{ s}$ $V_{pd(m)}=1.875*V_{IORM}$, $t_m=1\text{ s}$ (method b1) or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$ (method b2)			pC
	Method a, after Input/output safety test subgroup 2/3,	q_{pd}		pC

Description	Test Condition	Symbol	Value	Unit
			SOWW8	
	$V_{ini}=V_{IOTM}$, $t_{ini}=60s$, $V_{pd(m)}=1.2 \times V_{IORM}$, $t_m=10s$.			
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, $t_{ini}=60s$, $V_{pd(m)}=1.3 \times V_{IORM}$, $t_m=10s$			pC
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2 \times V_{IOTM}$, $t_{ini}=1s$ $V_{pd(m)}=1.5 \times V_{IORM}$, $t_m=1s$ (method b1) or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$ (method b2)			pC
Maximum transient isolation voltage	$t=60\text{ sec}$	V_{IOTM}	10600	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50 μs waveform per IEC62368-1	V_{IMP}	8000	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC60065, 1.2/50 μs waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$	V_{IOSM}	12800	V_{PEAK}
Isolation resistance	$V_{IO}=500V$, $T_{amb}=25^{\circ}C$	R_{IO}	$>10^{12}$	Ω
	$V_{IO}=500V$, $100^{\circ}C \leq T_{amb} \leq 125^{\circ}C$		$>10^{11}$	Ω
	$V_{IO}=500V$, $T_{amb}=T_s$		$>10^9$	Ω
Isolation capacitance	$f=1\text{ MHz}$	C_{IO}	0.6	pF
Withstand Isolation Voltage	$V_{TEST}=V_{ISO}$, $t=60s$ (qualification), $V_{TEST}=1.2 \times V_{ISO}$, $t=1\text{ s}$ (100% production test)	V_{ISO}	7500	V_{RMS}

7.3. Safety-Limiting Values

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI832xWx-DSWWAR SOWW8(600mil)

Description	Test Condition	Symbol	Value	Unit
Safety input, output, or total Power	$R_{\theta JA}=78.9^{\circ}C/W^{(1)}$, $T_J=150^{\circ}C$, $T_A=25^{\circ}C$		1584	mW
Safety input, output, or supply Current	$R_{\theta JA}=78.9^{\circ}C/W^{(1)}$, $V_I=5.5\text{ V}$, $T_J=150^{\circ}C$, $T_A=25^{\circ}C$		288	mA

Safety Temperature ²⁾		T _s	150	°C
----------------------------------	--	----------------	-----	----

- 1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOWW8(600mil) package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

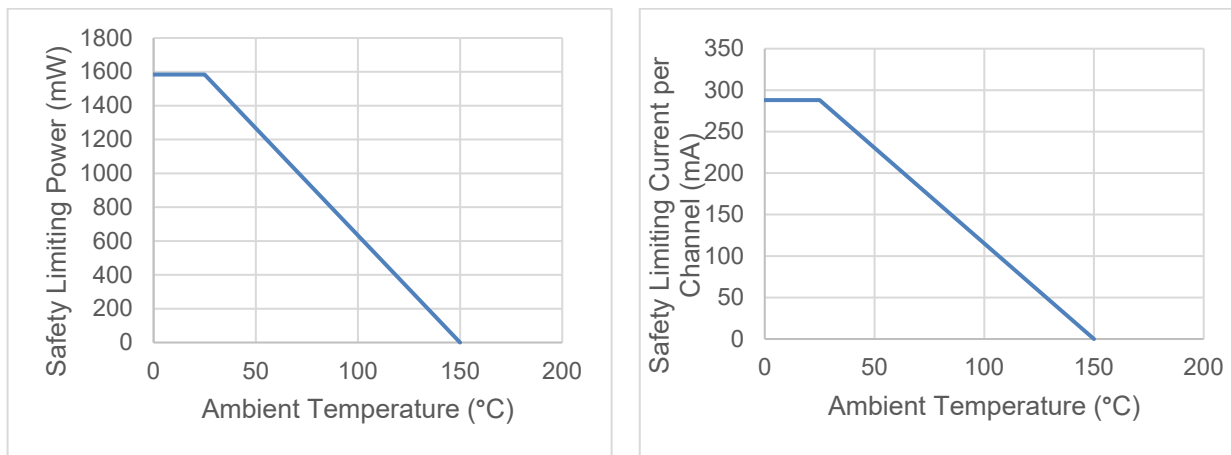


Figure 7.1 NSI832xWx-DSWWAR Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

7.4. Regulatory Information

The NSI832x-DSWWAR are approved by the organizations listed in table.

<i>UL</i>		<i>CQC</i>	<i>TUV</i>	
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to GB4943.1	DIN EN IEC 60747- 17 (VDE 0884-17)	Certified According to EN IEC 62368-1
Single Protection, 7500V _{rms} Isolation voltage	Single Protection, 7500V _{rms} Isolation voltage	Reinforced insulation	Reinforced Insulation V _{IORM} =2828V _{peak} V _{IOTM} =10600V _{peak} V _{IOSM} =12800V _{peak}	7500Vrms for 1min
Pending	Pending	Pending	Pending	Pending

8. Function Description

8.1. Overview

The NSI832x is a Dual-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NSI832x devices are high reliability dual-channel digital isolator. The NSI832x device is safety certified by UL1577 and supports 5kV_{rms} insulation withstand voltage, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI832x is up to 100Mbps, and the common-mode transient immunity (CMTI) is up to 250kV/μs. The NSI832x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI832x device supports to connect with most digital interface directly, making level shifting easy. High system level EMC performance enhances reliability and stability of use.

The NSI832x has a default output status when VDD_{IN} is unready and VDD_{OUT} is ready as shown in Table 8.1, which helps with diagnosis when power is missing at the transmitter side. The output B follows the same status as the input A within 60μs after powering up.

Table 8.1 Output status vs. power status

Input ¹	VDD _{IN} status	VDD _{OUT} status	Output	Comment
H	Ready	Ready	H	Normal operation.
L	Ready	Ready	L	
X	Unready	Ready	L(NSI832xx0) H(NSI832xx1)	The output follows the same status with the input within 60μs after input side VDD _{IN} is powered on.
X	Ready	Unready	Undetermined	The output follows the same status with the input within 60μs after output side VDD _{OUT} is powered on.
Note: H=Logic high; L=Logic low; X=Logic low or logic high; Z=High impedance. VDD _{IN} is input side power; VDD _{OUT} is output side power. (1) There is a protection diode between the input and the VDD _{IN} . When the VDD _{IN} is floating, the strong drive signal through the input pin will put the VDD _{IN} in an indeterminate state.				

8.2. OOK Modulation

NSI832x is based on a capacitive isolation barrier technique and the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, as shown in Figure 8.1, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI.

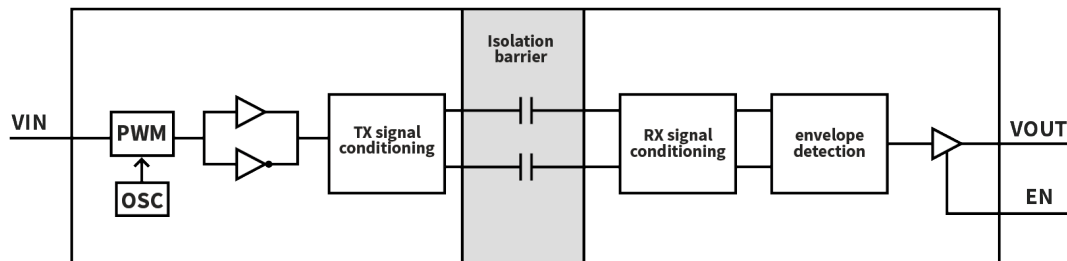


Figure 8.1 Single Channel Function Block Diagram

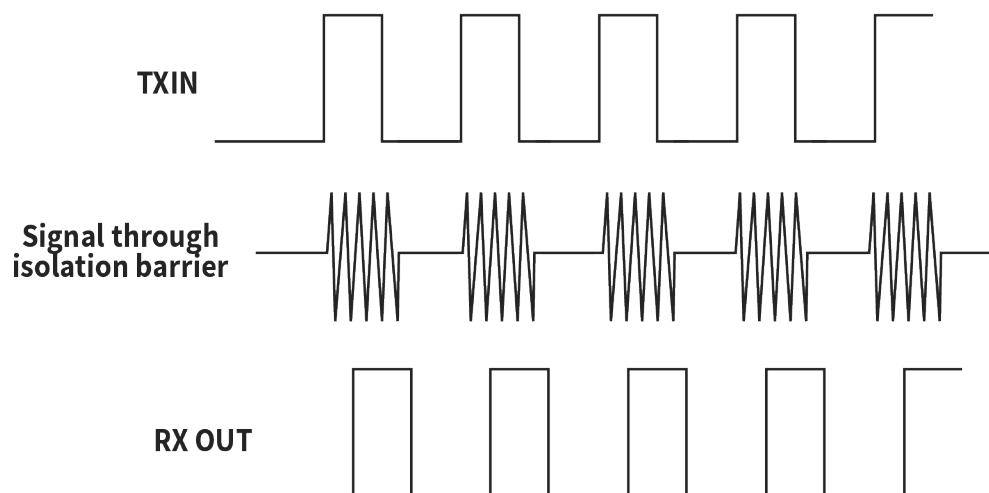


Figure 8.2 OOK Modulation

9. Application Note

9.1. Typical Application Circuit

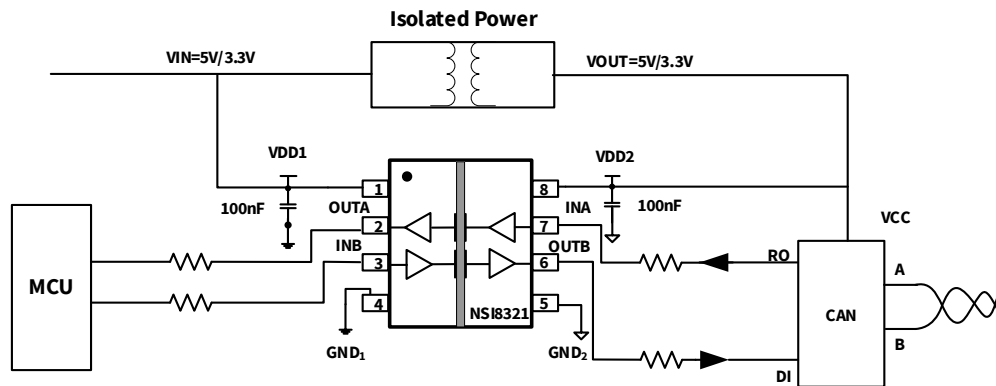


Figure 9.1 Typical SCH for ISO CAN Interface

9.2. PCB Layout

The NSI832x requires a 0.1 μ F bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. Figure 9.2 to Figure 9.3 show the recommended PCB layout, make sure the space under the chip should be kept free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω , $\pm 40\%$. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

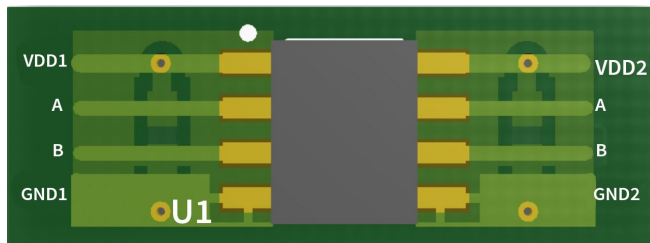


Figure 9.2 Recommended PCB Layout — Top Layer



Figure 9.3 Recommended PCB Layout — Bottom Layer

9.3. High Speed Performance

Figure 9.4 shows the eye diagram of NSI832x at 50Mbps data rate output. The result shows a typical measurement on NSI832x with low jitter and wide open eye characteristics.

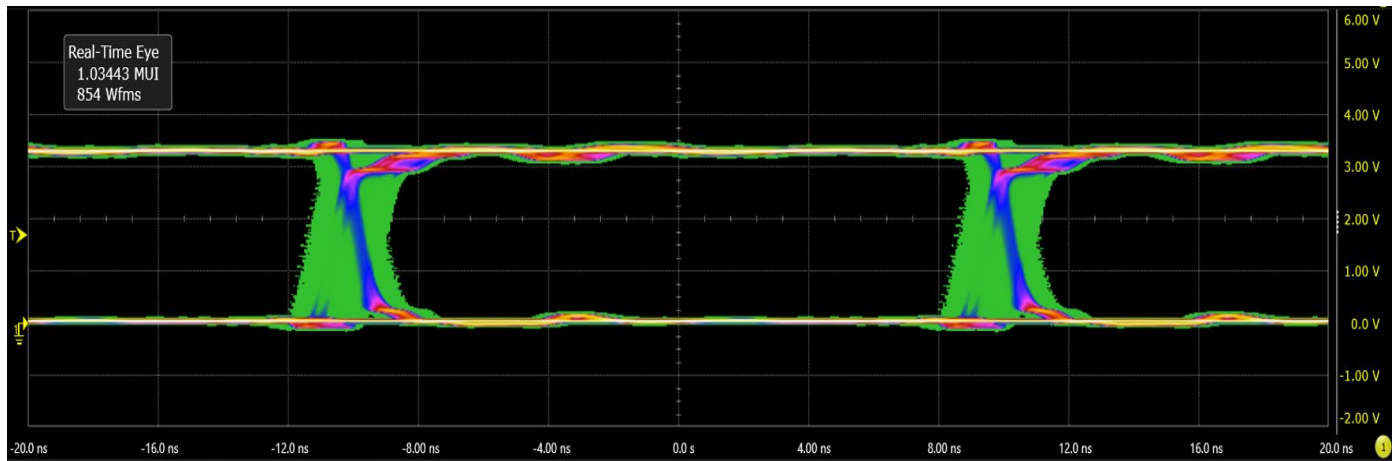
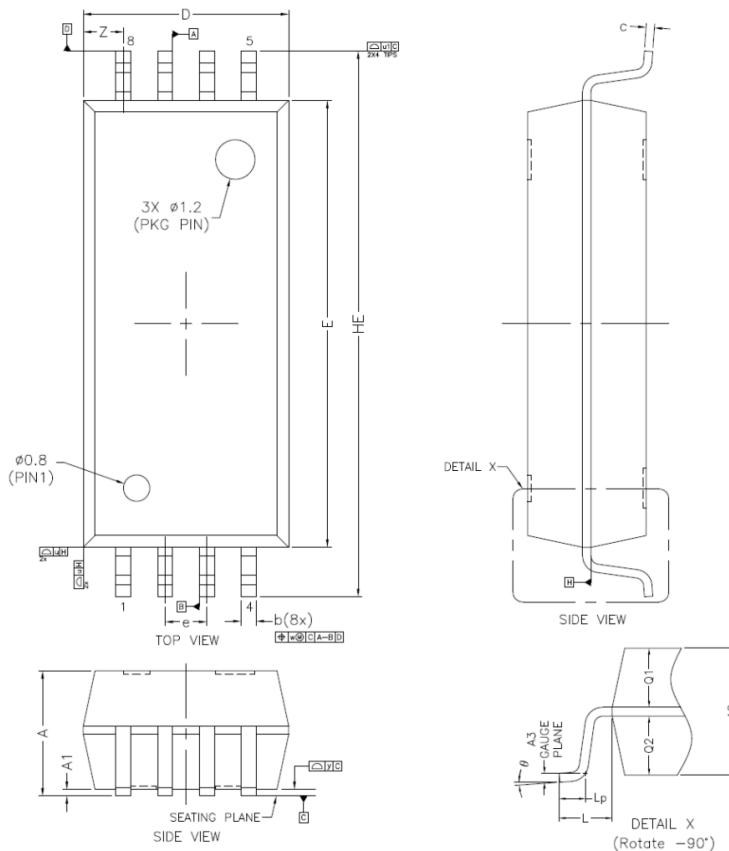


Figure9.4 Eye Diagram at 50Mbps PRBS $2^{16}-1$, 2.5V and 25°C

10. Package Information

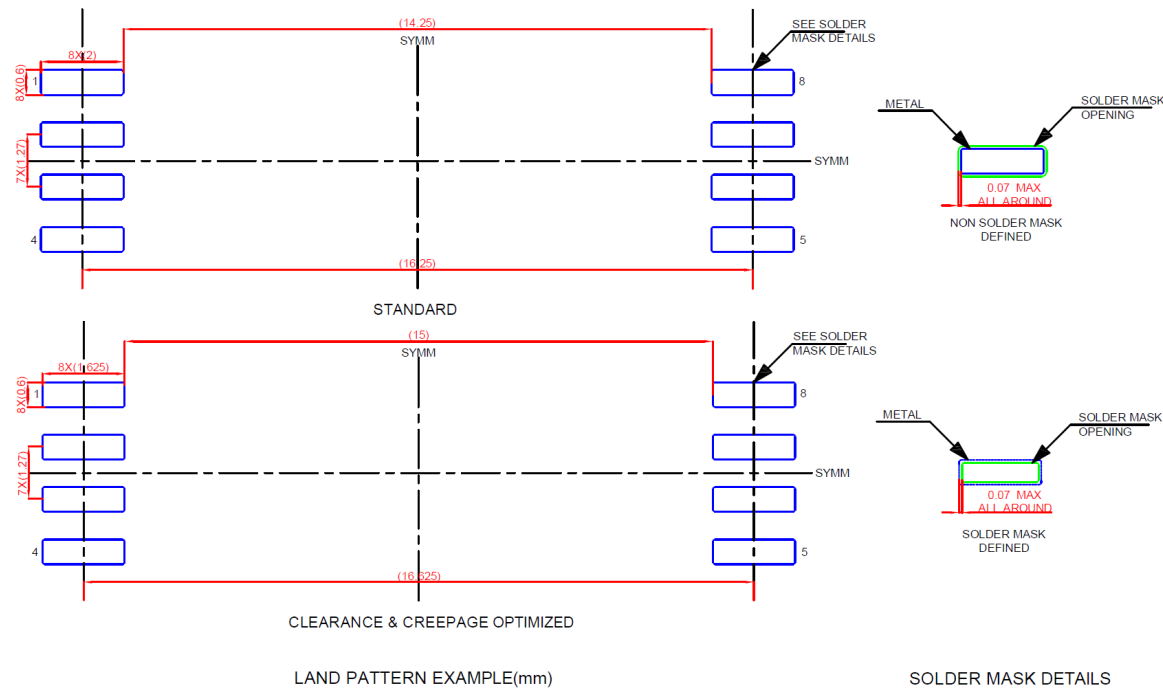


* CONTROLLING DIMENSION : MM

SYMBOL	MM		
	MIN.	NOM.	MAX.
A	3.580	3.807	4.034
A1	0.100	0.200	0.300
A2	3.480	3.607	3.734
b	0.357	0.457	0.557
c	0.254 REF		
D	6.121	6.248	6.375
E	13.473	13.600	13.727
HE	16.36	16.61	16.86
Q1	1.6515	1.6765	1.7015
Q2	1.6515	1.6765	1.7015
e	1.27 BSC		
A3	0.25 REF		
L	1.505 REF		
Lp	0.635	--	--
w	0.25		
y	0.10		
u	0.10		
u1	0.20		
Z	1.219		
θ	0°	--	8°

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.1 SOWW8 Package Shape and Dimension in millimeters

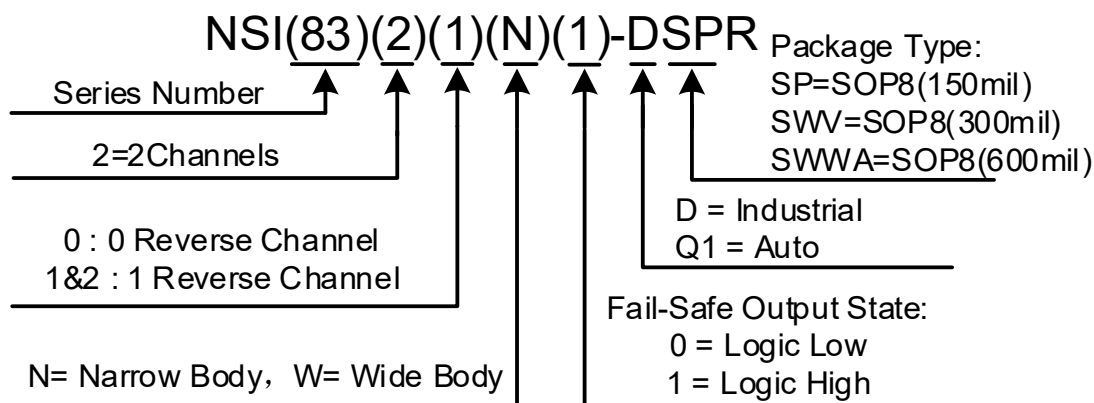


11. Order Information

Part Number	Isolation Rating (kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	MSL	Package Type	Package Drawing	SPQ	MPQ
NSI8320W0 -DSWWAR	7.5	2	0	100	Low	-55 to 125°C	3	SOWW8 (600mil)	SOWW8	1000	1000
NSI8320W1 -DSWWAR	7.5	2	0	100	High	-55 to 125°C	3	SOWW8 (600mil)	SOWW8	1000	1000
NSI8321W0 -DSWWAR	7.5	1	1	100	Low	-55 to 125°C	3	SOWW8 (600mil)	SOWW8	1000	1000
NSI8321W1 -DSWWAR	7.5	1	1	100	High	-55 to 125°C	3	SOWW8 (600mil)	SOWW8	1000	1000
NSI8322W0 -DSWWAR	7.5	1	1	100	Low	-55 to 125°C	3	SOWW8 (600mil)	SOWW8	1000	1000
NSI8322W1 -DSWWAR	7.5	1	1	100	High	-55 to 125°C	3	SOWW8 (600mil)	SOWW8	1000	1000

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.

Part Number Rule:



12. Tape and Reel Information

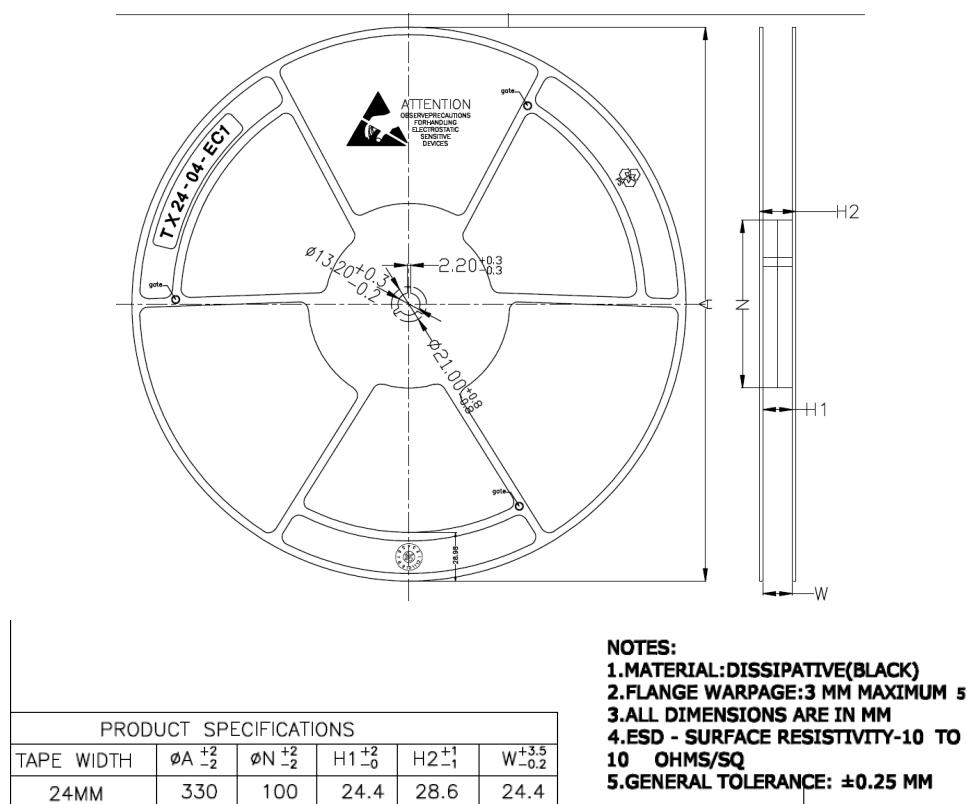


Figure 12.1 Reel Information of SOWW8(600mil)

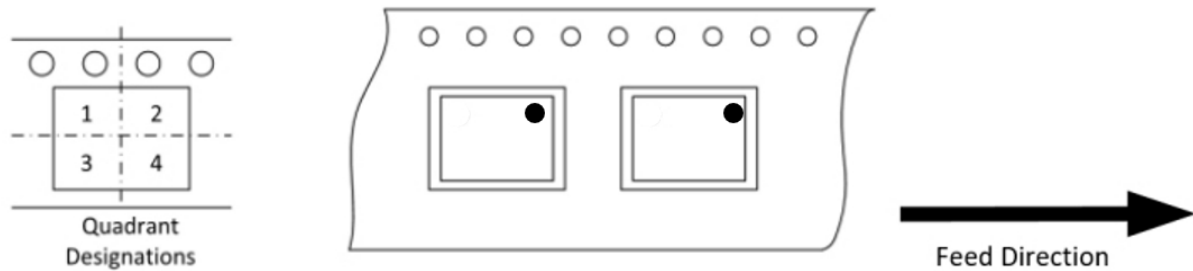
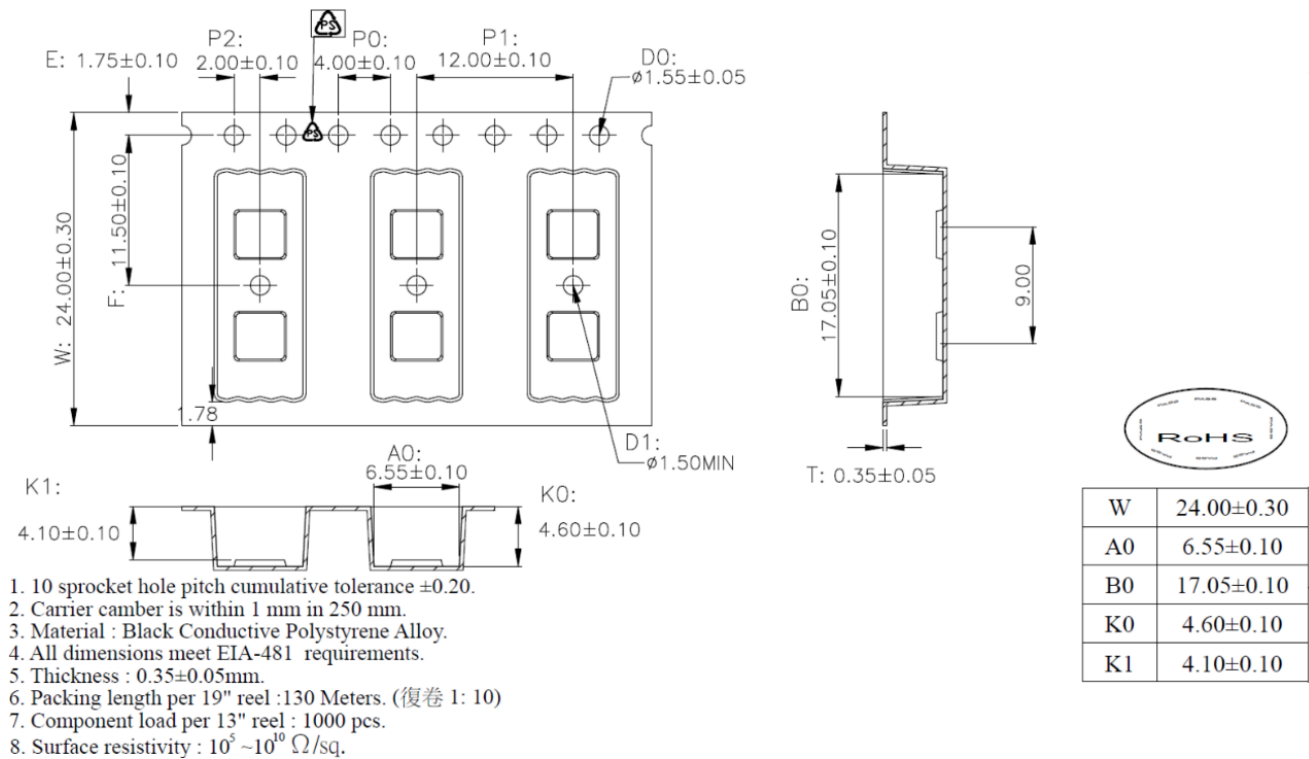


Figure 12.2 Tape Information of SOWW8(600mil)

13. Reflow Profiles

13.1. Classification Temperature

Nonhermetic surface mount devices are classified for Moisture and Reflow temperature sensitivity according the IPC/JEDEC J-STD-020 standard. The Classification Temperature is specified in dependence of package thickness and the package plastic volume. The Pb-Free Process Classification Temperatures (T_c) table in the IPC/JEDEC J-STD-020 standard lists the temperatures, which are shown in Table 13.1.

Table 13.1 Pb-Free Process Classification Temperatures (T_c)

Package Thickness	Volume < 350 mm ³	Volume 350 – 2000 mm ³	Volume >2000 mm ³
< 1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5mm	250°C	245°C	245°C

13.2. Reflow Profile for Pb-Free Soldering

The Classification Profile in the IPC/JEDEC J-STD-020 shows the classification reflow profile to be used for the surface mount device as the below Figure 14.1.

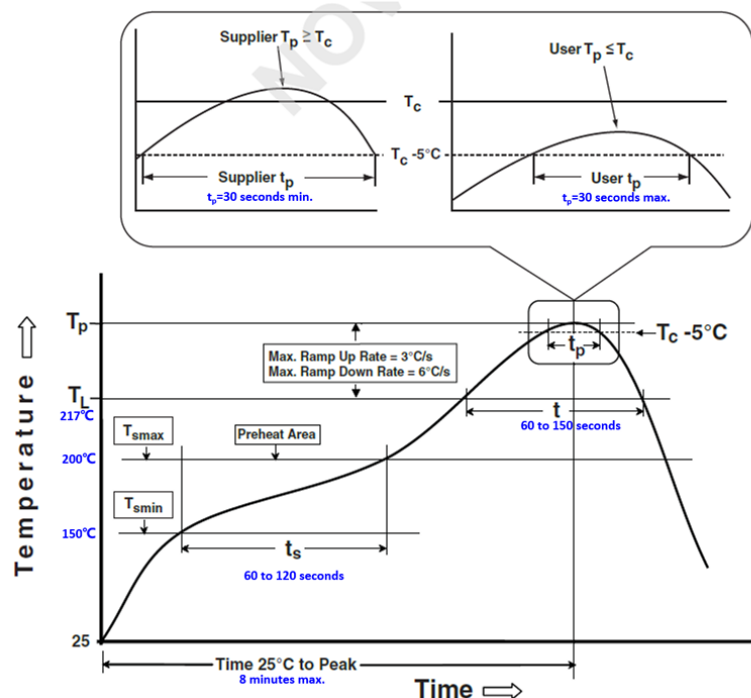


Figure 13.1 Classification Profile (not to scale)

Figure 14.1 illustrates the key temperature/times associated with the different Reflow oven zones. During the Preheat, the board and components are reaching a temperature where the flux in the solder paste is starting its activity.

The Peak temperature (T_p) for the reflow profile, measured at top of the package.

- For the IC supplier: T_p must equal or exceed T_c as shown in Table 13.1.
- For a user: T_p must not exceed T_c as shown in Table 13.1.
- Time that defines the peak temperate (t_p) starts/ends -5°C below T_c .

14. Revision History

<i>Revision</i>	<i>Description</i>	<i>Date</i>
1.0	Initial version	2026/7/10

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