

Product Overview

The NSI8310-Q1 devices are high reliability Single-channel digital isolators. The NSI8310 device is safety certified by UL1577 and supports 5kVrms insulation withstand voltage, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI8310 is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 250kV/μs. The NSI8310 device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI8310-Q1 device support connecting with most digital interfaces directly, making level shifting easy. High system level EMC performance enhances reliability and stability of use. AEC-Q100 (Grade 1) option is provided for all devices.

Key Features

- Up to 5000V_{rms} Insulation voltage
- Data rate: DC to 150Mbps
- Power supply voltage: 2.5V to 5.5V
- High CMTI: 250kV/μs
- Chip level ESD: HBM: ±8kV
- Robust EMC Reinforced Single-Channel Digital Isolators for SOW8 wide body
- Default output high level or low level option
- Isolation surge voltage: >10kV
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <18ns
- Operation temperature: -40°C~125°C
- RoHS-compliant packages:
 - SOP8 narrow body
 - SOW8 wide body

Safety Regulatory Approvals

- UL recognition: up to 5000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor control

Device Information

Part Number	Package	Body Size
NSI8310Nx-Q1SPR	SOP8	4.90mm × 3.90mm
NSI8310Wx-Q1SWVR	SOW8	5.85mm × 7.50mm

Functional Block Diagrams

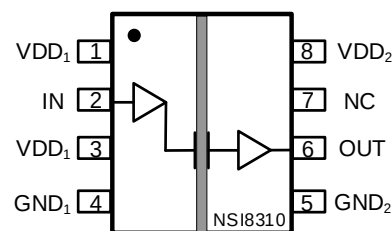


Figure 1.1 NSI8310 Block Diagram

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1. Pin Configuration and Functions

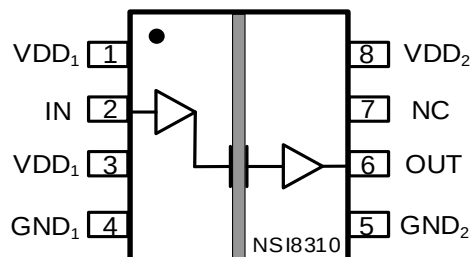


Figure 1.1 NSI8310 Package

Table1.1 NSI8310 Pin Configuration and Description

NSI8310 PIN NO.	SYMBOL	FUNCTION
1	VDD1	Power Supply for Isolator Side 1
2	IN	Logic Input
3	VDD1	Power Supply for Isolator Side 1
4	GND1	Ground 1, the ground reference for Isolator Side 1
5	GND2	Ground 2, the ground reference for Isolator Side 2
6	OUT	Logic Output
7	NC	Not connect pin; it has no internal connection
8	VDD2	Power Supply for Isolator Side 2

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	IN	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Output Voltage	OUT	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Input/Output Pulse Voltage	IN, OUT	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Output current	Io	-15		15	mA	
Operating Temperature	Topr	-40		125	°C	
Junction Temperature	Tj			150	°C	
Storage Temperature	Tstg	-65		150	°C	

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating conditions. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.
- (2) Power supply voltage and input/output voltage are respect to the local ground terminal (GND1 or GND2) voltage values.

3. ESD Ratings

Parameters	Ratings	Value	Unit
Electrostatic discharge (ESD)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽²⁾	±8000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽³⁾	±2000	V

- (1) Though this device features proprietary protection circuitry, proper ESD precautions should be considered to avoid performance degradation or damage due to high energy ESD event. Charged devices and circuit boards may discharge without detection.
- (2) Safe manufacturing requires 500-V HBM and standard ESD precautions, per JEDEC document JEP155.
- (3) Safe manufacturing requires 250-V CDM and standard ESD precautions, per JEDEC document JEP157.

4. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit
Power Supply Voltage	VDD1, VDD2	2.5		5.5	V

Operating Temperature	Topr	-40		125	°C
High Level Input Voltage	VIH	0.7*VDD			V
Low Level Input Voltage	VIL			0.3*VDD	V
Data rate	DR			150	Mbps

5. Thermal Characteristics

Parameters	Symbol	SOP8	SOW8	Unit
IC Junction-to-Air Thermal Resistance	R _{θJA}	137.7	84.3	°C/W
Junction-to-case (top) thermal resistance	R _{θJC (top)}	54.9	36.3	°C/W
Junction-to-board thermal resistance	R _{θJB}	71.7	47.0	°C/W
Junction-to-top characterization parameter	Ψ _{JT}	7.6	9.6	°C/W
Junction-to-board characterization parameter	Ψ _{JB}	31.0	29.2	°C/W

6. Specifications

6.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power on Reset	VDDPOR ⁽¹⁾	2	2.2	2.4	V	POR threshold as during power-up
	VDDHYS ⁽¹⁾		0.1		V	POR threshold Hysteresis
Rising input switching threshold	V _{IT+} ⁽¹⁾		0.6*VDD	0.7*VDD	V	
Falling input switching threshold	V _{IT-} ⁽¹⁾	0.3*VDD	0.4*VDD		V	
Input threshold voltage hysteresis	V _{IT_HYS} ⁽¹⁾		0.2*VDD		V	
High Level Output Voltage	V _{OH}	VDD-0.4			V	I _{OH} ≤ 4mA
Low Level Output Voltage	V _{OL}			0.4	V	I _{OL} ≤ 4mA
Output Impedance	R _{out} ⁽¹⁾		50		ohm	
Input Pull high or low Current	I _{pull}		5	10	μA	

	NSI8310Nx					
Start Up Time after POR	trbs ⁽²⁾		15	30	μs	
Common Mode Transient Immunity	CMTI	±150	±200		kV/μs	See Figure 6.10
	NSI8310Wx					
Start Up Time after POR	trbs ⁽²⁾		22	32	μs	
Common Mode Transient Immunity	CMTI	±200	±250		kV/μs	See Figure 6.10
⁽¹⁾ Not test covered, guaranteed by characterization.						
⁽²⁾ Not test covered, guaranteed by design.						

6.2. Supply Current Characteristics –5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSI8310Nx					
	I _{DD1} (Q0)		0.62	0.90	mA	All Input 0V for NSI8310N0 Or All Input at supply for NSI8310N1
	I _{DD2} (Q0)		1.25	1.84	mA	
	I _{DD1} (Q1)		1.51	2.19	mA	All Input at supply for NSI8310N0 Or All Input 0V for NSI8310N1
	I _{DD2} (Q1)		1.27	1.73	mA	
	I _{DD1} (1M)		1.08	1.45	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		1.33	1.76	mA	
	I _{DD1} (10M)		1.32	1.75	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		2.05	2.75	mA	
	I _{DD1} (100M)		1.45	1.96	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		8.18	11.04	mA	
	NSI8310Wx					
	I _{DD1} (Q0)		0.79	1.15	mA	All Input 0V for NSI8310W0 Or All Input at supply for NSI8310W1
	I _{DD2} (Q0)		1.84	2.67	mA	
	I _{DD1} (Q1)		2.11	2.79	mA	All Input at supply for NSI8310W0 Or All Input 0V for NSI8310W1
	I _{DD2} (Q1)		1.95	2.56	mA	
	I _{DD1} (1M)		1.50	2.62	mA	All Input with 1Mbps,

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I _{DD2} (1M)		1.88	2.48	mA	C _L =15pF
	I _{DD1} (10M)		2.00	2.63	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		2.44	3.05	mA	
	I _{DD1} (100M)		2.23	2.94	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		7.56	9.98	mA	

6.3. Supply Current Characteristics –3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 3.3V**, **VDD2 = 3.3V**, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSI8310Nx					
	I _{DD1} (Q0)		0.60	0.88	mA	All Input 0V for NSI8310N0 Or All Input at supply for NSI8310N1
	I _{DD2} (Q0)		1.22	1.79	mA	
	I _{DD1} (Q1)		1.46	2.12	mA	All Input at supply for NSI8310N0 Or All Input 0V for NSI8310N1
	I _{DD2} (Q1)		1.22	1.67	mA	
	I _{DD1} (1M)		1.03	1.39	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		1.27	1.71	mA	
	I _{DD1} (10M)		1.27	1.71	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		1.82	2.44	mA	
	I _{DD1} (100M)		1.39	1.88	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		6.06	8.18	mA	
	NSI8310Wx					
	I _{DD1} (Q0)		0.77	1.12	mA	All Input 0V for NSI8310W0 Or All Input at supply for NSI8310W1
	I _{DD2} (Q0)		1.80	2.61	mA	
	I _{DD1} (Q1)		2.08	2.75	mA	All Input at supply for NSI8310W0 Or All Input 0V for NSI8310W1
	I _{DD2} (Q1)		1.91	2.51	mA	
	I _{DD1} (1M)		1.44	1.90	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		1.84	2.43	mA	
	I _{DD1} (10M)		1.46	1.93	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		2.21	2.89	mA	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I _{DD1} (100M)		1.67	2.19	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		5.60	7.56	mA	

6.4. Supply Current Characteristics–2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSI8310Nx					
	I _{DD1} (Q0)		0.58	0.85	mA	All Input 0V for NSI8310N0 Or All Input at supply for NSI8310N1
	I _{DD2} (Q0)		1.19	1.74	mA	
	I _{DD1} (Q1)		1.42	1.87	mA	All Input at supply for NSI8310N0 Or All Input 0V for NSI8310N1
	I _{DD2} (Q1)		1.20	1.68	mA	
	I _{DD1} (1M)		1.00	1.33	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		1.23	1.62	mA	
	I _{DD1} (10M)		1.26	1.66	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		1.72	2.25	mA	
	I _{DD1} (100M)		1.38	1.86	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		4.50	6.08	mA	
	NSI8310Wx					
	I _{DD1} (Q0)		0.75	1.08	mA	All Input 0V for NSI8310W0 Or All Input at supply for NSI8310W1
	I _{DD2} (Q0)		1.77	2.56	mA	
	I _{DD1} (Q1)		2.05	2.71	mA	All Input at supply for NSI8310W0 Or All Input 0V for NSI8310W1
	I _{DD2} (Q1)		1.88	2.48	mA	
	I _{DD1} (1M)		1.41	1.86	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		1.30	1.71	mA	
	I _{DD1} (10M)		1.43	1.87	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		1.58	2.09	mA	
	I _{DD1} (100M)		1.64	2.16	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		4.16	5.62	mA	

6.5. Switching Characteristics - 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
NSI8310Nx						
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t _{PLH}		9.9	18	ns	See Figure 6.9 , C _L = 15pF
	t _{PHL}		8.7	18	ns	See Figure 6.9 , C _L = 15pF
NSI8310Wx						
Data Rate	DR	0		100	Mbps	
Minimum Pulse Width	PW			8.3	ns	
Propagation Delay	t _{PLH}		12.5	18	ns	See Figure 6.9 , C _L = 15pF
	t _{PHL}		12.1	18	ns	See Figure 6.9 , C _L = 15pF
NSI8310Nx / NSI8310Wx						
Pulse Width Distortion t _{PHL} - t _{PLH}	PWD			5.0	ns	See Figure 6.9 , C _L = 15pF
Rising Time	t _r			5.0	ns	See Figure 6.9 , C _L = 15pF
Falling Time	t _f			5.0	ns	See Figure 6.9 , C _L = 15pF
Peak Eye Diagram Jitter	t _{JIT(PK)}		2.5		ns	
Channel-to-Channel Delay Skew	t _{SK(c2c)}			2.5	ns	
Part-to-Part Delay Skew	t _{SK(p2p)}			5.0	ns	

6.6. Switching Characteristics - 3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
NSI8310Nx						
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t _{PLH}		10.8	19	ns	See Figure 6.9 , C _L = 15pF

	t_{PHL}		9.6	19	ns	See Figure 6.9 , $C_L = 15pF$
NSI8310Wx						
Data Rate	DR	0		100	Mbps	
Minimum Pulse Width	PW			8.3	ns	
Propagation Delay	t_{PLH}		13.0	19	ns	See Figure 6.9 , $C_L = 15pF$
	t_{PHL}		12.5	19	ns	See Figure 6.9 , $C_L = 15pF$
NSI8310Nx / NSI8310Wx						
Pulse Width Distortion $ t_{PHL} - t_{PLH} $	PWD			5.0	ns	See Figure 6.9 , $C_L = 15pF$
Rising Time	t_r			5.0	ns	See Figure 6.9 , $C_L = 15pF$
Falling Time	t_f			5.0	ns	See Figure 6.9 , $C_L = 15pF$
Peak Eye Diagram Jitter	$t_{JIT(PK)}$		2.5		ns	
Channel-to-Channel Delay Skew	$t_{SK(c2c)}$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK(p2p)}$			5.0	ns	

6.7. Switching Characteristics - 2.5V Supply

($V_{DD1}=2.5V \pm 10\%$, $V_{DD2}=2.5V \pm 10\%$, $T_a=-40^{\circ}C$ to $125^{\circ}C$. Unless otherwise noted, Typical values are at **VDD1 = 2.5V**, **VDD2 = 2.5V**, $T_a = 25^{\circ}C$)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
NSI8310Nx						
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}		12.0	20	ns	See Figure 6.9 , $C_L = 15pF$
	t_{PHL}		11.0	20	ns	See Figure 6.9 , $C_L = 15pF$
NSI8310Wx						
Data Rate	DR	0		100	Mbps	
Minimum Pulse Width	PW			8.3	ns	
Propagation Delay	t_{PLH}		14.2	20	ns	See Figure 6.9 , $C_L = 15pF$
	t_{PHL}		13.5	20	ns	See Figure 6.9 , $C_L = 15pF$
NSI8310Nx / NSI8310Wx						
Pulse Width Distortion	PWD			5.0	ns	See Figure 6.9 , $C_L = 15pF$

$ t_{PHL} - t_{PLH} $						
Rising Time	t_r			5.0	ns	See Figure 6.9 , $C_L = 15pF$
Falling Time	t_f			5.0	ns	See Figure 6.9 , $C_L = 15pF$
Peak Eye Diagram Jitter	$t_{JIT(PK)}$		2.5		ns	
Channel-to-Channel Delay Skew	$t_{SK(c2c)}$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK(p2p)}$			5.0	ns	

6.8. Typical Performance Characteristics

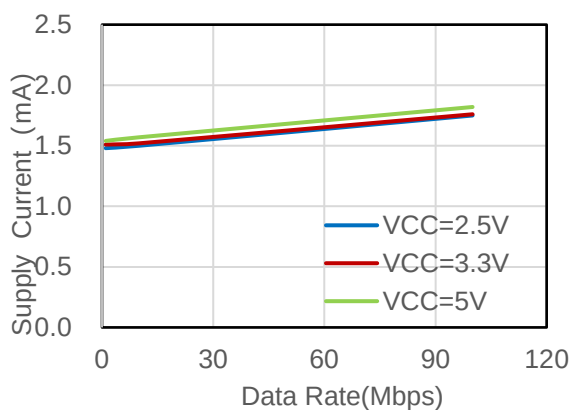


Figure 6.1 NSI8310Nx VDD1 Supply Current vs Data Rate

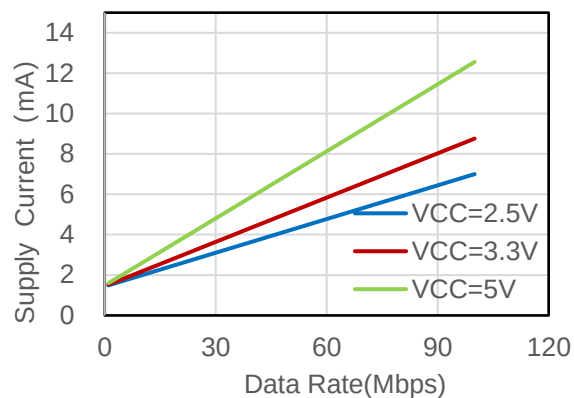


Figure 6.2 NSI8310Nx VDD2 Supply Current vs Data Rate

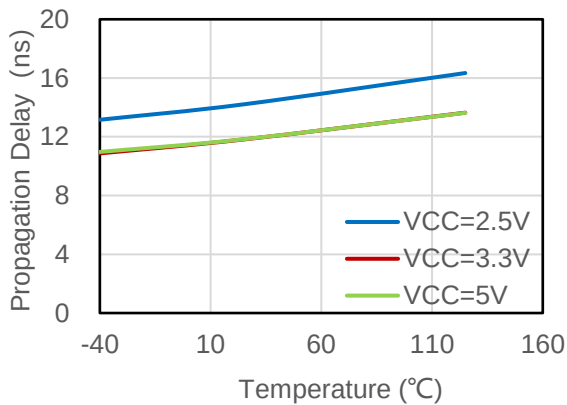


Figure 6.3 NSI8310Nx Rising Edge Propagation Delay Vs Temp

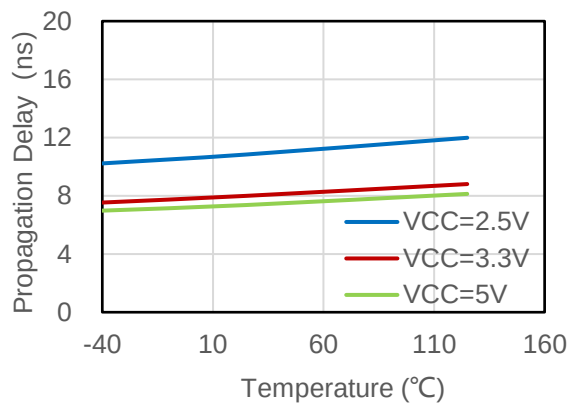


Figure 6.4 NSI8310Nx Falling Edge Propagation Delay Vs Temp

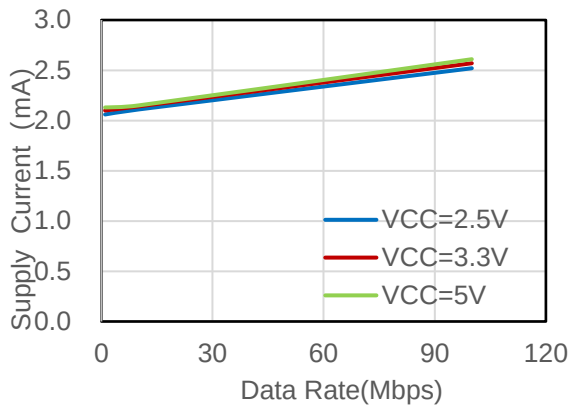


Figure 6.5 NSI8310Wx VDD1 Supply Current vs Data Rate

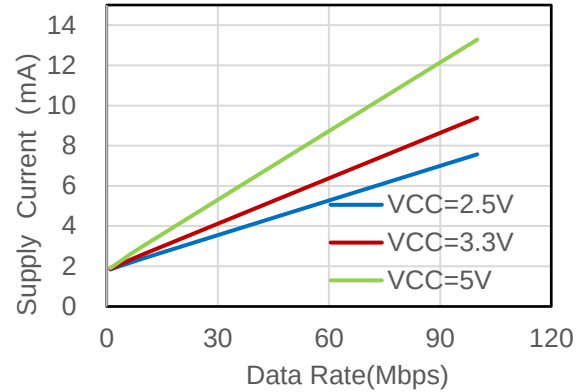


Figure 6.6 NSI8310Wx VDD2 Supply Current vs Data Rate

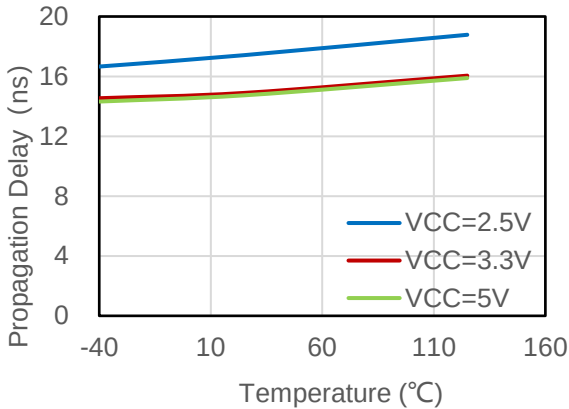


Figure 6.7 NSI8310Wx Rising Edge Propagation Delay Vs Temp

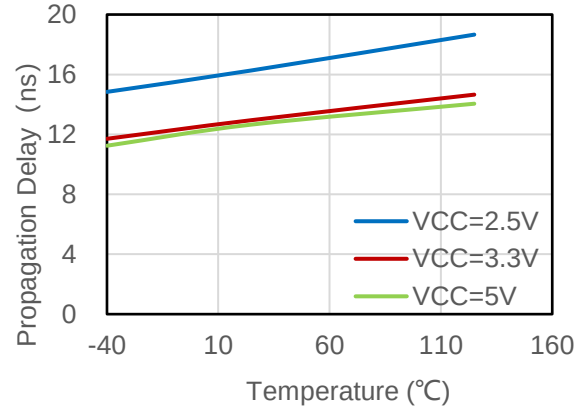
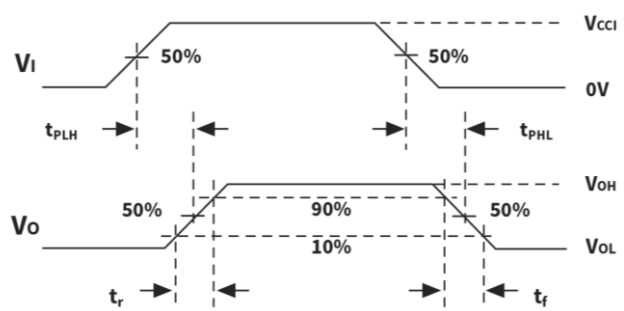
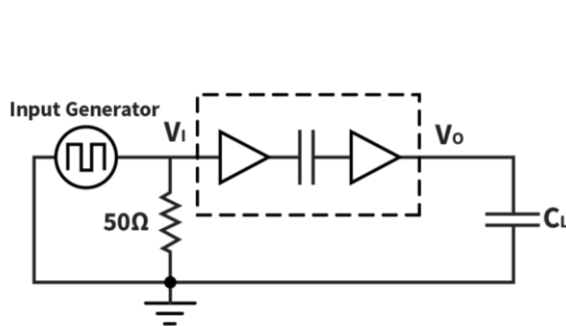


Figure 6.8 NSI8310Wx Falling Edge Propagation Delay Vs Temp

6.9. Parameter Measurement Information



(1) Input Generator Characteristics : PRR $\leq$ 50kHz, $t_r \leq$ 3ns, $t_f \leq$ 3ns, Duty cycle = 50%, $Z_o = 50 \Omega$.

Figure 6.9 Switching Characteristics Test Circuit and Waveform

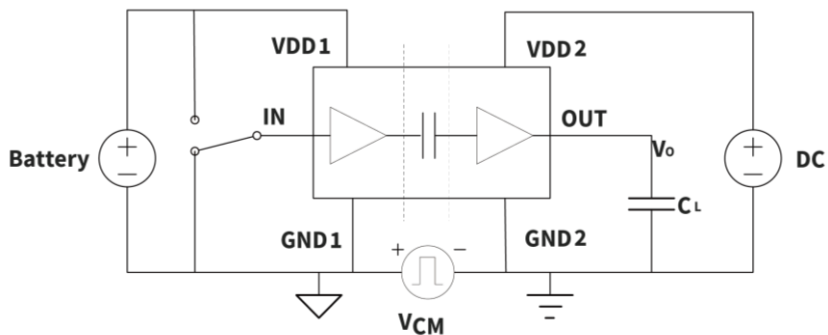


Figure 6.10 Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value		Unit	Comments
		SOP8	SOW8		
Minimum External Clearance	CLR	4.0	8.0	mm	IEC 60664-1
Minimum External Creepage	CPG	4.0	8.0	mm	IEC 60664-1
Distance Through Insulation	DTI	10	24	μm	
Tracking Resistance (Comparative Tracking Index)	CTI	>600	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I	I		IEC 60664-1

Description	Test Condition	Value	
		SOP8	SOW8
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	I to IV	I to IV
	For Rated Mains Voltage ≤ 300Vrms	I to III	I to IV
	For Rated Mains Voltage ≤ 600Vrms	I to II	I to IV
	For Rated Mains Voltage ≤ 1000Vrms	I	I to III
Climatic Classification		40/125/21	40/125/21
Pollution Degree per DIN VDE 0110,		2	2

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value		Unit
			SOP8	SOW8	
Maximum repetitive isolation voltage		V_{IORM}	565	2121	V_{PEAK}
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	400	1500	V_{RMS}
	DC voltage		565	2121	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, $t_{ini}=60\text{ s}$, $V_{pd(m)}=1.2*V_{IORM}$, $t_m=10\text{ s}$.	Q_{pd}		<5	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, $t_{ini}=60\text{ s}$, $V_{pd(m)}=1.6*V_{IORM}$, $t_m=10\text{ s}$				pC
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}$, $t_{ini}=1\text{ s}$ $V_{pd(m)}=1.875*V_{IORM}$, $t_m=1\text{ s}$ (method b1) or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$ (method b2)				pC
	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, $t_{ini}=60\text{ s}$, $V_{pd(m)}=1.2*V_{IORM}$, $t_m=10\text{ s}$.	Q_{pd}	<5		pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, $t_{ini}=60\text{ s}$, $V_{pd(m)}=1.3*V_{IORM}$, $t_m=10\text{ s}$				pC
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}$, $t_{ini}=1\text{ s}$ $V_{pd(m)}=1.5*V_{IORM}$, $t_m=1\text{ s}$ (method b1) or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$ (method b2)				pC
Maximum transient isolation voltage	$t=60\text{ sec}$	V_{IOTM}	5300	8000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50- μs waveform per IEC62368-1	V_{IMP}	5384	6250	V_{PEAK}

Description	Test Condition	Symbol	Value		Unit
			SOP8	SOW8	
Maximum Surge Isolation Voltage	Test method per IEC60065, 1.2/50 μ s waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$	V_{IOSM}	7000	10000	V_{PEAK}
Isolation resistance	$V_{IO} = 500V$, $T_{amb} = 25^{\circ}C$	R_{IO}	$>10^{12}$	$>10^{12}$	Ω
	$V_{IO} = 500V$, $100^{\circ}C \leq T_{amb} \leq 125^{\circ}C$		$>10^{11}$	$>10^{11}$	Ω
	$V_{IO} = 500V$, $T_{amb} = T_s$		$>10^9$	$>10^9$	Ω
Isolation capacitance	$f = 1MHz$	C_{IO}	0.6	0.6	pF
Withstand Isolation Voltage	$V_{TEST} = V_{ISO}$, $t = 60$ s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, $t = 1$ s (100% production test)	V_{ISO}	3750	5000	V_{RMS}

7.3. Safety-Limiting Values

Basic isolation safety-limiting values as outlined in VDE-0884-17 of NSI8310Nx SOP8(150mil)

Description	Test Condition	Symbol	Value	Unit
Safety Supply Power	$R_{\theta JA} = 137.7^{\circ}C/W^{1)}$, $T_J = 150^{\circ}C$, $T_A = 25^{\circ}C$		908	mW
Safety Supply Current	$R_{\theta JA} = 137.7^{\circ}C/W^{1)}$, $V_I = 5.5$ V, $T_J = 150^{\circ}C$, $T_A = 25^{\circ}C$		165	mA
Safety Temperature ²⁾		T_s	150	$^{\circ}C$

- 1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP8(150mil) package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

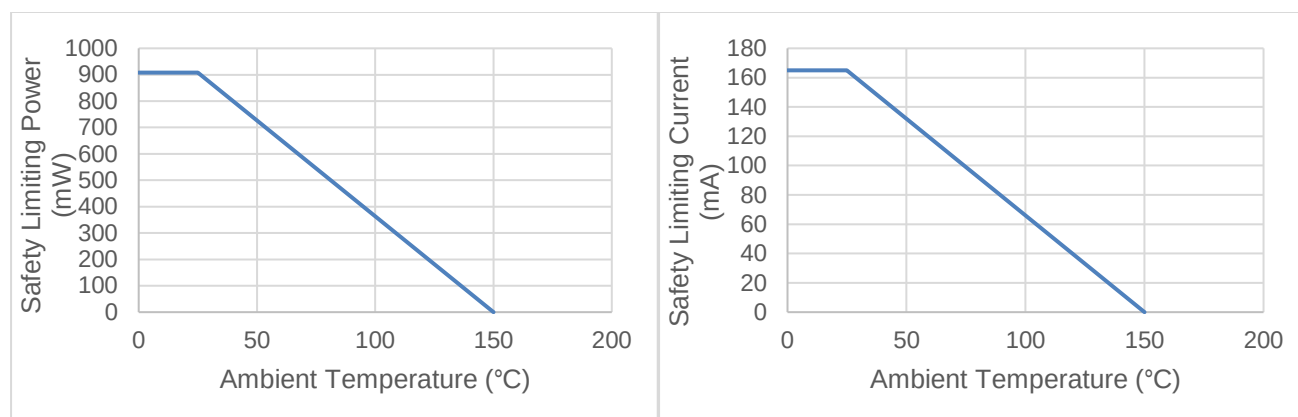


Figure 7.1 NSI8310Nx Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI8310Wx SOW8(300mil)

Description	Test Condition	Symbol	Value	Unit
Safety Supply Power	$R_{\theta JA} = 84.3 \text{ }^{\circ}\text{C/W}^{(1)}$, $V_I = 5.5 \text{ V}$, $T_J = 150 \text{ }^{\circ}\text{C}$, $T_A = 25 \text{ }^{\circ}\text{C}$		1483	mW
Safety Supply Current	$R_{\theta JA} = 84.3 \text{ }^{\circ}\text{C/W}^{(1)}$, $T_J = 150 \text{ }^{\circ}\text{C}$, $T_A = 25 \text{ }^{\circ}\text{C}$		269.6	mA
Safety Temperature ²⁾		T_s	150	$^{\circ}\text{C}$

- 1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOW8(300mil) package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

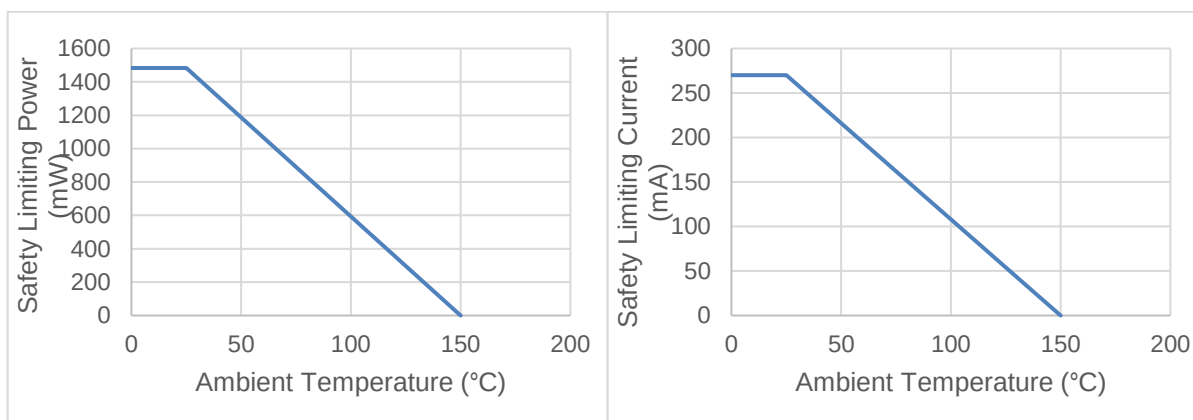


Figure 7.2 NSI8310Wx Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17

7.4. Regulatory Information

The NSI8310Nx-Q1SPR are approved by the organizations listed in table.

<i>UL</i>		<i>CQC</i>		<i>TUV</i>
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to GB4943.1	DIN EN IEC 60747- 17 (VDE 0884-17)	Certified According to EN IEC 62368-1
Single Protection, 3750V _{rms} Isolation voltage	Single Protection, 3750V _{rms} Isolation voltage	Basic Insulation	Basic insulation V _{IORM} =990V _{peak} V _{IOTM} =5300V _{peak} V _{IOSM} =8000V _{peak}	3000Vrms for 1min
E500602	E500602	CQC20001264940	40057024	R 50574061

The NSI8310Wx-Q1SWVR are approved by the organizations listed in table.

<i>UL</i>		<i>CQC</i>		<i>TUV</i>
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to GB4943.1	DIN EN IEC 60747- 17 (VDE 0884-17)	Certified According to EN IEC 62368-1
Single Protection, 5000V _{rms} Isolation voltage	Single Protection, 5000V _{rms} Isolation voltage	Reinforced Insulation	Reinforced insulation V _{IORM} =2121V _{peak} V _{IOTM} =8000V _{peak} V _{IOSM} =10000V _{peak}	5000Vrms for 1min
E500602	E500602	CQC20001264938	R 50632560	R 50574061

8. Function Description

8.1. Overview

The NSI8310-Q1 is a Single-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NSI8310 devices are high reliability Single-channel digital isolators. The NSI8310-Q1 device is safety certified by UL1577 and supports 5kV_{rms} insulation withstand voltage, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI8310 is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 250kV/μs. The NSI8310 device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI8310 device supports connecting with most digital interfaces directly, making level shifting easy. High system level EMC performance enhances reliability and stability of use.

The NSI8310 has a default output status when VDD_{IN} is unready and VDD_{OUT} is ready as shown in Table 8.1, which helps with diagnosis when power is missing at the transmitter side. The output B follows the same status as the input A within 60μs after powering up.

Table 8.1 Output status vs. power status

<i>Input¹</i>	<i>VDD_{IN} status</i>	<i>VDD_{OUT} status</i>	<i>Output</i>	<i>Comment</i>
H	Ready	Ready	H	Normal operation.
L	Ready	Ready	L	
X	Unready	Ready	L(NSI8310x0) H(NSI8310x1)	The output follows the same status with the input within 60μs after input side VDD _{IN} is powered on.
X	Ready	Unready	Undetermined	The output follows the same status with the input within 60μs after output side VDD _{OUT} is powered on.
Note: H=Logic high; L=Logic low; X=Logic low or logic high; Z=High impedance. VDD _{IN} is input side power; VDD _{OUT} is output side power. (1) There is a protection diode between the input and the VDD _{IN} . When the VDD _{IN} is floating, the strong drive signal through the input pin will put the VDD _{IN} in an indeterminate state.				

8.2. OOK Modulation

NSI8310-Q1 is based on a capacitive isolation barrier technique and the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, as shown in Figure 8.1, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI.

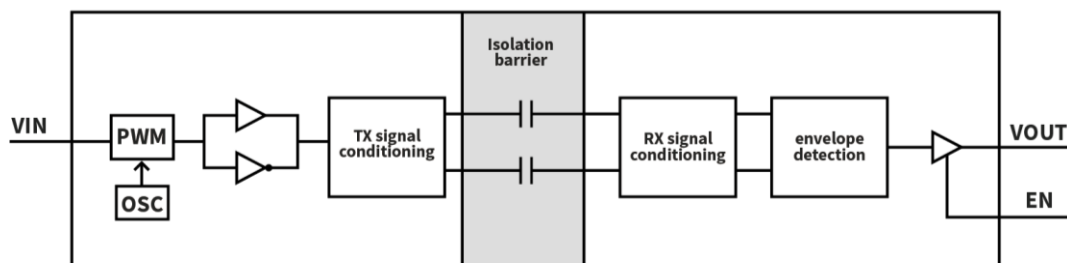


Figure 8.1 Single Channel Function Block Diagram

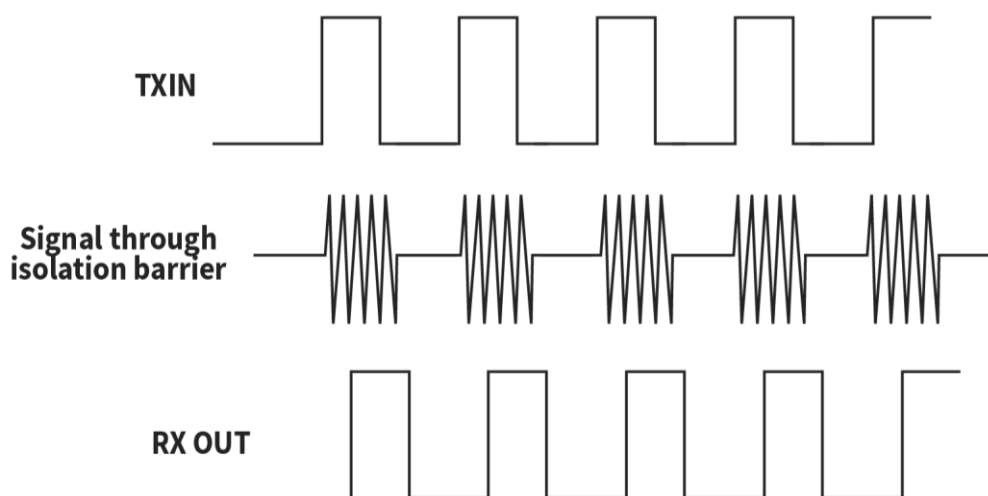


Figure 8.2 OOK Modulation

9. Application Note

9.1. Typical Application Circuit

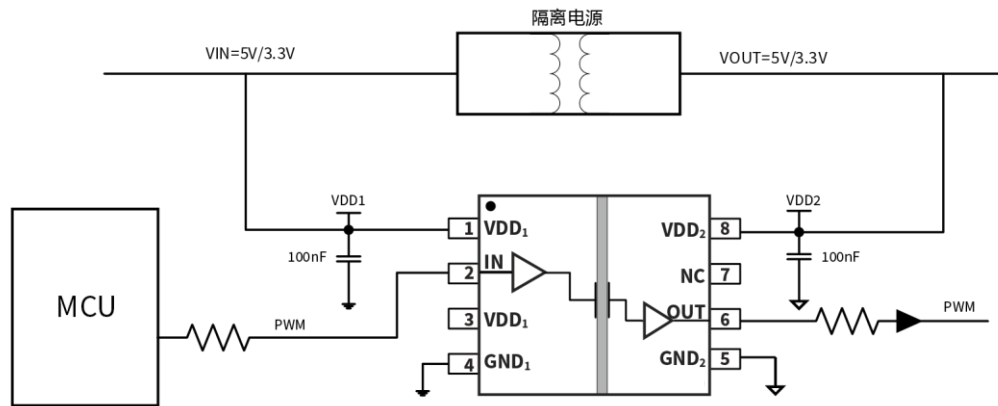


Figure 9.1 Typical PWM isolation circuit

9.2. PCB Layout

The NSI8310 requires a 0.1 μF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. Figure 9.2 to Figure 9.3 show the recommended PCB layout, make sure the space under the chip should be kept free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω , $\pm 40\%$. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

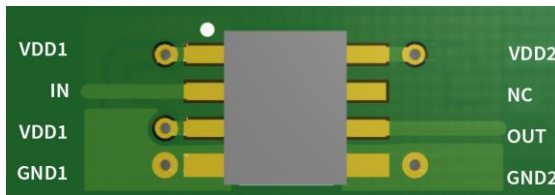


Figure 9.2 Recommended PCB Layout — Top Layer



Figure 9.3 Recommended PCB Layout — Bottom Layer

9.3. High Speed Performance

Figure 9.4 shows the eye diagram of NSI8310 at 50Mbps data rate output. The result shows a typical measurement on NSI8310 with low jitter and wide open eye characteristics.

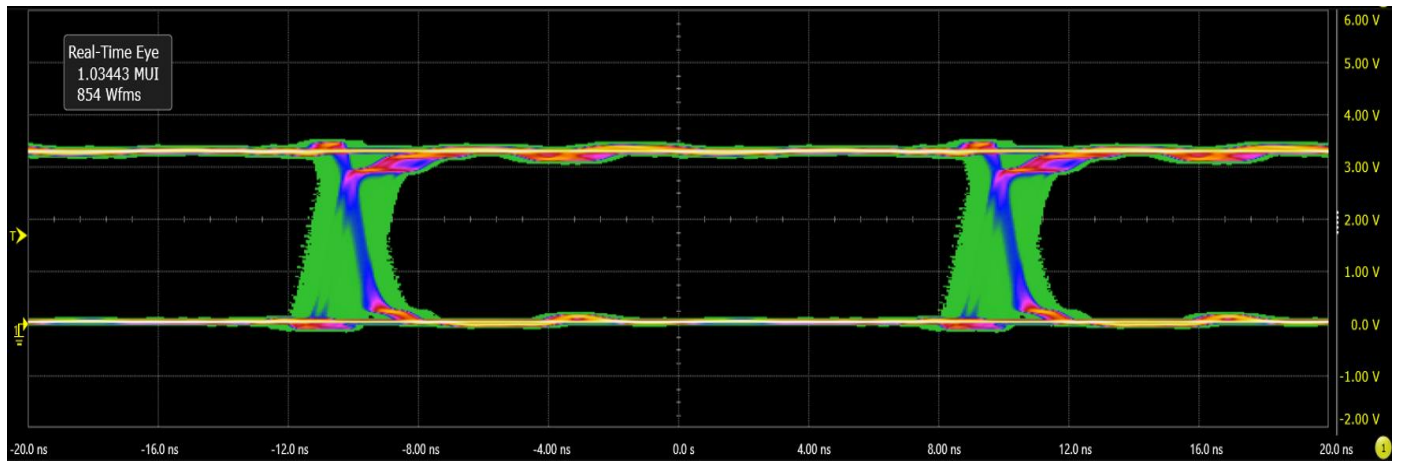
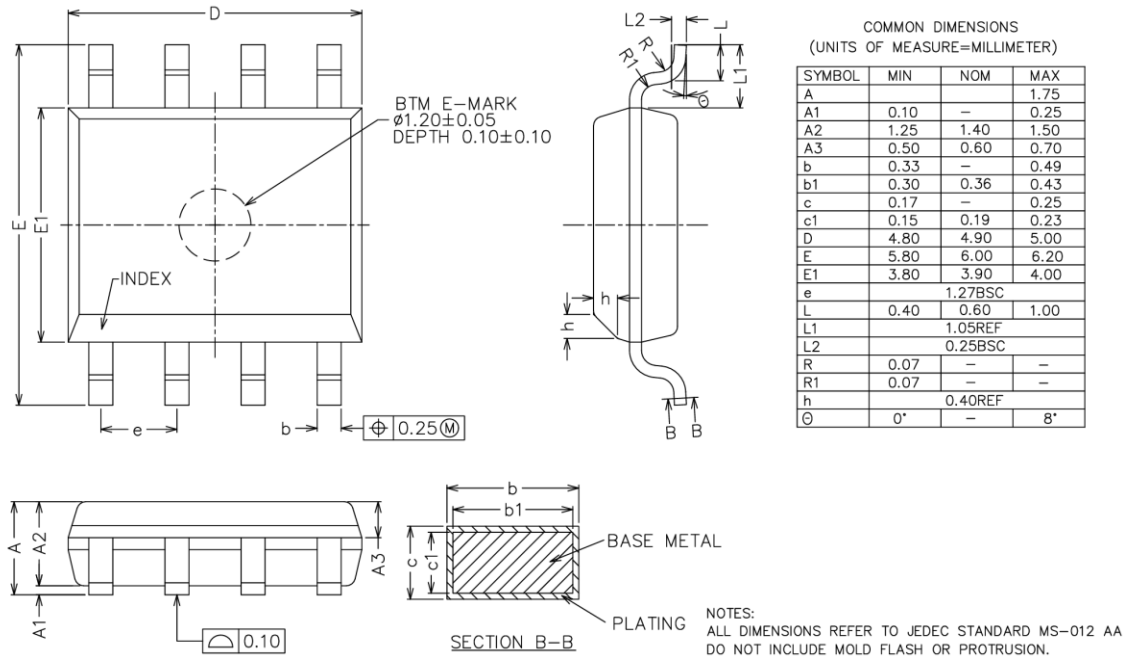


Figure9.4 Eye Diagram at 50Mbps PRBS $2^{16}-1$, 2.5V and 25°C

10. Package Information



NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.1 SOP8 Package Shape and Dimension in millimeters

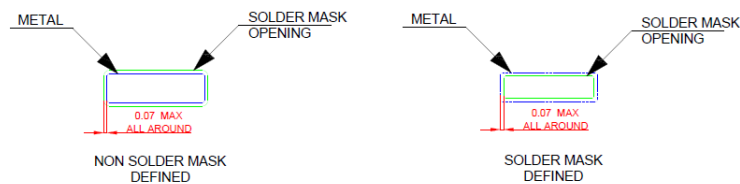
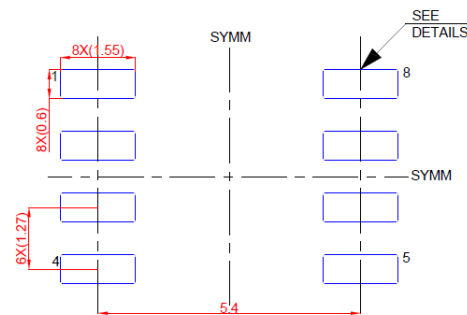
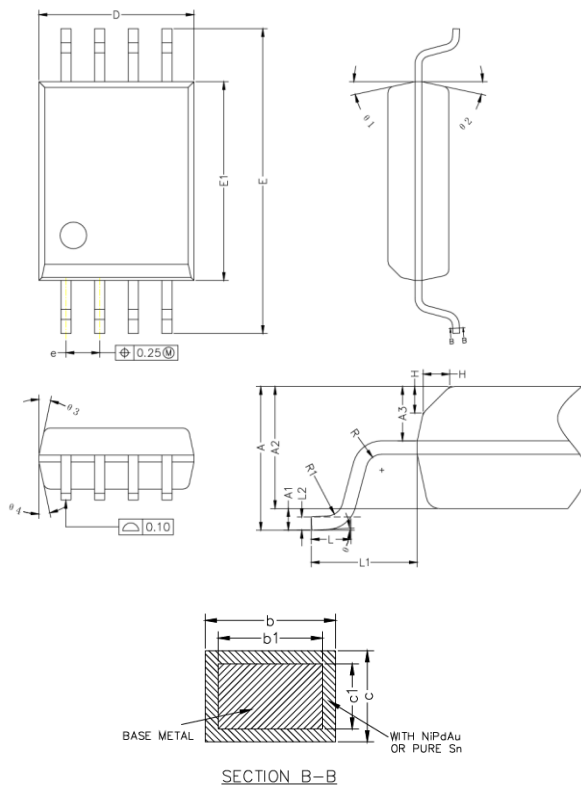


Figure 10.2 SOP8 Package Board Layout Example



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	2.85
A1	0.31	0.41	0.51
A2	2.20	2.30	2.40
A3	0.97	1.02	1.07
b PURE Sn	0.33	—	0.47
NiPdAu	0.31	—	0.51
b1	0.29	—	0.43
c PURE Sn	0.22	—	0.35
NiPdAu	0.13	—	0.33
c1	0.11	—	0.31
D	5.75	5.85	5.95
E	11.25	11.50	11.75
E1	7.40	7.50	7.60
e	1.27BSC		
H	0.50REF		
L	0.50	—	1.00
L1	2.00REF		
L2	0.25BSC		
R	0.07REF		
R1	0.07REF		
θ	0°	—	8°
θ 1	12°REF		
θ 2	12°REF		
θ 3	12°REF		
θ 4	12°REF		

NOTES:

1. ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.3 SOW8 Package Shape and Dimension in millimeters

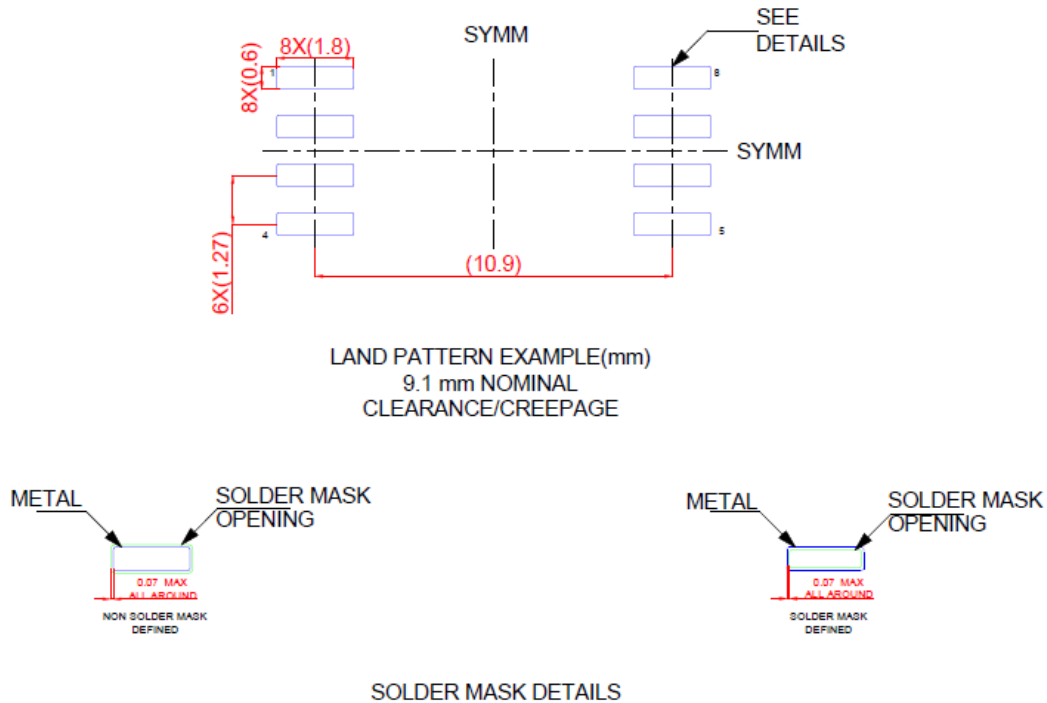


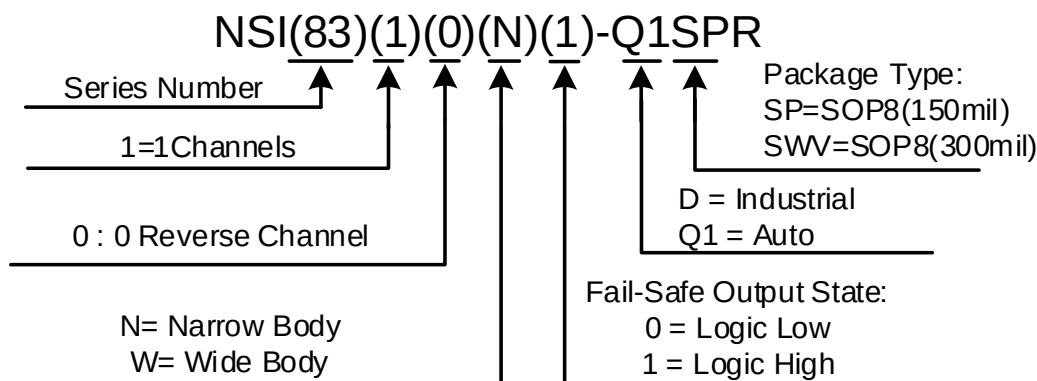
Figure 10.4 SOW8 Package Board Layout Example

11. Order Information

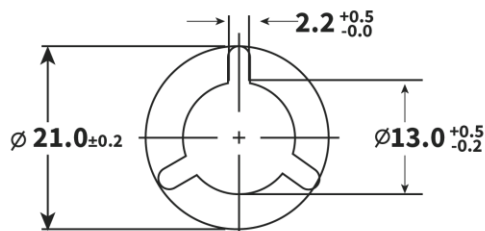
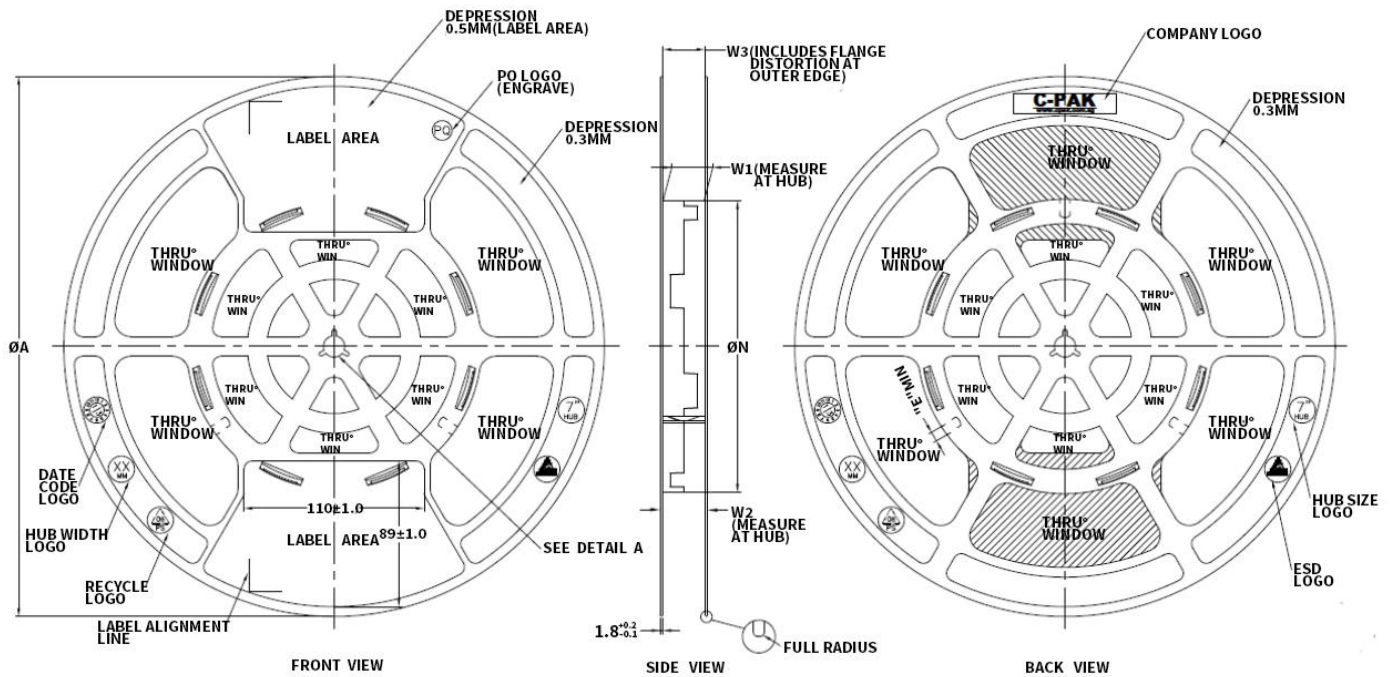
Part Number	Isolation Rating (kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	MSL	Package Type	Package Drawing	SPQ	MPQ
NSI8310N0-Q1SPR	3.75	1	0	150	Low	-40 to 125°C	3	SOP8 (150mil)	SOP8	2500	2500
NSI8310N1-Q1SPR	3.75	1	0	150	High	-40 to 125°C	3	SOP8 (150mil)	SOP8	2500	2500
NSI8310W0-Q1SWVR	5	1	0	100	Low	-40 to 125°C	3	SOP8 (300mil)	SOW8	1000	1000
NSI8310W1-Q1SWVR	5	1	0	100	High	-40 to 125°C	3	SOP8 (300mil)	SOW8	1000	1000

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
All devices are AEC-Q100 qualified.

Part Number Rule:



12. Tape and Reel Information

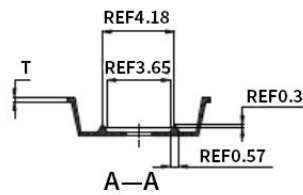
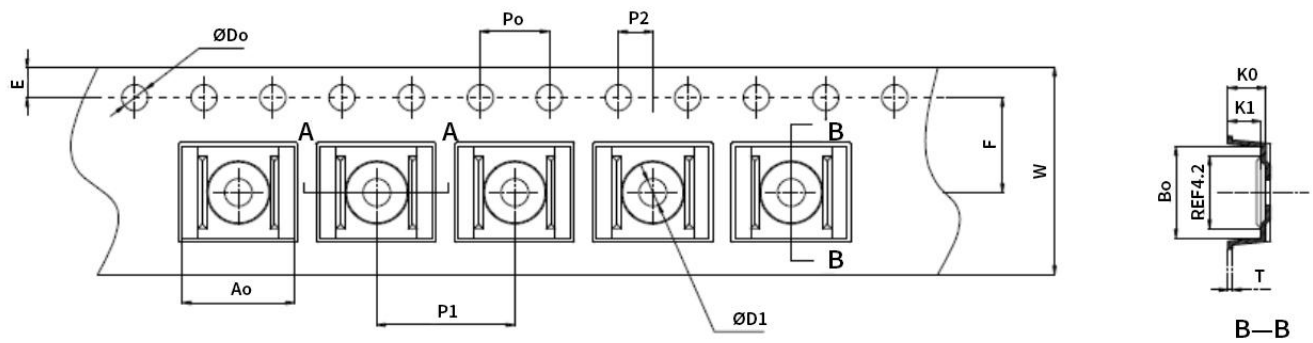


**ARBOR HOLE
DETAIL A
SCALE: 3:1**

PRODUCT SPECIFICATION						
TAPE WIDTH	Ø A ±2.0	Ø N ±2.0	W1	W2 (Max)	W3	E (MIN)
08MM	330	178	8.4 ^{+1.5} _{-0.0}	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 ^{+2.0} _{-0.0}	18.4		5.5
16MM	330	178	16.4 ^{+2.0} _{-0.0}	22.4		5.5
24MM	330	178	24.4 ^{+2.0} _{-0.0}	30.4		5.5
32MM	330	178	32.4 ^{+2.0} _{-0.0}	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10 ¹²	ANTISTATIC	ALL TYPES
B	10 ⁵ TO 10 ¹¹	STATIC DISSIPATIVE	BLACK ONLY
C	10 ⁵ & BELOW 10 ⁵	CONDUCTIVE(GENERIC)	BLACK ONLY
E	10 ⁹ TO 10 ¹¹	ANTISTATIC(COATED)	ALL TYPES

Figure 13.1 Reel Information (for all packages)



Common size

Appearance	Size(mm)
E	1.75±0.10
F	5.5±0.10
P2	2.00±0.10
D0	1.55±0.05
D1	1.6±0.10
P0	4.00±0.10
10P0	40.00±0.20

Pocket size

Appearance	Size(mm)
W	12.00±0.30
P1	8.00±0.10
A0	6.50±0.10
B0	5.30±0.10
K0	2.20±0.10
K1	1.90±0.10
T	0.30±0.05

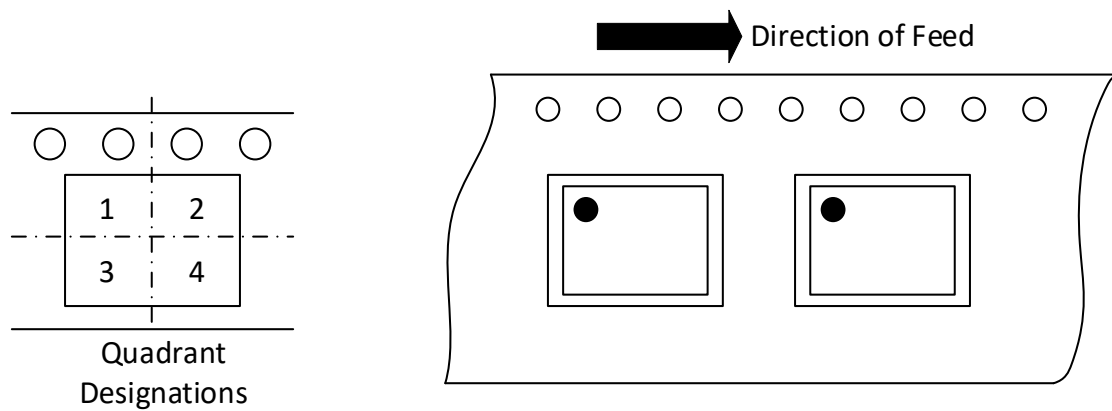
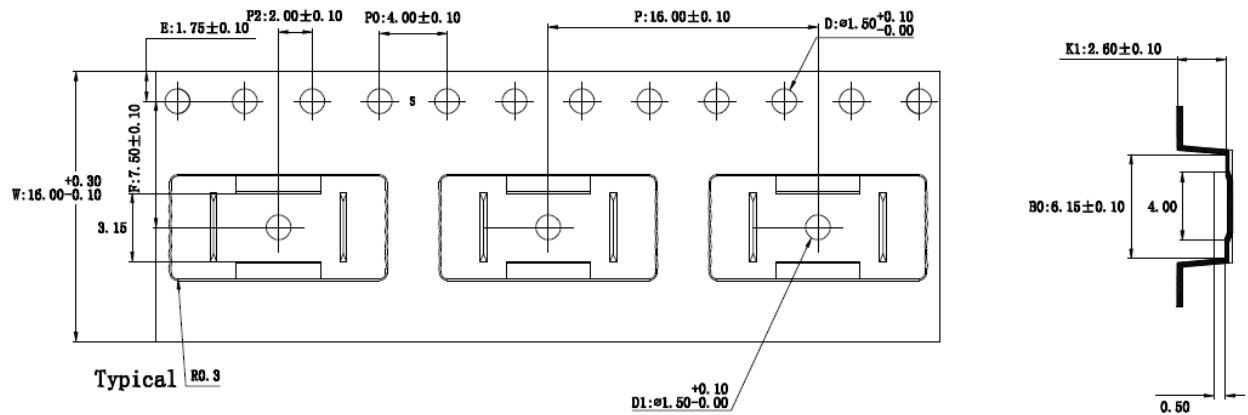


Figure 13.2 Tape Information of SOP8(150mil)



技术要求:

Technical Requirements:

- 每10个料带链孔直径累计公差为 ± 0.20 毫米。
10 sprocket hole pitch cumulative toleran ± 0.20 mm
- 料带弯曲每250毫米不可超过1毫米。
Carrier camber is within 1 mm in 250 mm
- 所有尺寸符合EIA-481-D标准要求。
All dimensions meet EIA-481-D requirements

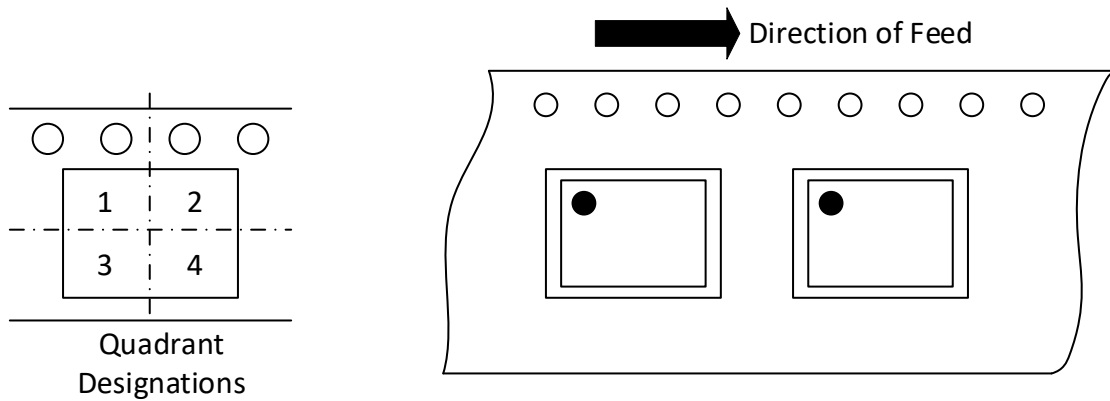


Figure 13.3 Tape Information of SOW8(300mil)

13. Reflow Profiles

13.1. Classification Temperature

Nonhermetic surface mount devices are classified for Moisture and Reflow temperature sensitivity according the IPC/JEDEC J-STD-020 standard. The Classification Temperature is specified in dependence of package thickness and the package plastic volume. The Pb-Free Process Classification Temperatures (T_c) table in the IPC/JEDEC J-STD-020 standard lists the temperatures, which are shown in Table 14.1.

Table 14.1 Pb-Free Process Classification Temperatures (T_c)

Package Thickness	Volume < 350 mm ³	Volume 350 – 2000 mm ³	Volume >2000 mm ³
< 1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5mm	250°C	245°C	245°C

13.2. Reflow Profile for Pb-Free Soldering

The Classification Profile in the IPC/JEDEC J-STD-020 shows the classification reflow profile to be used for the surface mount device as the below Figure 14.1.

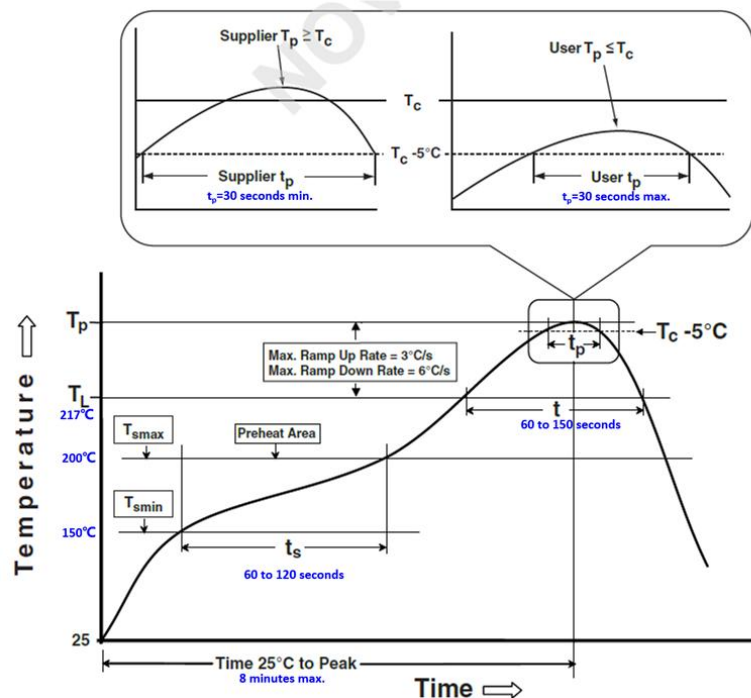


Figure 14.1 Classification Profile (not to scale)

Figure 14.1 illustrates the key temperature/times associated with the different Reflow oven zones. During the Preheat, the board and components are reaching a temperature where the flux in the solder paste is starting its activity.

The Peak temperature (T_p) for the reflow profile, measured at top of the package.

- For the IC supplier: T_p must equal or exceed T_c as shown in Table 14.1.
- For a user: T_p must not exceed T_c as shown in Table 14.1.
- Time that defines the peak temperate (t_p) starts/ends -5°C below T_c .

14. Revision History

Revision	Description	Date
1.0	Initial Version.	2026/7/13

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