

Product Overview

The NSI72xx devices are high speed single-channel and dual channel opto-emulator, it's certified by UL1577 and support 3750/7500V_{rms} insulation withstand voltage. The NSI72xx series operates from both 3.3V and 5V supply voltages with two logic-output options: CMOS output and Open-drain output. The data rate of NSI72xx is up to 15Mbps, and the common-mode transient immunity (CMTI) is up to 100kV/μs. These devices are pin-compatible and replace many traditional optocouplers, allowing enhancement of industrial standard packages without PCB redesign.

Key Features

- Up to 3750V_{rms} Insulation voltage: SOP5, SOP8
- Up to 7500V_{rms} Insulation voltage: SOP8(600mil)
- Data rate: DC to 15Mbps
- Power supply voltage: 2.7V to 5.5V
- High CMTI: 100kV/μs
- Chip level ESD: HBM: ±8kV
- Single or dual diode-emulator input
- Output options:
 NSI7210: CMOS
 NSI7221/ NSI7211: Open-drain
- Low propagation delay: <70ns
- Operation temperature: -40°C ~125°C
- RoHS-compliant packages: SOP5, SOP8, SOP8 (600mil)

Safety Regulatory Approvals

- UL recognition:
 - SOP5: 3750V_{rms} for 1 minute per UL1577
 - SOP8: 3750V_{rms} for 1 minute per UL1577
 - SOP8(600mil): 7500V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A approval IEC60950-1 standard

- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Industrial automation system
- Motor Control
- Power supplies
- Isolated line receiver

Device Information

| Part Number | Package | Body Size |
|----------------|--------------|------------------|
| NSI7210-DSPAR | SOP5 | 3.60mm × 4.40mm |
| NSI7210-DSWWAR | SOP8(600mil) | 6.25mm × 13.60mm |
| NSI7211-DSPAR | SOP5 | 3.60mm × 4.40mm |
| NSI7211-DSWWAR | SOP8(600mil) | 6.25mm × 13.60mm |
| NSI7211-DSPR | SOP8 | 4.90mm × 3.90mm |
| NSI7221-DSPR | SOP8 | 4.90mm × 3.90mm |

Functional Block Diagrams

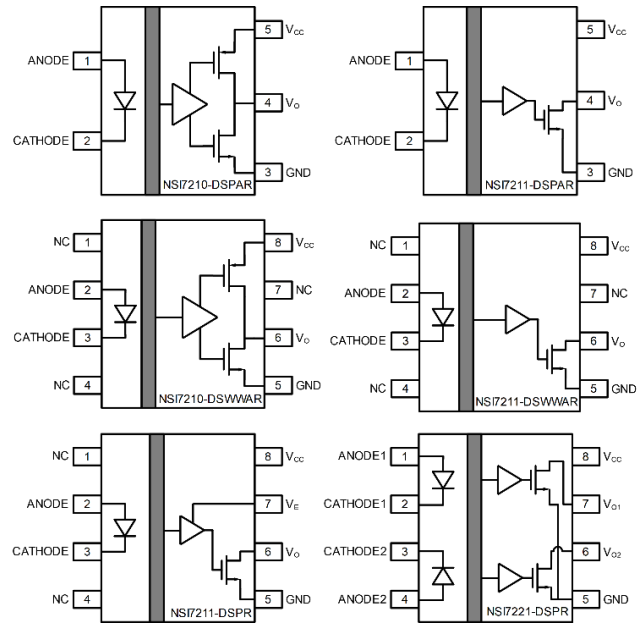


Figure 1. NSI72xx Block Diagram

INDEX

| | |
|---|----|
| 1. PIN CONFIGURATION AND FUNCTIONS | 3 |
| 2. ABSOLUTE MAXIMUM RATINGS | 5 |
| 3. ESD RATINGS ⁽¹⁾ | 5 |
| 4. RECOMMENDED OPERATING CONDITIONS | 6 |
| 5. THERMAL INFORMATION | 6 |
| 6. SPECIFICATIONS | 7 |
| 6.1. ELECTRICAL CHARACTERISTICS | 7 |
| 6.2. SWITCHING CHARACTERISTICS, NSI7210 | 8 |
| 6.3. SWITCHING CHARACTERISTICS, NSI7211 | 8 |
| 6.4. SWITCHING CHARACTERISTICS, NSI7221 | 9 |
| 6.5. TYPICAL CHARACTERISTICS | 10 |
| 6.6. PARAMETER MEASUREMENT INFORMATION | 13 |
| 7. HIGH VOLTAGE FEATURE DESCRIPTION | 15 |
| 7.1. INSULATION AND SAFETY RELATED SPECIFICATIONS | 15 |
| 7.2. INSULATION CHARACTERISTICS | 16 |
| 7.3. SAFETY-LIMITING VALUES | 18 |
| 7.4. REGULATORY INFORMATION | 20 |
| 8. FUNCTION DESCRIPTION | 21 |
| 8.1. OVERVIEW | 21 |
| 8.2. OOK MODULATION | 21 |
| 9. APPLICATION NOTE | 23 |
| 9.1. TYPICAL APPLICATION CIRCUIT | 23 |
| 9.2. PCB LAYOUT | 24 |
| 10. PACKAGE INFORMATION | 25 |
| 11. ORDERING INFORMATION | 28 |
| 12. DOCUMENTATION SUPPORT | 28 |
| 13. TAPE AND REEL INFORMATION | 29 |
| 14. REVISION HISTORY | 35 |

1. Pin Configuration and Functions

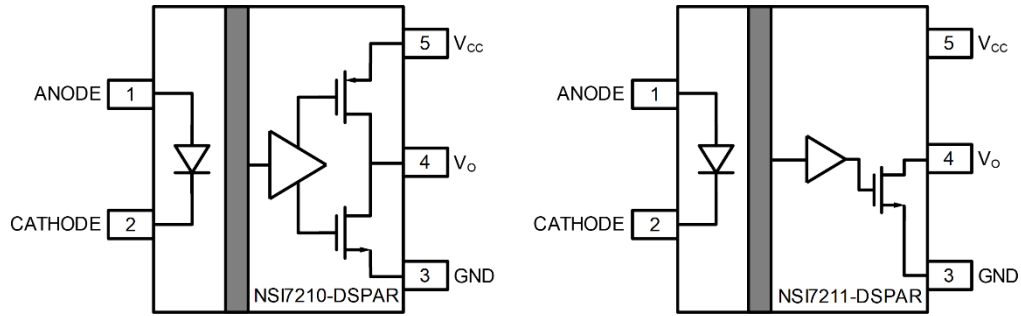


Figure 1.1 NSI721x SOP5 Package

Table 1.1 NSI721x SOP5 Package Pin Configuration and Description

| NSI721x SOP5 PIN NO. | SYMBOL | FUNCTION |
|-----------------------------|---------------|---|
| 1 | ANODE | Anode connection of diode emulator |
| 2 | CATHODE | Cathode connection of diode emulator |
| 3 | GND | Ground reference for V_O and V_{CC} |
| 4 | V_O | Logic output |
| 5 | V_{CC} | Power Supply for output |

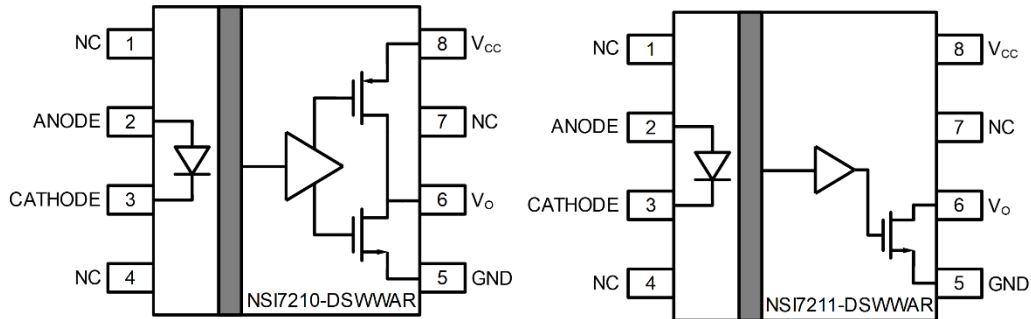


Figure 1.2 NSI721x SOP8(600mil) Package

Table 1.2 NSI721x SOP8(600mil) Package Pin Configuration and Description

| NSI721x SOP8(600mil) PIN NO. | SYMBOL | FUNCTION |
|-------------------------------------|---------------|--|
| 1 | NC | Not connect pin; it has no internal connection |
| 2 | ANODE | Anode connection of diode emulator |
| 3 | CATHODE | Cathode connection of diode emulator |
| 4 | NC | Not connect pin; it has no internal connection |
| 5 | GND | Ground reference for V_O and V_{CC} |
| 6 | V_O | Logic output |

| NSI721x SOP8(600mil) PIN NO. | SYMBOL | FUNCTION |
|---|-----------------|--|
| 7 | NC | Not connect pin; it has no internal connection |
| 8 | V _{CC} | Power Supply for output |

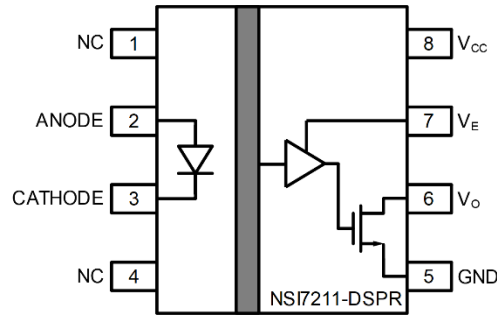


Figure 1.3 NSI7211 SOP8 Package

Table 1.3 NSI7211 SOP8 Package Pin Configuration and Description

| NSI7211 SOP8 PIN NO. | SYMBOL | FUNCTION |
|---------------------------------|-----------------|--|
| 1 | NC | Not connect pin; it has no internal connection |
| 2 | ANODE | Anode connection of diode emulator |
| 3 | CATHODE | Cathode connection of diode emulator |
| 4 | NC | Not connect pin; it has no internal connection |
| 5 | GND | Ground reference for V _O and V _{CC} |
| 6 | V _O | Logic output |
| 7 | V _E | Output Enable. Active high logic input. When EN is high or NC, the output side is enabled. When EN is low, the output side is disabled to high impedance state |
| 8 | V _{CC} | Power Supply for output |

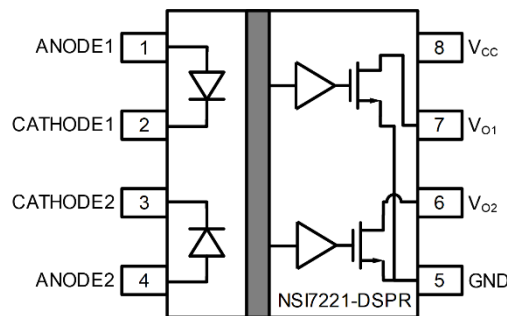


Figure 1.4 NSI7221 SOP8 Package

Table 1.4 NSI7221 SOP8 Pin Configuration and Description

| NSI7221 SOP8 PIN NO. | SYMBOL | FUNCTION |
|----------------------|-----------------|--|
| 1 | ANODE1 | Anode connection of diode emulator 1 |
| 2 | CATHODE1 | Cathode connection of diode emulator 1 |
| 3 | CATHODE2 | Cathode connection of diode emulator 2 |
| 4 | ANODE2 | Anode connection of diode emulator 2 |
| 5 | GND | Ground reference for V _{O1} , V _{O2} and V _{CC} |
| 6 | V _{O2} | Logic output 2 |
| 7 | V _{O1} | Logic output 1 |
| 8 | V _{CC} | Power Supply for output |

2. Absolute Maximum Ratings

| Parameters | Symbol | Min | Typ | Max | Unit | Comments |
|------------------------------|---------------------|------|-----|----------------------|------|----------------------|
| Supply Voltage | V _{CC} | -0.3 | | 6.5 | V | |
| Output Collector Voltage | V _{OC} | -0.3 | | V _{CC} +0.5 | V | NSI72x1 only |
| Reverse Input Voltage | V _{R_MAX} | 5 | | | V | I _R =10μA |
| Enable Voltage | V _E | -0.3 | | V _{CC} +0.5 | V | NSI7211-DSPR only |
| Input forward Current | I _F | | | 25 | mA | |
| Peak Transient Input Current | I _{F_PEAK} | | | 1 | A | |
| Output Collector Current | I _{OC} | | | 50 | mA | NSI72x1 only |
| Output Current | I _O | -15 | | 15 | mA | NSI7210 only |
| Operating Temperature | T _{opr} | -40 | | 125 | °C | |
| Junction Temperature | T _J | | | 150 | °C | |
| Storage Temperature | T _{stg} | -65 | | 125 | °C | |

3. ESD Ratings ⁽¹⁾

| Parameters | Ratings | Value | Unit |
|-------------------------------|--|-------|------|
| Electrostatic discharge (ESD) | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽²⁾ | ±8000 | V |
| | Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽³⁾ | ±2000 | V |

(1) Though this device features proprietary protection circuitry, proper ESD precautions should be considered to avoid performance degradation of damage due to high energy ESD event. Charged devices and circuit boards may discharge without detection.

(2) Safe manufacturing requires 500-V HBM and standard ESD precautions, per JEDEC document JEP155.

(3) Safe manufacturing requires 250-V CDM and standard ESD precautions, per JEDEC document JEP157.

4. Recommended Operating Conditions

| Parameters | Symbol | Min | Typ | Max | Unit | Comments |
|---|-------------------|-----|-----|----------|--------------|-----------------------------|
| Supply Voltage | V_{CC} | 2.7 | | 5.5 | V | |
| Input ON Forward Current | $I_{F(ON)}$ | 2 | | 20 | mA | |
| Input OFF Forward Current | $I_{F(OFF)}$ | 0 | | 250 | μ A | |
| Output Current | I_O | -4 | | 4 | mA | NSI7210 only |
| Logic Low Output Open-Drain Sinking Current | $I_{OL(sinking)}$ | | | 13 | mA | NSI7211, NSI7221 only |
| Enable High Level Input Voltage | V_{EH} | 2 | | V_{CC} | V | NSI7211-DSPR only |
| Enable Low Level Input Voltage | V_{EL} | 0 | | 0.8 | V | NSI7211-DSPR only |
| Data Rate | DR | | | 15 | Mbps | $I_F \geq 6$ mA |
| | | | | 10 | Mbps | 3 mA $\leq I_F \leq 6$ mA |
| | | | | 5 | Mbps | 2 mA $\leq I_F \leq 3$ mA |
| Ambient Temperature | T_A | -40 | | 125 | $^{\circ}$ C | |

5. Thermal Information

| Parameters | Symbol | SOP5 | SOP8 | SOP8(600mil) | Unit |
|--|----------------------|-------|-------|--------------|-----------------|
| Junction-to-Air thermal resistance | $R_{\theta JA}$ | 215.9 | 137.7 | 78.9 | $^{\circ}$ C /W |
| Junction-to-Case(top) thermal resistance | $R_{\theta JC(top)}$ | 125.7 | 54.9 | 41.6 | $^{\circ}$ C /W |
| Junction-to-Board thermal resistance | $R_{\theta JB}$ | 153.9 | 71.7 | 43.6 | $^{\circ}$ C /W |

6. Specifications

6.1. Electrical Characteristics

$V_{CC}=2.7V$ to $5.5V$, $T_A=-40^{\circ}C$ to $125^{\circ}C$. Unless otherwise noted, typical values are at $V_{CC} = 3.3V$, $T_A = 25^{\circ}C$

| Parameters | Symbol | Min | Typ | Max | Unit | Comments |
|-----------------------------------|-----------|--------------|--------------|-----|---------|---|
| Forward Voltage | V_F | 1.3 | 1.7 | 2 | V | $I_F=6mA$ |
| Input Reverse Current | I_R | | | 10 | μA | |
| Input Threshold Current | I_{TH} | 0.6 | 1 | 1.4 | mA | |
| Input Current Hysteresis | I_{HYS} | | 0.1 | | mA | |
| Logic High Supply Current | I_{CCH} | | 0.73 | 1.2 | mA | NSI721x only |
| | | | 1.38 | 2 | mA | NSI7221 only |
| Logic Low Supply Current | I_{CCL} | | 0.74 | 1.2 | mA | NSI721x only |
| | | | 1.39 | 2 | mA | NSI7221 only |
| Enable High-level Input Current | I_{EH} | | -5.4 | | μA | NSI7211-DSPR only; $V_{CC}=5V$, $V_E=2V$ |
| Enable Low-level Input Current | I_{EL} | | -5.8 | | μA | NSI7211-DSPR only; $V_{CC}=5V$, $V_E=0.5V$ |
| Enable Threshold Voltage, rising | V_{EH} | | | 2 | V | NSI7211-DSPR only |
| Enable Threshold Voltage, falling | V_{EL} | 0.8 | | | V | NSI7211-DSPR only |
| Logic High Output Voltage | V_{OH} | $V_{CC}-0.3$ | $V_{CC}-0.2$ | | V | NSI7210 only, $I_O = -4$ mA See Figure 6.20 , $C_L = 15pF$ |
| Logic Low Output Voltage | V_{OL} | | 0.19 | 0.4 | V | NSI7210 only, $I_F = 6$ mA, $I_{OL} = 4$ mA See Figure 6.20 , $C_L = 15pF$ |
| | | | 0.46 | 0.6 | V | NSI7211 only, $I_F = 6$ mA, I_{OL} (sinking)= 13 mA |
| | | | 0.55 | 0.7 | V | NSI7221 only, $I_F = 6$ mA, I_{OL} (sinking)= 13 mA See Figure 6.21 , $C_L = 15pF$ |
| | | | 0.22 | 0.4 | V | NSI7221 only, $I_F = 6$ mA, I_{OL} (sinking)= 5 mA See Figure 6.21 , $C_L = 15pF$ |
| Logic High Output Current | I_{OH} | | | 10 | μA | NSI72x1 only, $V_{OUT} = V_{CC}$ |
| Terminal Capacitance | C_i | | 30 | | pF | Anode to Cathode capacitance; 1MHz, $V_F = 0$ V |

6.2. Switching Characteristics, NSI7210

V_{CC}=2.7V to 5.5V, T_A=-40°C to 125°C. Unless otherwise noted, I_F=6mA, typical values are at V_{CC} = 3.3V, T_A = 25°C

| Parameters | Symbol | Min | Typ | Max | Unit | Comments |
|--|-------------------|-----|-----|-----|-------|--|
| Propagation Delay Time to High Output Level | t _{PLH} | | 56 | 70 | ns | See Figure 6.18 , C _L = 15pF |
| Propagation Delay Time to Low Output Level | t _{PHL} | | 53 | 70 | ns | See Figure 6.18 , C _L = 15pF |
| Pulse Width Distortion t _{PHL} - t _{PLH} | t _{PWD} | | 3 | 25 | ns | See Figure 6.18 , C _L = 15pF |
| Rising Time | t _r | | 2 | | ns | See Figure 6.18 , C _L = 15pF |
| Falling Time | t _f | | 2 | | ns | See Figure 6.18 , C _L = 15pF |
| Propagation Delay Difference Between Any Two Parts (t _{PHL} -t _{PLH}) (1) | PDD | -15 | | 15 | ns | |
| Common Mode Transient Immunity | CMTI _L | 100 | | | kV/μs | See Figure 6.23 , I _F =6mA, output=LOW |
| | CMTI _H | 100 | | | kV/μs | See Figure 6.23 , I _F =0mA, output=HIGH |

6.3. Switching Characteristics, NSI7211

V_{CC}=2.7V to 5.5V, T_A=-40°C to 125°C. Unless otherwise noted, pull-up resistor is 390 Ω, I_F=6mA, typical values are at V_{CC} = 3.3V, T_A = 25°C

| Parameters | Symbol | Min | Typ | Max | Unit | Comments |
|--|-------------------|-----|-----|-----|-------|---|
| Propagation Delay Time to High Output Level | t _{PLH} | | 57 | 70 | ns | See Figure 6.19 , C _L = 15pF |
| Propagation Delay Time to Low Output Level | t _{PHL} | | 56 | 70 | ns | See Figure 6.19 , C _L = 15pF |
| Pulse Width Distortion t _{PHL} - t _{PLH} | t _{PWD} | | 1 | 25 | ns | See Figure 6.19 , C _L = 15pF |
| Rising Time (10%-90%) | t _r | | 20 | | ns | See Figure 6.19 , C _L = 15pF |
| Falling Time (90%-10%) | t _f | | 3 | | ns | See Figure 6.19 , C _L = 15pF |
| Propagation Delay Difference Between Any Two Parts (t _{PHL} -t _{PLH}) (1) | PDD | -15 | | 15 | ns | |
| Propagation Delay Time of Enable from V _{EL} to V _{EH} | t _{ELH} | | 13 | | ns | V _{EH} =2.5V, NSI7211-DSPR only See Figure 6.22 |
| Propagation Delay Time of Enable from V _{EH} to V _{EL} | t _{EHL} | | 13 | | ns | V _{EH} =2.5V, NSI7211-DSPR only See Figure 6.22 |
| Common Mode Transient Immunity | CMTI _L | 100 | | | kV/μs | See Figure 6.24 , I _F =6mA, output=LOW |
| | CMTI _H | 100 | | | kV/μs | See Figure 6.24 , I _F =0mA, output=HIGH |

6.4. Switching Characteristics, NSI7221

VCC=2.7V to 5.5V, TA=-40°C to 125°C. Unless otherwise noted, pull-up resistor is 390 Ω, typical values are at IF=6mA, VCC = 3.3V, TA = 25°C

| Parameters | Symbol | Min | Typ | Max | Unit | Comments |
|--|---------------|-----|-----|-----|-------|---|
| Propagation Delay Time to High Output Level | t_{PLH} | | 60 | 70 | ns | See Figure 6.19 , $C_L = 15pF$ |
| Propagation Delay Time to Low Output Level | t_{PHL} | | 56 | 70 | ns | See Figure 6.19 , $C_L = 15pF$ |
| Pulse Width Distortion $ t_{PHL} - t_{PLH} $ | t_{PWD} | | 4 | 25 | ns | See Figure 6.19 , $C_L = 15pF$ |
| Rising Time (10%-90%) | t_r | | 20 | | ns | See Figure 6.19 , $C_L = 15pF$ |
| Falling Time (90%-10%) | t_f | | 3 | | ns | See Figure 6.19 , $C_L = 15pF$ |
| Propagation Delay Difference Between Any Two Parts ($t_{pHL} - t_{pLH}$) (1) | PDD | -15 | | 15 | ns | |
| Channel-to-Channel Delay Skew | $t_{sk(c2c)}$ | | | 10 | ns | |
| Common Mode Transient Immunity | $ CMTI_L $ | 100 | | | kV/μs | See Figure 6.24 , $I_F=6mA$, output=LOW |
| | $ CMTI_H $ | 100 | | | kV/μs | See Figure 6.24 , $I_F=0mA$, output=HIGH |

6.5. Typical Characteristics

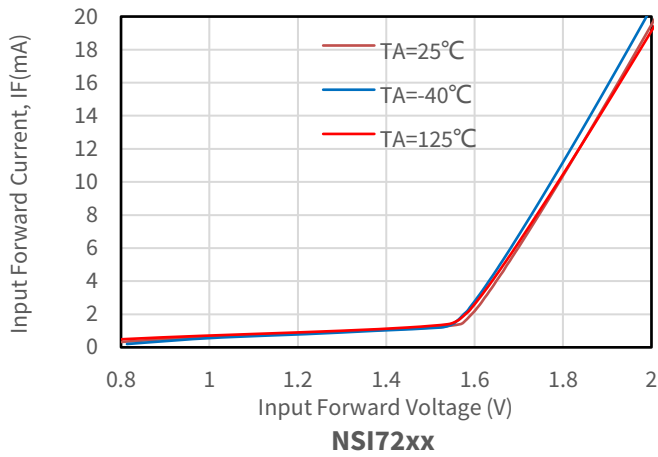


Figure 6.1 Input Forward Current vs Input Forward Voltage

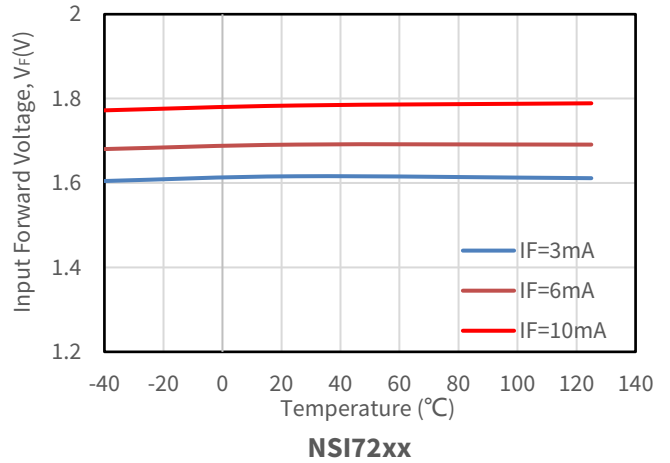


Figure 6.2 Input Forward Voltage vs Ambient Temperature

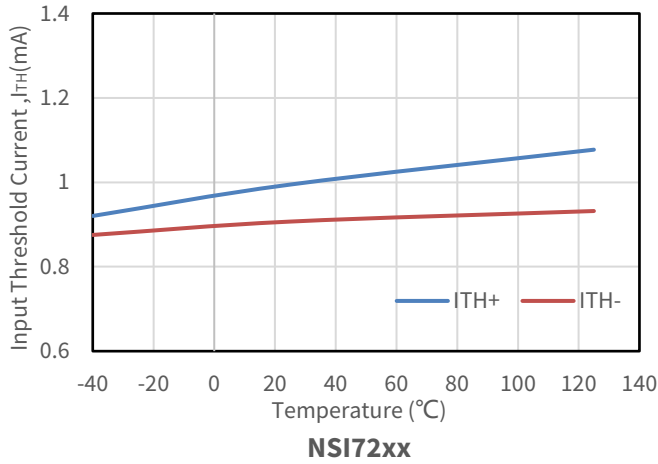


Figure 6.3 Input Threshold Current vs Ambient Temperature [11](#)

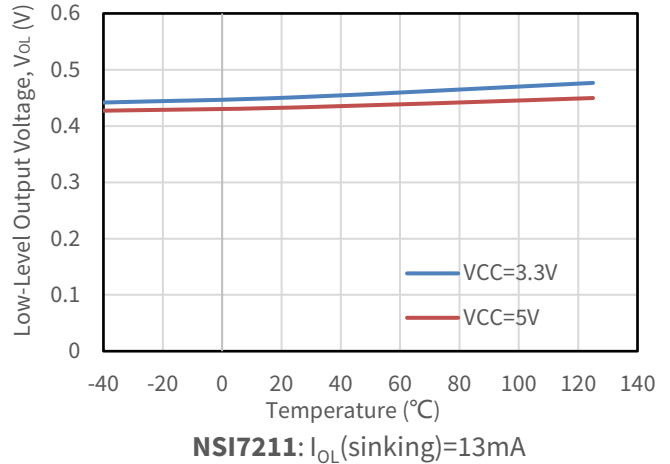


Figure 6.4 Low-Level Output Voltage vs Ambient Temperature

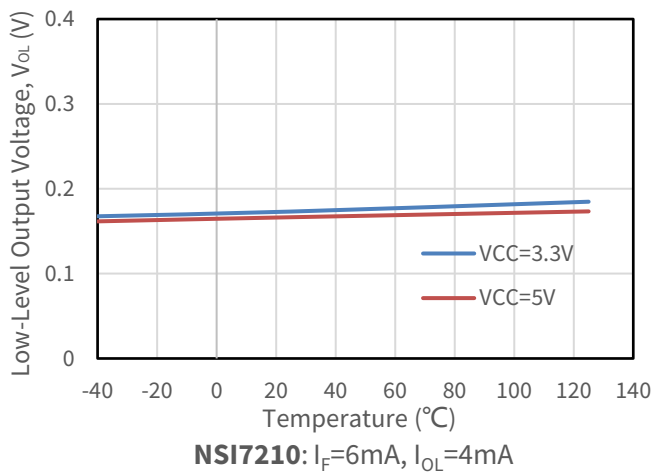


Figure 6.5 Low-Level Output Voltage vs Ambient Temperature

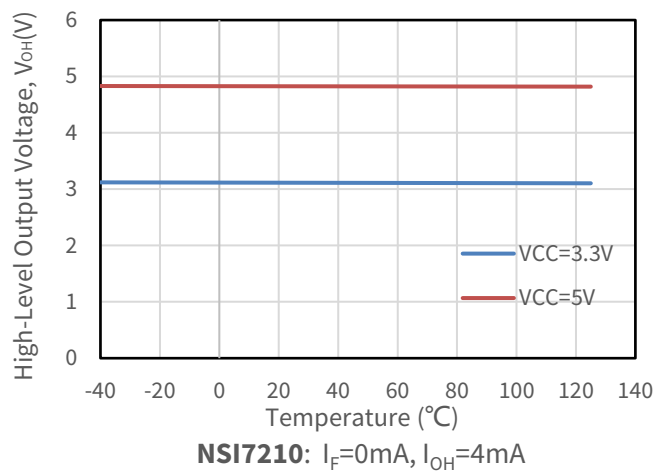
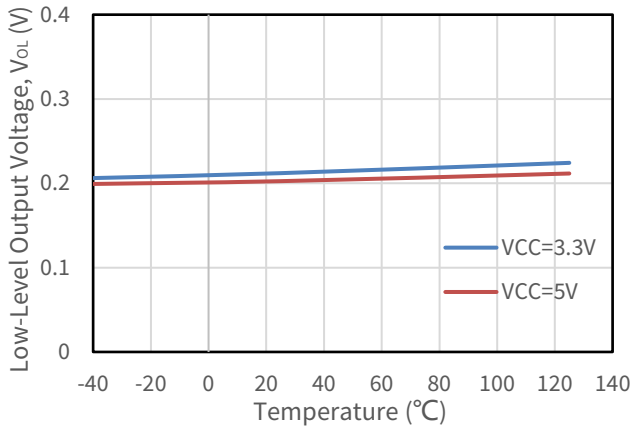
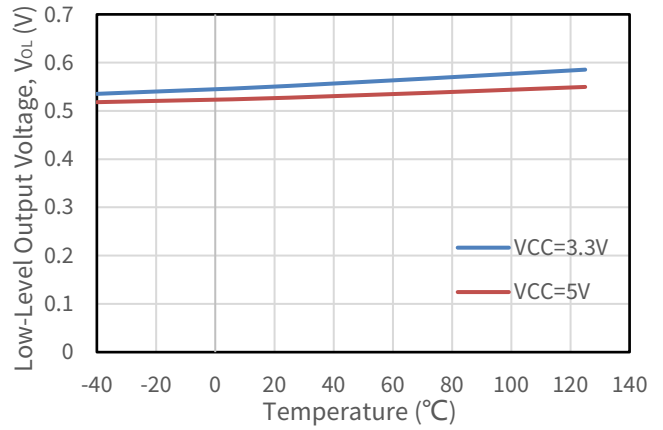


Figure 6.6 High-Level Output Voltage vs Ambient Temperature



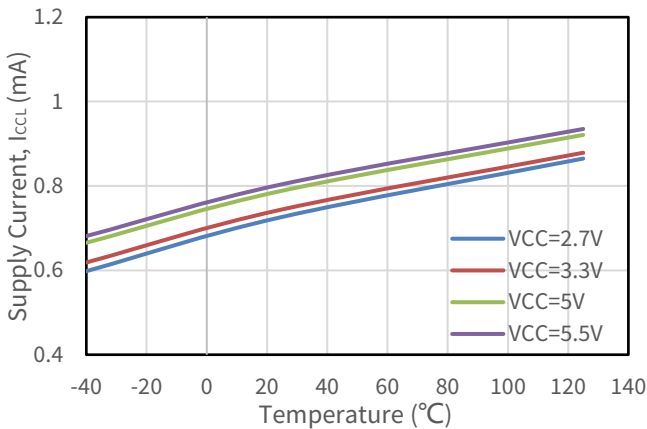
NSI7221: $I_F=6\text{mA}$, $I_{OL}=5\text{mA}$

Figure 6.7 Low-Level Output Voltage vs Ambient Temperature



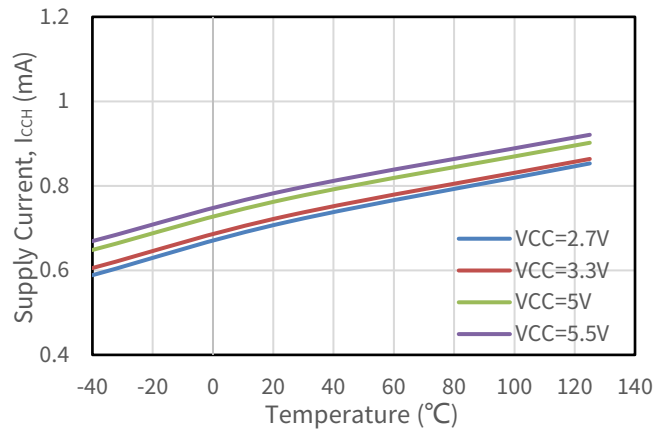
NSI7221: $I_F=6\text{mA}$, $I_{OL}=13\text{mA}$

Figure 6.8 Low-Level Output Voltage vs Ambient Temperature



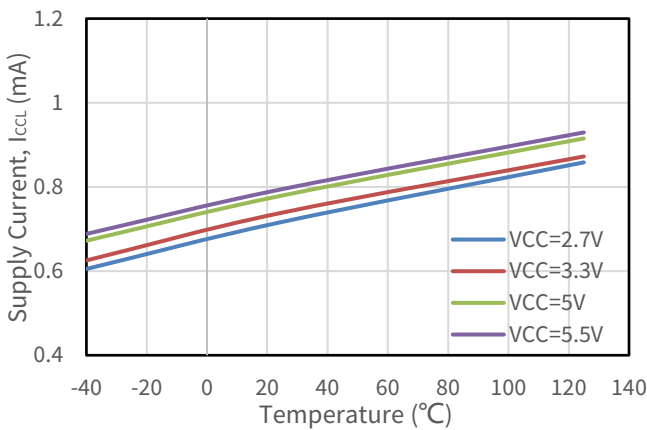
NSI7210: $I_F=6\text{mA}$

Figure 6.9 Logic Low Output Supply Current vs Ambient Temperature



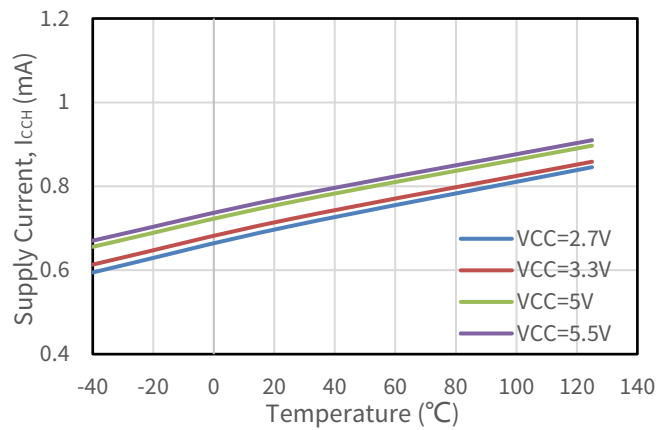
NSI7210: $I_F=0\text{mA}$

Figure 6.10 Logic High Output Supply Current vs Ambient Temperature



NSI7211: $I_F=6\text{mA}$

Figure 6.11 Logic Low Output Supply Current vs Ambient Temperature



NSI7211: $I_F=0\text{mA}$

Figure 6.12 Logic High Output Supply Current vs Ambient Temperature

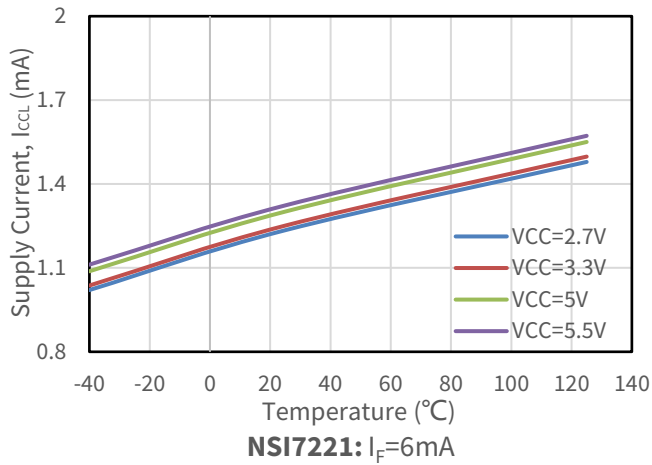


Figure 6.13 Logic Low Output Supply Current vs Ambient Temperature

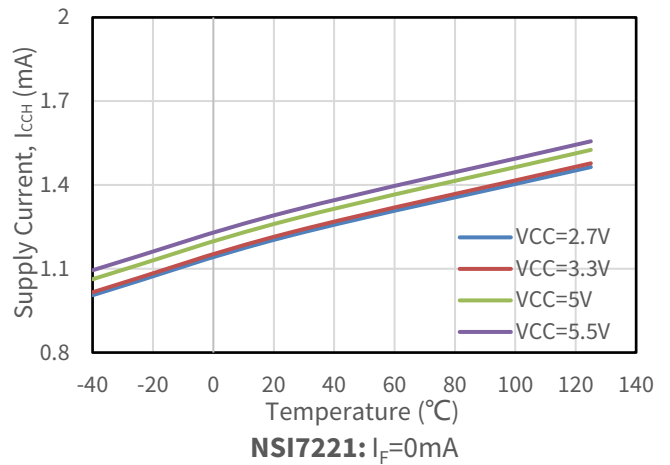


Figure 6.14 Logic Low Output Supply Current vs Ambient Temperature

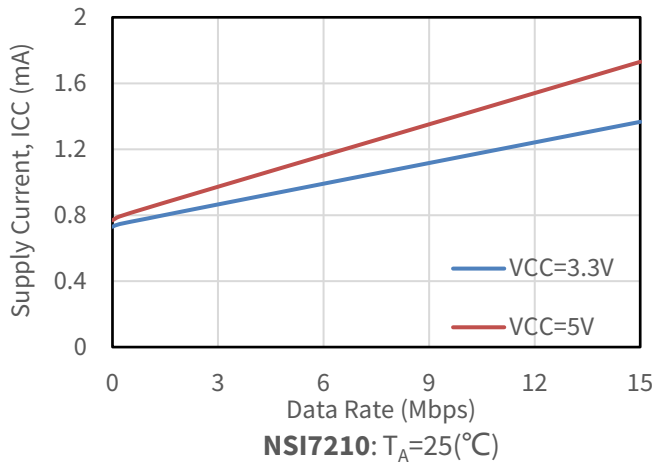


Figure 6.15 Output Supply Current vs Data Rate

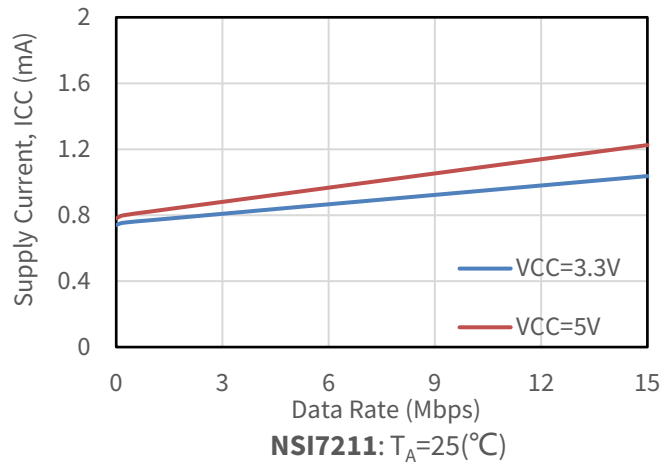


Figure 6.16 Output Supply Current vs Data Rate

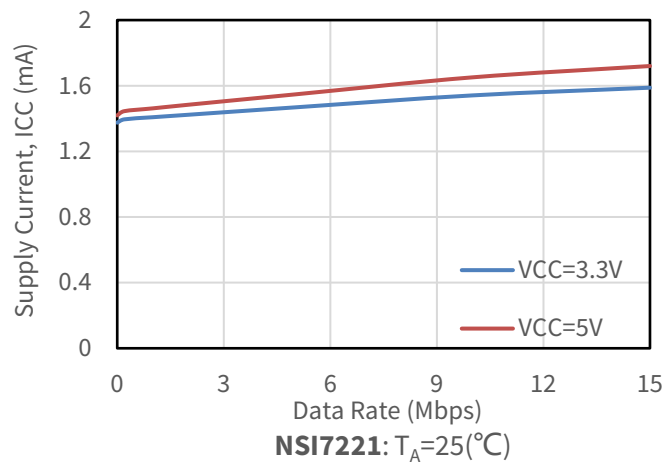


Figure 6.17 Output Supply Current vs Data Rate

[1] ITH+ represents the threshold current when the diode simulator is turned on, and ITH- represents the threshold current when it is turned off.

6.6. Parameter Measurement Information

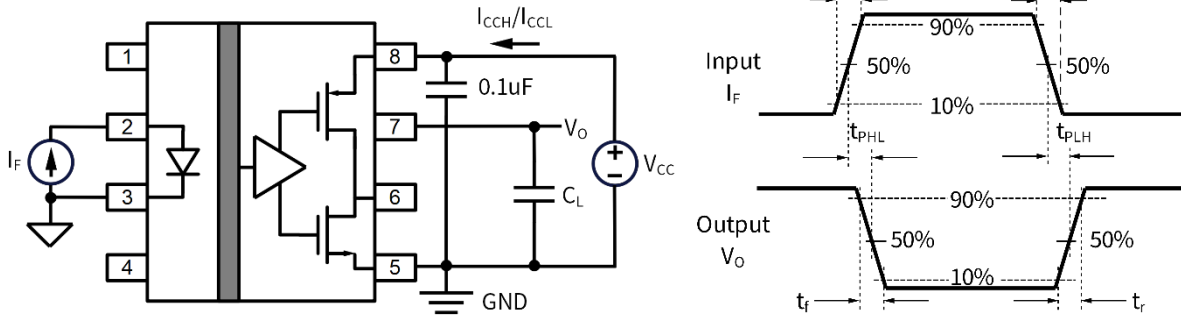


Figure 6.18 Electrical and Switching Characteristics Test Circuit for NSI7210

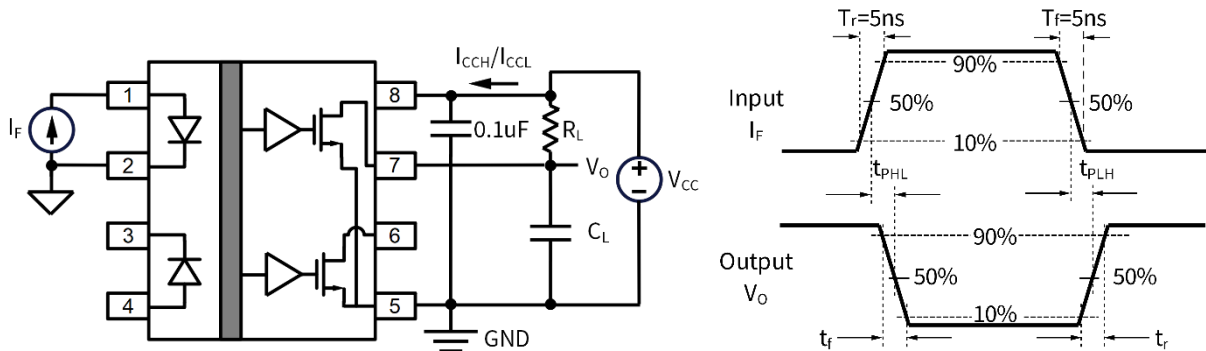


Figure 6.19 Electrical and Switching Characteristics Test Circuit for NSI7221

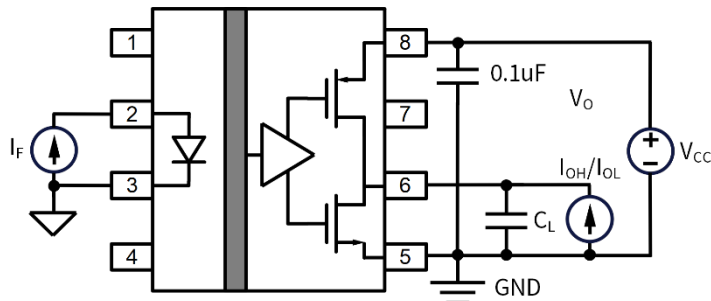


Figure 6.20 V_{OL} and V_{OH} Test Circuit for NSI7210

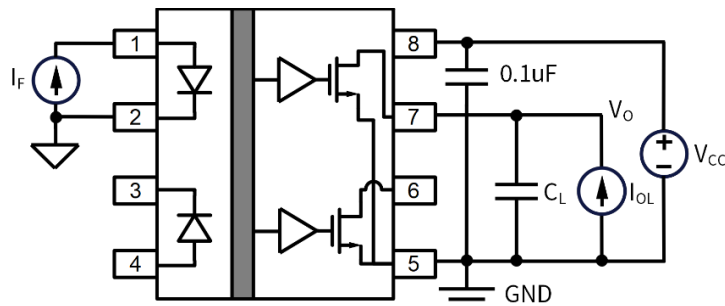


Figure 6.21 V_{OL} Test Circuit for NSI7221

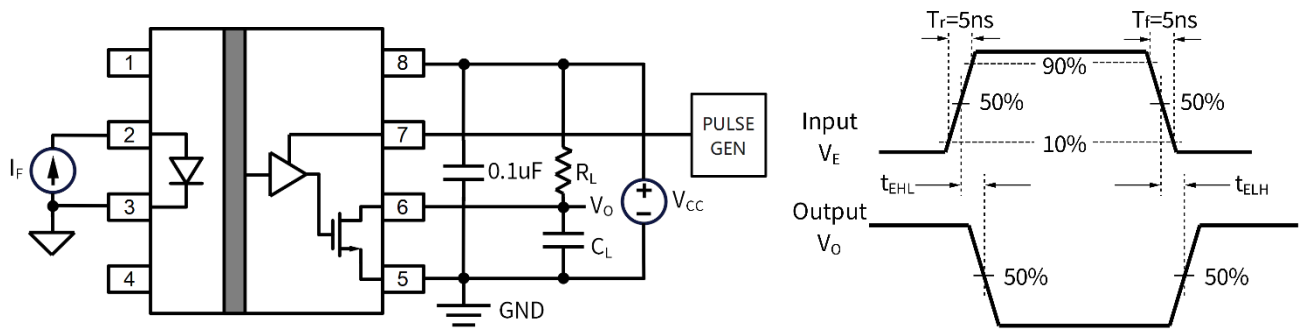


Figure 6.22 Enable Propagation Delay Test Circuit and Waveforms for NSI7211-DSRP

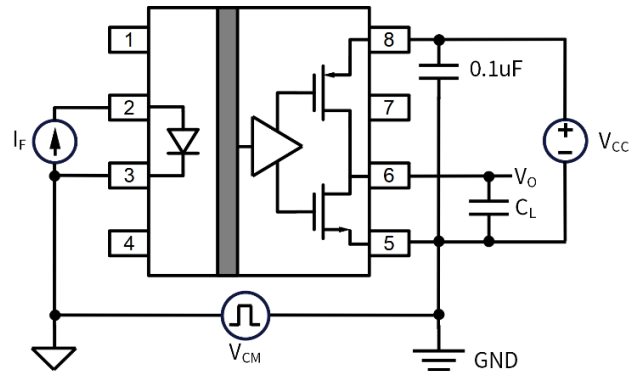


Figure 6.23 Common-Mode Transient Immunity Test Circuit for NSI7210

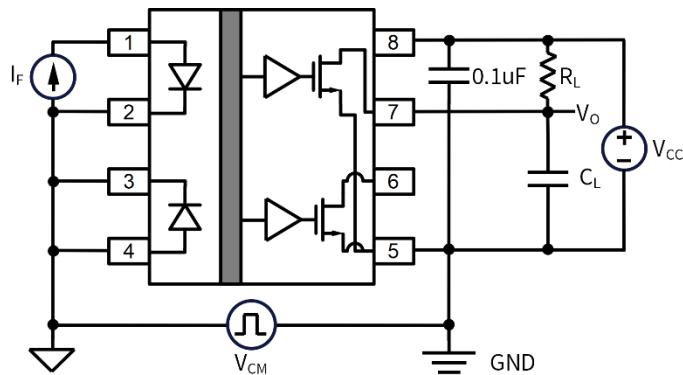


Figure 6.24 Common-Mode Transient Immunity Test Circuit for NSI7221

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

| Parameters | Symbol | Value | | | Unit | Comments |
|---|--------|-------|------|--------------|------|---------------------------------------|
| | | SOP5 | SOP8 | SOP8(600mil) | | |
| Minimum External Clearance | CLR | 4 | 4 | 15 | mm | IEC 60664-1:2007 |
| Minimum External Creepage | CPG | 4 | 4 | 15 | mm | IEC 60664-1:2007 |
| Distance Through Insulation | DTI | 24 | | | µm | |
| Tracking Resistance (Comparative Tracking Index) | CTI | >600 | >600 | >600 | V | DIN EN 60112 (VDE 0303-11); IEC 60112 |
| Material Group | | I | I | I | | IEC 60664-1 |

| Description | Test Condition | Value | | |
|-------------------------------------|--|-----------|----------|--------------|
| | | SOP5 | SOP8 | SOP8(600mil) |
| Overvoltage Category per IEC60664-1 | For Rated Mains Voltage $\leq 150V_{rms}$ | I to IV | I to IV | I to IV |
| | For Rated Mains Voltage $\leq 300V_{rms}$ | I to III | I to III | I to IV |
| | For Rated Mains Voltage $\leq 600V_{rms}$ | / | / | I to IV |
| | For Rated Mains Voltage $\leq 1000V_{rms}$ | / | / | I to III |
| Climatic Classification | | 40/125/21 | | |
| Pollution Degree per DIN VDE 0110, | | 2 | | |

7.2. Insulation Characteristics

| Description | Test Condition | Symbol | Value | | | Unit |
|--------------------------------------|--|-------------------|-------|------|--------------|-------------------|
| | | | SOP5 | SOP8 | SOP8(600mil) | |
| Maximum Working Isolation Voltage | AC voltage | V _{IOWM} | 400 | 400 | 1500 | V _{RMS} |
| | DC voltage | | 565 | 565 | 2121 | V _{DC} |
| Maximum Repetitive Isolation Voltage | | V _{IORM} | 565 | 565 | 2121 | V _{PEAK} |
| Apparent Charge | Method a, after Input/output safety test subgroup 2/3, V _{ini} =V _{IOTM} , t _{ini} = 60 s, V _{pd(m)} =1.2*V _{IORM} , t _m =10s. | q _{pd} | / | / | <5 | pC |
| | Method a, after environmental tests subgroup 1, V _{ini} =V _{IOTM} , t _{ini} =60s, V _{pd(m)} =1.6*V _{IORM} , t _m =10s | | | | | pC |
| | Method b, routine test (100% production) and preconditioning (type test); V _{ini} =1.2*V _{IOTM} , t _{ini} =1s V _{pd(m)} =1.875*V _{IORM} , t _m =1s (method b1) or V _{pd(m)} =V _{ini} , t _m =t _{ini} (method b2) | | | | | pC |
| Apparent Charge | Method a, after Input/output safety test subgroup 2/3, V _{ini} =V _{IOTM} , t _{ini} = 60 s, V _{pd(m)} =1.2*V _{IORM} , t _m =10s. | q _{pd} | <5 | <5 | / | pC |
| | Method a, after environmental tests subgroup 1, V _{ini} =V _{IOTM} , t _{ini} =60s, V _{pd(m)} =1.3*V _{IORM} , t _m =10s | | | | | pC |
| | Method b, routine test (100% production) and preconditioning (type test); V _{ini} =1.2*V _{IOTM} , t _{ini} =1s V _{pd(m)} =1.5*V _{IORM} , t _m =1s (method b1) or V _{pd(m)} =V _{ini} , t _m =t _{ini} (method b2) | | | | | pC |
| Maximum Transient Isolation Voltage | t = 60 sec | V _{IOTM} | 5300 | 5300 | 12000 | V _{PEAK} |
| Maximum impulse voltage | Tested in air, 1.2/50µs waveform per IEC62368-1 | V _{IMP} | 3000 | 3000 | 6250 | V _{PEAK} |
| Maximum Surge Isolation Voltage | Test method per IEC62368-1, 1.2/50µs waveform, V _{IOSM} ≥V _{IMP} × 1.3 | V _{IOSM} | 6000 | 6000 | 10000 | V _{PEAK} |

| Description | Test Condition | Symbol | Value | | | Unit |
|-----------------------------|--|-----------|------------|------|------|-----------|
| Isolation Resistance | $V_{IO} = 500V, T_A = 25^\circ C$ | R_{IO} | $>10^{12}$ | | | Ω |
| | $V_{IO} = 500 V, 100^\circ C \leq T_A \leq 125^\circ C$ | | $>10^{11}$ | | | Ω |
| | $V_{IO} = 500 V, T_A = T_S$ | | $>10^9$ | | | Ω |
| Isolation Capacitance | $f = 1MHz$ | C_{IO} | 1.2 | | | pF |
| UL1577 | | | | | | |
| Withstand Isolation Voltage | $V_{TEST} = V_{ISO}, t = 60 s$ (qualification), $V_{TEST} = 1.2 \times V_{ISO}, t = 1$ sec, 100% production test | V_{ISO} | 3750 | 3750 | 7500 | V_{RMS} |

7.3. Safety-Limiting Values

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI7210-DSPAR and NSI7211-DSPAR.

| Description | Test Condition | Value | Unit |
|---|---|-------|------------------|
| Safety input, output, or total Power | $R_{\theta JA} = 215.9 \text{ }^\circ\text{C/W}^1$, $T_J = 150 \text{ }^\circ\text{C}$, $T_A = 25 \text{ }^\circ\text{C}$ | 579 | mW |
| Safety input, output, or supply Current | $R_{\theta JA} = 215.9 \text{ }^\circ\text{C/W}^1$, $V_I = 5.5\text{V}$, $T_J = 150 \text{ }^\circ\text{C}$, $T_A = 25 \text{ }^\circ\text{C}$ | 105 | mA |
| Safety Temperature ²⁾ | | 150 | $^\circ\text{C}$ |

- 1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP5 package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

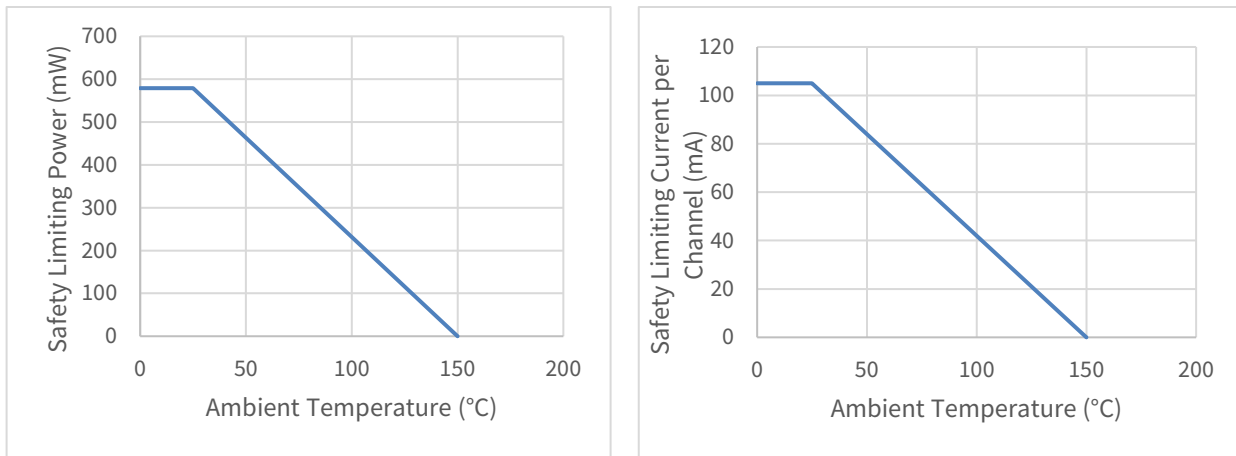


Figure 7.1 NSI7210-DSPAR and NSI7211-DSPAR Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI7211-DSPR and NSI7221-DSPR.

| Description | Test Condition | Value | Unit |
|---|---|-------|------------------|
| Safety input, output, or total Power | $R_{\theta JA} = 137.7 \text{ }^\circ\text{C/W}^1$, $T_J = 150 \text{ }^\circ\text{C}$, $T_A = 25 \text{ }^\circ\text{C}$ | 908 | mW |
| Safety input, output, or supply Current | $R_{\theta JA} = 137.7 \text{ }^\circ\text{C/W}^1$, $V_I = 5.5 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$, $T_A = 25 \text{ }^\circ\text{C}$ | 165 | mA |
| Safety Temperature ²⁾ | | 150 | $^\circ\text{C}$ |

- 1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP8 package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

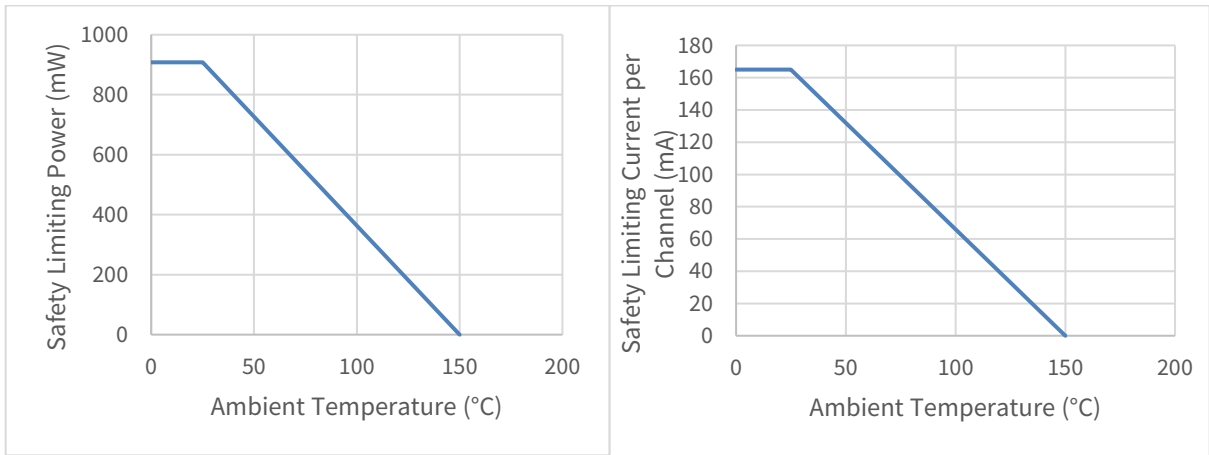


Figure 7.2 NSI7211-DSPR and NSI7221-DSPR Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI7210-DSWWAR and NSI7211-DSWWAR.

| Description | Test Condition | Value | Unit |
|---|--|-------|------|
| Safety input, output, or total Power | $R_{\theta JA} = 78.9 \text{ }^\circ\text{C/W}^1$, $T_J = 150 \text{ }^\circ\text{C}$, $T_A = 25 \text{ }^\circ\text{C}$ | 1584 | mW |
| Safety input, output, or supply Current | $R_{\theta JA} = 78.9 \text{ }^\circ\text{C/W}^1$, $V_I = 5.5 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$, $T_A = 25 \text{ }^\circ\text{C}$ | 288 | mA |
| Safety Temperature ²⁾ | | 150 | °C |

- Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP8(600mil) package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

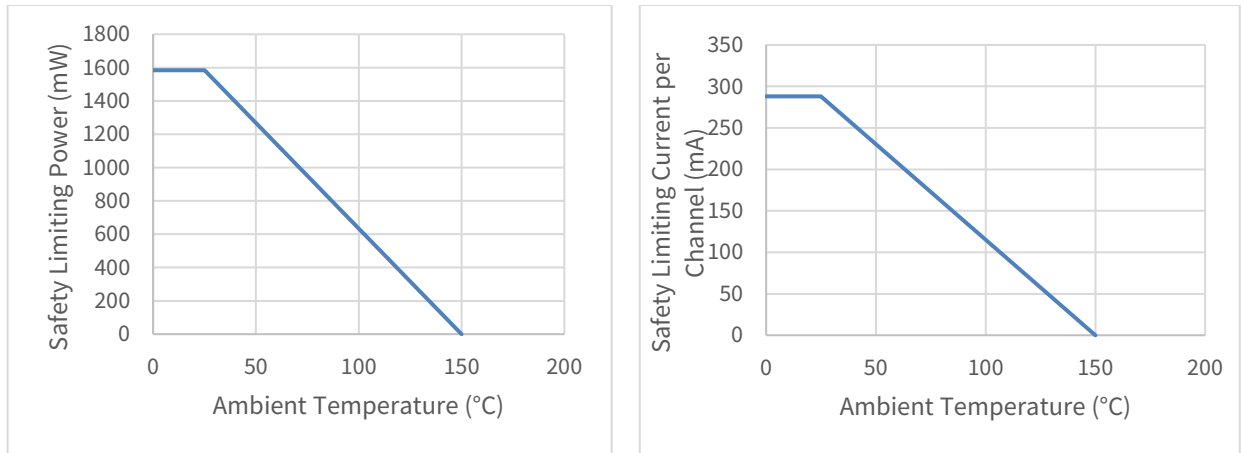


Figure 7.3 NSI7210-DSWWAR and NSI7211-DSWWAR Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

7.4. Regulatory Information

The NSI7210-DSPAR and NSI7211-DSPAR are approved or pending approval by the organizations listed in table.

| <i>UL</i> | | <i>CQC</i> | <i>TUV</i> | |
|---|---|---------------------------------|---|---------------------------------------|
| UL 1577 Component Recognition Program | Approved under CSA Component Acceptance Notice 5A | Certified according to GB4943.1 | DIN EN IEC 60747-17 (VDE 0884-17) | Certified According to EN IEC 62368-1 |
| Single Protection, 3750V _{rms} Isolation voltage | Single Protection, 3750V _{rms} Isolation voltage | Basic insulation | Basic Insulation V _{IORM} =565V _{PEAK} V _{IOTM} =5300V _{PEAK} | Basic Insulation |
| E500602 | E500602 | CQC24001426622 | R50632636 | R50574061 |

The NSI7211-DSPR and NSI7221-DSPR are approved or pending approval by the organizations listed in table.

| <i>UL</i> | <i>VDE</i> | <i>CQC</i> | <i>TUV</i> | |
|---|---|---|---------------------------------|---------------------------------------|
| UL 1577 Component Recognition Program | Approved under CSA Component Acceptance Notice 5A | DIN EN IEC 60747-17 (VDE 0884-17) | Certified according to GB4943.1 | Certified According to EN IEC 62368-1 |
| Single Protection, 3750V _{rms} Isolation voltage | Single Protection, 3750V _{rms} Isolation voltage | Basic Insulation V _{IORM} =565V _{PEAK} V _{IOTM} =5300V _{PEAK} V _{IOSM} =6000V _{PEAK} | Basic insulation | Basic Insulation |
| E500602 | E500602 | File (pending) | CQC20001264940 | R50574061 |

The NSI7210-DSWWAR and NSI7211-DSWWAR are approved or pending approval by the organizations listed in table.

| <i>UL</i> | <i>VDE</i> | <i>CQC</i> | <i>TUV</i> | |
|---|---|---|---------------------------------|---------------------------------------|
| UL 1577 Component Recognition Program | Approved under CSA Component Acceptance Notice 5A | DIN EN IEC 60747-17 (VDE 0884-17) | Certified according to GB4943.1 | Certified According to EN IEC 62368-1 |
| Single Protection, 7500V _{rms} Isolation voltage | Single Protection, 7500V _{rms} Isolation voltage | Reinforced Insulation V _{IORM} =2121V _{PEAK} V _{IOTM} =12000V _{PEAK} V _{IOSM} =10000V _{PEAK} | Reinforced insulation | Reinforced Insulation |
| E500602 | E500602 | File (pending) | CQC24001426054 | R50574061 |

8. Function Description

8.1. Overview

The NSI72xx devices are high speed and high reliability Single-Channel and Dual-Channel Opto-Emulator. NSI72xx is safety certified by UL1577 support 3.75kVrms and 7.5kVrms insulation withstand voltages, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate is up to 15Mbps, and the common-mode transient immunity (CMTI) is up to 100kV/μs. Wide supply voltage of NSI72xx support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

Table 8.1 Output status vs. Power status

| <i>V_{CC}</i> status | <i>V_E</i> status | Input Current <i>I_F</i> | Output | Comment |
|--|--|------------------------------------|-------------------------|---|
| Ready | / | > <i>I_{TH}</i> | L | Only for NSI7210. The output assumes the inverse logic state of the input single. |
| | / | < <i>I_{TH}</i> | H | |
| | / | > <i>I_{TH}</i> | L | Only for NSI72x1 with no output enable. The output assumes the inverse logic state of the input single. |
| | / | < <i>I_{TH}</i> | Z | |
| | H or NC | > <i>I_{TH}</i> | L | |
| | Only for NSI7211-DSPR. The output assumes the inverse logic state of the input single. | L | > <i>I_{TH}</i> | Z |
| | | H or NC | < <i>I_{TH}</i> | Z |
| L | | < <i>I_{TH}</i> | Z | |
| Unready | | X | Undetermined | When VCC is unready ⁽²⁾ , the output is in an undetermined state. |
| Note: 1) H=Logic high; L=Logic low; Z= High Impedance, X= Logic low or logic high; 2) The outputs are in an undetermined state when 2 V < VCC < 2.7 V. | | | | |

8.2. OOK Modulation

The NSI72xx devices are based on a capacitive isolation barrier technique and the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, as shown in Fig.8.1 & Fig.8.2, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI.

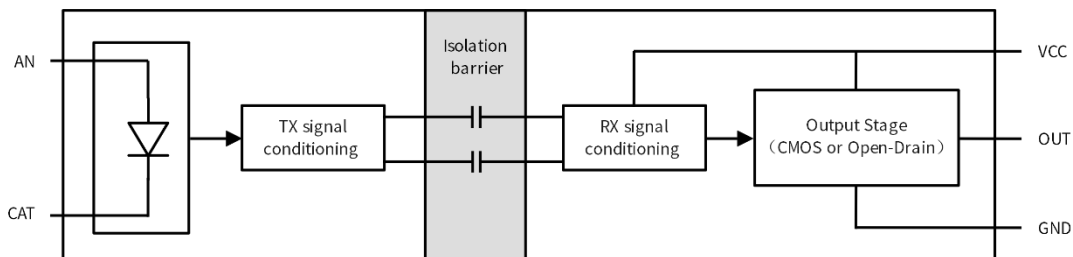


Figure 8.1 Single Channel Function Block Diagram

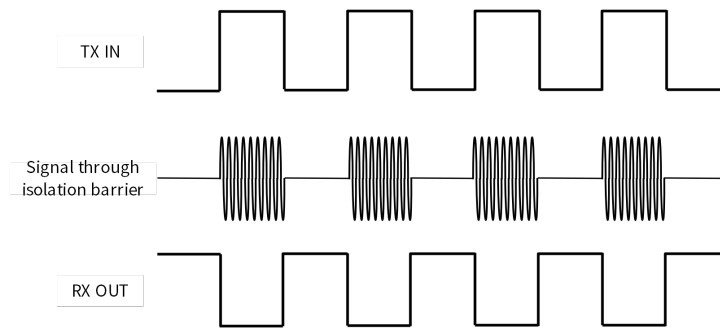


Figure 8.2 OOK Modulation

9. Application Note

9.1. Typical Application Circuit

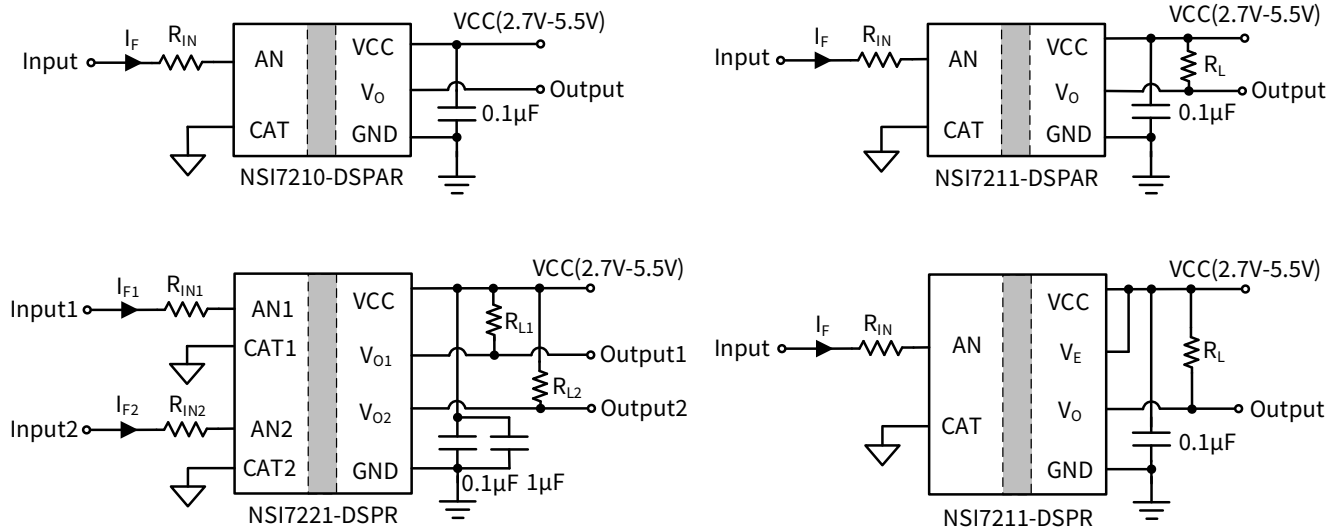


Figure9.1 Simplified Application Circuit

Note: For NSI7221, when V_O and VCC are connected to different power rails, ensure that the power rail voltage amplitude corresponding to V_O is smaller than the power rail voltage amplitude corresponding to VCC . Since there is a clamping diode between V_{O1}/V_{O2} and VCC to enhance the ESD capability of the V_{O1}/V_{O2} . If the voltage difference between V_O and VCC is too large, resulting in the diode conduction, there will be too much reverse current between VCC and V_{O1}/V_{O2} , which will quickly overload the clamping diode and damage it.

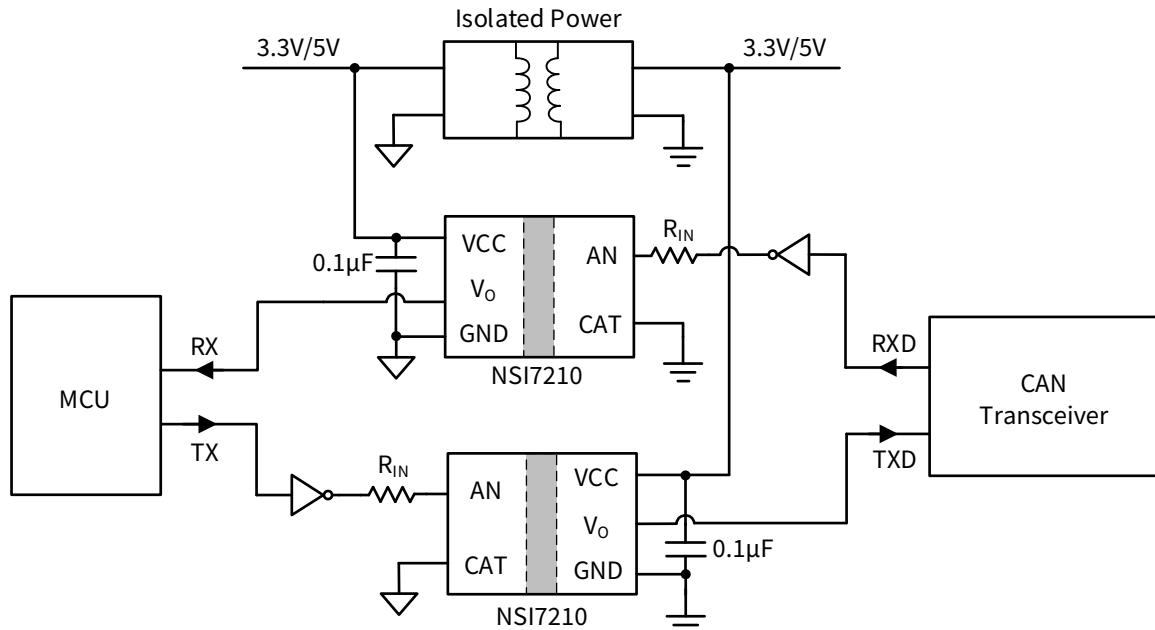


Figure9.2 Typical Isolated CAN Application

9.2. PCB Layout

NSI72xx requires a 0.1 μF bypass capacitor between VCC and GND. The capacitor should be placed as close as possible to the package. Figure 9.3 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via.

When the device operates in environments with high-frequency noise interference, it is recommended to use two parallel-connected low-ESR bypass capacitors (e.g., 0.1 μF +1 μF) on the VCC supply pin for high-frequency noise suppression across different bands. Ceramic capacitors with X5R or X7R dielectric grades are preferred for optimal performance.

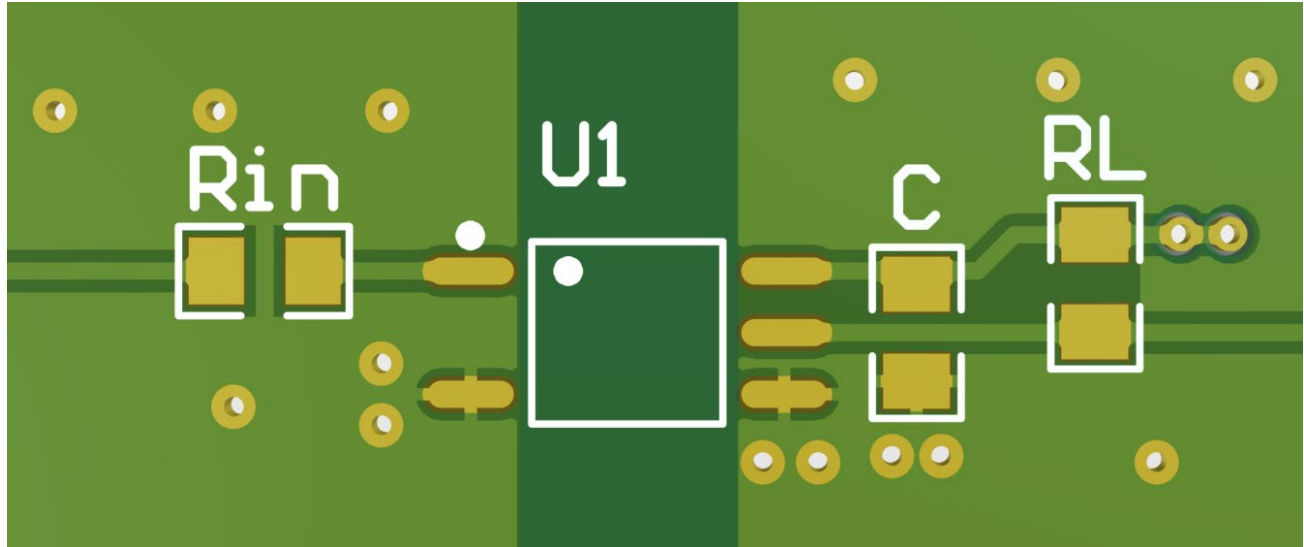
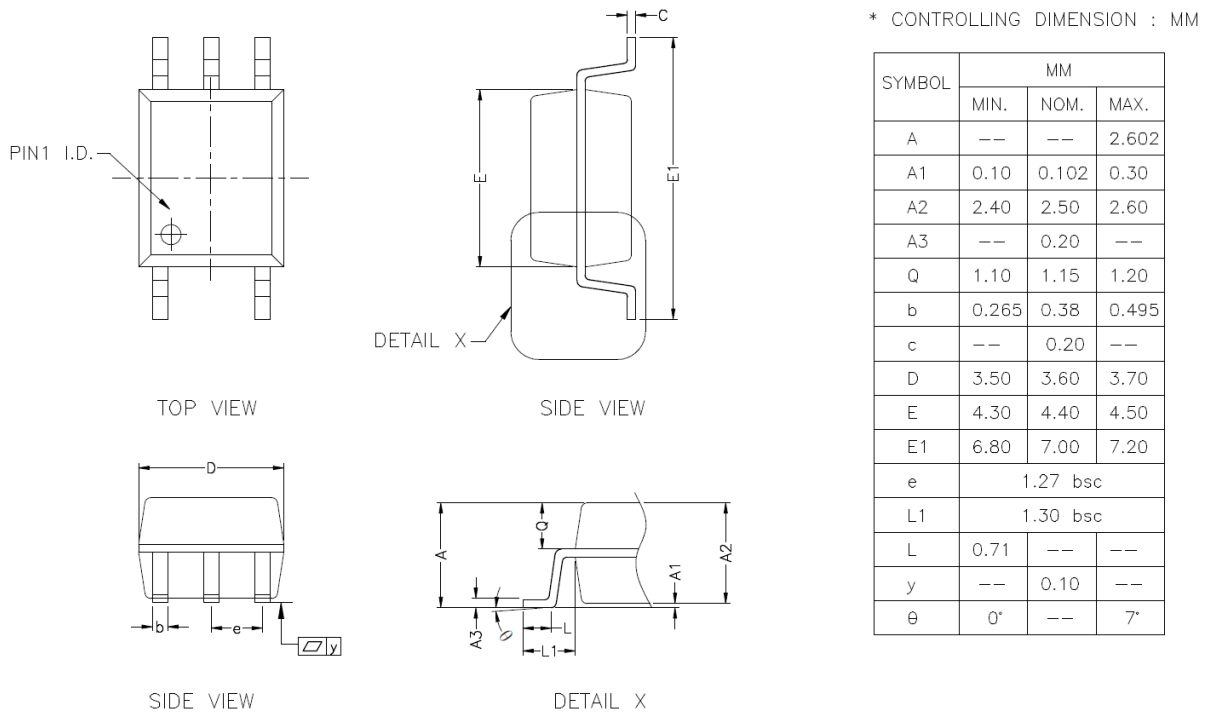


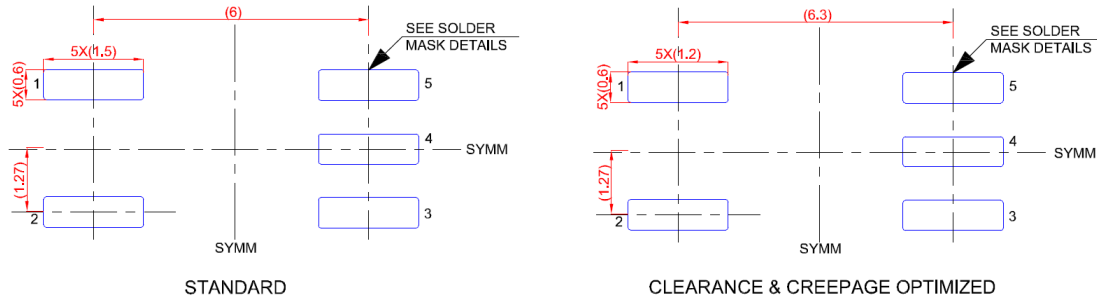
Figure 9.3 Recommended PCB Layout

10. Package Information

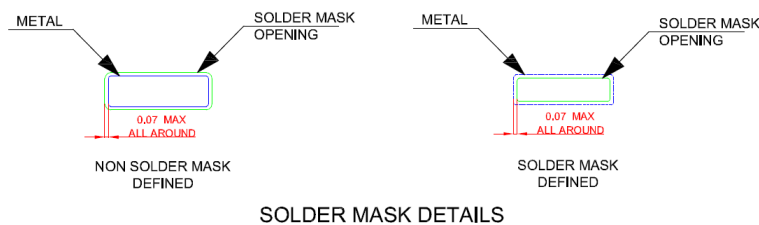


NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.1 SOP5 Package Shape and Dimension in millimeters

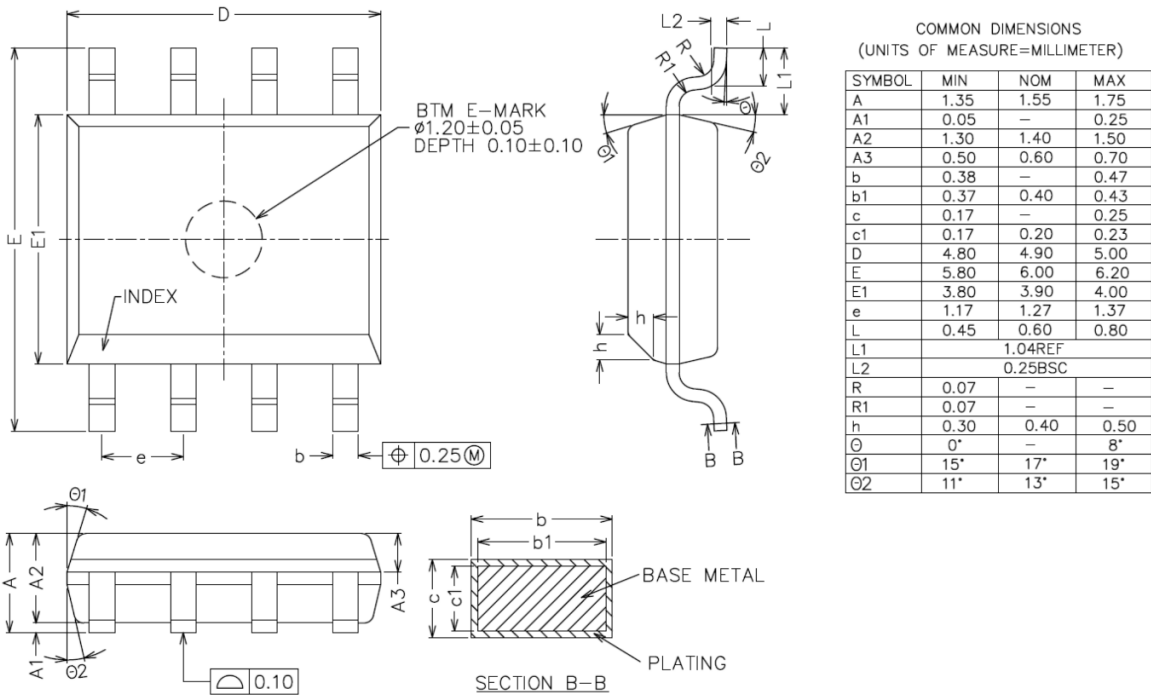


LAND PATTERN EXAMPLE(mm)



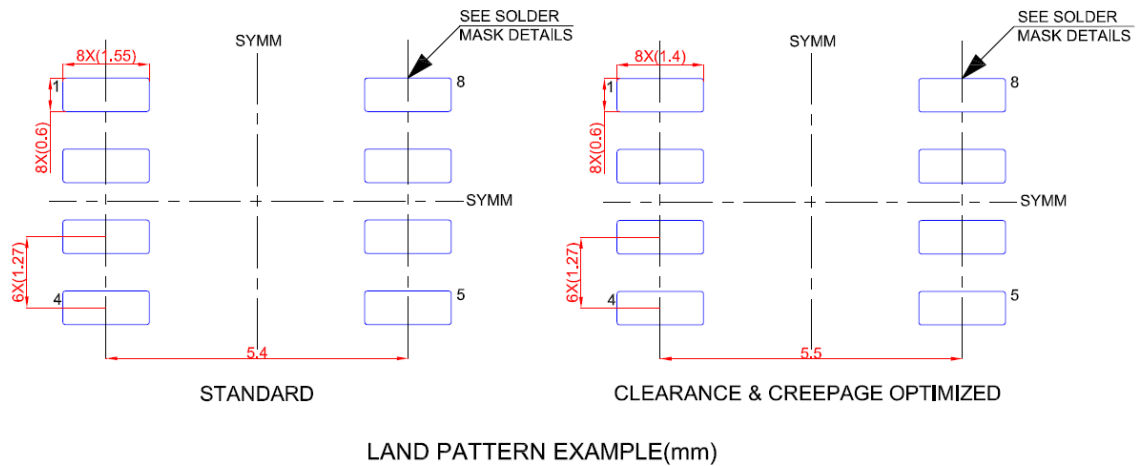
SOLDER MASK DETAILS

Figure 10.2 SOP5 Package Board Layout Example

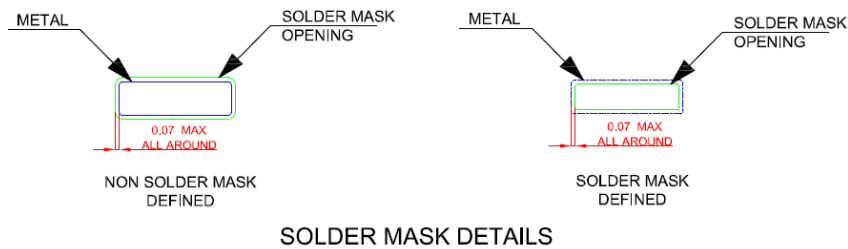


NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.3 SOP8 Package Shape and Dimension in millimeters

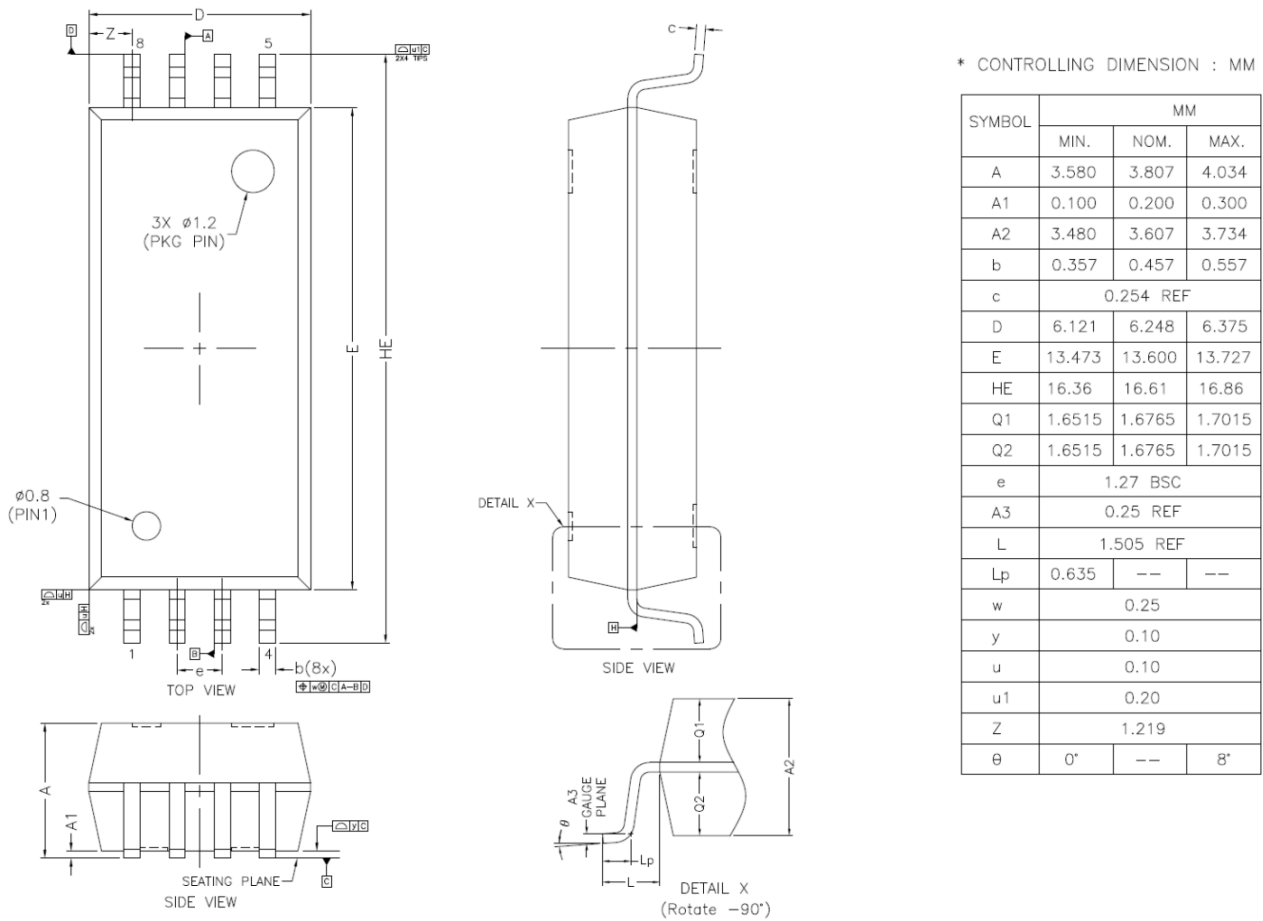


LAND PATTERN EXAMPLE(mm)



SOLDER MASK DETAILS

Figure 10.4 SOP8 Package Board Layout Example



NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.5 SOP8(600mil) Package Shape and Dimension in millimeters

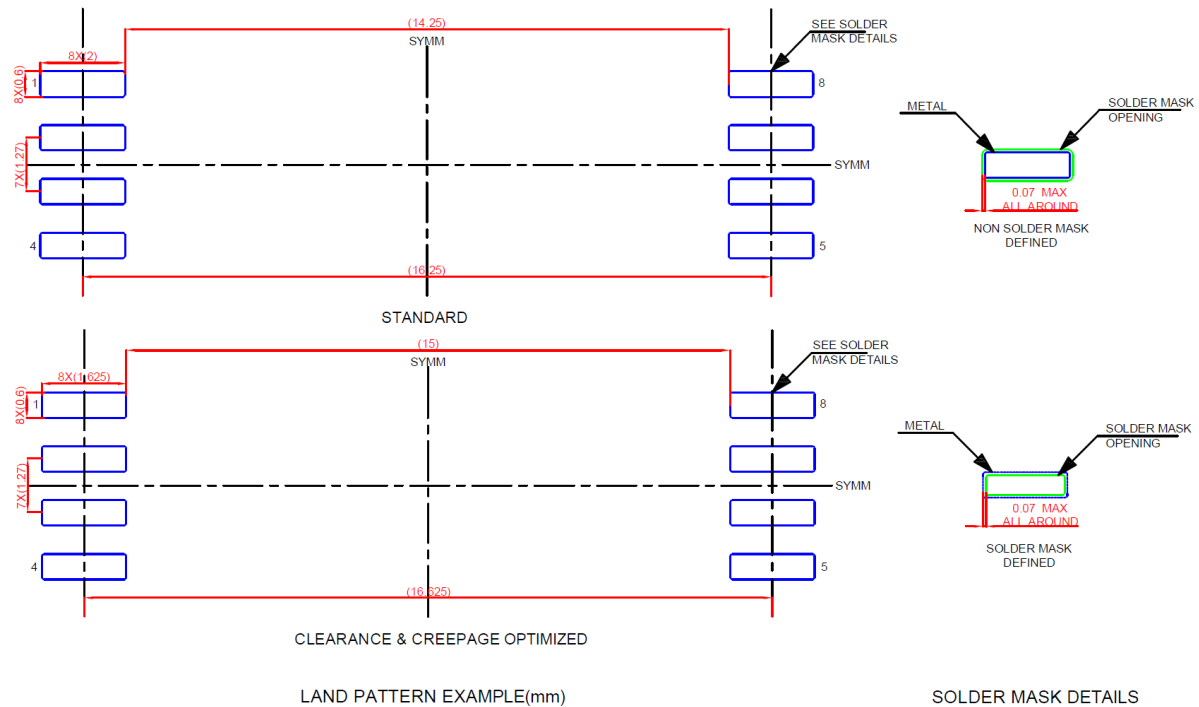


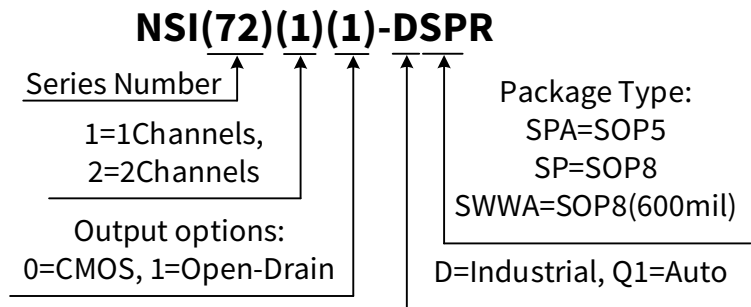
Figure 10.6 SOP8(600mil) Package Board Layout Example

11. Ordering Information

| Part Number | Output Enable | Isolation Rating (kV) | Number of inputs | Output Option | Max Data Rate (Mbps) | Default Output State | Temperature | MSL | Package Type | Package Drawing | SPQ |
|----------------|---------------|-----------------------|------------------|---------------|----------------------|----------------------|--------------|-----|--------------|-----------------|------|
| NSI7210-DSPAR | No | 3.75 | 1 | CMOS | 15 | H | -40 to 125°C | 3 | SOP5 | SOP5 | 2500 |
| NSI7211-DSPAR | No | 3.75 | 1 | Open-Drain | 15 | Z | -40 to 125°C | 3 | SOP5 | SOP5 | 2500 |
| NSI7211-DSPR | Yes | 3.75 | 1 | Open-Drain | 15 | Z | -40 to 125°C | 3 | SOP8 | SOP8 | 2500 |
| NSI7221-DSPR | No | 3.75 | 2 | Open-Drain | 15 | Z | -40 to 125°C | 3 | SOP8 | SOP8 | 2500 |
| NSI7211-DSWWAR | No | 7.5 | 1 | Open-Drain | 15 | Z | -40 to 125°C | 3 | SOP8(600mil) | SOWW8 | 1000 |
| NSI7210-DSWWAR | No | 7.5 | 1 | CMOS | 15 | H | -40 to 125°C | 3 | SOP8(600mil) | SOWW8 | 1000 |

¹ H= Logic High, Z= High Impedance.

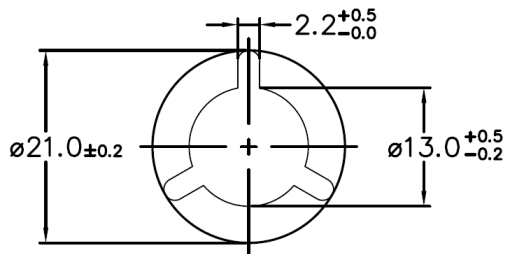
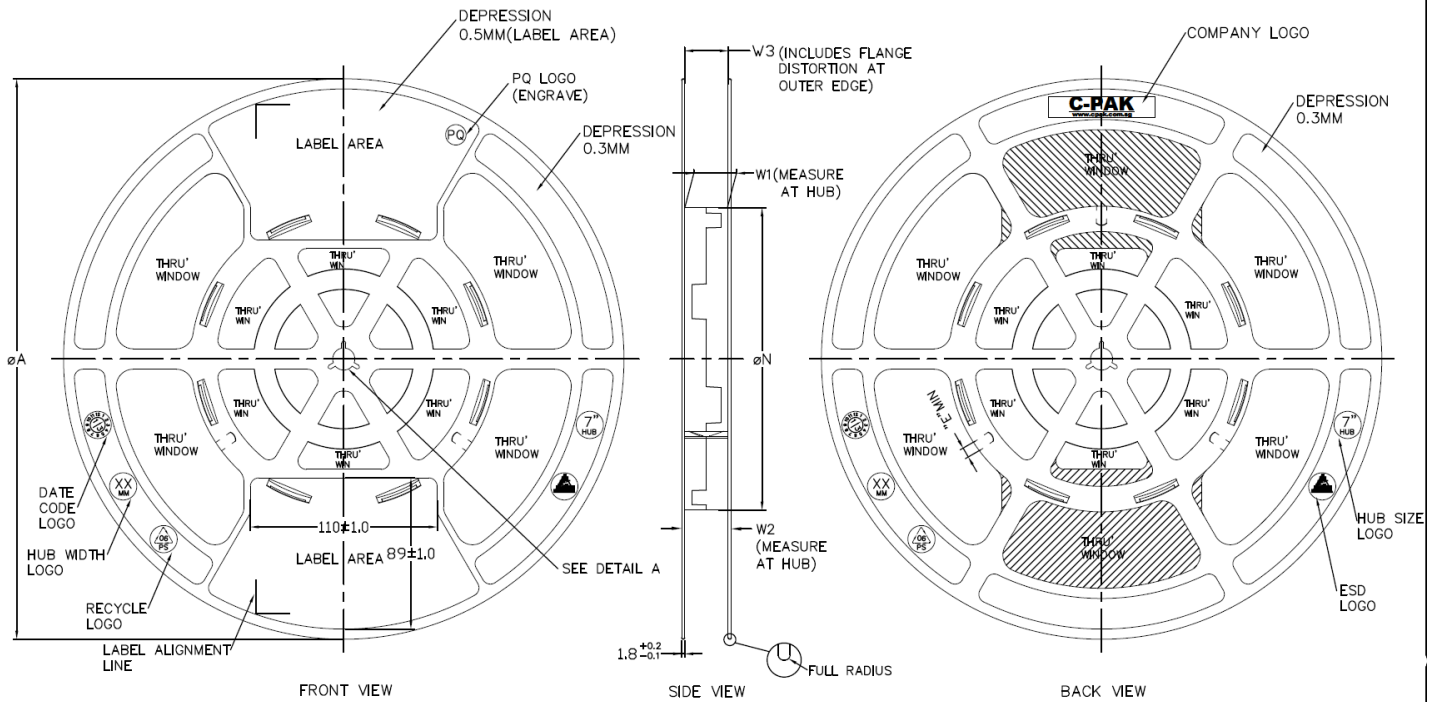
Part Number Rule:



12. Documentation Support

| Part Number | Product Folder | Datasheet | Technical Documents | Isolator selection guide |
|-------------|----------------------------|----------------------------|----------------------------|----------------------------|
| NSI72xx | Click here | Click here | Click here | Click here |

13. Tape and Reel Information

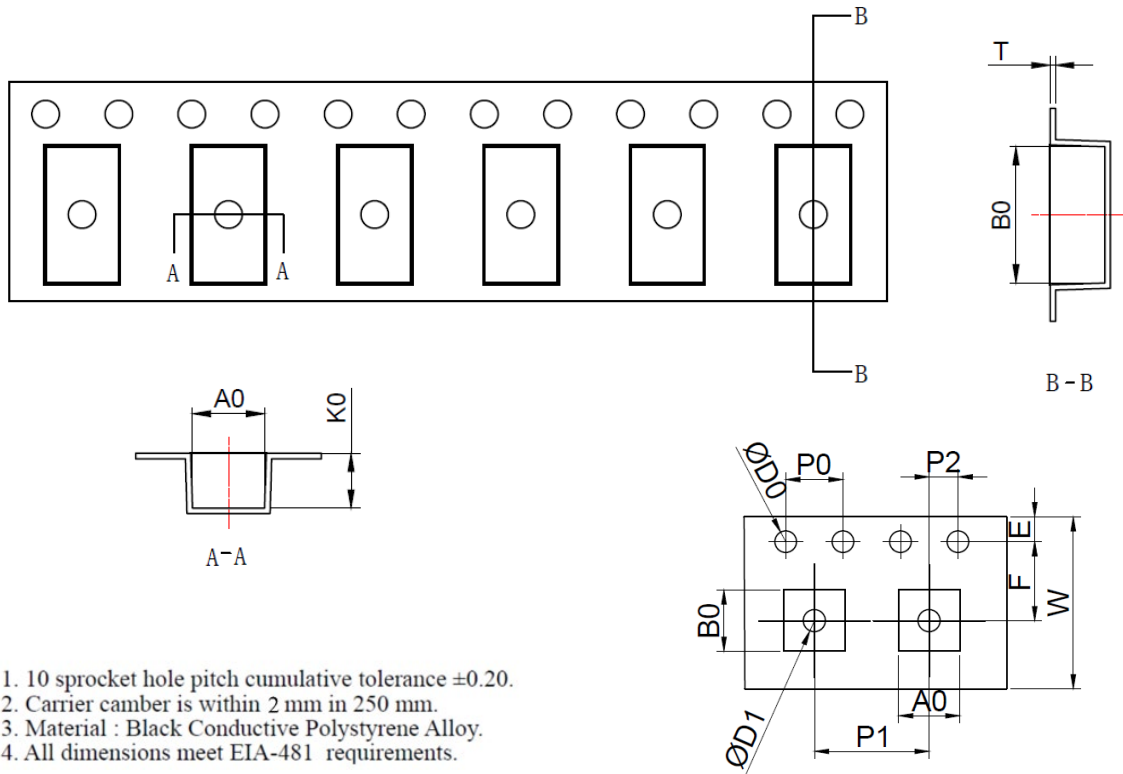


ARBOR HOLE
DETAIL A
SCALE : 3:1

| PRODUCT SPECIFICATION | | | | | | |
|-----------------------|-----------------------|-----------------------|----------------------|----------|---|---------|
| TAPE WIDTH | ϕA ± 2.0 | ϕN ± 2.0 | W1 | W2 (MAX) | W3 | E (MIN) |
| 08MM | 330 | 178 | $8.4^{+1.5}_{-0.0}$ | 14.4 | SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE | 5.5 |
| 12MM | 330 | 178 | $12.4^{+2.0}_{-0.0}$ | 18.4 | | 5.5 |
| 16MM | 330 | 178 | $16.4^{+2.0}_{-0.0}$ | 22.4 | | 5.5 |
| 24MM | 330 | 178 | $24.4^{+2.0}_{-0.0}$ | 30.4 | | 5.5 |
| 32MM | 330 | 178 | $32.4^{+2.0}_{-0.0}$ | 38.4 | | 5.5 |

| SURFACE RESISTIVITY | | | |
|---------------------|-----------------------|----------------------|------------|
| LEGEND | SR RANGE | TYPE | COLOUR |
| A | BELOW 10^{12} | ANTISTATIC | ALL TYPES |
| B | 10^6 TO 10^{11} | STATIC DISSIPATIVE | BLACK ONLY |
| C | 10^5 & BELOW 10^5 | CONDUCTIVE (GENERIC) | BLACK ONLY |
| E | 10^9 TO 10^{11} | ANTISTATIC (COATED) | ALL TYPES |

| 规格 | W | E | F | D0 | D1 | P0 | P2 | 10P0 | P1 | A0 | A1 | B0 | B1 | K0 | K1 | T |
|----|----------------|---------------|---------------|------------------|------------------|---------------|---------------|----------------|---------------|---------------|----|---------------|----|---------------|----|---------------|
| 尺寸 | 12.00 ±0.30 | 1.75 ±0.10 | 5.50 ±0.10 | 1.50 +0.10/-0 | 1.50 +0.10/-0 | 4.00 ±0.10 | 2.00 ±0.10 | 40.00 ±0.20 | 8.00 ±0.10 | 3.95 ±0.10 | / | 7.45 ±0.10 | / | 3.00 ±0.10 | / | 0.30 ±0.05 |



1. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 2 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.

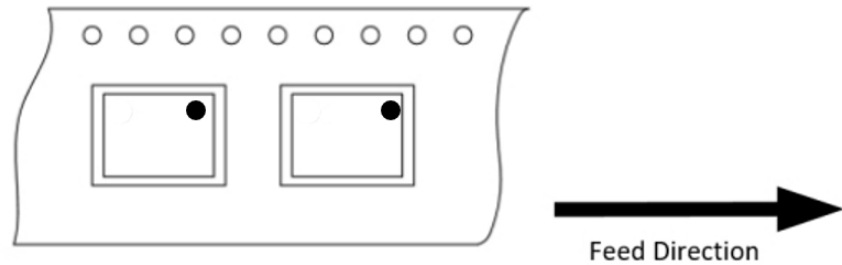
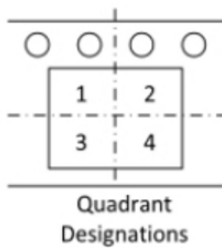
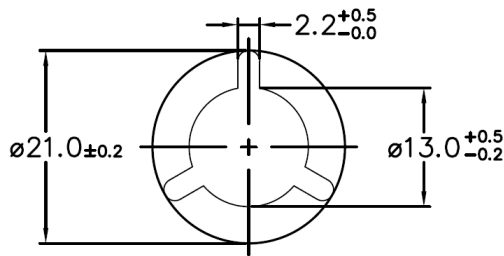
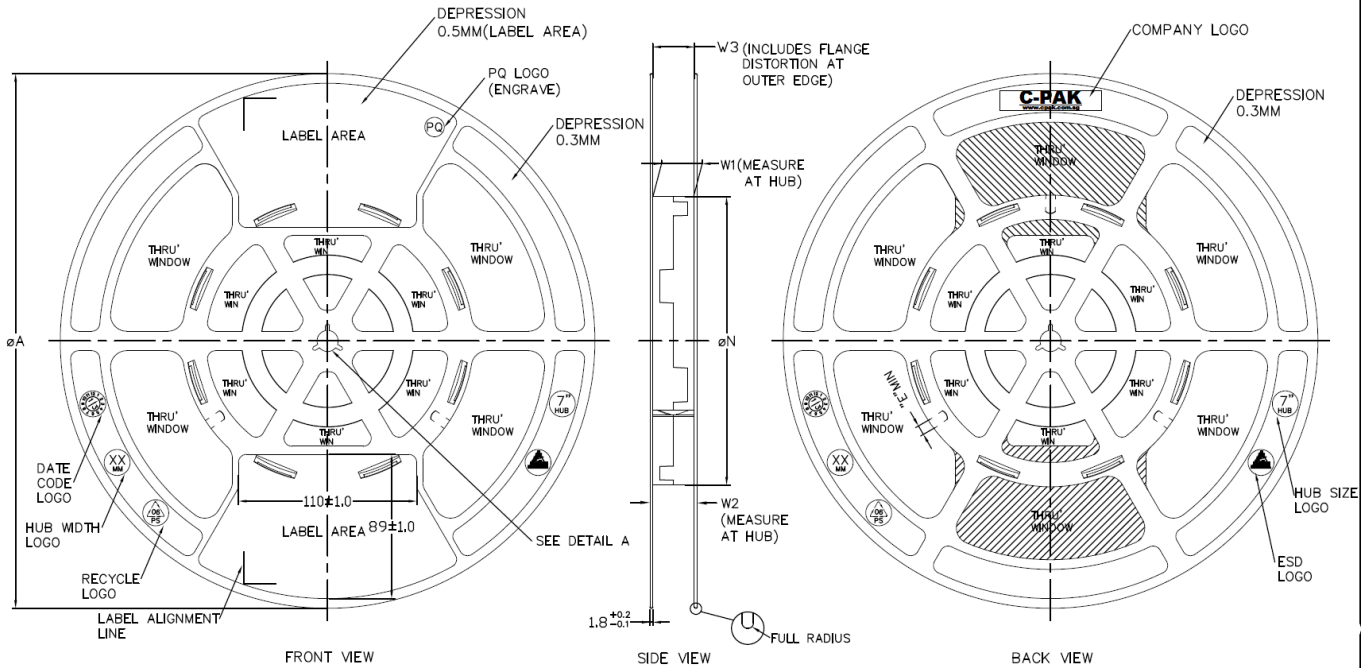


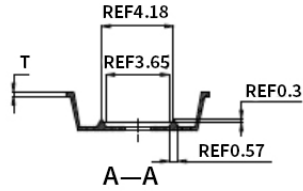
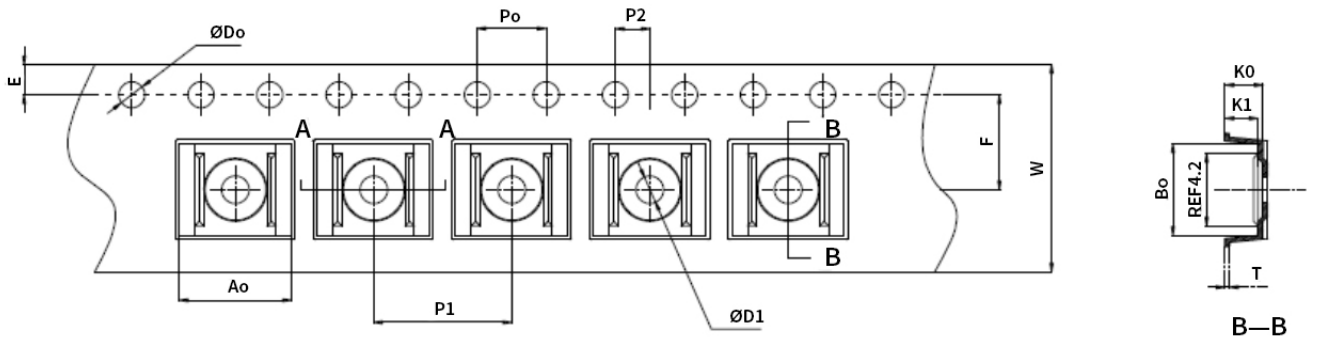
Figure 13.1 Tape and Reel Information of SOP5



ARBOR HOLE
 DETAIL A
 SCALE : 3:1

| PRODUCT SPECIFICATION | | | | | | |
|-----------------------|------------|------------|--|-------------|---|------------|
| TAPE WIDTH | ∅A ±2.0 | ∅N ±2.0 | W1 | W2 (MAX) | W3 | E (MIN) |
| 08MM | 330 | 178 | 8.4 ^{+1.5} / _{-0.0} | 14.4 | SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE | 5.5 |
| 12MM | 330 | 178 | 12.4 ^{+2.0} / _{-0.0} | 18.4 | | 5.5 |
| 16MM | 330 | 178 | 16.4 ^{+2.0} / _{-0.0} | 22.4 | | 5.5 |
| 24MM | 330 | 178 | 24.4 ^{+2.0} / _{-0.0} | 30.4 | | 5.5 |
| 32MM | 330 | 178 | 32.4 ^{+2.0} / _{-0.0} | 38.4 | | 5.5 |

| SURFACE RESISTIVITY | | | |
|---------------------|---|----------------------|------------|
| LEGEND | SR RANGE | TYPE | COLOUR |
| A | BELOW 10 ¹² | ANTISTATIC | ALL TYPES |
| B | 10 ⁸ TO 10 ¹¹ | STATIC DISSIPATIVE | BLACK ONLY |
| C | 10 ⁵ & BELOW 10 ⁵ | CONDUCTIVE (GENERIC) | BLACK ONLY |
| E | 10 ⁹ TO 10 ¹¹ | ANTISTATIC (COATED) | ALL TYPES |



Common size

| Appearance | Size(mm) |
|------------|------------|
| E | 1.75±0.10 |
| F | 5.5±0.10 |
| P2 | 2.00±0.10 |
| D0 | 1.55±0.05 |
| D1 | 1.6±0.10 |
| P0 | 4.00±0.10 |
| 10P0 | 40.00±0.20 |

Pocket size

| Appearance | Size(mm) |
|------------|------------|
| W | 12.00±0.30 |
| P1 | 8.00±0.10 |
| Ao | 6.50±0.10 |
| Bo | 5.30±0.10 |
| Ko | 2.20±0.10 |
| K1 | 1.90±0.10 |
| T | 0.30±0.05 |

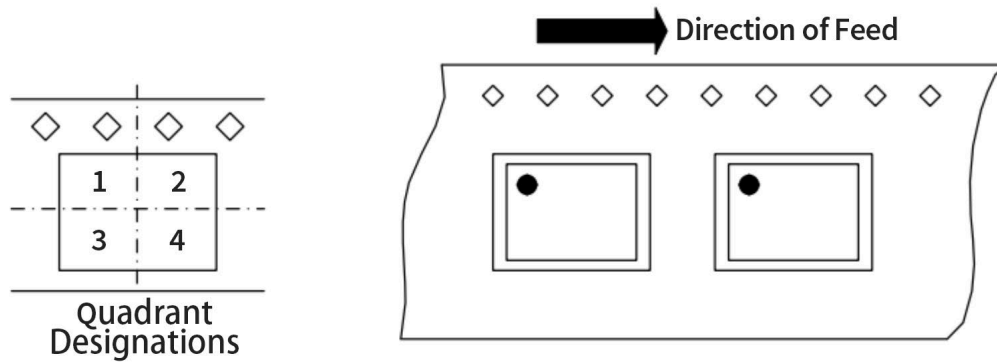
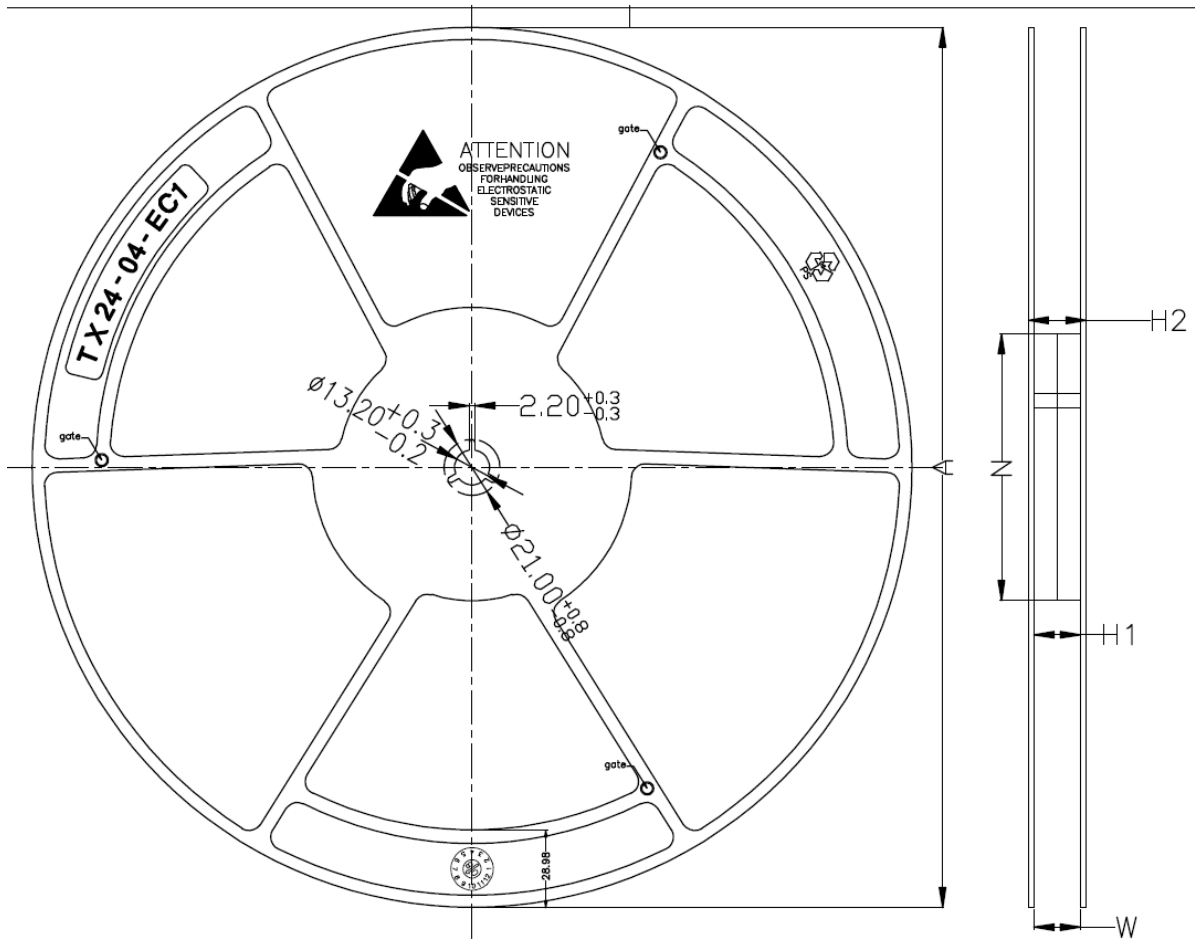
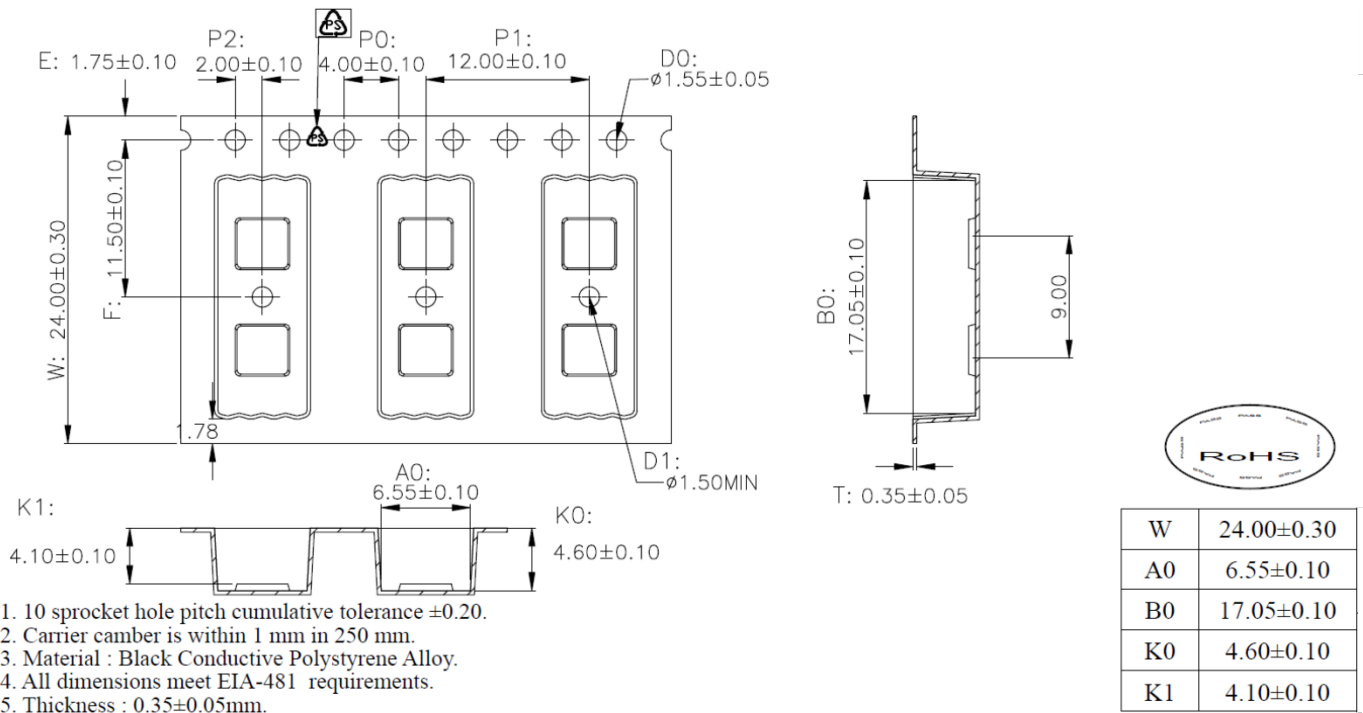


Figure 13.2 Tape and Reel Information of SOP8



| PRODUCT SPECIFICATIONS | | | | | |
|------------------------|---|---|---|---|--|
| TAPE WIDTH | $\phi A \begin{smallmatrix} +2 \\ -2 \end{smallmatrix}$ | $\phi N \begin{smallmatrix} +2 \\ -2 \end{smallmatrix}$ | $H1 \begin{smallmatrix} +2 \\ -0 \end{smallmatrix}$ | $H2 \begin{smallmatrix} +1 \\ -1 \end{smallmatrix}$ | $W \begin{smallmatrix} +3.5 \\ -0.2 \end{smallmatrix}$ |
| 24MM | 330 | 100 | 24.4 | 28.6 | 24.4 |

- NOTES:**
1. MATERIAL: DISSIPATIVE (BLACK)
 2. FLANGE WARPAGE: 3 MM MAXIMUM
 3. ALL DIMENSIONS ARE IN MM
 4. ESD - SURFACE RESISTIVITY - 10 TO 10 OHMS/SQ
 5. GENERAL TOLERANCE: ± 0.25 MM



1. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.35 ± 0.05 mm.
6. Packing length per 19" reel :130 Meters. (復卷 1: 10)
7. Component load per 13" reel : 1000 pcs.
8. Surface resistivity : $10^5 \sim 10^{10} \Omega/\text{sq}$.

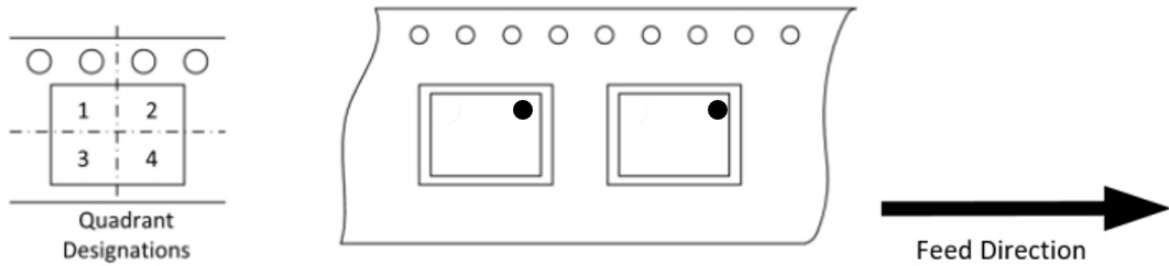


Figure 13.3 Tape and Reel Information of SOP8 (600mil)

14. Revision History

| Revision | Description | Date |
|----------|--|------------|
| 1.0 | Initial Version. | 2024/5/10 |
| 1.1 | Updated the format of Chapter 3. CMTI is divided into “CMTI _L ” and “CMTI _H ” in section 6.2, 6.3 and 6.4. Added a note for “ITH+” and “ITH-” in section 6.5. Updated DTI from “28” to “24” in section 7.1. Updated “Overvoltage Category per IEC60664-1” in section 7.1. Updated the withstand isolation voltage from 8kv to 7.5kv. Updated regulatory information in section 7.4. Added notes for NSI7221 under special application conditions in Chapter 9. | 2024/12/26 |

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as any warranty or authorization of, express or implied, including but not limited to accuracy, completeness, merchantability, fitness for a particular purpose or infringement of any third party's intellectual property rights.

You are solely responsible for your use of Novosense' products and applications, and for the safety thereof. You shall comply with all laws, regulations and requirements related to Novosense's products and applications, although information or support related to any application may still be provided by Novosense.

The resources are intended only for skilled developers designing with Novosense' products. Novosense reserves the rights to make corrections, modifications, enhancements, improvements or other changes to the products and services provided. Novosense authorizes you to use these resources exclusively for the development of relevant applications designed to integrate Novosense's products. Using these resources for any other purpose, or any unauthorized reproduction or display of these resources is strictly prohibited. Novosense shall not be liable for any claims, damages, costs, losses or liabilities arising out of the use of these resources.

For further information on applications, products and technologies, please contact Novosense (www.novosns.com).

Suzhou Novosense Microelectronics Co., Ltd