

### Product Overview

The NSI6713 is a single-channel reinforced isolated smart gate driver to drive IGBT and SiC MOSFETs in many applications. It can source and sink 10A peak current. System robustness is supported by 150kV/ $\mu$ s minimum common-mode transient immunity (CMTI). The NSI6713 includes crucial protection features such as miller clamp, DESAT, UVLO and soft turn off. UVLO and short circuit fault are reported through separate pins.

### Key Features

- 5.7kV<sub>RMS</sub> withstand isolation voltage
- SiC MOSFETs and IGBTs up to 2121V<sub>pk</sub>
- Driver side supply voltage: up to 33V with UVLO
- 10A peak source and sink output current
- High CMTI:  $\pm 150\text{kV}/\mu\text{s}$
- Monitor status of device on FLT and RDY
- 80ns typical propagation delay
- 420mA soft turn off current
- 50ns maximum pulse width distortion
- Active short circuit protection option
- RoHS & REACH Compliant
- Lead-free component, suitable for lead-free soldering profile: 260°C, MSL3
- AEC-Q100 Qualified for Grade1: T<sub>A</sub> from -40°C to 125°C

### Safety Regulatory Approvals

- UL recognition: 5700V<sub>RMS</sub>
- DIN EN IEC 60747-17(VDE 0884-17)
- CSA component notice 5A
- CQC certification per GB4943.1

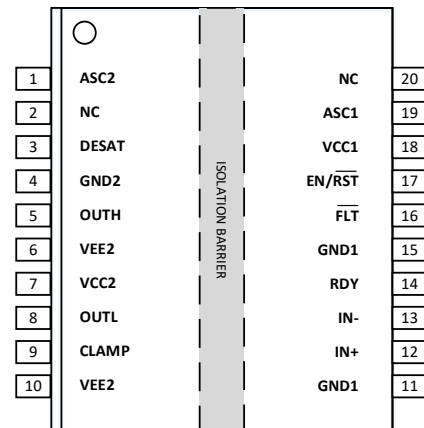
### Applications

- Traction Inverter for EVs
- On-board Charger and charging pile
- DC/DC Converter for HEV/EVs

### Device Information

| Part Number        | over current protection | ASC       | STO current             |
|--------------------|-------------------------|-----------|-------------------------|
| NSI6713ASC-Q1SSWAR | DESAT(9V)               | ASC1/ASC2 | I <sub>STO</sub> =420mA |

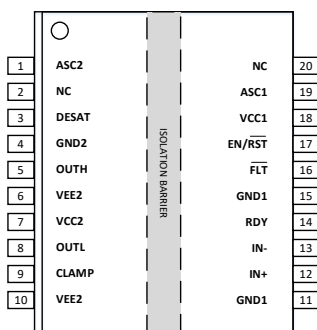
### Pin map



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## 1. Pin Configuration and Functions



NSI6713ASC

| <b>SYMBOL</b>       | <b>Pin NO.</b> | <b>FUNCTION</b>                                                                                                                |
|---------------------|----------------|--------------------------------------------------------------------------------------------------------------------------------|
| <b>NSI6713ASC</b>   |                |                                                                                                                                |
| ASC2                | 1              | Active Short Circuit pin in output side. If ASC is set to high, the OUTH pin will be forced to output high under the emergency |
| NC                  | 2, 20          | Not connect                                                                                                                    |
| DESAT               | 3              | DESAT for Fast overcurrent and short circuit protection                                                                        |
| GND2                | 4              | Driver side ground pin                                                                                                         |
| OUTH                | 5              | Driver source output pin                                                                                                       |
| VEE2                | 6, 10          | Driver side negative supply pin                                                                                                |
| VCC2                | 7              | Driver side positive supply pin                                                                                                |
| OUTL                | 8              | Driver sink output pin                                                                                                         |
| CLAMP               | 9              | Internal active miller clamp to prevent false turn-on                                                                          |
| GND1                | 11, 15         | Input-side ground pin                                                                                                          |
| IN+                 | 12             | Non-inverting gate driver control input                                                                                        |
| IN-                 | 13             | Inverting gate driver control input                                                                                            |
| RDY                 | 14             | Power good signal. Active low to report under voltage lock                                                                     |
| $\overline{FLT}$    | 16             | Fault output pin. Active low to report over current or short circuit                                                           |
| $\overline{RST}/EN$ | 17             | Enable the device if this pin is set to high, or set low to reset the fault signal under DESAT condition                       |
| VCC1                | 18             | Input-side power supply                                                                                                        |
| ASC1                | 19             | Active Short Circuit pin in input side. If ASC is set to high, the OUTH pin will be forced to output high under the emergency  |

## 2. Absolute Maximum Ratings

| Parameters                        | Symbol                                   | Min           | Max           | Unit |
|-----------------------------------|------------------------------------------|---------------|---------------|------|
| Driver Side Supply Voltage        | $V_{CC2}-V_{EE2}$                        | -0.3          | 38            | V    |
| Driver Side Supply Voltage        | $V_{CC2}-GND2$                           | -0.3          | 38            | V    |
| Driver Side Supply Voltage        | $V_{EE2}-GND2$                           | -17.5         | 0.3           | V    |
| Output Signal Voltage – DC        | $V_{OUTH}$ , $V_{OUTL}$ ,<br>$V_{CLAMP}$ | $V_{EE2}-0.3$ | $V_{CC2}$     | V    |
| Input Side Supply Voltage         | $V_{CC1}$                                | -0.3          | 6             | V    |
| Input Signal Voltage – DC         | $V_{IN+}$ , $V_{IN-}$ , $V_{RST}$        | $GND1-0.3$    | $V_{CC1}+0.3$ | V    |
| RDY, FLT (Input Side) voltage     | $V_{RDY}$ , $V_{FLT}$                    | $GND1-0.3$    | $V_{CC1}$     | V    |
| DESAT (Driver Side) input voltage | $V_{DESAT}$                              | $GND2-0.3$    | $V_{CC2}+0.3$ | V    |
| ASC2 input voltage                | $V_{ASC2}$                               | $GND2-0.3$    | $GND2+6$      | V    |
| ASC1 input voltage                | $V_{ASC1}$                               | $GND1-0.3$    | $GND1+6$      | V    |
| FLT and RDY input current         | $I_{FLT}$ , $I_{RDY}$                    |               | 20            | mA   |
| Operating Junction Temperature    | $T_J$                                    | -40           | 150           | °C   |
| Storage Temperature               | $T_{stg}$                                | -65           | 150           | °C   |

## 3. ESD Ratings

|                         |                                                         | Symbol         | Value | Unit |
|-------------------------|---------------------------------------------------------|----------------|-------|------|
| Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> | $V_{ESD\_HBM}$ | ±3000 | V    |
|                         | Charged-device model (CDM), per AEC Q100-011            | $V_{ESD\_CDM}$ | ±1500 | V    |

- 1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 4. Recommended Operating Conditions

| Parameters                                      | Symbol                   | Min                  | Max                  | Unit |
|-------------------------------------------------|--------------------------|----------------------|----------------------|------|
| Ambient Temperature                             | $T_A$                    | -40                  | 125                  | °C   |
| Input Side Supply Voltage                       | $V_{CC1-GND1}$           | 3                    | 5.5                  | V    |
| Driver Side Supply Voltage                      | $V_{CC2-GND2}$           | 13                   | 33                   | V    |
| Driver Side Supply Voltage                      | $V_{CC2-V_{EE2}}$        | -                    | 33                   | V    |
| ASC (Reference to GND1 or GND2)                 | $V_{ASC1}$               | GND1                 | GND1+5               | V    |
|                                                 | $V_{ASC2}$               | GND2                 | GND2+5               | V    |
| IN+, IN-, $\overline{RST}/EN$ (Respect to GND1) | High level input voltage | $0.7 \times V_{CC1}$ | $V_{CC1}$            | V    |
|                                                 | Low level input voltage  | 0                    | $0.3 \times V_{CC1}$ |      |

## 5. Thermal Information

| Parameters                                   | Symbol          | SSOW20 | Unit |
|----------------------------------------------|-----------------|--------|------|
| Junction-to-ambient thermal resistance       | $R_{\theta JA}$ | 77.7   | °C/W |
| Junction-to-top characterization parameter   | $\Psi_{JT}$     | 9.4    | °C/W |
| Junction-to-board characterization parameter | $\Psi_{JB}$     | 27     | °C/W |
| Junction-to-case(top) thermal resistance     | $R_{JC(top)}$   | 38.5   | °C/W |
| Junction-to-board thermal resistance         | $R_{\theta JB}$ | 30     | °C/W |

- 1) Standard JESD51-7 High Effective Thermal Conductivity Test Board (2S2P) in an environment described in JESD51-2a.
- 2) Standard JESD51-7 High Effective Thermal Conductivity Test Board (2S2P) by transient dual interface test method described in JESD51-14.
- 3) Obtained by Simulating in an environment described in JESD51-2a.

## 6. Specifications

### 6.1. DC Electrical Characteristics

All min and max specifications are at  $T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . Typical values are tested at  $V_{CC1} = 3.3\text{V}$  or  $5\text{V}$ ,  $V_{CC2} = 15\text{V}$  or  $33\text{V}$ ,  $V_{EE2} = \text{GND2}$ .

| Parameter                                     | Symbol                                | Min  | Typ  | Max  | Unit | Condition                                                     |
|-----------------------------------------------|---------------------------------------|------|------|------|------|---------------------------------------------------------------|
| Input Side Supply                             |                                       |      |      |      |      |                                                               |
| Input side Supply Quiescent Current           | I <sub>CC1_ON</sub>                   | 2.5  | 3.6  | 4.5  | mA   | V <sub>CC1</sub> =5V,<br>OUT=High                             |
|                                               | I <sub>CC1_OFF</sub>                  | 0.6  | 1.5  | 2.6  |      | V <sub>CC1</sub> =5V,<br>OUT=Low                              |
| V <sub>CC1</sub> UVLO Rising Threshold        | V <sub>CC1_ON</sub>                   | 2.5  | 2.72 | 2.95 | V    |                                                               |
| V <sub>CC1</sub> UVLO Falling Threshold       | V <sub>CC1_OFF</sub>                  | 2.35 | 2.57 | 2.75 | V    |                                                               |
| V <sub>CC1</sub> UVLO Hysteresis              | V <sub>CC1_HYS</sub> <sup>(1)</sup>   |      | 0.15 |      | V    |                                                               |
| V <sub>CC1</sub> UVLO deglitch time           | t <sub>VCC1_FIL</sub> <sup>(1)</sup>  |      | 7    |      | μs   |                                                               |
| V <sub>CC1</sub> UVLO on delay to output high | t <sub>VCC1H_OUT</sub> <sup>(1)</sup> |      | 60   |      |      | IN+=V <sub>CC1</sub> IN-<br>=GND1                             |
| V <sub>CC1</sub> UVLO on delay to output low  | t <sub>VCC1L_OUT</sub> <sup>(1)</sup> |      | 5    |      |      |                                                               |
| V <sub>CC1</sub> UVLO on delay to RDY high    | t <sub>VCC1H_RDY</sub> <sup>(1)</sup> |      | 60   |      |      | $\overline{RST}/EN$ =V <sub>CC1</sub>                         |
| V <sub>CC1</sub> UVLO on delay to RDY low     | t <sub>VCC1L_RDY</sub> <sup>(1)</sup> |      | 5    |      |      |                                                               |
| Driver Side Supply                            |                                       |      |      |      |      |                                                               |
| Driver side Supply Quiescent Current          | I <sub>CC2_ON</sub>                   | 3.4  | 4.6  | 6    | mA   | V <sub>CC2</sub> =15V,<br>V <sub>EE2</sub> =GND2,<br>OUT=High |
|                                               | I <sub>CC2_OFF</sub>                  | 2    | 4    | 5.5  |      | V <sub>CC2</sub> =15V,<br>V <sub>EE2</sub> =GND2,<br>OUT=Low  |
| V <sub>CC2</sub> UVLO Rising Threshold        | V <sub>CC2_ON</sub>                   | 10.5 | 12.1 | 13   | V    |                                                               |
| V <sub>CC2</sub> UVLO Falling Threshold       | V <sub>CC2_OFF</sub>                  | 9.9  | 11.1 | 11.8 | V    |                                                               |
| V <sub>CC2</sub> UVLO Hysteresis              | V <sub>CC2_HYS</sub> <sup>(1)</sup>   |      | 1    |      | V    |                                                               |
| V <sub>CC2</sub> UVLO deglitch time           | t <sub>VCC2_FIL</sub> <sup>(1)</sup>  |      | 4.9  |      | μs   |                                                               |
| V <sub>CC2</sub> UVLO on delay to output high | t <sub>VCC2H_OUT</sub> <sup>(1)</sup> |      | 14   |      |      | IN+=V <sub>CC1</sub> IN-<br>=GND1                             |
| V <sub>CC2</sub> UVLO on delay to output low  | t <sub>VCC2L_OUT</sub> <sup>(1)</sup> |      | 5.5  |      |      |                                                               |
| V <sub>CC2</sub> UVLO on delay to RDY high    | t <sub>VCC2H_RDY</sub> <sup>(1)</sup> |      | 18   |      |      | $\overline{RST}/EN$ =V <sub>CC1</sub> ,<br>DESAT=GND2         |
| V <sub>CC2</sub> UVLO on delay to RDY low     | t <sub>VCC2L_RDY</sub> <sup>(1)</sup> |      | 10   |      |      |                                                               |
| Input Pin Characteristic                      |                                       |      |      |      |      |                                                               |
| Logic High Input Threshold (IN+, IN-, RST)    | V <sub>INH</sub>                      | 2.2  | 2.8  | 3.5  | V    | V <sub>CC1</sub> =5V                                          |
| Logic Low Input Threshold (IN+, IN-, RST)     | V <sub>INL</sub>                      | 1.5  | 2.2  | 2.9  | V    | V <sub>CC1</sub> =5V                                          |

| Parameter                                    | Symbol           | Min  | Typ            | Max | Unit       | Condition                                                                          |
|----------------------------------------------|------------------|------|----------------|-----|------------|------------------------------------------------------------------------------------|
| Input Hysteresis Voltage (IN+, IN-, RST)     | $V_{hys\_IN}$    |      | 0.6            |     | V          | $V_{CC1}=5V$                                                                       |
| IN+ Input Current                            | $I_{IN+\_H}$     |      | 95             |     | $\mu A$    | $V_{IN+}=5V$                                                                       |
| IN- Input Current                            | $I_{IN-\_L}$     |      | -95            |     | $\mu A$    | $V_{IN-}=GND1$                                                                     |
| RST Input Current                            | $I_{RST\_H}$     |      | 105            |     | $\mu A$    | $V_{RST}=5V$                                                                       |
| IN+ pull down resistance                     | $R_{IN+}$        |      | 55             |     | k $\Omega$ |                                                                                    |
| IN- pull up resistance                       | $R_{IN-}$        |      | 55             |     |            |                                                                                    |
| RST pull down resistance                     | $R_{RST}$        |      | 50             |     |            |                                                                                    |
| RST deglitch filter time for Enable/Shutdown | $t_{min\_RST}$   | 28   | 40             | 60  | ns         |                                                                                    |
| RST deglitch filter time for Resetting FLT   | $t_{RST\_FIL}$   | 400  | 660            | 800 | ns         |                                                                                    |
| <b>FLT Reporting</b>                         |                  |      |                |     |            |                                                                                    |
| Open drain low output voltage                | $V_{FLT\_L}$     |      |                | 0.3 | V          | $I_{SINK\_FLT}=5mA$                                                                |
| FLT mute time                                | $t_{FLT\_MUTE}$  | 0.55 |                | 1   | ms         |                                                                                    |
| FLT open drain output on resistance          | $R_{ODON\_FLT}$  |      | 31             |     | $\Omega$   | $I_{SINK\_FLT}=5mA$                                                                |
| <b>RDY Reporting</b>                         |                  |      |                |     |            |                                                                                    |
| Open drain low output voltage                | $V_{RDY\_L}$     |      |                | 0.3 | V          | $I_{SINK\_RDY}=5mA$                                                                |
| $V_{CC2}$ UVLO RDY low minimum holding time  | $t_{RDY\_HLD}$   | 0.55 |                | 1   | ms         |                                                                                    |
| RDY open drain output on resistance          | $R_{ODON\_RDY}$  |      | 31             |     | $\Omega$   | $I_{SINK\_RDY}=5mA$                                                                |
| <b>Output Pin Characteristic</b>             |                  |      |                |     |            |                                                                                    |
| High Level Output Voltage                    | $V_{OH}$         |      | $V_{CC2}-0.1$  |     | V          | $I_{OUT}=-100mA$ ,<br>$V_{IN+}=High$ , $V_{IN-}=Low$                               |
| Low Level Output Voltage                     | $V_{OL}$         |      | 40             |     | mV         | $I_{OUT}=100mA$ ,<br>$V_{IN+}=Low$ , $V_{IN-}=Low$                                 |
| Output pull-up resistance                    | $R_{OH}$         |      | 0.7            |     | $\Omega$   | $I_{OUT}=-100mA$ ,<br>$V_{IN+}=High$ ,<br>$V_{IN-}=Low$                            |
| Output pull-down resistance                  | $R_{OL}$         |      | 0.4            |     | $\Omega$   | $I_{OUT}=100mA$ ,<br>$V_{IN+}=Low$ ,<br>$V_{IN-}=High$                             |
| High Level Peak Output Current               | $I_{OUTH}^{(1)}$ |      | 10             |     | A          |                                                                                    |
| Low Level Peak Output Current                | $I_{OUTL}^{(1)}$ |      | 10             |     | A          |                                                                                    |
| OUT Short Circuit Clamping Voltage           | $V_{CLP\_OUT}$   |      | $V_{CC2}+1.35$ |     | V          | $V_{IN+}=High$ , $V_{IN-}=Low$ ,<br>$I_{OUTL}=0.5A$ ,<br>pulse<br>width<10 $\mu s$ |

| Parameter                            | Symbol                                | Min | Typ                   | Max  | Unit | Condition                                                                                      |
|--------------------------------------|---------------------------------------|-----|-----------------------|------|------|------------------------------------------------------------------------------------------------|
| OUT Active Pull-Down Voltage         | V <sub>SD_OUT</sub>                   | 1.5 | 2.4                   | 3    | V    | V <sub>CC2</sub> =OPEN,<br>I <sub>OUTL</sub> =0.1×I <sub>OUTL</sub> (ty<br>p)                  |
| Internal miller clamp                |                                       |     |                       |      |      |                                                                                                |
| Clamp Threshold Voltage              | V <sub>CLAMP_TH</sub>                 | 1.5 | 2.1                   | 2.5  | V    | V <sub>CLAMP</sub> falling,<br>V <sub>IN+</sub> =Low, V <sub>IN-</sub> =Low                    |
| Clamp Delay                          | t <sub>DCLMP</sub> <sup>(2)</sup>     |     | 70                    |      | ns   |                                                                                                |
| Miller clamp pull down resistance    | R <sub>clamp</sub>                    |     | 0.6                   |      | Ω    | I <sub>CLAMP</sub> =0.1A                                                                       |
| Output low clamp voltage             | V <sub>clamp_L</sub>                  |     | 60                    |      | mV   | I <sub>CLAMP</sub> =0.1A                                                                       |
| Output low clamp current             | I <sub>clamp</sub> <sup>(1)</sup>     |     | 5.7                   |      | A    |                                                                                                |
| CLAMP Short Circuit Clamping Voltage | V <sub>CLP_CLAMP</sub> <sup>(1)</sup> |     | V <sub>CC2</sub> +1.4 |      | V    | V <sub>IN+</sub> =High, V <sub>IN-</sub> =Low,<br>I <sub>OUTH</sub> =0.5A, pulse<br>width<10μs |
|                                      |                                       |     | V <sub>CC2</sub> +0.9 |      |      | V <sub>IN+</sub> =High, V <sub>IN-</sub> =Low,<br>I <sub>CLAMP</sub> =20mA                     |
| DESAT PROTECTION                     |                                       |     |                       |      |      |                                                                                                |
| Blanking Capacitor Discharge Current | I <sub>DCHG</sub>                     | 20  | 43                    | 60   | mA   | V <sub>DESAT</sub> =6V                                                                         |
| Blanking Capacitor Charge Current    | I <sub>CHG</sub>                      | 430 | 510                   | 570  | μA   | V <sub>DESAT</sub> =2V                                                                         |
| Leading edge blank time              | t <sub>DESAT_LEB</sub> <sup>(1)</sup> |     | 230                   |      | ns   |                                                                                                |
| DESAT deglitch filter time           | t <sub>DESAT_FIL</sub>                | 50  | 160                   | 230  | ns   |                                                                                                |
| DESAT sense to OUT(L) 90% delay      | t <sub>DESAT_OFF</sub>                | 150 | 230                   | 300  | ns   |                                                                                                |
| DESAT sense to FLT low delay         | t <sub>DESAT_FLT</sub>                |     | 1.4                   |      | μs   |                                                                                                |
| Detection Threshold                  | V <sub>DESAT_TH</sub>                 | 8.5 | 9.1                   | 10   | V    |                                                                                                |
| Soft turn off current                | I <sub>STO</sub>                      | 250 | 420                   | 600  | mA   |                                                                                                |
| ASC2 Pin Characteristic              |                                       |     |                       |      |      |                                                                                                |
| Logic High Input Threshold           | V <sub>ASC2H</sub>                    | 2.7 | 2.8                   | 3.2  | V    |                                                                                                |
| Logic Low Input Threshold            | V <sub>ASC2L</sub>                    | 1.3 | 1.52                  | 1.8  | V    |                                                                                                |
| ASC2 to output rising edge delay     | t <sub>ASC2_r</sub>                   | 390 | 560                   | 1100 | ns   |                                                                                                |
| ASC2 to output falling edge delay    | t <sub>ASC2_f</sub>                   | 150 | 230                   | 480  | ns   |                                                                                                |
| ASC1 Pin Characteristic              |                                       |     |                       |      |      |                                                                                                |
| Logic High Input Threshold           | V <sub>ASC1H</sub>                    | 2.7 | 3.1                   | 3.5  | V    | V <sub>CC1</sub> =5V                                                                           |
| Logic Low Input Threshold            | V <sub>ASC1L</sub>                    | 1.5 | 1.9                   | 2.3  | V    | V <sub>CC1</sub> =5V                                                                           |
| ASC1 to output rising edge delay     | t <sub>ASC1_r</sub>                   | 50  | 120                   | 200  | ns   |                                                                                                |
| ASC1 to output falling edge delay    | t <sub>ASC1_f</sub>                   | 50  | 150                   | 250  | ns   |                                                                                                |

## 6.2. Switching Electrical Characteristics

Typical values are at  $V_{CC1}=5V$ ,  $V_{CC2}=15V$ ,  $V_{EE2}=GND2$ . All min and max specifications are at  $T_A=-40^{\circ}C$  to  $125^{\circ}C$ . If not mentioned,  $C_L=0.1nF$ .

| Parameter                                  | Symbol           | Min | Typ | Max | Unit       | Condition        |
|--------------------------------------------|------------------|-----|-----|-----|------------|------------------|
| Minimum Pulse Width                        | $t_{PWmin\_IN+}$ | 10  | 30  | 60  | ns         |                  |
| Output Rise Time                           | $t_R$            |     | 45  |     | ns         | $C_{LOAD}=10nF$  |
| Output Fall Time                           | $t_F$            |     | 47  |     | ns         |                  |
| Propagation Delay                          | $t_{pLH\_IN+}$   | 50  | 80  | 140 | ns         | $C_{LOAD}=0.1nF$ |
|                                            | $t_{pHL\_IN+}$   | 50  | 90  | 140 | ns         |                  |
| Pulse Width Distortion $ t_{pHL}-t_{pLH} $ | $t_{PWD}$        |     |     | 50  | ns         |                  |
| Common Mode Transient Immunity             | $CMTI^{(1)}$     | 150 |     |     | $kV/\mu s$ |                  |

<sup>(1)</sup> Not test covered, guaranteed by characterization.

<sup>(2)</sup> Not test covered, guaranteed by design.

## 7. High Voltage Feature Description

### 7.1. Insulation and Safety Related Specifications

| Parameter                                           | Symbol | SSOW20 | Unit | Comments                                 |
|-----------------------------------------------------|--------|--------|------|------------------------------------------|
| Minimum External Clearance                          | CLR    | 8.0    | mm   | IEC 60664-1:2007                         |
| Minimum External Creepage                           | CPG    | 8.0    | mm   | IEC 60664-1:2007                         |
| Distance Through Insulation                         | DTI    | 20     | μm   | Minimum internal gap                     |
| Tracking Resistance<br>(Comparative Tracking Index) | CTI    | >600   | V    | DIN EN 60112 (VDE 0303-11);<br>IEC 60112 |
| Material Group                                      |        | I      |      |                                          |

| Description                         | Test Condition                          | Value     |
|-------------------------------------|-----------------------------------------|-----------|
| Overvoltage Category per IEC60664-1 | For Rated Mains Voltage $\leq$ 150Vrms  | I to IV   |
|                                     | For Rated Mains Voltage $\leq$ 300Vrms  | I to IV   |
|                                     | For Rated Mains Voltage $\leq$ 600Vrms  | I to IV   |
|                                     | For Rated Mains Voltage $\leq$ 1000Vrms | I to III  |
| Climatic Classification             |                                         | 40/125/21 |
| Pollution Degree per DIN VDE 0110   |                                         | 2         |

## 7.2. Insulation Characteristics for SSOW20 Package

| Description                               | Test Condition                                                                                                                                                                                                                        | Symbol     | Value      | Unit       |
|-------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|------------|------------|
| Maximum Working Isolation Voltage         | AC voltage (sine wave) Time dependent dielectric breakdown (TDDb) test                                                                                                                                                                | $V_{IOWM}$ | 1500       | $V_{RMS}$  |
|                                           | DC voltage                                                                                                                                                                                                                            |            | 2121       | $V_{DC}$   |
| Maximum Repetitive Peak Isolation Voltage | AC voltage(bipolar)                                                                                                                                                                                                                   | $V_{IORM}$ | 2121       | $V_{PEAK}$ |
| Apparent Charge                           | Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$ , $t_{ini} = 60s$ , $V_{pd}(m)=1.2 \times V_{IORM}$ , $t_m=10s$ .                                                                                           | $q_{pd}$   | <5         | pC         |
|                                           | Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$ , $t_{ini}=60s$ , $V_{pd}(m)=1.6 \times V_{IORM}$ , $t_m=10s$                                                                                                      |            |            |            |
|                                           | Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2 \times V_{IOTM}$ , $t_{ini}=1s$<br>$V_{pd}(m)=1.875 \times V_{IORM}$ , $t_m=1s$ (method b1) or $V_{pd}(m)=V_{ini}$ , $t_m=t_{ini}$ (method b2) |            |            |            |
| Maximum Transient Isolation Voltage       | $t = 60s$                                                                                                                                                                                                                             | $V_{IOTM}$ | 8000       | $V_{PEAK}$ |
| Maximum impulse voltage                   | Tested in air, 1.2/50- $\mu s$ waveform per IEC62368-1                                                                                                                                                                                | $V_{IMP}$  | 6250       | $V_{PEAK}$ |
| Maximum Surge Isolation Voltage           | Test method per IEC60065, 1.2/50 $\mu s$ waveform, $V_{TEST}=V_{IOSM} \times 1.6$                                                                                                                                                     | $V_{IOSM}$ | 10000      | $V_{PEAK}$ |
| Isolation Resistance                      | $V_{IO}=500V$ at $T_A=T_S$                                                                                                                                                                                                            | $R_{IO}$   | $>10^9$    | $\Omega$   |
|                                           | $V_{IO}=500V$ at $100^\circ C \leq T_A \leq 125^\circ C$                                                                                                                                                                              |            | $>10^{11}$ | $\Omega$   |
|                                           | $V_{IO}=500V$ , $T_A=25^\circ C$                                                                                                                                                                                                      |            | $>10^{12}$ | $\Omega$   |
| Isolation Capacitance                     | $f = 1MHz$                                                                                                                                                                                                                            | $C_{IO}$   | 0.8        | pF         |
| <b>UL1577</b>                             |                                                                                                                                                                                                                                       |            |            |            |
| Maximum Withstanding Isolation Voltage    | $V_{TEST}=V_{ISO}$ , $t = 60s$ (qualification); $V_{TEST}= 1.2 \times V_{ISO}$ , $t = 1s$ (100%production)                                                                                                                            | $V_{ISO}$  | 5700       | $V_{RMS}$  |

### 7.3. Safety Limiting Values for SSOW20 Package

| Description                      | Test Condition                                                                                                                                  | Symbol | Value       |      | Unit |
|----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------------|------|------|
| Maximum Safety Temperature       |                                                                                                                                                 | $T_s$  | 150         |      | °C   |
| Maximum Safety Power Dissipation | $R_{\theta JA}=77.7^{\circ}\text{C/W}$ , $T_J=150^{\circ}\text{C}$ ,<br>$V_{CC2}=20\text{V}$ , $V_{EE2}=-5\text{V}$ $T_A=25^{\circ}\text{C}$    | $P_s$  | Total       | 1160 | mW   |
| Maximum Safety Current           | $R_{\theta JA}=77.7^{\circ}\text{C/W}$ , $V_{CC2}=15\text{V}$ ,<br>$V_{EE2}=-5\text{V}$<br>$T_J=150^{\circ}\text{C}$ , $T_A=25^{\circ}\text{C}$ | $I_s$  | Driver side | 58   | mA   |
|                                  | $R_{\theta JA}=77.7^{\circ}\text{C/W}$ , $V_{CC2}=20\text{V}$ ,<br>$V_{EE2}=-5\text{V}$<br>$T_J=150^{\circ}\text{C}$ , $T_A=25^{\circ}\text{C}$ |        | Driver side | 46   |      |

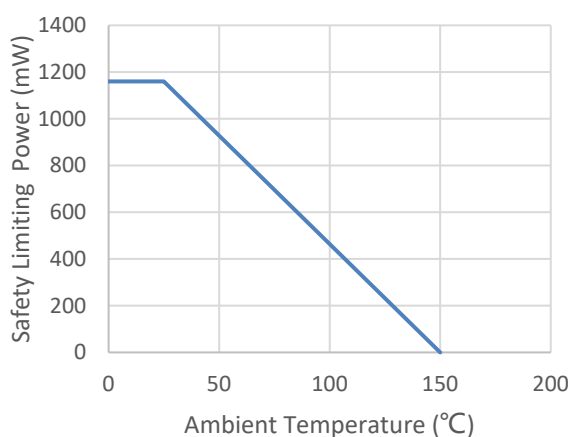


Figure 7.1 Thermal Derating Curve for Limiting Power per DIN VDE V 0884-17 for SSOW20 Package

#### 7.4. Regulatory Information for SSOW20 Package

| <i>UL</i>                                                 |                                                           | <i>TUV</i>                                                                                                      | <i>CQC</i>                      |
|-----------------------------------------------------------|-----------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------|---------------------------------|
| UL 1577 Component Recognition Program                     | Approved under CSA Component Acceptance Notice 5A         | DIN EN IEC 60747-17 (VDE 0884-17)                                                                               | Certified according to GB4943.1 |
| Single Protection, 5700V <sub>RMS</sub> Isolation Voltage | Single Protection, 5700V <sub>RMS</sub> Isolation voltage | Reinforced Insulation<br>V <sub>IORM</sub> =2121V <sub>PEAK</sub> ,<br>V <sub>IOTM</sub> =8000V <sub>PEAK</sub> | Reinforced Insulation           |
| TBD                                                       |                                                           | TBD                                                                                                             | TBD                             |

## 8. Typical Characteristics

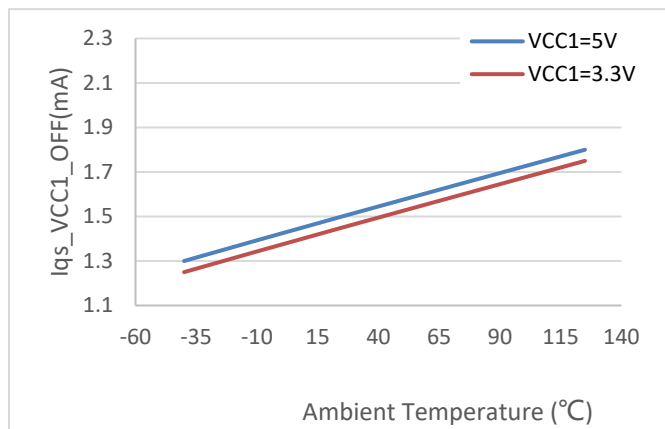


Figure 8.1 VCC1 OFF supply current vs temperature

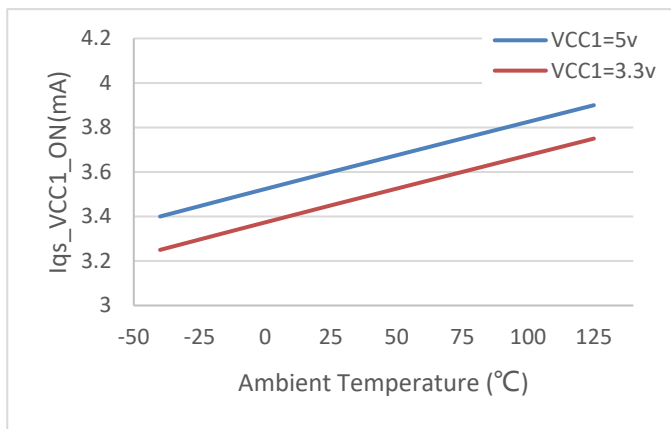


Figure 8.2 VCC1 ON supply current vs temperature

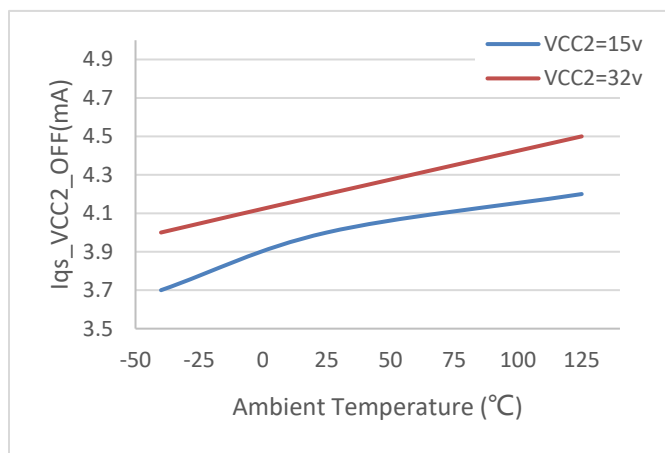


Figure 8.3 VCC2 OFF supply current vs temperature

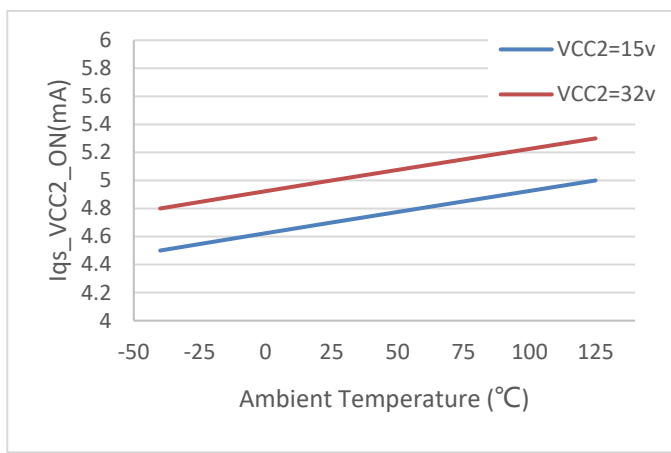


Figure 8.4 VCC2 ON supply current vs temperature

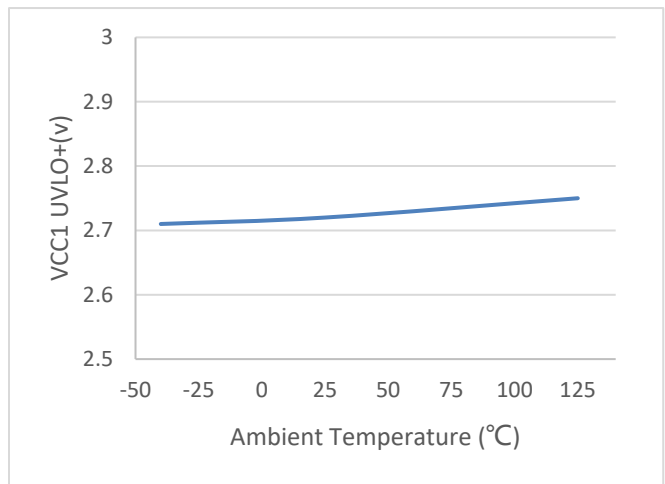


Figure 8.5 VCC1 UVLO+ vs temperature

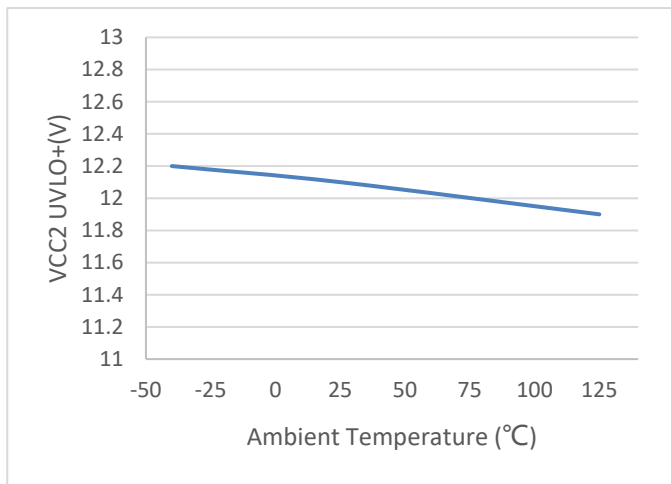


Figure 8.6 VCC2 UVLO+ vs temperature

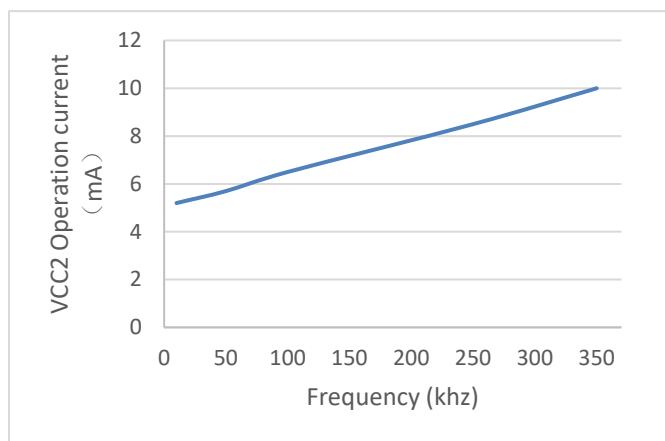


Figure 8.7 VCC2 operation current vs temperature

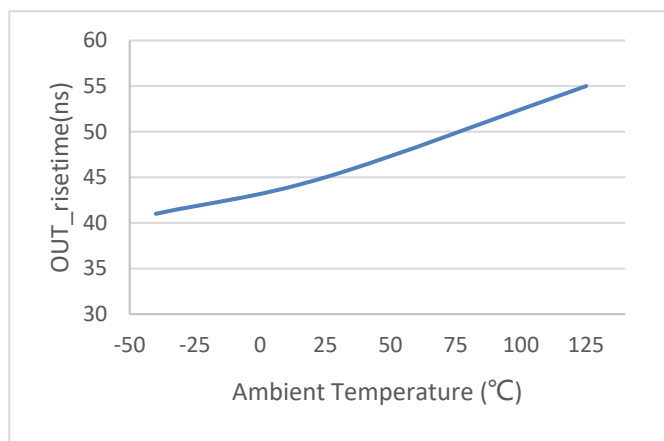


Figure 8.8 risetime vs temperature

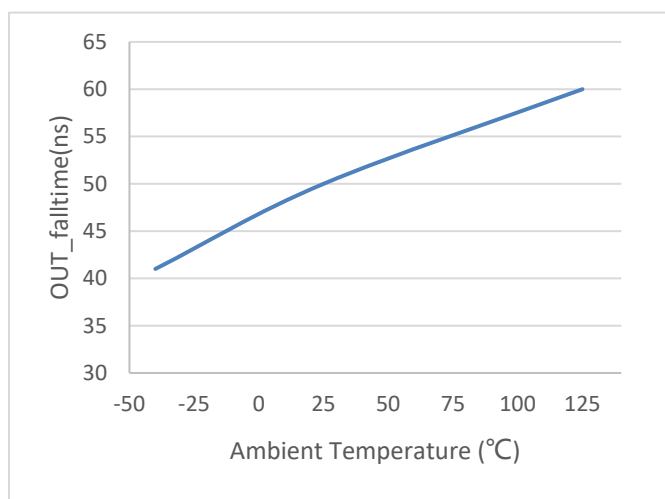


Figure 8.9 fall time vs temperature

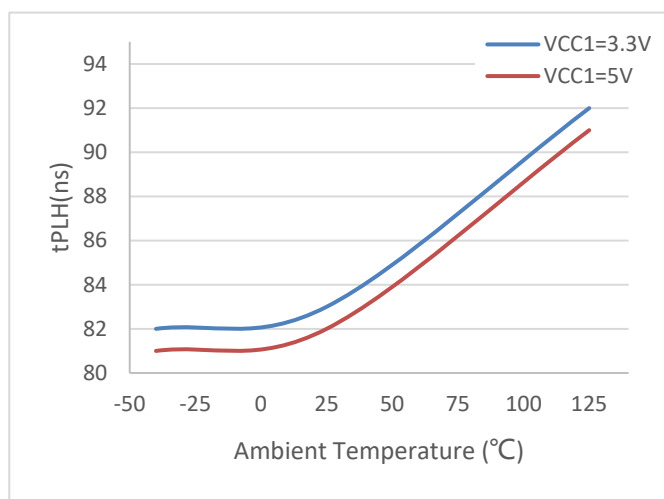


Figure 8.10  $t_{PLH\_IN+}$  vs temperature

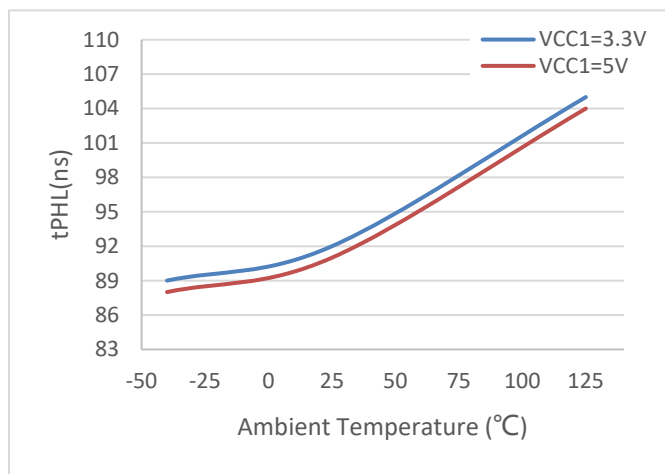


Figure 8.11  $t_{PHL\_IN+}$  vs temperature

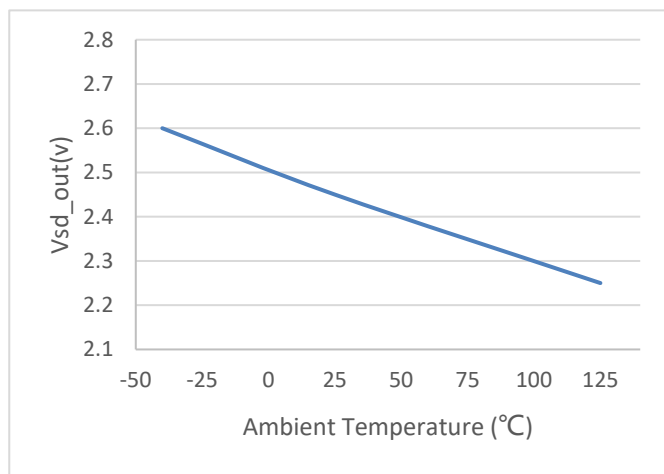


Figure 8.12 Active pulldown voltage vs temperature

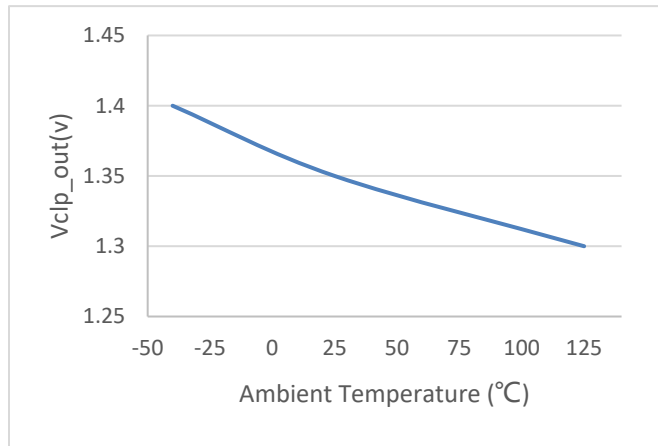


Figure 8.13 short circuit clamp vs temperature

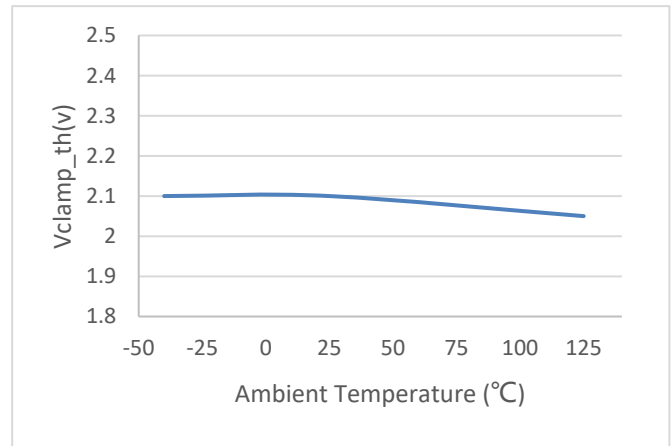


Figure 8.14 miller clamp threshold vs temperature

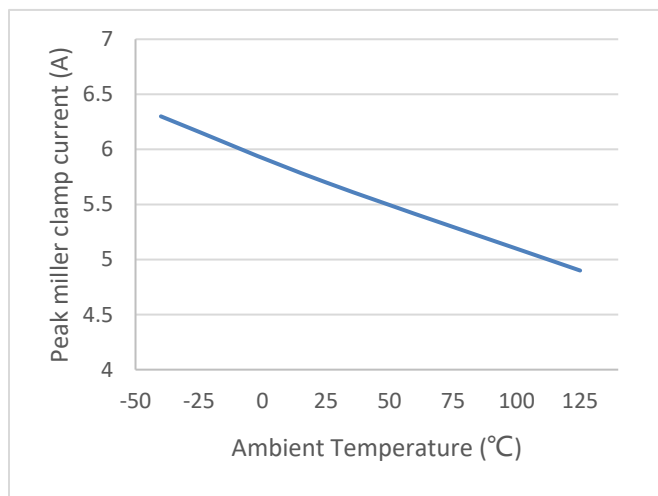


Figure 8.15 peak miller clamp current vs temperature

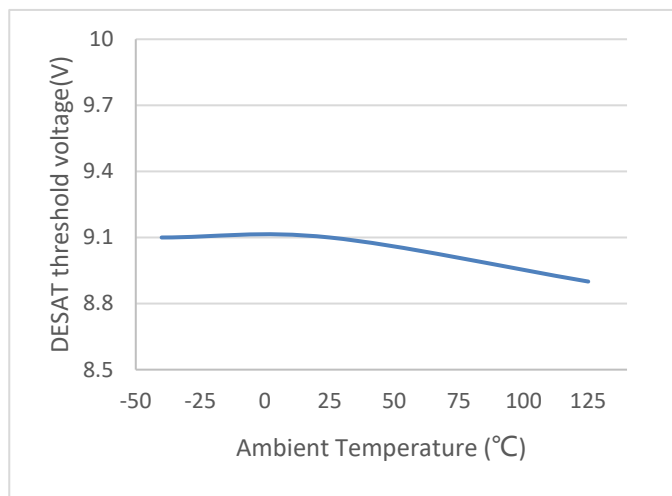


Figure 8.16 DESAT threshold vs temperature

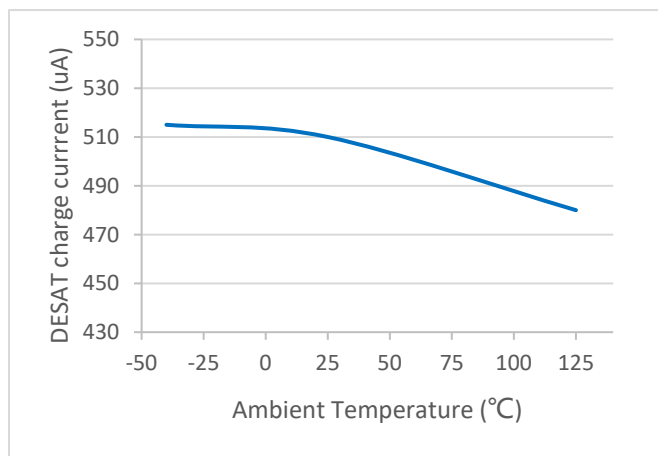


Figure 8.17 DESAT charge current vs temperature

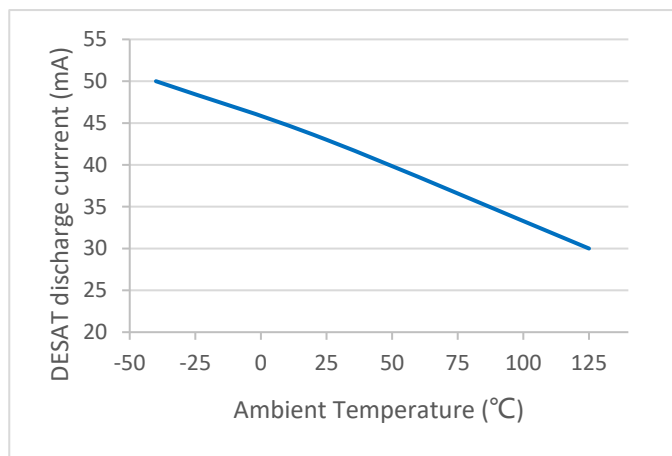


Figure 8.18 DESAT discharge current vs temperature

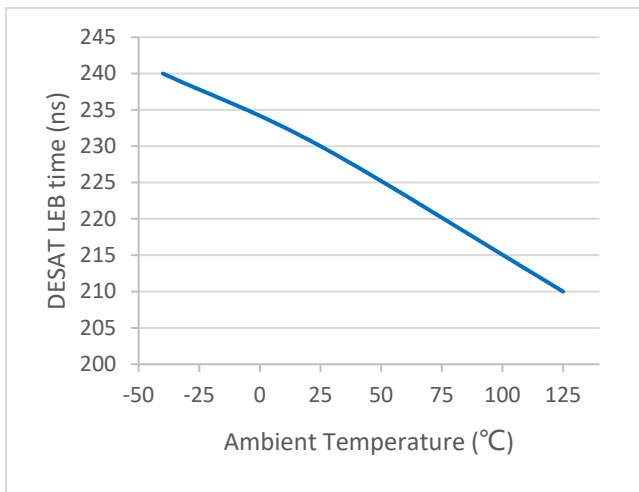


Figure 8.19 DESAT LEB time vs temperature

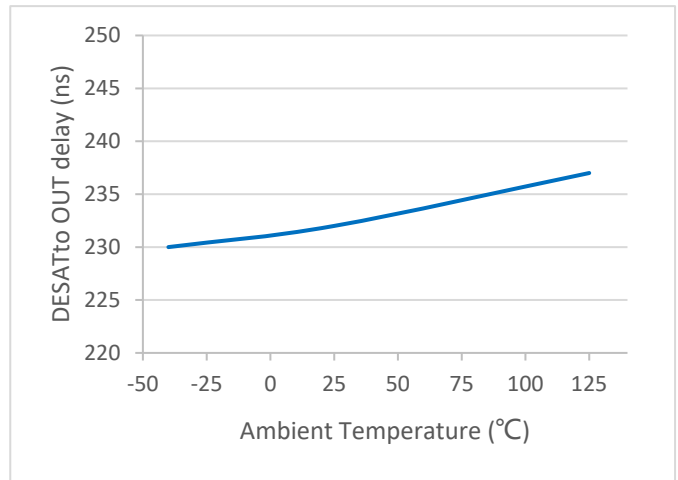


Figure 8.20 DESAT to OUT delay vs temperature

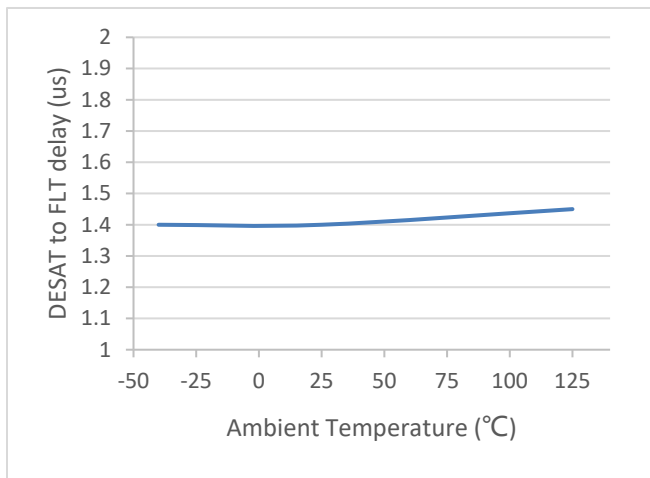


Figure 8.21 DESAT to FLT delay vs temperature

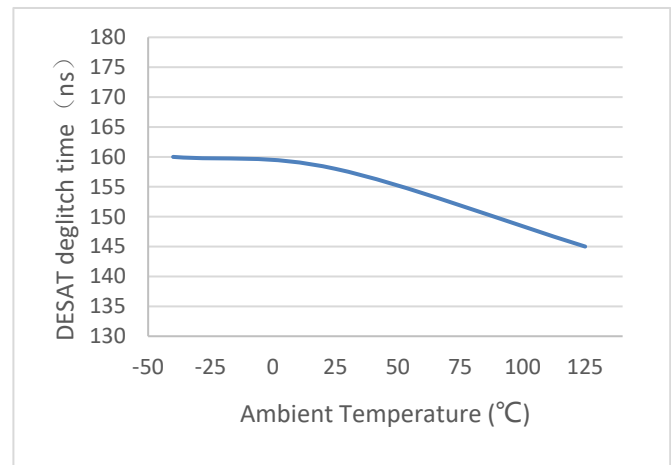


Figure 8.22 DESAT deglitch time vs temperature

## 9. Function Description

### 9.1. Overview

The NSI6713 is a highly reliable power transistor gate driver. It can source and sink 10A peak current, which is suitable for driving MOSFET, IGBT, or SiC MOSFET. The NSI6713 is available in SSOW20 package, which can support 5700V<sub>RMS</sub> isolation per UL1577. System robustness is supported by 150kV/ $\mu$ s minimum common-mode transient immunity (CMTI).

Besides, the NSI6713 includes crucial protection features such as miller clamp, DESAT short circuit detection and soft turn off. UVLO and short circuit fault are reported through separate pins.

The isolation barrier inside NSI6713 is based on the capacitive isolation. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI. The digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side.

The functional block diagram of NSI6713 is shown below. Two input pins with non-inverting and inverting logic support interlock and shoot through protection. Low resistance of high side and low side MOSFET in the output stage ensures high driving capability. Split outputs can control the rise and fall time individually. Active pull-down and short circuit clamping features are implemented to protect power transistor.

In summary, the NSI6713 is suitable to replace source and sink reinforced gate driver in high reliability, power density and efficiency switching power system.

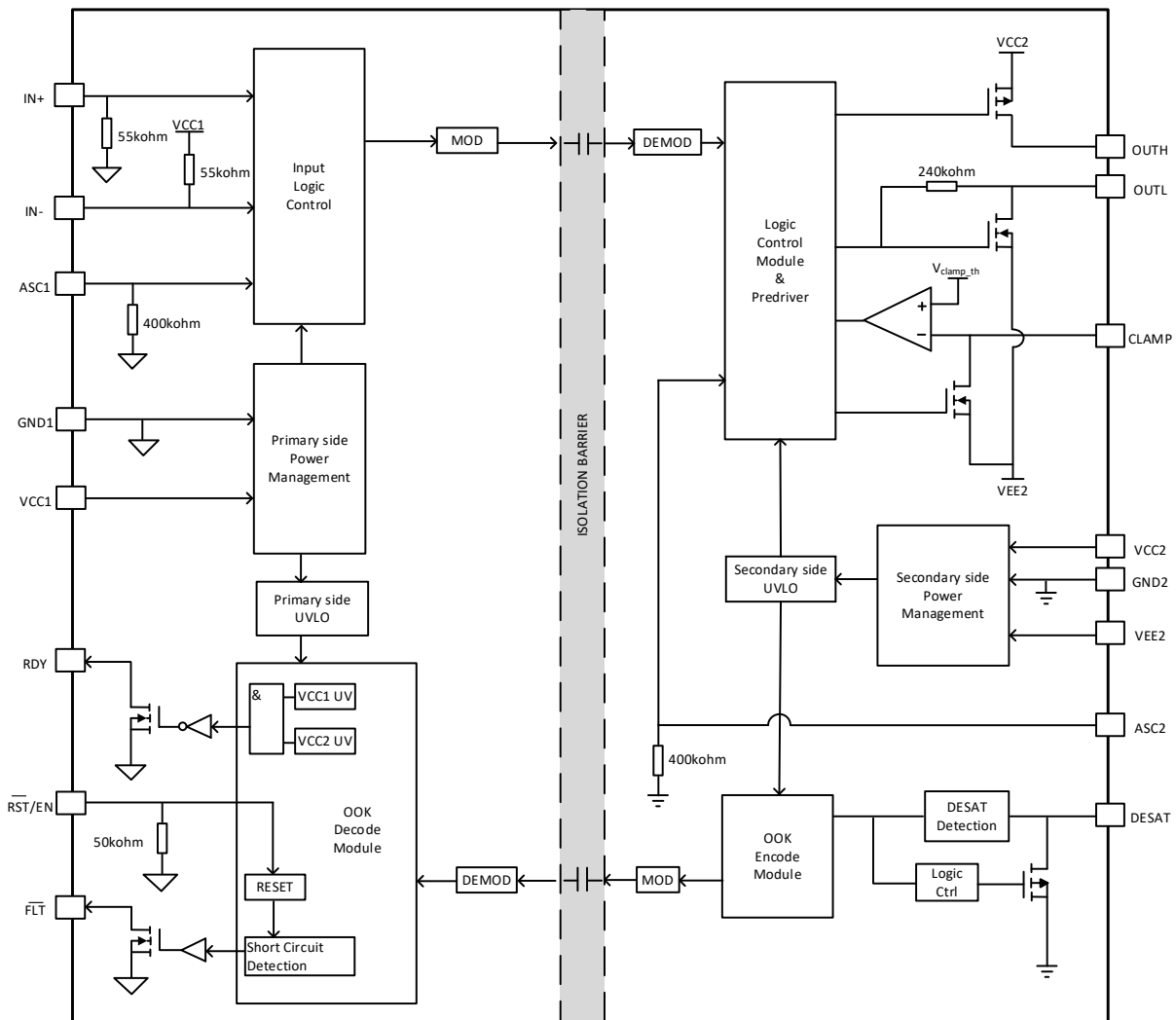


Figure 9.1 NSI6713 Function Blocks

## 9.2. Power Supply

Power supply  $V_{CC1}$  is able to support from 3.3V to 5.5V. Power supply  $V_{CC2}$  is able to support from 13V to 32V. To be mentioned, NSI6713 also supports bipolar power supply mode on the driver side. In the case of fast switching speed, the negative power supply is crucial to prevent false turn on from parasitic Miller capacitor.

## 9.3. Output Stage

NSI6713 supports the split output, which means the rising time and falling time can be adjusted independently. The output voltage is switched between  $V_{CC2}$  and  $VEE2$ . It can be controlled by  $IN+$ ,  $IN-$  and  $\overline{RST/EN}$ . The NSI6713 has a P-channel MOSFET pulled up the OUTH pin when turning on external power transistor. The measurement result  $R_{OH}$  represents the on-resistance of P-channel MOSFET. The voltage and current of external power transistor drain to source or collector to emitter change during turn on. The pull-down structure of NSI6713 is simply composed of an N-channel MOSFET with on-resistance of  $R_{OL}$ . The result is quite small, indicating the strong driving capability of NSI6713.

## 9.4. Active Pull-Down

The Active Pull-Down feature ensures a safe IGBT or MOSFET off-state if  $V_{CC2}$  is not connected to the power supply. When  $V_{CC2}$  is floating, the driver output is still able to be held low.

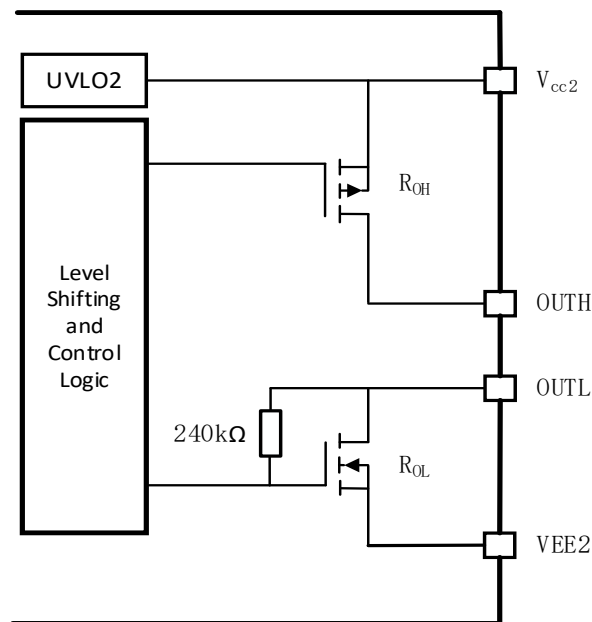


Figure 9.2 NSI6713 output stage

## 9.5. Internal Active Miller Clamp

Active miller clamp is used to prevent false turn on. After the external power transistor is turned off, the other one of the phase leg is turned on. The voltage of the drain-source or collector-emitter rises instantly. The  $dv/dt$  will cause a high current on miller parasitic capacitor. The voltage drops on the gate resistor possibly turn on the external power transistor unintentionally, which will cause a catastrophic damage. To deal with that, NSI6713 is equipped with a miller clamp pin. The clamp pin detects the gate voltage of IGBT or MOSFET. When the gate voltage is decreasing and reaches the  $V_{CLAMP\_TH}$ , the clamp pin will be pulled down by the internal MOSFET, providing a low impedance path to avoid the false turn on.

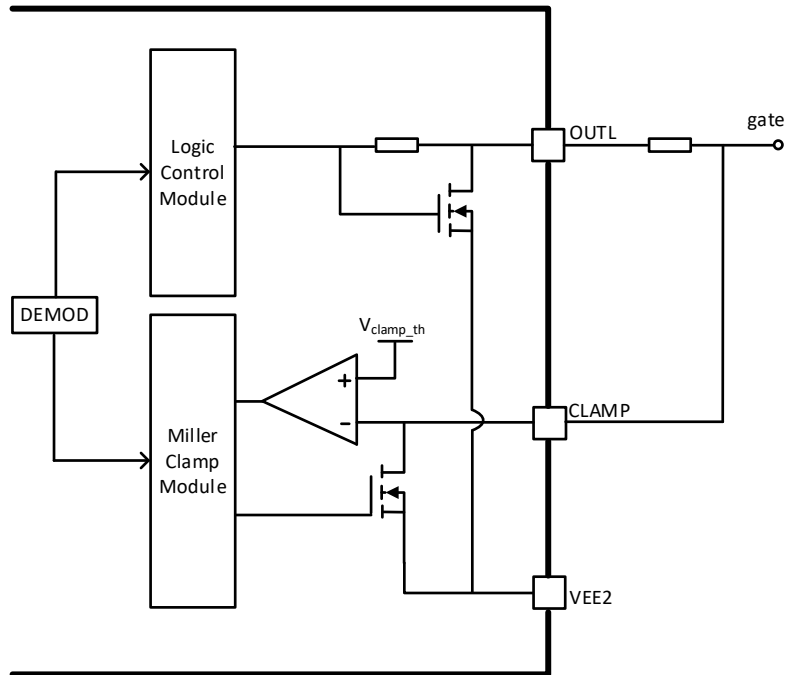


Figure 9.3 Active Miller Clamp

## 9.6. Short circuit Clamping

During a short circuit, the gate voltage of IGBT or MOSFET tends to rise because of the feedback via the miller capacitance. The diode between OUTH/OUTL/CLAMP and  $V_{CC2}$  pins inside the driver limits this voltage when the output voltage is higher than the supply voltage. A maximum current of 500mA may be fed back to the supply through this path for 10 $\mu$ s. If higher currents are expected or tighter clamping is desired, external Schottky diodes may be added.

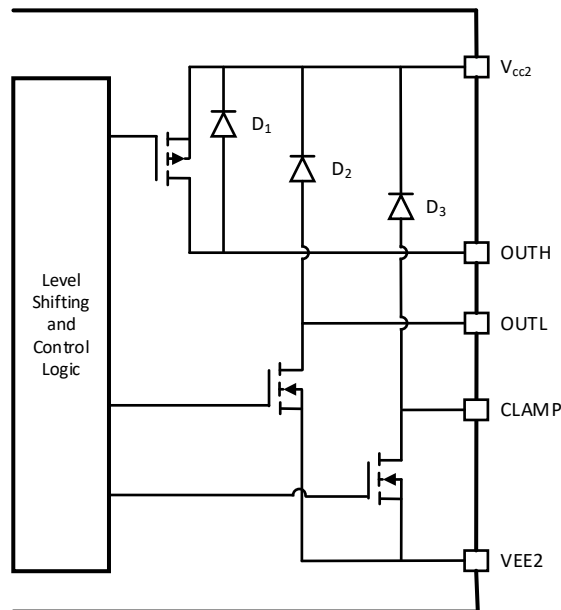


Figure 9.4 Short circuit Clamping



### 9.10. Fault ( $\overline{\text{FLT}}$ and $\overline{\text{RST/EN}}$ )

The  $\overline{\text{FLT}}$  pin of NSI6713 is used to report a warning signal if the fault is detected on DESAT. If the fault occurs, the  $\overline{\text{FLT}}$  pin will be pulled down and held in low state for a mute time. During the mute time, NSI6713 ignores any reset signal. After that, the  $\overline{\text{FLT}}$  pin will be reset to high impedance status if the reset signal is checked. The  $\overline{\text{RST/EN}}$  pin is pulled down to GND1 by an internal resistor, which means the device is disabled by default. Therefore, the  $\overline{\text{RST/EN}}$  pin must be pulled up externally to enable the device. Timing diagram of fault report is shown below.

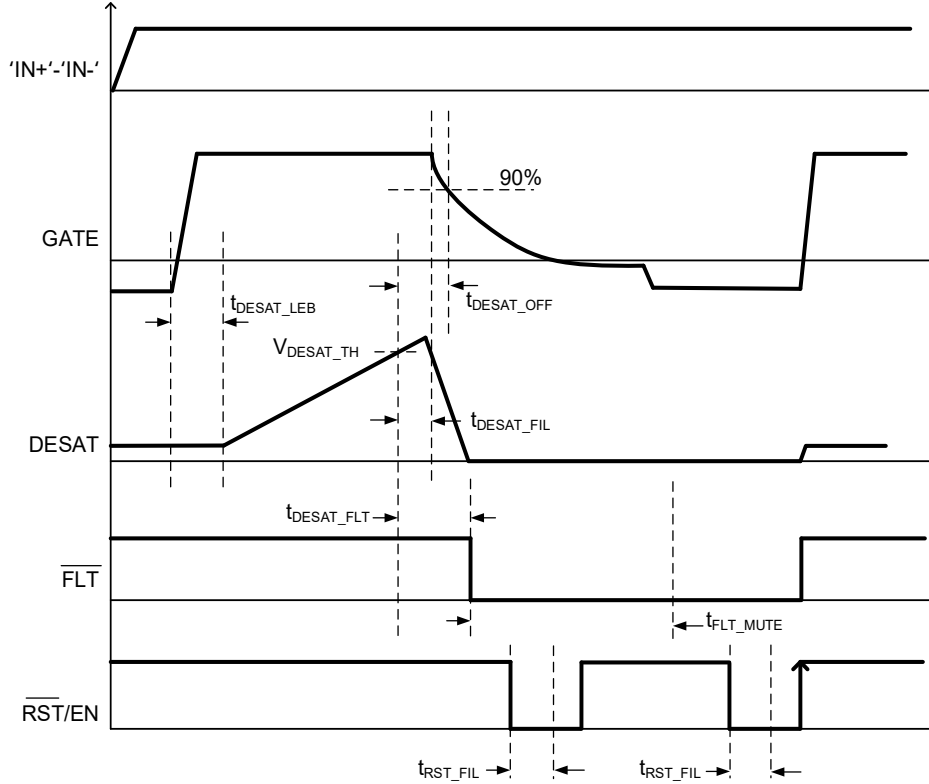


Figure 9.6 DESAT protection Timing Diagram

### 9.11. ASC Protection

If the active short circuit (ASC) pin is set to be high, the output will be high regardless of the input-side configuration. To be mentioned, the priority of ASC2 protection is higher than the  $V_{CC1}$  UVLO but lower than the  $V_{CC2}$  UVLO and DESAT protection. The priority of ASC1 protection is higher than the  $EN/\overline{RST}$ , but lower than the  $V_{CC1}$  UVLO and output side function.

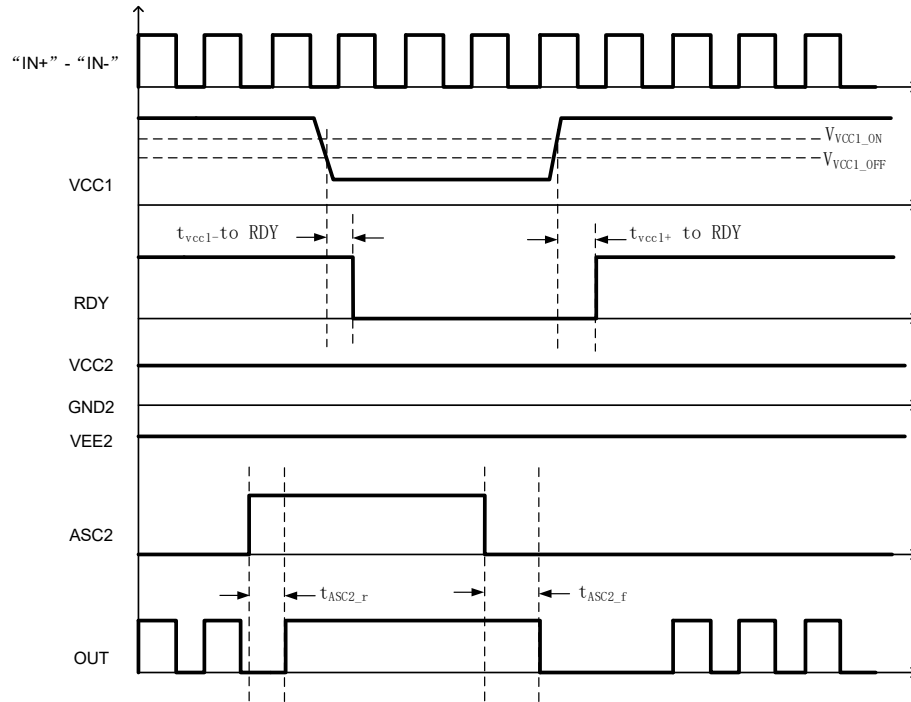


Figure 9.7 ASC2 protection with  $V_{CC1}$  UVLO Timing Diagram

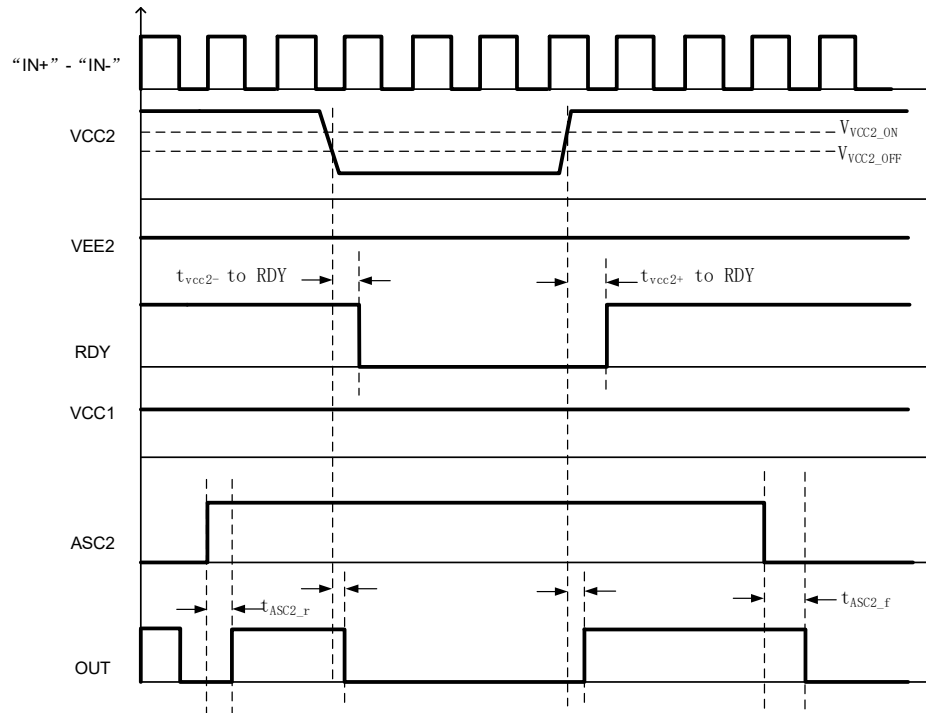


Figure 9.8 ASC2 protection with  $V_{CC2}$  UVLO Timing Diagram

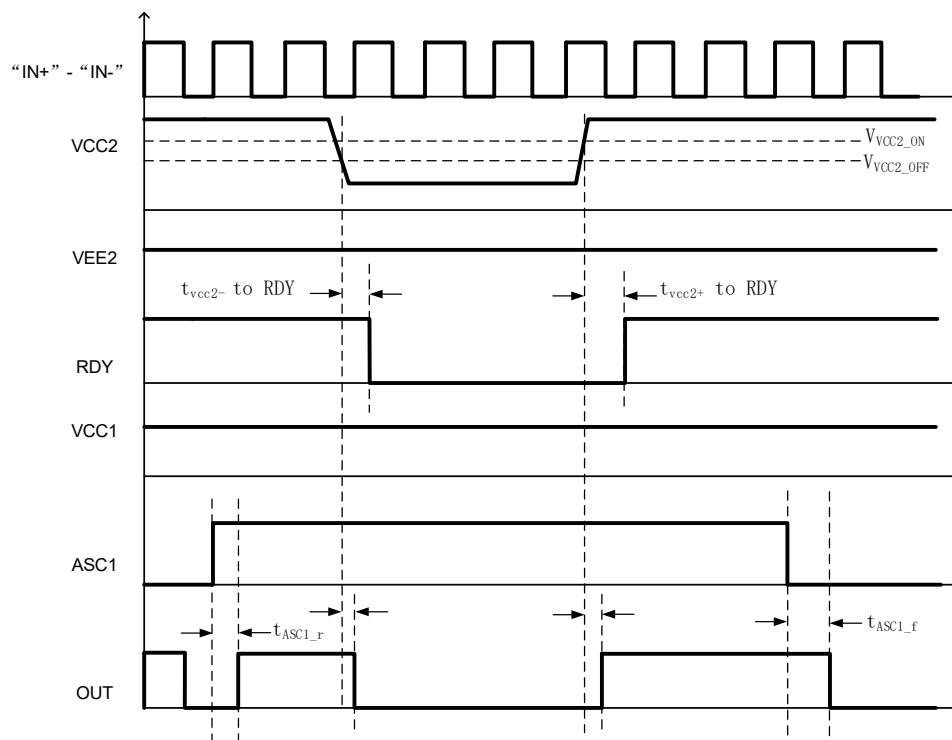


Figure 9.9 ASC1 protection with VCC2 UVLO Timing Diagram

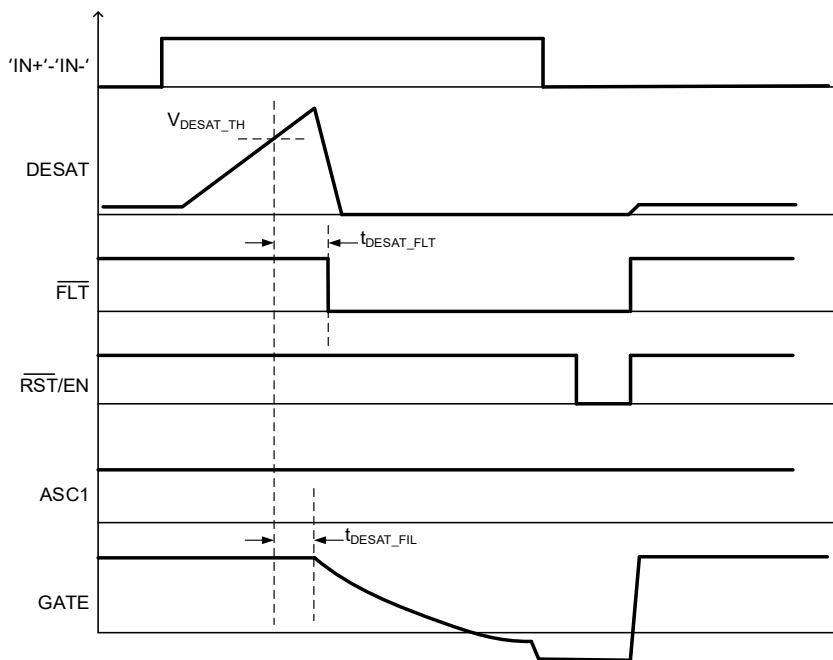


Figure 9.10 ASC1 protection with DESAT protection Timing Diagram

## 9.12. Device Functional Modes

Table lists the common functional modes of the device.

Table1. NSI6713 function modes

| Input            |                  |      |      | Output |       |      |      |     |     |           |       |
|------------------|------------------|------|------|--------|-------|------|------|-----|-----|-----------|-------|
| V <sub>CC1</sub> | V <sub>CC2</sub> | IN+  | IN-  | EN/RST | DESAT | ASC1 | ASC2 | RDY | FLT | OUTH/OUTL | CLAMP |
| PU               | PD/OPEN          | X    | X    | X      | X     | X    | X    | LOW | HIZ | LOW       | LOW   |
| PD               | PU               | X    | X    | X      | X     | X    | LOW  | LOW | HIZ | LOW       | LOW   |
| OPEN             | X                | X    | X    | X      | X     | X    | LOW  | HIZ | HIZ | LOW       | LOW   |
| PU               | PU               | X    | X    | LOW    | X     | LOW  | LOW  | HIZ | HIZ | LOW       | LOW   |
| PU               | PU               | LOW  | X    | HIGH   | X     | LOW  | LOW  | HIZ | HIZ | LOW       | LOW   |
| PU               | PU               | HIGH | LOW  | HIGH   | HIGH  | X    | X    | HIZ | LOW | LOW       | LOW   |
| PU               | PU               | HIGH | LOW  | HIGH   | LOW   | LOW  | LOW  | HIZ | HIZ | HIGH      | HIZ   |
| PU               | PU               | HIGH | HIGH | HIGH   | X     | LOW  | LOW  | HIZ | HIZ | LOW       | LOW   |
| PU               | PU               | X    | X    | X      | LOW   | HIGH | X    | HIZ | HIZ | HIGH      | HIZ   |
| PU               | PU               | X    | X    | X      | HIGH  | HIGH | X    | HIZ | LOW | LOW       | LOW   |
| PD               | PU               | X    | X    | X      | X     | X    | HIGH | LOW | HIZ | HIGH      | HIZ   |
| OPEN             | PU               | X    | X    | X      | X     | X    | HIGH | HIZ | HIZ | HIGH      | HIZ   |
| PU               | PU               | X    | X    | X      | LOW   | X    | HIGH | HIZ | HIZ | HIGH      | HIZ   |

Open: V<sub>CCx</sub> < POR ; PU: V<sub>CCx</sub> > V<sub>CCx</sub> UVLO ; PD: POR < V<sub>CCx</sub> < V<sub>CCx</sub> UVLO ; X: Irrelevant ; HIZ :High impedance  
 POR is around 1.8V.

## 10. Application Note

### 10.1. Typical Application Circuit

Bypassing capacitors for  $V_{CC1}$  and  $V_{CC2}$  supplies are needed to achieve reliable performance. To filter noise,  $0.1\mu\text{F}/50\text{V}$  ceramic capacitor is recommended to be placed as close as possible to NSI6713, both at  $V_{CC1}$  and  $V_{CC2}$  side. For  $V_{CC2}$  supply, additional  $10\mu\text{F}/50\text{V}$  ceramic capacitor is recommended, to support high peak currents when turning on external power transistor. If the  $V_{CC1}$  or  $V_{CC2}$  power supply is located long distance from the IC, bigger capacitance is essential.

The input filter composed by  $R_{in}$  and  $C_{in}$  can be used if input PWM has ring due to long traces or bad PCB layout. However, it will introduce longer propagation delay.

A  $4.7\text{k}\Omega$  resistor can be used as pull-up resistor for  $\overline{\text{FLT}}$ ,  $\text{RDY}$  and  $\overline{\text{RST/EN}}$  pins.

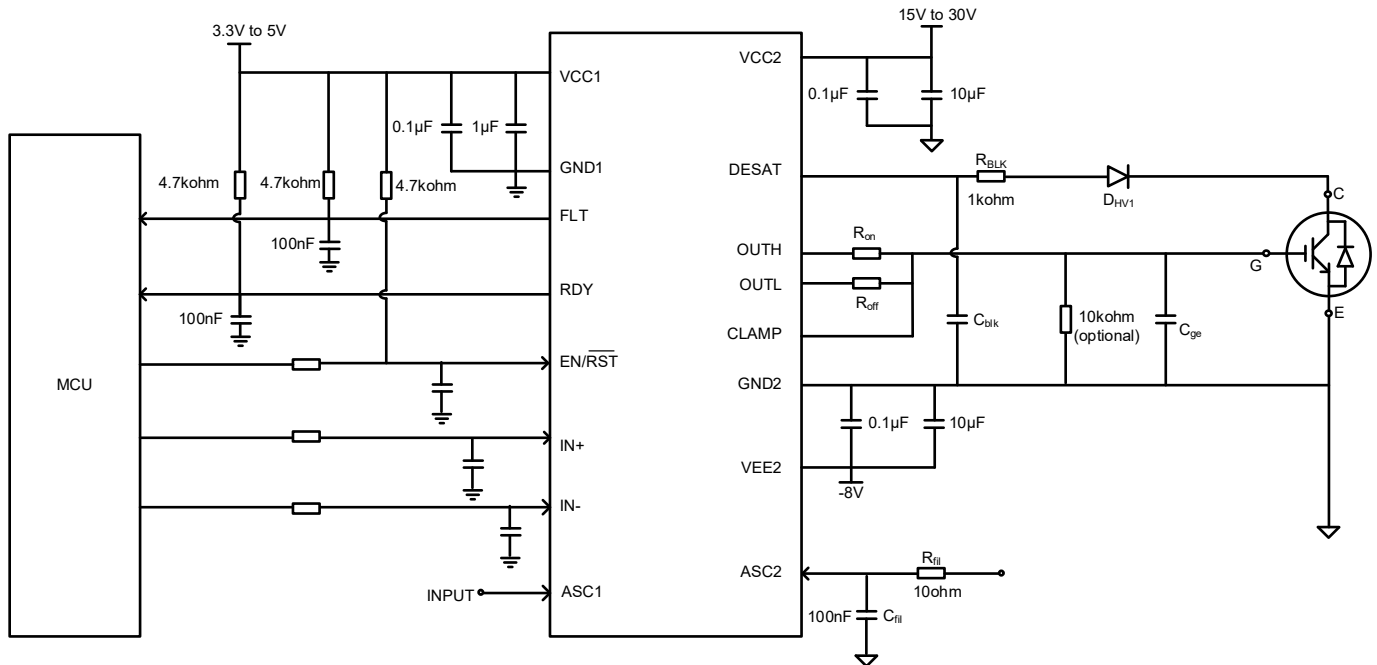


Figure 10.1 Typical Application

### 10.2. Design for IN+, IN- and $\overline{\text{RST/EN}}$

In the application with NSI6713, the noise from parasitic inductance and coupled capacitance cannot be ignored. To filter the noise, NSI6713 is designed with a 40ns deglitch filter. Besides, the external low pass filter can also be placed near the input pins. Low pass filter will increase the noise immunity and delay time, so it should be based on the requirements.

### 10.3. Design for $\overline{\text{EN/RST}}$ , $\text{RDY}$ and $\overline{\text{FLT}}$

$\overline{\text{EN/RST}}$  pin is used to enable the device and reset the fault signal. It is pulled down by default.  $\overline{\text{FLT}}$  and  $\text{RDY}$  pin are open-drain output, which means they cannot work without an external pull-up resistor. In this application, a  $4.7\text{k}\Omega$  pull-up resistor is recommended for  $\text{RDY}$ ,  $\overline{\text{FLT}}$  and  $\overline{\text{EN/RST}}$  pin. A  $100\text{nF}$  can be placed near the device if it is necessary.

### 10.4. Design for Automatic Reset Control

$\overline{\text{RST/EN}}$  pin has two functions. It is used to enable the device and reset the fault signal after  $\text{DESAT}$  is detected. The  $\overline{\text{RST/EN}}$  pin is pulled down to GND by an internal resistor, so the  $\overline{\text{RST/EN}}$  pin must be pulled up externally to enable the device.

After  $\text{DESAT}$  is detected, the  $\overline{\text{FLT}}$  pin will be pulled down until the rising edge of the  $\overline{\text{RST/EN}}$  pin is coming. To be mentioned, there is a  $\text{FLT}$  mute time, which means the reset signal must be held for at least  $t_{\text{FLT\_MUTE}}$ .

NSI6713 can be designed for automatic reset mode.  $\overline{\text{RST/EN}}$  pin can be connected to  $\text{IN+}$  directly when the PWM is applied to the  $\text{IN+}$ . Besides,  $\overline{\text{RST/EN}}$  pin can be connected with  $\text{IN-}$  through a NOT logic if the PWM is applied to the  $\text{IN-}$ . Whichever mode is used, the PWM off time should be longer than the  $t_{\text{FLT\_MUTE}}$ .

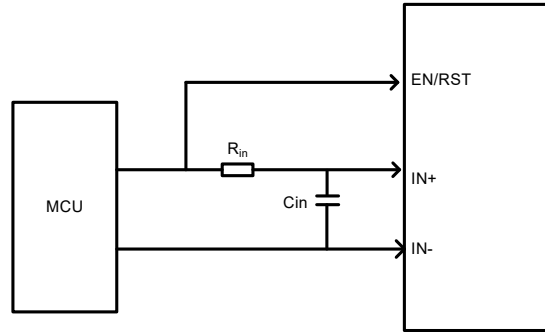


Figure10.2 Auto-reset control

### 10.5. PWM Interlock Protection

For applications to drive power transistors in half bridge configuration, two NSI6713 can be used. NSI6713 supports Interlock protection. If the controller has some mistakes, leading to negative dead time, the output PWM of NSI6713 is adjusted to avoid power transistor shoot through.

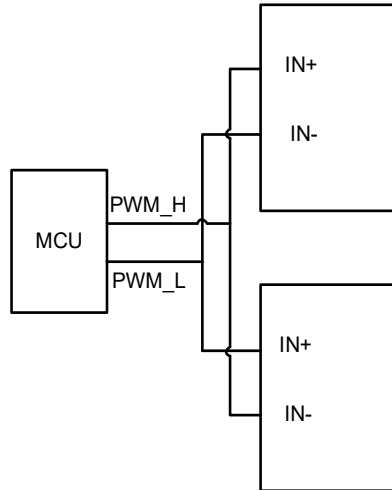


Figure10.3 Interlock Protection

### 10.6. Design for R<sub>on</sub> and R<sub>off</sub>

NSI6713 features split output, so the turn on and turn off switching speed can be independently controlled. The turn on and turn off resistance determine the peak source and sink current, which can be estimated by the formula:

$$I_{SOURCE} = \min\left(\frac{V_{CC2} - V_{EE2}}{R_{ON} + R_{OH} + R_{Gint}}, 10A\right)$$

$$I_{SINK} = \min\left(\frac{V_{CC2} - V_{EE2}}{R_{OFF} + R_{OL} + R_{Gint}}, 10A\right)$$

Where

R<sub>Gint</sub> is the internal resistance of the SiC or IGBT.

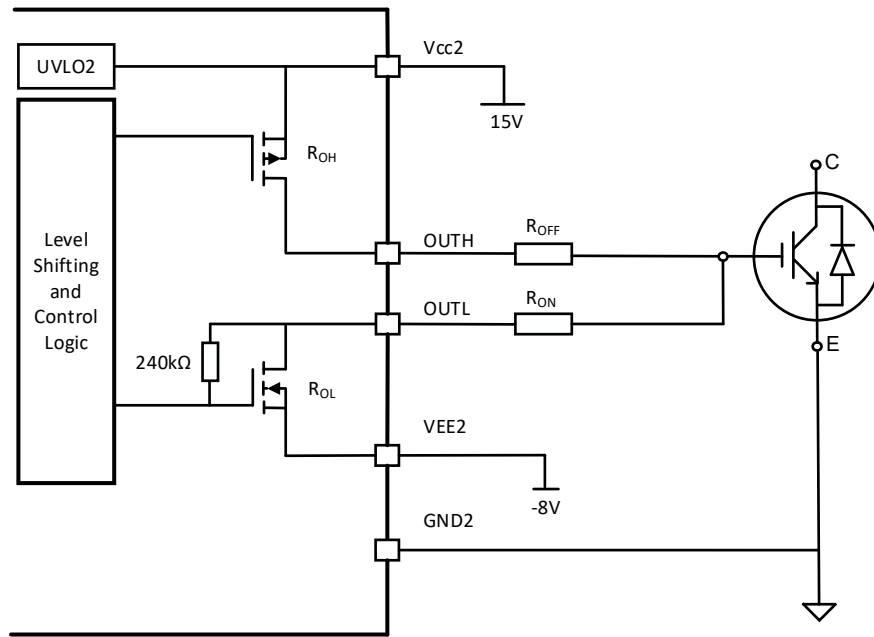


Figure10.4 Gate resistor design

## 10.7. Design for DESAT Protection

DESAT is used to protect the power semiconductor from overcurrent. When the voltage of DESAT is over the  $V_{DESAT\_TH}$ , the block of soft turn off will be activated and the fault pin will be pulled down. For typical application, the crucial components required to build the DESAT circuit are the DESAT diode, DESAT resistor and the blank capacitor.

The DESAT diode function is to conduct forward current. In order to avoid the false detection caused by the reverse recovery spikes, a very fast reverse recovery time diode with small reverse parasitic capacitance is recommended. The DESAT detection threshold voltage of 9V can be reduced by the DESAT diode, which can be calculated as:

$$V_{DESAT} = V_{DESAT\_TH} - n \times V_F$$

The anti-parallel diode of IGBT has a large transient forward voltage of the diode, which may result in a large negative voltage spike on the DESAT pin, then it may draw a large current from driver. DESAT resistor is used to limit the current. From 100Ω to 1kohm resistor is recommended to be added in series with the DESAT diode.

The DESAT fault detection should remain a short blanking time so that the collector voltage can fall below the  $V_{DESAT\_TH}$ . This blanking time can make sure that there is no nuisance tripping during the IGBT turn-on. It is based on the blank capacitor, which can be estimated as:

$$t_{BLK} = \frac{C_{BLK} \times V_{DESAT\_TH}}{I_{CHG}}$$

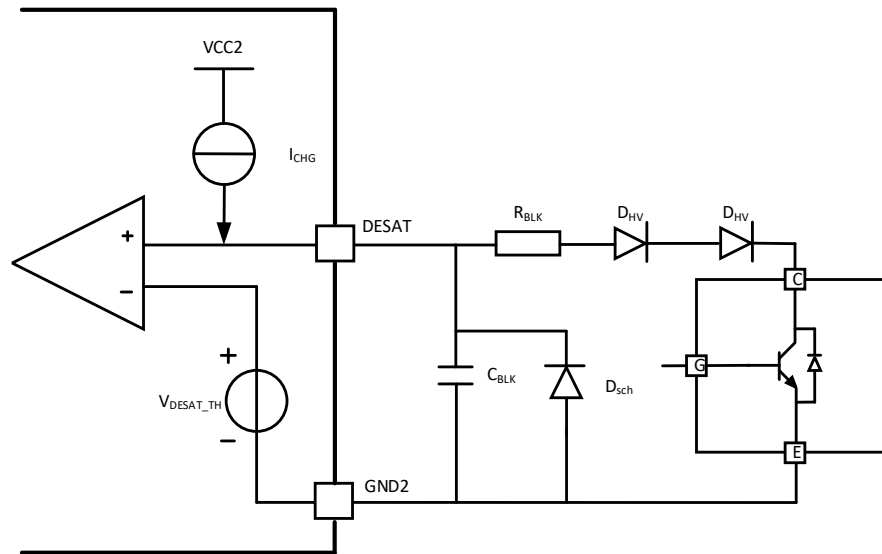


Figure10.5 DESAT protection

## 10.8. PCB Layout

Careful PCB layout is essential for optimal performance. Some key guidelines are:

- The bypass capacitors should be placed close to NSI6713, between  $V_{CC1}$  to GND1,  $V_{CC2}$  to GND2 and  $V_{EE2}$  to GND2.
- The decoupling capacitors of the input power supply should be connected to pin15 and pin9 through a dependent trace. The voltage spike on the parasitic inductance may affect the internal control logic.
- There is high switching current that charges and discharges the gate of external power transistor, leading to EMI and ring issues. The parasitic inductance of this loop should be minimized, by decreasing loop area and placing NSI6713 close to power transistor.
- Place a large amount of copper connecting to  $V_{EE2}$  pin and  $V_{CC2}$  pin for thermal dissipation, with priority on  $V_{EE2}$  pin. If the system has multi-layers of  $V_{EE2}$  or  $V_{CC2}$ , use multiple vias of adequate size for connection.
- To ensure isolation performance between primary and secondary side, the space under the chip should keep free from planes, traces, pads or via.

# 11. Package Information

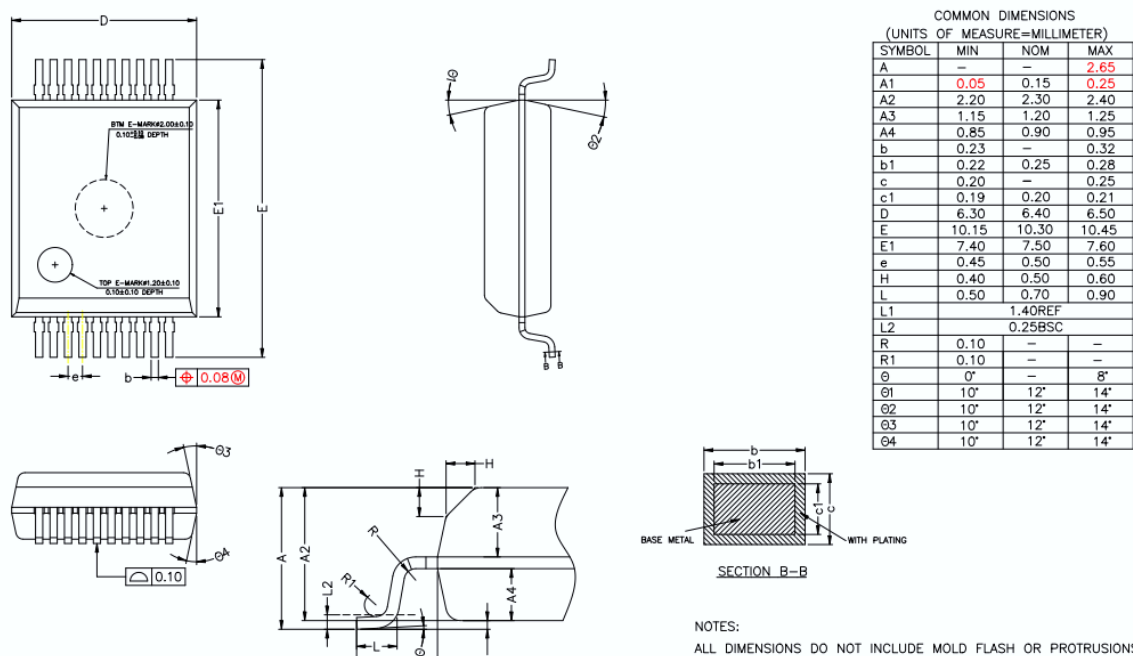
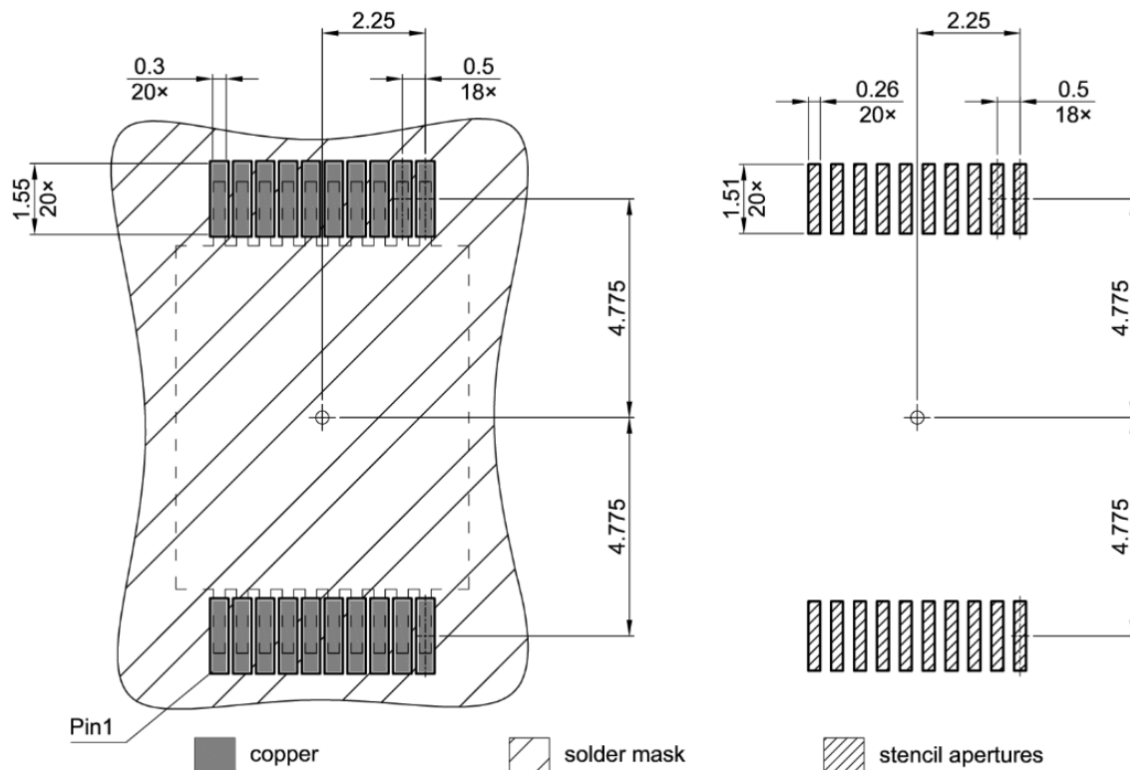


Figure 11.1 SSOW20 Package Shape and Dimension



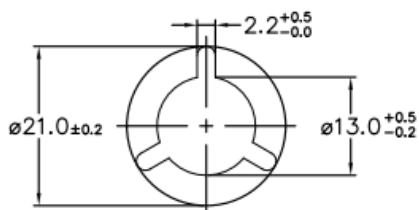
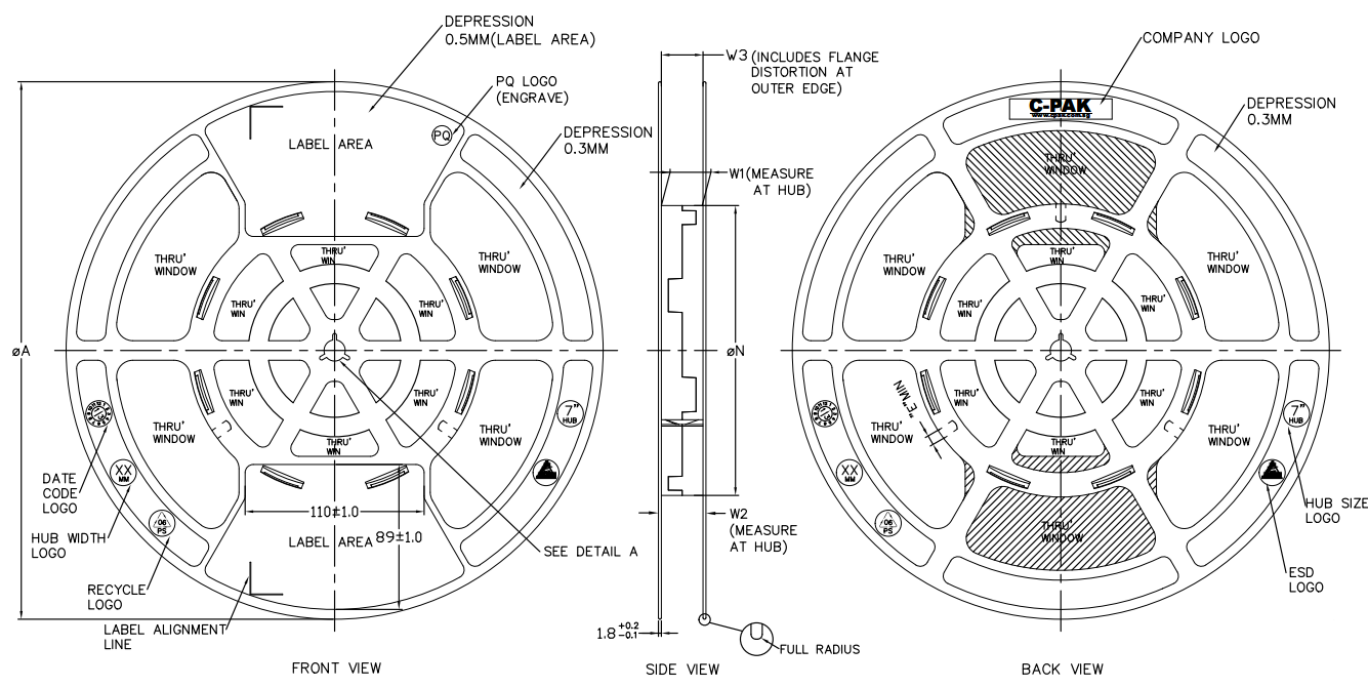
All dimensions are in units mm

Figure 11.2 Land pattern example

## 12. Ordering Information

| <i>Part Number</i>     | <i>Over<br/>current<br/>Protection</i> | <i>Ambient<br/>Temperature</i> | <i>Soft turn off<br/>current</i> | <i>MSL</i> | <i>Category</i> | <i>SPQ</i> | <i>MPQ</i> | <i>Packag<br/>e Type</i> |
|------------------------|----------------------------------------|--------------------------------|----------------------------------|------------|-----------------|------------|------------|--------------------------|
| NSI6713ASC-<br>Q1SSWAR | DESAT(9V)                              | -40°C to 125°C                 | I <sub>STO</sub> =400mA          | 3          | Automotive      | 1000       | 1000       | SSOW<br>20               |

# 13. Tape and Reel Information



ARBOR HOLE  
DETAIL A  
SCALE : 3:1

| PRODUCT SPECIFICATION |                       |                       |                      |             |                                                               |            |
|-----------------------|-----------------------|-----------------------|----------------------|-------------|---------------------------------------------------------------|------------|
| TAPE WIDTH            | $\phi A$<br>$\pm 2.0$ | $\phi N$<br>$\pm 2.0$ | W1                   | W2<br>(MAX) | W3                                                            | E<br>(MIN) |
| 08MM                  | 330                   | 178                   | $8.4^{+1.5}_{-0.5}$  | 14.4        | SHALL<br>ACCOMMODATE<br>TAPE WIDTH<br>WITHOUT<br>INTERFERENCE | 5.5        |
| 12MM                  | 330                   | 178                   | $12.4^{+2.5}_{-0.5}$ | 18.4        |                                                               | 5.5        |
| 16MM                  | 330                   | 178                   | $16.4^{+2.5}_{-0.5}$ | 22.4        |                                                               | 5.5        |
| 24MM                  | 330                   | 178                   | $24.4^{+2.5}_{-0.5}$ | 30.4        |                                                               | 5.5        |
| 32MM                  | 330                   | 178                   | $32.4^{+2.5}_{-0.5}$ | 38.4        |                                                               | 5.5        |

| SURFACE RESISTIVITY |                       |                      |            |
|---------------------|-----------------------|----------------------|------------|
| LEGEND              | SR RANGE              | TYPE                 | COLOUR     |
| A                   | BELOW $10^{12}$       | ANTISTATIC           | ALL TYPES  |
| B                   | $10^8$ TO $10^{11}$   | STATIC DISSIPATIVE   | BLACK ONLY |
| C                   | $10^5$ & BELOW $10^8$ | CONDUCTIVE (GENERIC) | BLACK ONLY |
| E                   | $10^8$ TO $10^{11}$   | ANTISTATIC (COATED)  | ALL TYPES  |

Figure 13.1 Reel information

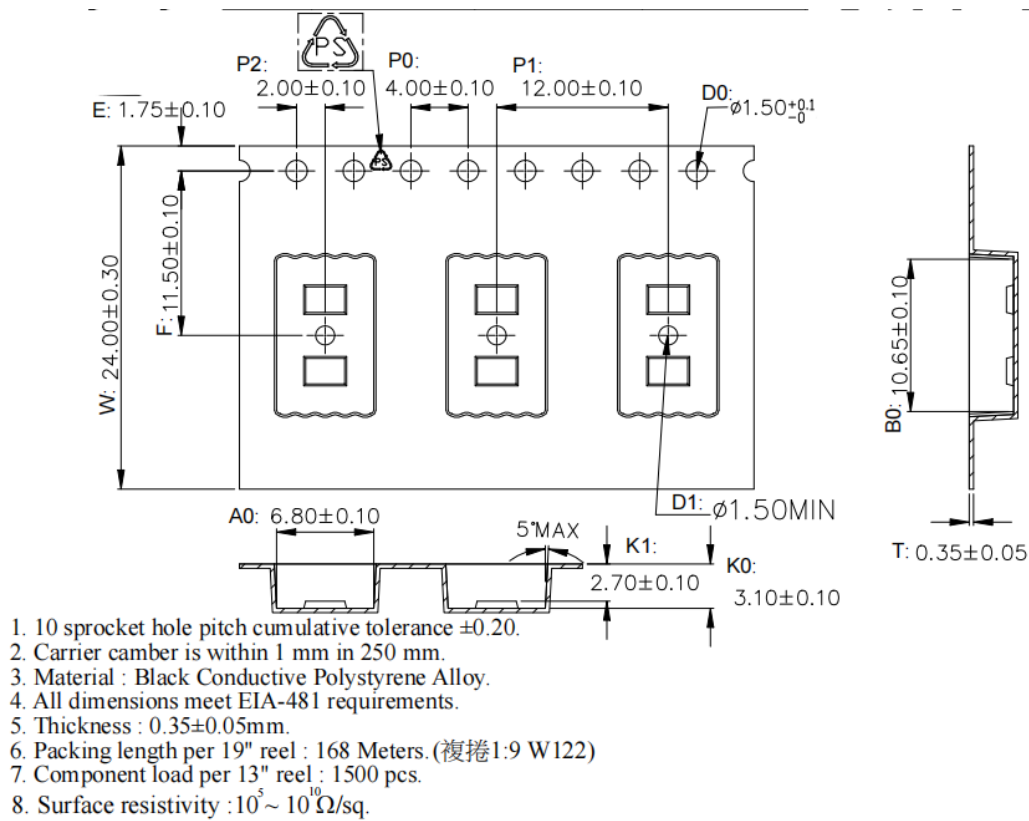


Figure 13.2 Tape information

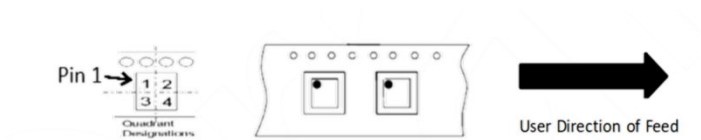


Figure 13.3 Quadrant Designation for Pin1 Orientation in Tape

## 14. Revision History

| Revision | Description     | Date       |
|----------|-----------------|------------|
| 1.0      | Initial version | 2026/02/26 |

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