

Product Overview

NSI6602MxEx is a family of high reliability isolated dual-channel gate driver ICs which can be designed to drive power transistor up to 2MHz switching frequency. It can source and sink 10A peak current and has an integrated active Miller Clamp circuit with 5A current rating to prevent false turn on caused by Miller current.

The NSI6602MxEx provides 5700Vrms isolation in SOW18 wide package. System robustness is supported by typical $\pm 200\text{V/ns}$ (min. $\pm 150\text{V/ns}$) common-mode transient immunity (CMTI).

The driver operates with a maximum supply voltage of 32V, while the input-side accepts from 3V to 18V supply voltage. Under voltage lock-out (UVLO) protection is supported by all the power supply voltage pins.

With all these excellent features, NSI6602MxEx is suitable for high reliability, power density and efficiency switching power system.

Key Features

- Isolated dual-channel driver
- Input side supply voltage: 3V to 18V
- Driver side supply voltage: up to 32V with UVLO
- Typical 10A peak source and Typical 10A peak sink output
- Typical 5A peak sink Active Miller Clamp
- Typical High CMTI: $\pm 200\text{kV}/\mu\text{s}$
- Programmable deadtime
- Operation temperature: $-40^\circ\text{C} \sim 125^\circ\text{C}$
- RoHS & REACH Compliance
- AEC-Q100 (Grade1) qualified for Auto-motive Application

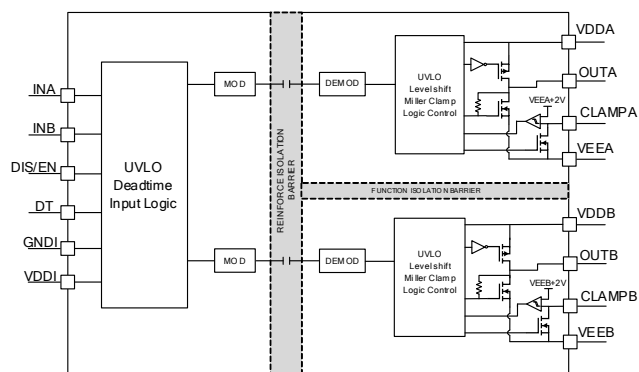
Safety Regulatory Approvals

- UL recognition: 5700V_{rms} for 1 minute per UL1577
- DIN EN IEC 60747-17 (VDE 0884-17)
- CSA component notice 5A
- CQC certification per GB4943.1

Applications

- Isolated DC-DC and AC-to-DC power supplies in server, telecom and industry
- DC-to-AC solar inverters
- Motor drives and EV charging
- UPS and battery chargers

Functional Block Diagram



NSI6602MxEx Block Diagram

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1. Pin Configuration and Functions

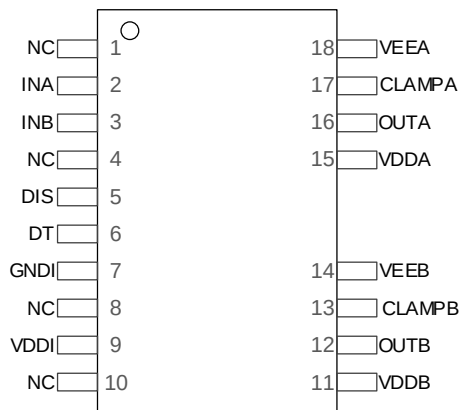


Figure 1.1 NSI6602MEx SOW18 Package

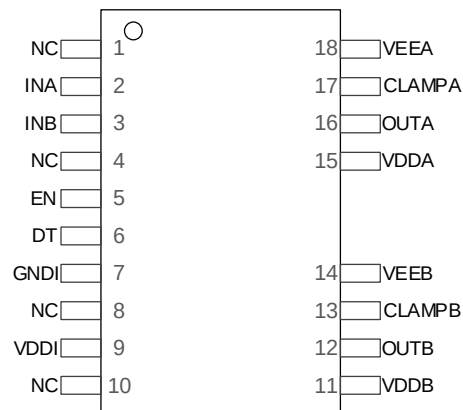


Figure 1.2 NSI6602MNEEx SOW18 Package

Table 1.1 Pin Configuration and Description

PIN NO. SOW18	SYMBOL	FUNCTION
2	INA	TTL compatible input signal for channel A with internal pull down to GNDI. It is recommended to connect this pin to GNDI if not used.
3	INB	TTL compatible input signal for channel B with internal pull down to GNDI. It is recommended to connect this pin to GNDI if not used.
5	DIS	Disable the isolator inputs and driver outputs if asserted high, enable if asserted low or left open. It is recommended to connect this pin to GNDI if not used.
	EN	Enable the isolator inputs and driver outputs if asserted high, disable if asserted low or left open. It is recommended to connect this pin to VDDI if not used.
6	DT	Programmable deadtime control. - DT pin short to VDDI disables dead time interlock function to allow the outputs overlapping. - DT pin open or floating enables interlock function, deadtime will be typically 8ns. - Place a 1kΩ to 200kΩ resistor (R_{DT}) between DT and GNDI to adjust deadtime following: $t_{DT} (ns) = 10 \times R_{DT} (k\Omega)$. Connecting with a low ESR 2.2nF capacitor to GNDI is recommended to limit the noise interference.
7	GNDI	Input-side ground reference.
9	VDDI	Input-side supply voltage. It is recommended to place a bypass capacitor from this pin to GNDI as close as possible.
11	VDDDB	Positive output supply rail of channel B
12	OUTB	Gate Driver Output of channel B
13	CLAMPB	Active Miller-Clamp input of channel B
14	VEEB	Driver-side ground reference of channel B

PIN NO. SOW18	SYMBOL	FUNCTION
15	VDDA	Positive output supply rail of channel A
16	OUTA	Gate Driver Output of channel A
17	CLAMPA	Active Miller-Clamp input of channel A
18	VEEA	Driver-side ground reference of channel A
1, 4, 8, 10	NC	Not connected

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
Input Side Supply Voltage	VDDI - GNDI	-0.3	24	V
Output Side Supply Voltage	VDDA - VEEA, VDDDB - VEEB	-0.3	35	V
Input Signal Voltage	INA, INB, DIS/EN, DT - GNDI	-0.3	$V_{VDDI}+0.3$	V
	INA, INB, DIS/EN, DT - GNDI, Transient for 50ns	-5	$V_{VDDI}+0.3$	V
Output Signal Voltage	OUTA - VEEA, OUTB - VEEB CLAMPA - VEEA, CLAMPB - VEEB	-0.3	$V_{VDDA}+0.3$ $V_{VDDDB}+0.3$	V
	OUTA - VEEA, OUTB - VEEB, CLAMPA - VEEA, CLAMPB - VEEB, Transient for 100ns	-2	$V_{VDDA}+0.3$ $V_{VDDDB}+0.3$	V
Channel A to Channel B Voltage	VEEA to VEEB		1850	V
Junction Temperature	T_J	-40	150	°C
Storage Temperature	T_{stg}	-65	150	°C

3. ESD Ratings

	Ratings	Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD ● All pins	± 3000	V
	Charged device model (CDM), per AEC-Q100-011-RevB ● All pins	± 1500	V

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
Input Side Supply Voltage	VDDI - GNDI	3	18	V
Driver Side Supply Voltage	VDDA - VEEA, VDDDB - VEEB (NSI6602MxEB)	9.5	32	V

Parameters	Symbol	Min	Max	Unit
Driver Side Supply Voltage	VDDA - VEEA, VDDB – VEEB (NSI6602MxEC)	13.5	32	V
Driver Side Supply Voltage	VDDA - VEEA, VDDB – VEEB (NSI6602MxED)	6	32	V
Driver Side Supply Voltage	VDDA - VEEA, VDDB – VEEB (NSI6602MxEF)	18.5	32	V
Input Signal Voltage	INA, INB, DIS/EN, DT -GNDI	0	V _{VDDI}	V
Ambient Temperature	T _A	-40	125	°C

5. Thermal Information

Parameters	Symbol	Typical	Unit
Junction-to-ambient thermal resistance ¹⁾	R _{JA}	59.4	°C/W
Junction-to-case(top) thermal resistance ²⁾	R _{JC (top)}	28.3	°C/W
Junction-to-top characterization parameter ³⁾	Ψ _{JT}	8	°C/W
Junction-to-board characterization parameter ³⁾	Ψ _{JB}	19.8	°C/W

- 1) Standard JESD51-7 Low Effective Thermal Conductivity Test Board (2s2p) in an environment described in JESD51-2a.
- 2) Standard JESD51-7 Low Effective Thermal Conductivity Test Board (2s2p) by transient dual interface test method described in JESD51-14.
- 3) Obtained by Simulating in an environment described in JESD51-2a.

6. Specifications

6.1. Electrical Characteristics

VDDI=3.3V or 5V, VDDA=VDDB=15V for NSI6602MxEB/C/D, VDDA=VDDB=18V for NSI6602MxEF, T_A=-40°C to 125°C. Unless otherwise noted, typical values are at T_A=25°C.

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Input Side Supply						
VDDI Quiescent Current	I _{VDDIQ}		0.9	2	mA	INA=0, INB=0
VDDI Operation Current	I _{VDDI}		1.6		mA	Input frequency 500kHz, C _{OUTA/B} =100pF
VDDI UVLO Rising Threshold	V _{VDDI_ON}	2.5	2.7	2.9	V	
VDDI UVLO Falling Threshold	V _{VDDI_OFF}	2.3	2.5	2.7	V	
VDDI UVLO Hysteresis ⁽¹⁾	V _{VDDI_HYS}		0.2		V	
Output Side Supply						

Parameter				Symbol	Min	Typ	Max	Unit	Comments
VDDA/B Channel	Quiescent	Current, per		I _{VDDAQ} , I _{VDDBQ}		1.3	2.2	mA	VDDA/B=15V
VDDA/B Channel	Operation	Current, per		I _{VDDA} , I _{VDDB}		3.4	4	mA	Input frequency 500kHz, C _{OUTA/B} =100pF, VDDA/B=15V
VDDA/B UVLO Rising Threshold				V _{VDDA_ON} , V _{VDDB_ON}	8.1	8.5	8.9	V	NSI6602MxEB (8V)
VDDA/B UVLO Falling Threshold				V _{VDDA_OFF} , V _{VDDB_OFF}	7.6	8	8.4	V	
VDDA/B UVLO Hysteresis				V _{VDDA_HYS} , V _{VDDB_HYS}		0.5		V	
VDDA/B UVLO Rising Threshold				V _{VDDA_ON} , V _{VDDB_ON}	11.4	12	12.6	V	NSI6602MxEC (12V)
VDDA/B UVLO Falling Threshold				V _{VDDA_OFF} , V _{VDDB_OFF}	10.4	11	11.6	V	
VDDA/B UVLO Hysteresis ⁽¹⁾				V _{VDDA_HYS} , V _{VDDB_HYS}		1		V	
VDDA/B UVLO Rising Threshold				V _{VDDA_ON} , V _{VDDB_ON}	4.5	5	5.5	V	NSI6602MxED (5V)
VDDA/B UVLO Falling Threshold				V _{VDDA_OFF} , V _{VDDB_OFF}	4.0	4.5	5.0	V	
VDDA/B UVLO Hysteresis ⁽¹⁾				V _{VDDA_HYS} , V _{VDDB_HYS}		0.5		V	
VDDA/B UVLO Rising Threshold				V _{VDDA_ON} , V _{VDDB_ON}	16.3	17	17.7	V	NSI6602MxEF (17V)
VDDA/B UVLO Falling Threshold				V _{VDDA_OFF} , V _{VDDB_OFF}	15.3	16	16.7	V	
VDDA/B UVLO Hysteresis ⁽¹⁾				V _{VDDA_HYS} , V _{VDDB_HYS}		1		V	
Input Side Characteristic									
Input Pin Pull Down Resistance, INA, INB				R _{INA_PD} , R _{INB_PD}	80	100	140	kΩ	
Input Pin Pull Down Resistance, DIS				R _{DIS_PD} / R _{EN_PD}	80	100	140	kΩ	
Logic High Input Threshold				V _{INA_H} , V _{INB_H} , V _{DIS_H} / V _{EN_H}	1.5	1.8	2.1	V	
Logic Low Input Threshold				V _{INA_L} , V _{INB_L} , V _{DIS_L} / V _{EN_L}	0.8	1.1	1.4	V	
Input Hysteresis ⁽¹⁾				V _{INA_HYS} , V _{INB_HYS} , V _{DIS_HYS} / V _{EN_HYS}		0.7		V	

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Output Side Characteristic						
Logic High Output Voltage	$V_{VDDA} - V_{OUTA_H}, V_{VDDB} - V_{OUTB_H}$		55		mV	I _{OUTA, OUTB} =-100mA, V _{INA, INB} =High
Logic Low Output Voltage	$V_{OUTA_L} - V_{VEEA}, V_{OUTB_L} - V_{VEEB}$		45		mV	I _{OUTA, OUTB} =100mA, V _{INA, INB} =Low
Output Source Resistance	R _{OUTA_H, OUTB_H}		0.55		Ω	I _{OUTA, OUTB} = -100mA
Output Sink Resistance	R _{OUTA_L, OUTB_L}		0.45		Ω	I _{OUTA, OUTB} = 100mA
Peak Output Sink Current ⁽¹⁾	I _{OUTAL, OUTBL}		10		A	V _{INA, INB} =Low, pulse width<10us
Peak Output Source Current ⁽¹⁾	I _{OUTAH, OUTBH}		10		A	V _{INA, INB} =High, pulse width<10us
Active Miller Clamp						
Low Level Clamp Voltage	V _{CLAMPA, CLAMPB}		70		mV	I _{CLAMPA, CLAMPB} =100mA, V _{INA, INB} =Low, refer to VEEA, VEEB
Clamp Low-level Current	I _{CLAMPA, CLAMPB}		5		A	
Clamp Threshold Voltage	V _{CLAMPA_TH, CLAMPB_TH}		2	2.3	V	
Short Circuit Clamping						
VOUT Short Circuit Clamping Voltage	V _{CLP_OUT}		0.3		V	V _{INA, INB} =High, I _{OUTA, OUTB} =0.5A, pulse width<=10us, refer to VDDA, VDDB
VCLAMP Short Circuit Clamping Voltage	V _{CLP_CLAMP}		1.2		V	V _{INA, INB} =High, I _{CLAMPA, CLAMPB} =0.5A, pulse width<=10us, refer to VDDA, VDDB
			0.7		V	V _{INA, INB} =High, I _{CLAMPA, CLAMPB} =20mA, refer to VDDA, VDDB
Active Pull Down						
Active Pulldown Voltage on OUT	V _{ACTPD}		2.1		V	VDDI, VDDA/B=OPEN, I _{OUTA, OUTB} =500mA

⁽¹⁾ Not test covered, guaranteed by characterization.

6.2. Switching Characteristics

VDDI=3.3V or 5V, VDDA=VDDB=15V for NSI6602MxExB/C/D, $T_A = -40^\circ C$ to $125^\circ C$. Unless otherwise noted, typical values are at $T_A = 25^\circ C$.

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Minimum Pulse Width	t_{PWmin}		35	50	ns	
Propagation Delay	t_{PDHL}, t_{PDLH}		80	100	ns	$C_{load}=100pF$
Pulse Width Distortion $ t_{PDLH}-t_{PDHL} $	t_{PWD}		2	10	ns	$C_{load}=100pF$
Channel to Channel Delay Matching	t_{DMLH}, t_{DMHL}			10	ns	
Programmed Deadtime	t_{DT}	160	200	250	ns	$t_{DT}(ns)=10 \cdot R(k\Omega)$; Test for $R = 20k\Omega$
Output Rise Time (20% to 80%)	t_R		10		ns	$C_{OUTA/B}=1nF$
Output Fall Time (80% to 20%)	t_F		10		ns	$C_{OUTA/B}=1nF$
Shutdown Time from Disable True	t_{DIS}		110	145	ns	
Recovery Time from Disable False	t_{EN}		110	145	ns	
VDDI Power-up Time Delay (Time from VDDI = VDDI_ON to OUTA/B = INA/B)	t_{start_VDDI}		10	19	μs	INA or INB tied to VDDI
VDDA,VDDB Power-up Time Delay (Time from VDDA, VDDB = VDDA_ON, VDDB_ON to OUTA/B = INA/B)	$t_{start_VDDA},$ t_{start_VDDB}		14	20	μs	INA or INB tied to VDDI
Common Mode Transient Immunity ⁽²⁾	CMTI	150	200		V/ns	verified by design

⁽¹⁾ Not test covered, guaranteed by characterization.

⁽²⁾ Not test covered, guaranteed by Design.

6.3. Typical Performance Characteristics

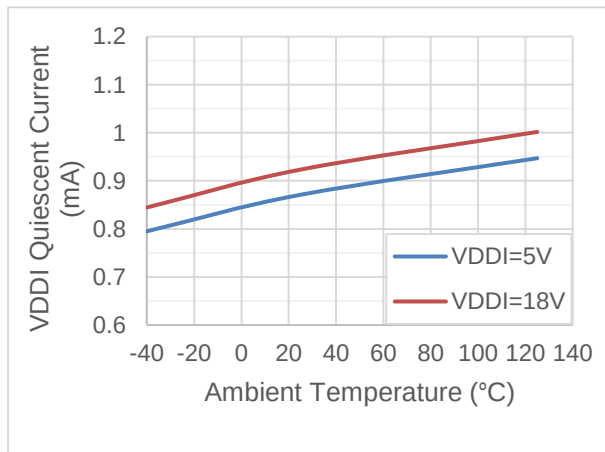


Figure 6.1 VDDI Quiescent Current vs Temperature

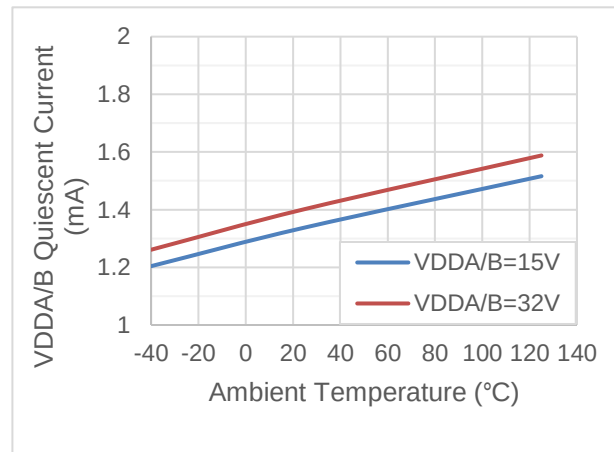


Figure 6.2 VDDA/B Quiescent Current vs Temperature

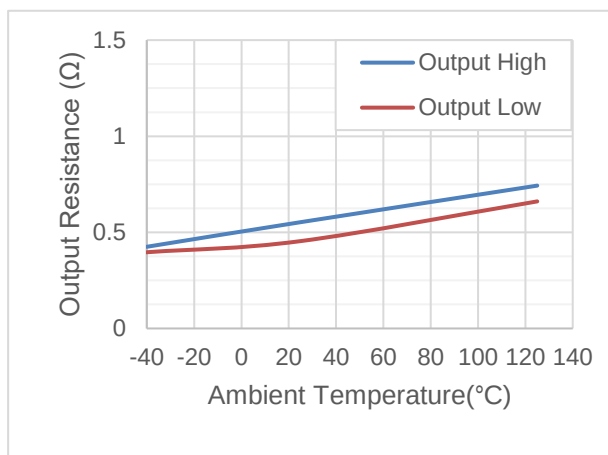


Figure 6.3 Output Resistance vs Temperature

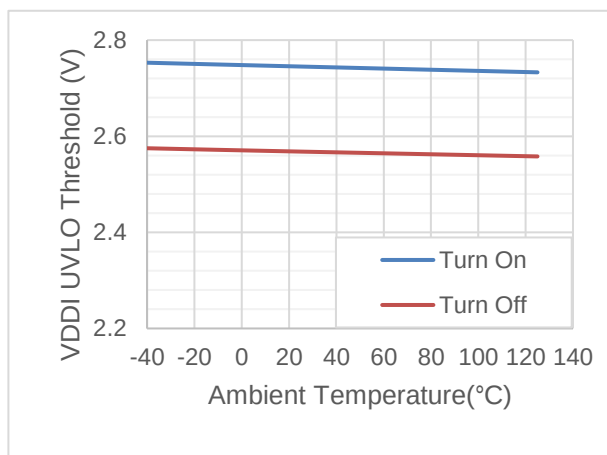


Figure 6.4 VDDI UVLO Threshold vs Temperature

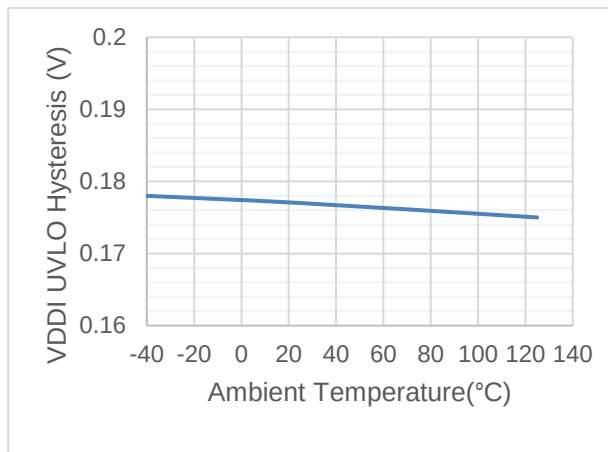


Figure 6.5 VDDI UVLO Hysteresis vs Temperature

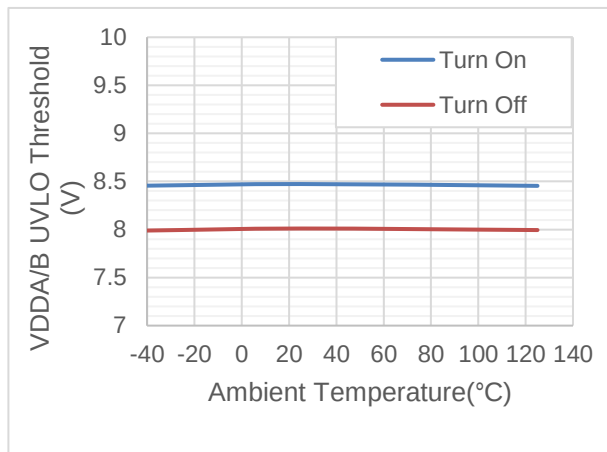


Figure 6.6 6602MxEB VDDA/B UVLO Threshold vs Temperature

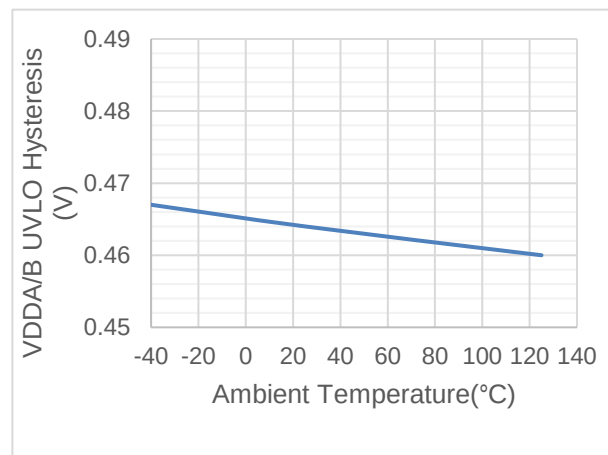


Figure 6.7 6602MxEB VDDA/B UVLO Hysteresis vs Temperature

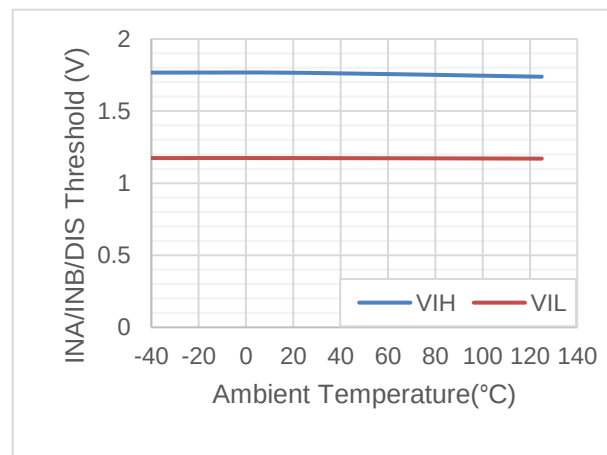


Figure 6.8 INA/INB/DIS Threshold vs Temperature

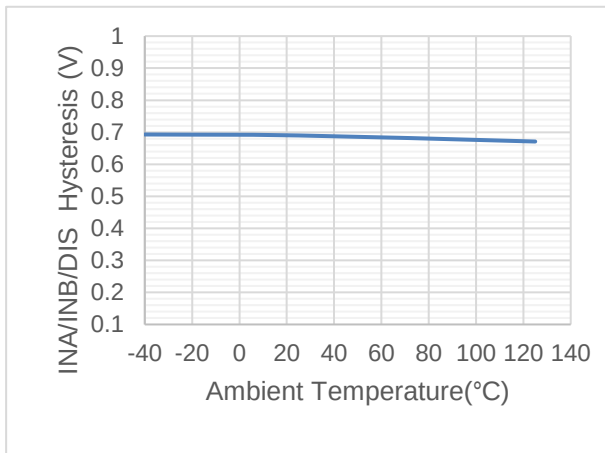


Figure 6.9 INA/INB/DIS Hysteresis vs Temperature

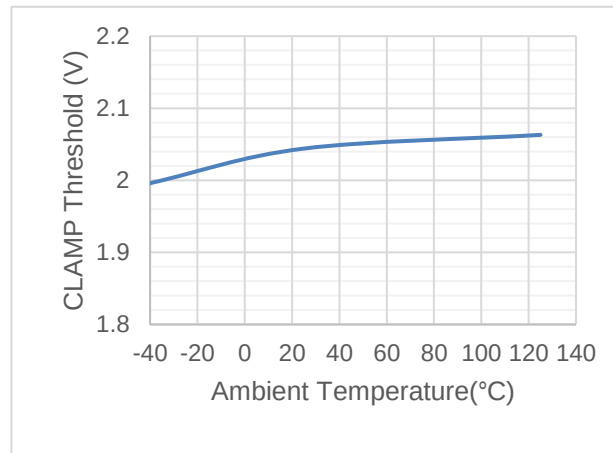


Figure 6.10 CLAMP Threshold Voltage vs Temperature

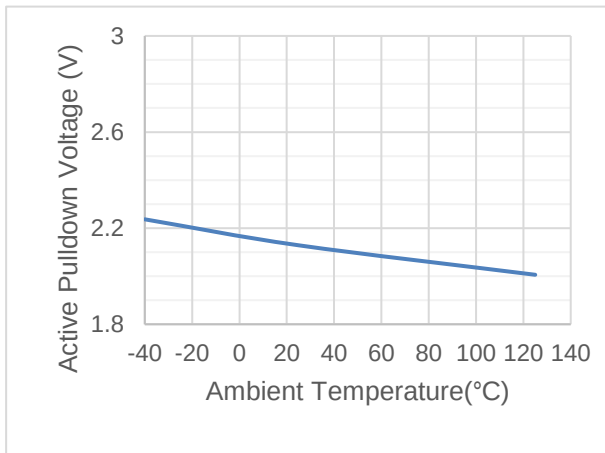


Figure 6.11 Active Pulldown Voltage vs Temperature

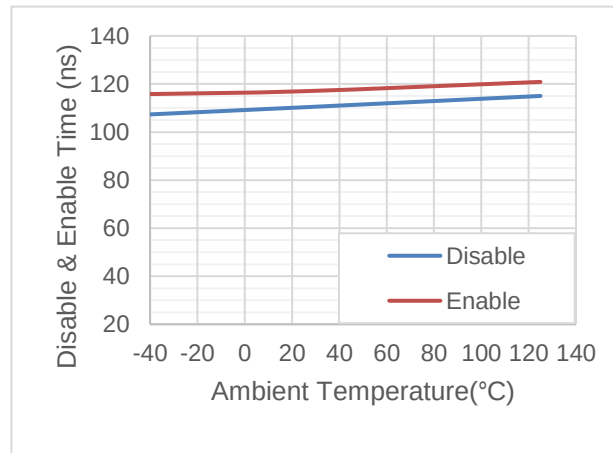


Figure 6.12 Disable & Enable Time vs Temperature

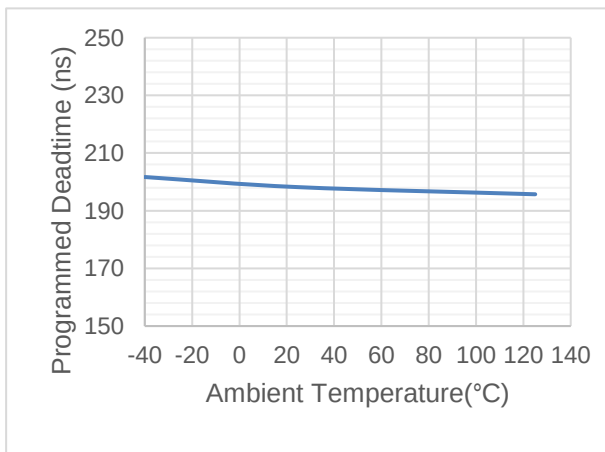


Figure 6.13 Deadtime (RDT=20kΩ) vs Temperature

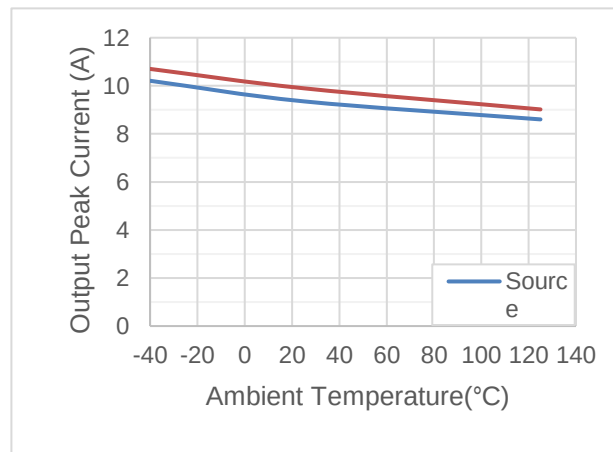


Figure 6.14 Output Peak Current vs Temperature

6.4. Parameter Measurement Information

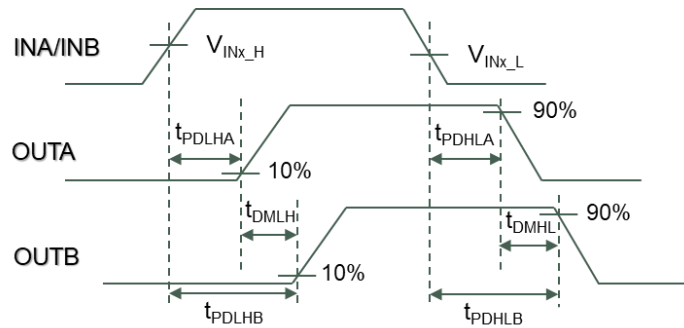


Figure 6.15 Propagation Delay and Channel to Channel Delay Match Time, connect DT to VDDI

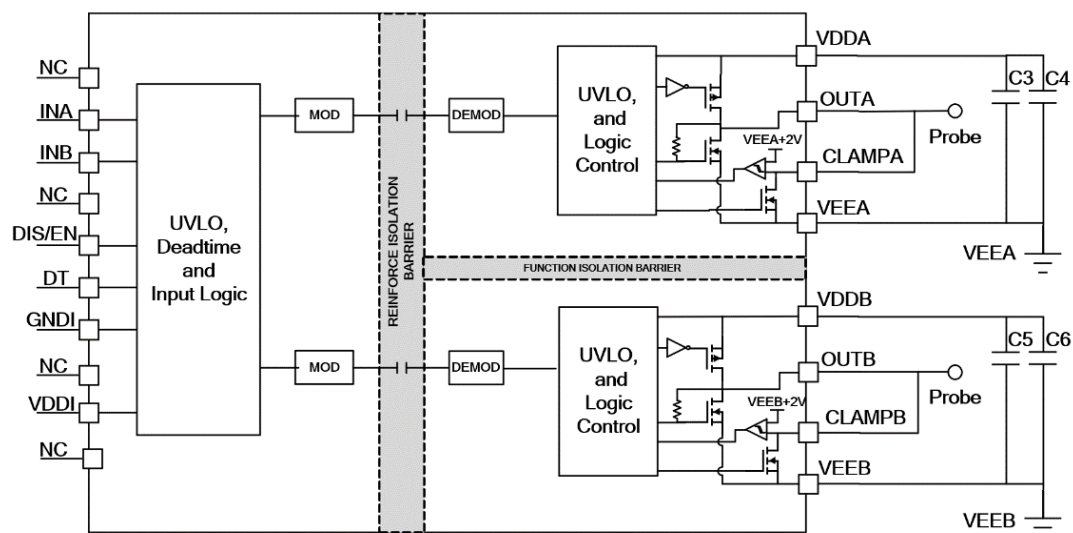


Figure 6.16 Channel to Channel Delay Match Test Circuit

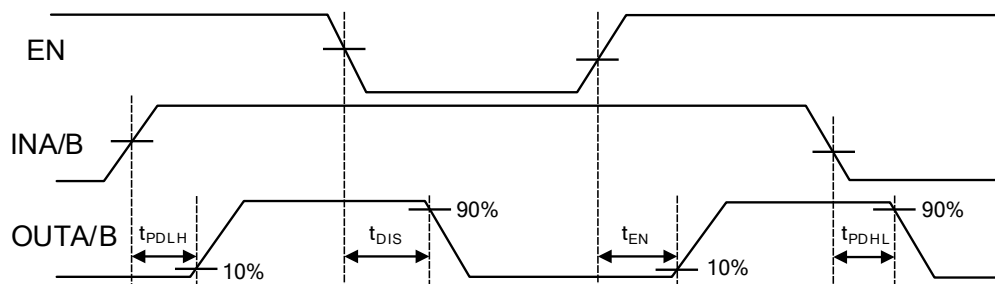


Figure 6.17 Disable Time and Enable Time (NSI6602MNEx)

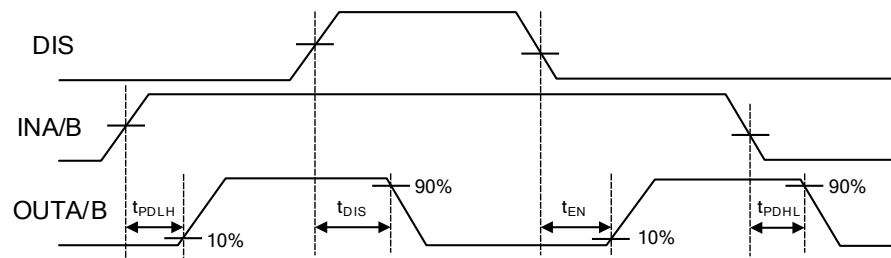


Figure 6.18 Disable Time and Enable Time (NSI6602MEx)

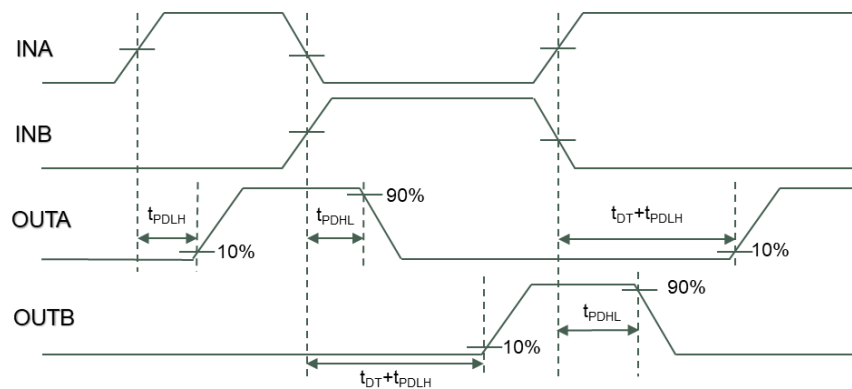


Figure 6.19 Deadtime, Determined by RDT

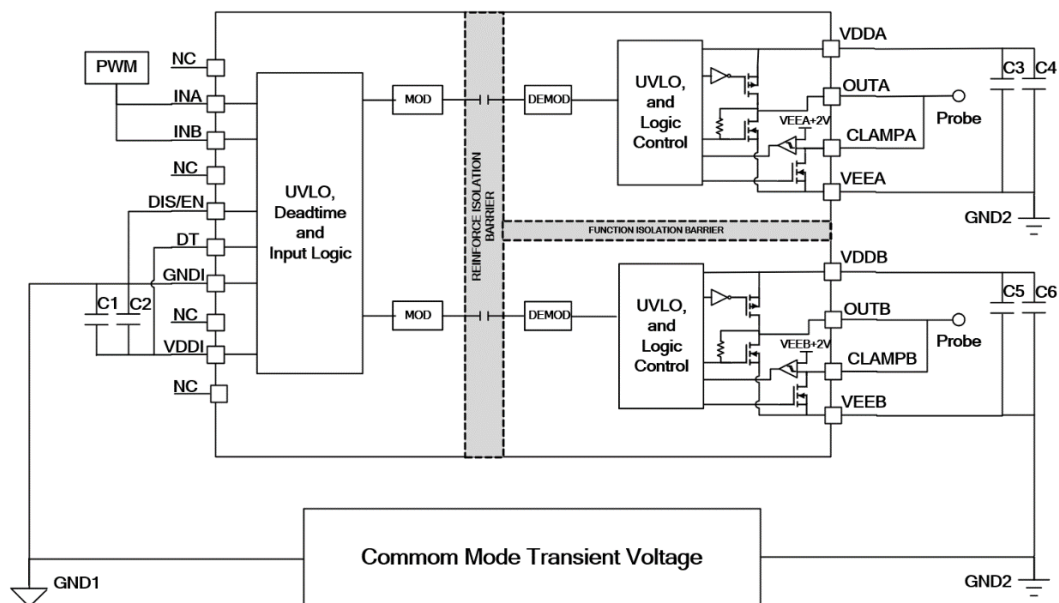


Figure 6.20 Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value	Unit	Comments
Minimum External Air Gap (Clearance)	CLR	8	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	CPG	8	mm	Shortest terminal-to-terminal distance across the package surface
Distance Through Insulation	DTI	32	μm	internal gap
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value	Unit
Overvoltage Category per IEC60664-1	For Rated Mains Voltage $\leq 150\text{Vrms}$		I to IV	
	For Rated Mains Voltage $\leq 300\text{Vrms}$		I to IV	
	For Rated Mains Voltage $\leq 600\text{Vrms}$		I to IV	
	For Rated Mains Voltage $\leq 1000\text{Vrms}$		I to III	
Climatic Category			40/125/21	
Pollution Degree	per DIN VDE 0110, Table 1		2	
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	1500	V_{RMS}
	DC voltage		2121	V_{DC}
Maximum Repetitive Isolation Voltage		V_{IORM}	2121	V_{peak}
Apparent Charge	Method B, Routine test(100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}$, $V_{pd(m)}=V_{IORM}\times 1.875$, $t_{ini}=t_m=1s$	q_{pd}	<5	pC
	Method A, after Environmental Tests Subgroup 1, $V_{pd(m)}=V_{IORM}\times 1.6$, $t_{ini}=60s$, $t_m=10s$			pC
	Method A, after Input and Output Safety Test Subgroup 2 and Subgroup 3, $V_{pd(m)}=V_{IORM}\times 1.2$, $t_{ini}=60s$, $t_m=10s$			pC
Maximum Transient Isolation Voltage	$t = 60 \text{ sec}$	V_{IOTM}	8000	V_{peak}

Description	Test Condition	Symbol	Value	Unit
Maximum Impulse Voltage	Tested in air, 1.2/50μs waveform per IEC62368-1	V_{IMP}	6000	V_{peak}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50μs waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$	V_{IOSM}	10000	V_{peak}
Isolation Resistance	$V_{IO} = 500V$ at $T_A = T_S = 25^\circ C$	R_{IO}	$> 10^{12}$	Ω
	$V_{IO} = 500V$ at $T_A = T_S = 150^\circ C$		$> 10^9$	Ω
	$V_{IO} = 500V$ at $100^\circ C \leq T_A \leq 125^\circ C$		$> 10^{11}$	Ω
Isolation Capacitance	$f = 1MHz$	C_{IO}	1.2	pF
Insulation Specification per UL1577				
Withstand Isolation Voltage	$V_{TEST} = 1.2 \times V_{ISO}$, $t = 1$ sec, 100% production test	V_{ISO}	5700	V_{rms}

- 1) This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

7.3. Safety-Limiting Values

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI6602MxEx

Description	Test Condition	Side	Value	Unit
Safety Supply Power	$R_{\theta JA} = 59.4^\circ C/W^{(1)}$, $T_J = 150^\circ C$, $T_A = 25^\circ C$	Input	100	mW
		Driver A, Driver B	1	W
		Total	2.1	W
Safety Supply Current	$R_{\theta JA} = 59.4^\circ C/W^{(1)}$, $V_{DDA/B} = 25V$, $T_J = 150^\circ C$, $T_A = 25^\circ C$	Driver A, Driver B	40	mA
Safety Temperature ²⁾			150	$^\circ C$

- 1) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.
- 2) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOW18 package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

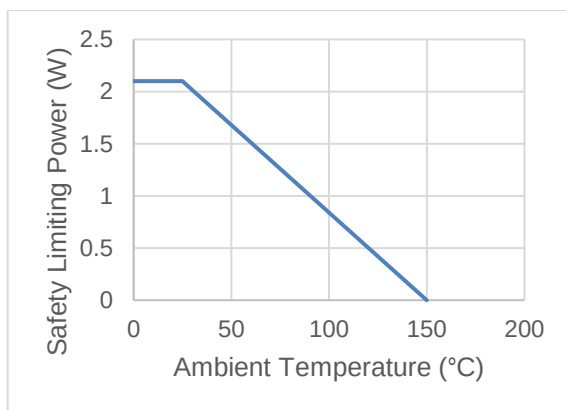


Figure 7.1 NSI6602MxEx Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI6602MxEx

7.4. Safety-Related Certifications

The NSI6602MxEx are approved or pending approval by the organizations listed in table.

UL		CQC		TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to GB4943.1	DIN EN IEC 60747- 17 (VDE 0884-17)	Certified According to EN IEC 62368-1
Single Protection, 5700Vrms Isolation voltage	Single Protection, 5700Vrms Isolation voltage	Reinforced insulation	Reinforced insulation $V_{IORM}=2121V_{peak}$ $V_{IOTM}=8000V_{peak}$	5000Vrms for 1min
E500602	E500602	File (pending)	R50632560	R50574061

8. Function Description

8.1. Overview

NSI6602MxEx is a high reliability dual channel isolated gate driver which could be designed in variety switching power and motor drive topologies. NSI6602MxEx has some useful protections, such as under voltage lock-out (UVLO) for both input and output supply, a disable pin, dead-time control, active miller clamp, short circuit clamping, active pull down, and default low output as input is floating. The functional circuit block diagram is shown as below:

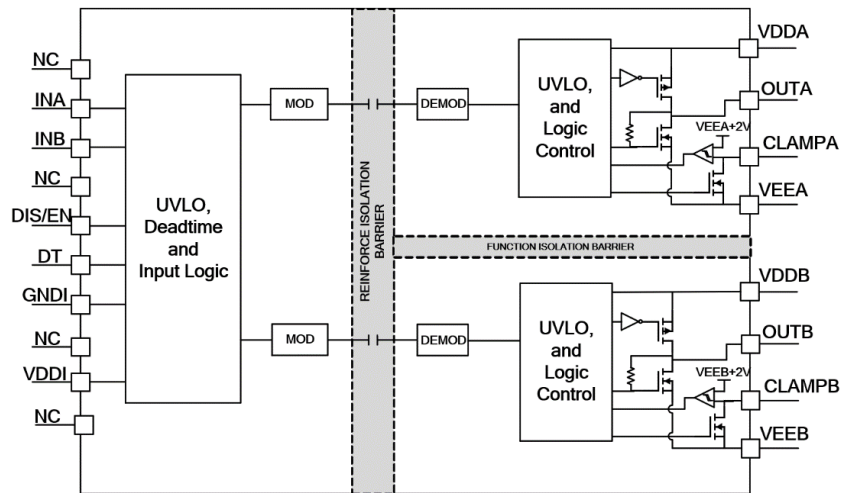


Figure 8.1 Functional Block Diagram

8.2. Under Voltage Lock Out (UVLO)

The NSI6602MxEx has an internal under voltage lock out (UVLO) protection on the both input and output supply circuit blocks. The driver output is held low by an active clamp circuit when the supply voltage of VDDI or VDDA/VDDB is lower than V_{VDD_ON} at power-up status or lower than V_{VDD_OFF} after power-up, regardless of the status of the input pins.

The VDDI and VDDA/B ULVO protections have hysteresis (V_{VDD_HYS}) to prevent chatter noise from VDD supply and allow small drops in supply power which are usually happened in startup.

8.3. Input and Output Logic Table

When the device is power up, setting the DIS pin high can shut down both outputs simultaneously. Left open or grounding the DIS pin can allow the device operating normally.

Table 8.1 Output status vs. Input and Power status (NSI6602MEx)

VDDI status	VDDA/B status	DIS	IN		OUT		NOTE ¹⁾
			A	B	A	B	
PU	PU	L or O	L	H	L	H	If Deadtime function is used, output transits to high after the deadtime expires.
PU	PU	L or O	H	L	H	L	
PU	PU	L or O	H	H	H	H	DT pin is pulled to VDDI.
PU	PU	L or O	H	H	L	L	DT is left open or programmed with R _{DT} .
PU	PU	L or O	L	L	L	L	
PU	PU	L or O	O	O	L	L	
PU	PU	H	X	X	L	L	
PU	PD	X	X	X	L	L	Active pull-down
PD	PU	X	X	X	L	L	Active pull-down

Table 8.2 Output status vs. Input and Power status (NSI6602MNEEx)

VDDI status	VDDA/B status	EN	IN		OUT		NOTE ¹⁾
			A	B	A	B	
PU	PU	H	L	H	L	H	If Deadtime function is used, output transits to high after the deadtime expires.
PU	PU	H	H	L	H	L	
PU	PU	H	H	H	H	H	DT pin is pulled to VDDI.
PU	PU	H	H	H	L	L	DT is left open or programmed with R _{DT} .
PU	PU	H	L	L	L	L	
PU	PU	H	O	O	L	L	
PU	PU	L or O	X	X	L	L	
PU	PD	X	X	X	L	L	Active pull-down
PD	PU	X	X	X	L	L	Active pull-down

1) PD= Power Down; PU= Power Up; H= Logic High; L= Logic Low; O= Left Open; X= Irrelevant;

8.4. Programmable Deadtime (DT pin)

8.4.1 Pulling the DT Pin to VDDI

This allows outputs match inputs completely and no deadtime is asserted.

8.4.2 DT Pin Left Open or Connected to a Programming Resistor between DT and GND Pins

Left DT pin opened or floating enables interlock function, deadtime will be typically 8ns, connecting with a 2.2nF capacitor to GNDI is recommended to limit the noise interference. t_{DT} can be programmed by placing a resistor, R_{DT} , between the DT pin and GNDI. The appropriate R_{DT} value can be determined from Equation 1, where R_{DT} is in k Ω and t_{DT} in ns:

$$t_{DT} \approx 10 \times R_{DT} \quad (1)$$

The recommended value of R_{DT} is between from 1k Ω to 200k Ω . The steady state voltage at DT pin is about 0.8V and the DT pin current will be less than 10uA when $R_{DT} = 100k\Omega$. It is also recommended to parallel a ceramic capacitor, for example 2.2nF, with R_{DT} to achieve better noise immunity.

The programmed deadtime is activated by the input signal's falling edge to prevent shoot-through when the device is designed in an application of high side and low side driver. The details of input and output logic with deadtime are shown as Figure 8.2:

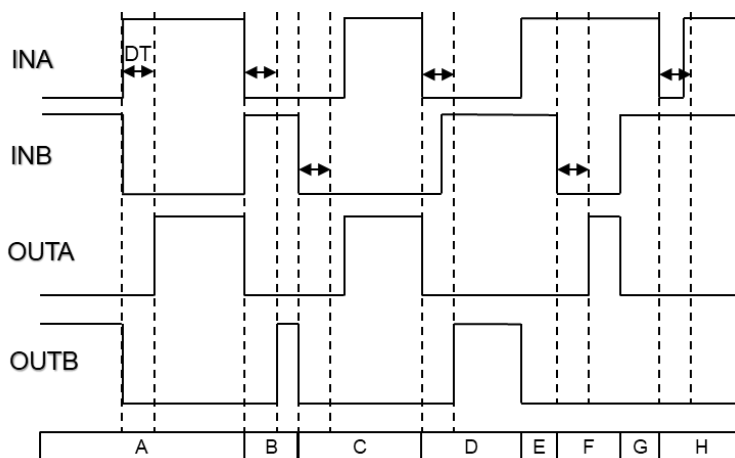


Figure 8.2 Input and Output Logic with the Programmed Deadtime

Condition	Result
A: INA goes high, and INB goes low.	OUTB goes low immediately, then OUTA goes high after the programmed deadtime which is assigned at INB goes low.
B: INA goes low, and INB goes high.	OUTA goes low immediately, then OUTB goes high after the programmed deadtime which is assigned at INA goes low.
C: INB goes low, then INA goes high after deadtime.	OUTB goes low immediately, then OUTA goes high immediately when INA goes high.
D: INA goes low, then INB goes high before deadtime.	OUTA goes low immediately, then OUTB goes high after deadtime
E: INA goes high, INB is still high.	OUTB goes low immediately and OUTA keeps low.
F: INA is still high, INB goes low.	OUTA goes high after deadtime while INB is low and OUTB keeps low.
G: INA is still high, INB goes high after deadtime	OUTA goes low immediately and OUTB keeps low.
H: INA goes low then goes high before deadtime while INB is still high.	OUTA keeps low and OUTB keeps low because deadtime control.

8.5. Active Pull Down

This function helps to pull the IGBT or MOSFET gate to the off-state when VDDA/B is not connected to the power supply. This feature prevents the false turn-on of OUT and CLAMP pins by clamping the output to approximately 2V.

8.6. Short Circuit Clamping

Short circuit is used to clamp the deriver output voltage as well as to pull the miller clamp pins CLAMPA or CLAMPB to a bit higher than their drive-side supply pins respectively. This function helps to protect the gate of a MOSFET or IGBT from overvoltage breakdown. The short circuit clamping is implemented by adding an additional circuit between the dedicated pins and the drive-side supply. The internal diode circuitry can conduct 500mA current to the supply for 10us. Use of external schottky diode may be added to improve the current capability and tighter clamping.

8.7. Active Miller Clamp

The active miller clamp function helps to prevent the false turn-on of the power switches caused by the miller current in applications, such as half bridge configuration, where switched off IGBT turns to dynamically turn-on during turn on period of the opposite IGBT. It usually happens when a unipolar power supply is used. To avoid such false turn-on of switches a miller clamp allows sinking the miller current across a low impedance path in this dv/dt situation. During turn-off the gate voltage is monitored and the power-switch gate voltage is clamped to less than 2V referred to VEEA/B. The clamp is designed for a miller current in the same range as the nominal output current.

8.8. ESD Protection

Figure 8.3 shows the multiple diodes involved in the ESD protection part of NSI6602MxEx.

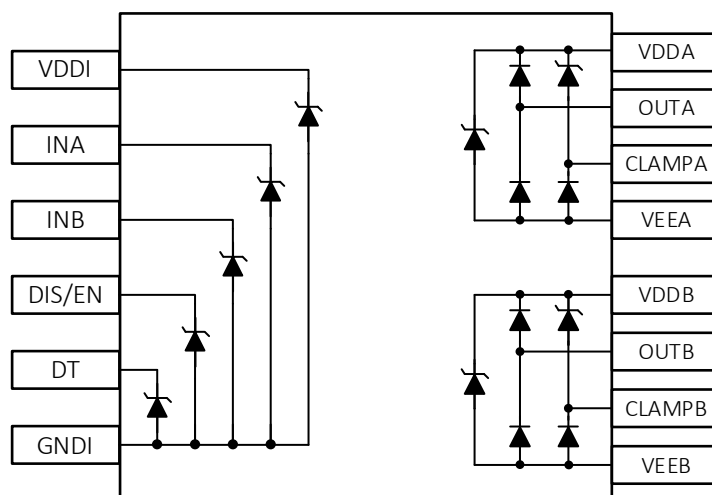


Figure 8.3 ESD Structure

9. Application Note

9.1. Typical Application Circuit

The circuit shows a typical half-bridge configuration by using the driver NSI6602MxEx which could be used in several popular power converter topologies such as half-bridge/full bridge/LLC isolated topologies, buck-boost topologies and 3-phase motor drive applications.

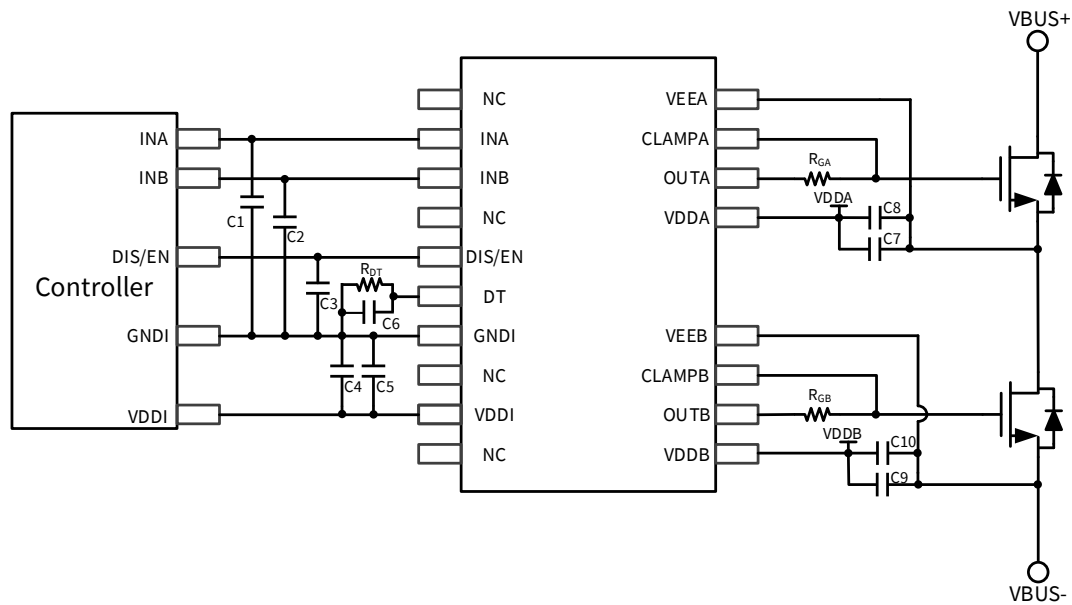


Figure 9.1 Typical Half-Bridge Application Schematic

9.2. PCB Layout

PCB layout is important to get optimal performance. Some key guidelines are:

- Low-ESR and low-ESL bypass capacitors should be placed close to the device between pin VDDI to GNDI and pin VDDA/B to VEEA/B.
- There is high switching current that charges and discharges the gate of external power transistor, leading to EMI and ring issues. The parasitic inductance of this loop should be minimized, by decreasing loop area and place NSI6602MxEx close to power transistor.
- Place large amount of copper connecting to VDDA/B pin and VEEA/B pin for thermal dissipation.
- To ensure isolation performance between primary and secondary side, the space under the device should keep free from any plane, trace, pad or via.

10.Package information

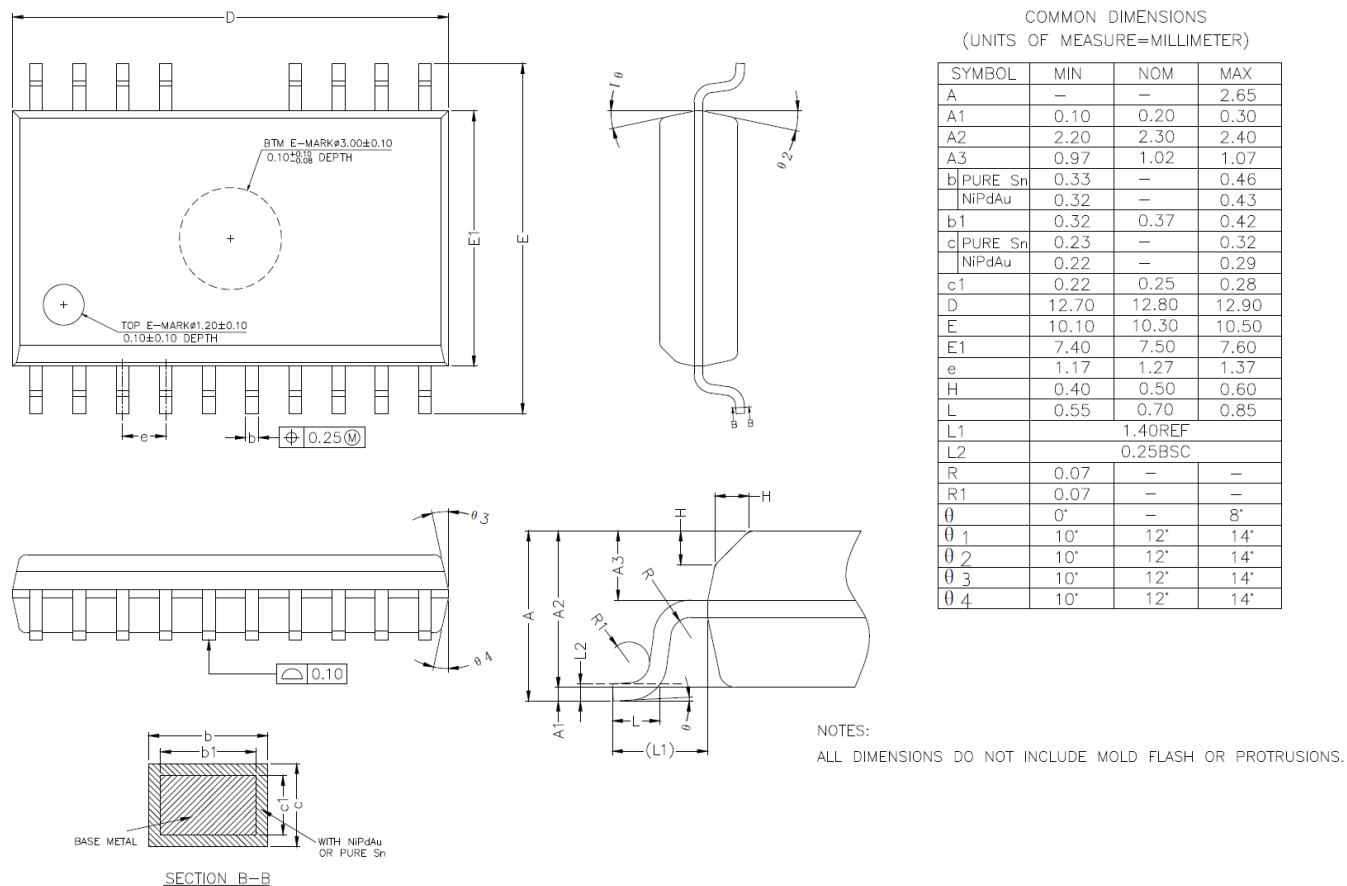


Figure 10.1 SOW18 Package Shape and Dimension

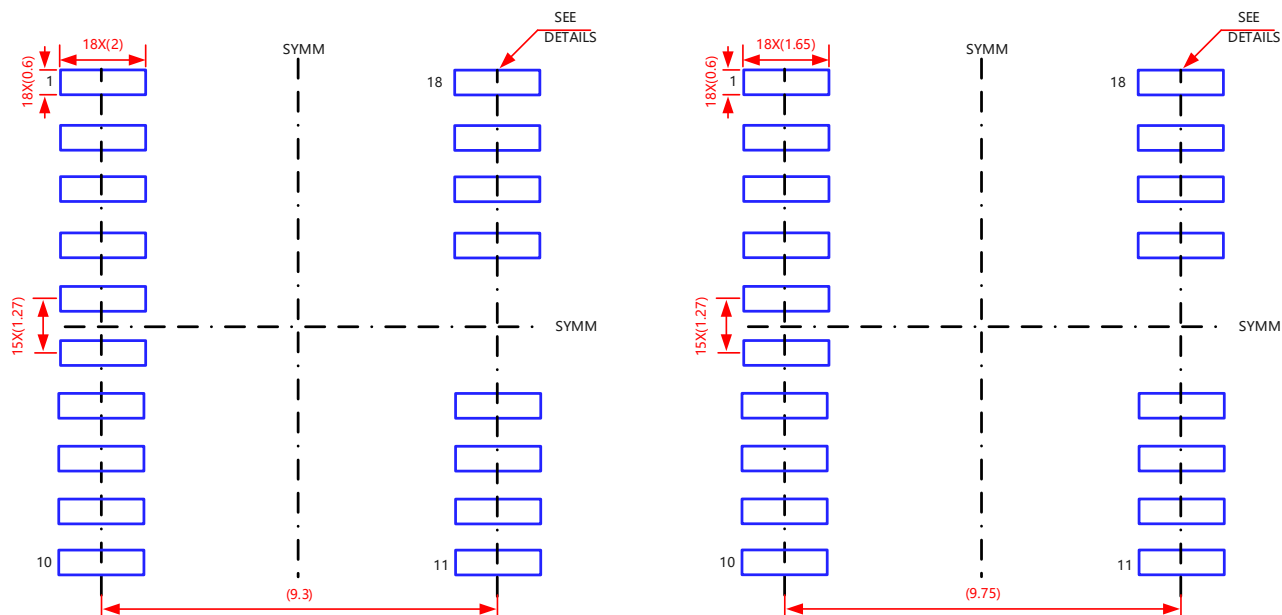


Figure 10.2 SOW18 Package Board Layout Example(mm)

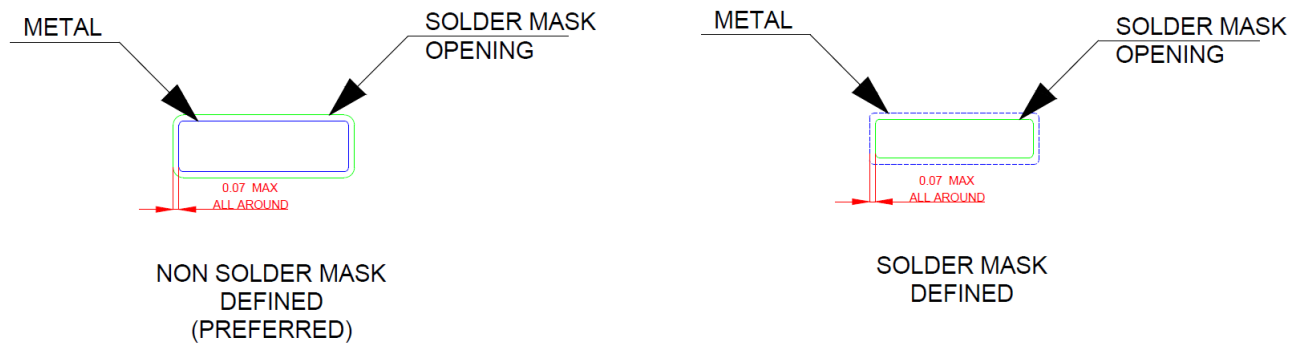


Figure 10.3 Solder Mask Details(mm)

11. Ordering Information

Part No.	Isolation Rating(kV_{RMS})	Driver-side UVLO TYP.	DIS or EN	Temperature	Auto-motive	Package Drawing	MSL	SPQ
NSI6602MEB-Q1SWDR	5.7	8V	DIS	-40 to 125°C	YES	SOW18	3	1000
NSI6602MEC-Q1SWDR	5.7	12V	DIS	-40 to 125°C	YES	SOW18	3	1000
NSI6602MED-Q1SWDR	5.7	5V	DIS	-40 to 125°C	YES	SOW18	3	1000
NSI6602MEF-Q1SWDR	5.7	17V	DIS	-40 to 125°C	YES	SOW18	3	1000
NSI6602MNE-B-Q1SWDR	5.7	8V	EN	-40 to 125°C	YES	SOW18	3	1000
NSI6602MNE-C-Q1SWDR	5.7	12V	EN	-40 to 125°C	YES	SOW18	3	1000
NSI6602MNE-D-Q1SWDR	5.7	5V	EN	-40 to 125°C	YES	SOW18	3	1000
NSI6602MNE-F-Q1SWDR	5.7	17V	EN	-40 to 125°C	YES	SOW18	3	1000

12. Tape and Reel Information

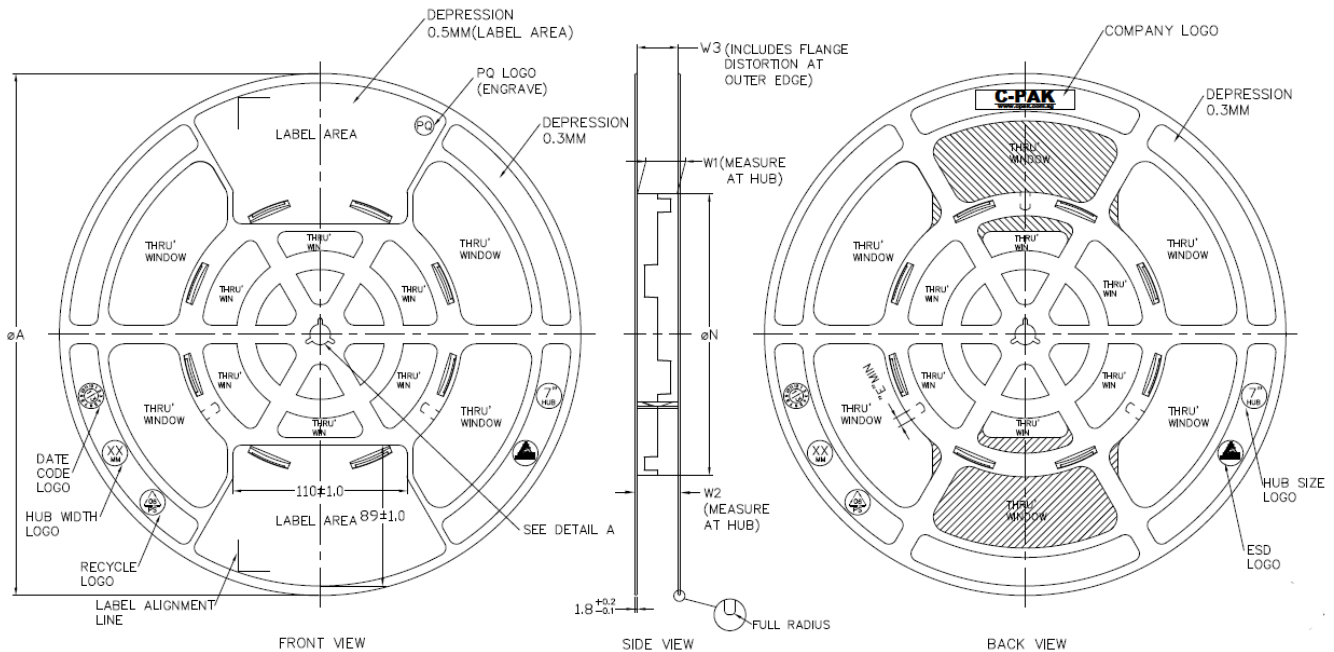


Figure 12.1 Tape Information

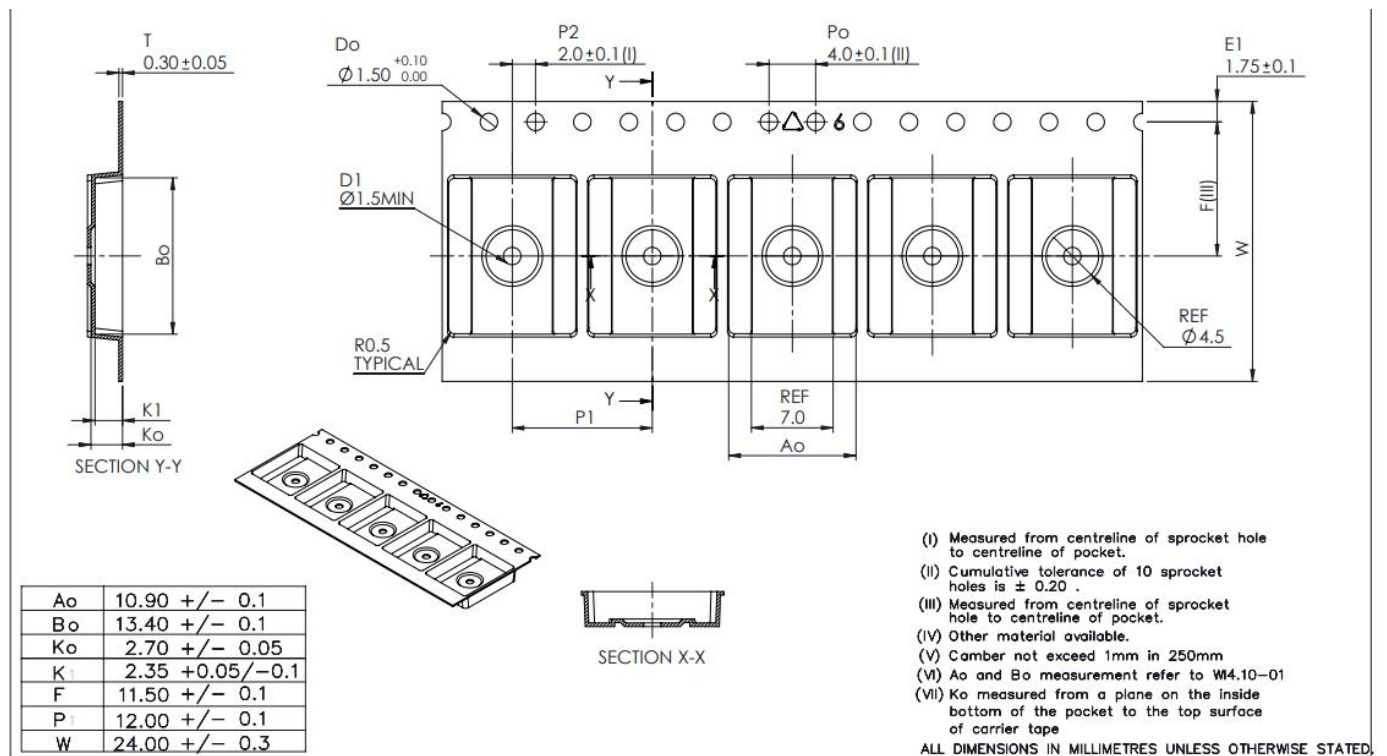


Figure 12.2 Reel Information

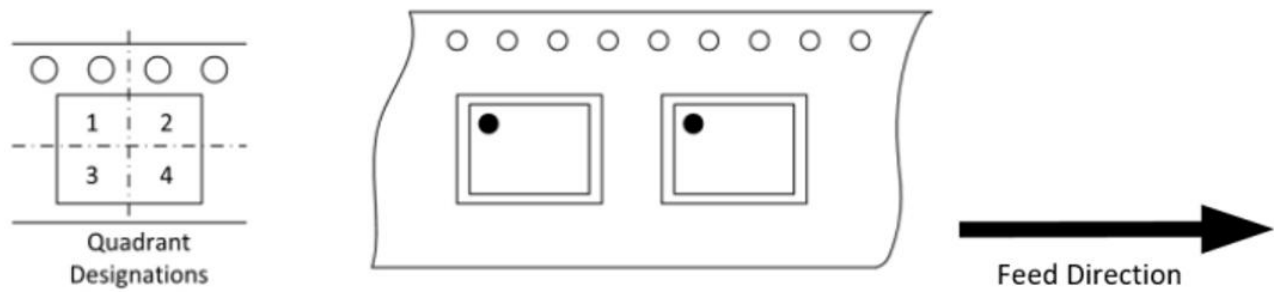


Figure 12.3 Quadrant Designation for Pin1 Orientation in Tape

13.Revision History

Revision	Description	Date
1.0	Initial version	2025/12/31
1.1	1.Update the AMR of CLAMP-VEE voltage 2.Update the number of safety - related certifications.	2026/6/1

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